# Automotive Buck-Boost DC-DC Converter for USB PD

# Design guide

RD227-DGUIDE-01

## **TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION**

## **Table of Contents**

1.	Introduction4
2.	Components Used5
2.1.	Automotive Power MOSFET XPN7R104NC5
2.2.	Automotive Power MOSFET SSM6K804R6
2.3.	Automotive Power MOSFET XPN3R804NC7
2.4.	High-Side Gate Driver TPD7104AF8
3.	Buck-Boost DC-DC Converter9
3.1.	Outline of Operation9
3.2 3.2	Operation of Each Mode112.1. Buck Mode112.2. Boost Mode132.3. Buck-Boost Mode15
4.	Circuit Design16
4.1 4.1 4.1	Buck-Boost DC-DC Converter171.Bootstrap Circuit172.Buck Mode Operation183.Boost Mode Operation184.Buck-Boost Mode Operation19
4.2.	Power Switch and Reverse Connection Protection Circuit
4.3.	Shield Short Circuit Protection Circuit
5.	Performance22
5.1.	Switching MOSFET Characteristics

5.2.	Power Supply Efficiency23	3
5.3.	Temperature Rise	ł

## 1. Introduction

This Design Guide (hereafter referred to as this guide) describes the design of the Automotive Buck-Boost DC-DC Converter for USB PD (hereafter referred to as this power supply).

Recently, USB Power Delivery (hereafter referred to as USB PD) power supply (for recharging) has become popular for smart phones, tablets, laptop PC, etc. In response to the growing demand for power supply not only indoors but also inside vehicles, USB Type-C<sup>®</sup> connectors have been installed, and power supply by USB PD has become popular. Since the output voltage is determined by the power receiving device in USB PD, DC-DC converter for automotive USB PD requires a buck-boost converter to generate the output voltage from the vehicle battery voltage. This power supply is an H-bridge type buck-boost DC-DC converter with four switching elements. By using our small-package automotive MOSFETs as switching devices, we have realized an automotive buck-boost DC-DC converter that is highly efficient and has a small board mounting area.

We have prepared two types of automotive MOSFETs which are used in the H-bridge buck-boost DC-DC converter section of this power supply. Option 1 uses a <u>XPN7R104NC</u>, and Option 2 uses a <u>SSM6K804R</u>. In addition, our automotive MOSFET <u>XPN3R804NC</u> is used as a switching device in reverse-connection protection circuit and shield short-circuit protection circuit.

## 2. Components Used

This section introduces the components used in this power supply. We have an extensive lineup of automotive power semiconductor devices, including the components used this time.

#### 2.1. Automotive Power MOSFET XPN7R104NC

Option 1 of this power supply uses <u>XPN7R104NC</u> of  $V_{DSS}$  = 40 V (Max.),  $I_D$  = 20 A (Max.) for switching the buck-boost H-bridge.

#### Features

- AEC-Q101 qualified
- Small size, low profile and small mounting area
- Low on-resistance:  $R_{DS(ON)} = 5.6 \text{ m}\Omega \text{ (Typ.)} (V_{GS} = 10 \text{ V})$
- Low leakage current:  $I_{DSS} = 10 \ \mu A \ (Max.) \ (V_{DS} = 40 \ V)$
- Easy-to-use enhancement type:  $V_{th} = 1.5$  to 2.5 V ( $V_{DS} = 10$  V,  $I_D = 0.2$  mA)

#### Appearance and Terminal Layout





1, 2, 3: Source 4: Gate 5, 6, 7, 8: Drain

TSON Advance(WF)

### 2.2. Automotive Power MOSFET SSM6K804R

Option-2 of this power supply uses <u>SSM6K804R</u> of  $V_{DSS}$  = 40 V (Max.),  $I_D$  = 12 A (Max.) for switching the buck-boost H-bridge.

#### Features

- AEC-Q101 qualified
- MOSFET for 175 °C
- 4.5 V drive
- Low on-resistance

$$\begin{split} R_{DS(ON)} &= 12 \ m\Omega \ (Typ.) \ (@V_{GS} = 4.5 \ V) \\ R_{DS(ON)} &= 9 \ m\Omega \ (Typ.) \ (@V_{GS} = 10 \ V) \end{split}$$

#### **Appearance and Terminal Layout**



1: Drain 2: Drain 3: Gate 4: Source 5: Drain 6: Drain

4

3

### 2.3. Automotive Power MOSFET XPN3R804NC

<u>XPN3R804NC</u> of  $V_{DSS}$  = 40 V(Max.),  $I_D$  = 40 A(Max.) is used as MOSFET for the power switch, reverse-connection protection, and shielded short-circuit protection of this power supply.

#### Features

- AEC-Q101 qualified
- Small size, low profile and small mounting area
- Low on-resistance:  $R_{DS(ON)} = 3.0 \text{ m}\Omega \text{ (Typ.)} (V_{GS} = 10 \text{ V})$
- Low leakage current:  $I_{DSS} = 10 \ \mu A (Max.) (V_{DS} = 40 \ V)$
- Easy-to-use enhancement type:  $V_{th} = 1.5$  to 2.5 V ( $V_{DS} = 10$  V,  $I_D = 0.3$  mA)

#### **Appearance and Terminal Layout**





1, 2, 3: Source 4: Gate 5, 6, 7, 8: Drain

TSON Advance(WF)

### 2.4. High-Side Gate Driver TPD7104AF

<u>TPD7104AF</u> is used as a gate driver for the power switch and the reverse-connection protection MOSFET in this power supply.

#### Features

- Built-in charge pump circuit
- Built-in load short (overcurrent detection) and power reverse connection protection function
- Compact with surface mount package (PS-8)

#### **Appearance and Terminal Layout**



## 3. Buck-Boost DC-DC Converter

### 3.1. Outline of Operation

The configuration of the buck-boost DC-DC converter is shown in Fig. 3.1.



Fig. 3.1 Configuration of Buck-Boost DC-DC Converter

The non-inverting buck-boost DC-DC converter circuit, which combines a buck DC-DC converter circuit and a boost DC-DC converter circuit, can be more efficient by using synchronous rectification with MOSFET instead of the diodes as used in the buck DC-DC converter and the boost DC-DC converter. It contains four MOSFETs surrounding the inductor and is also called H-bridge buck-boost DC-DC converter. The buck-boost DC-DC converter is suitable for switching between step-up and step-down operation. It can output a constant voltage even when the input voltage fluctuates, such as with battery, and it can also change the output voltage depending on the output loads, such as in USB Power Delivery powered equipment. The buck-boost DC-DC converter has the following operating modes.

#### (1) Buck Mode (when the input voltage is sufficiently higher than the output voltage)

Switching  $Q_1$  and  $Q_2$  shown in Fig. 3.1 enables buck mode.  $Q_1$  and  $Q_2$  operate in a complementary fashion and  $Q_2$  behave as a synchronous rectifier. At this time,  $Q_4$  is fixed to on and  $Q_3$  is fixed to off.

#### (2) Boost Mode (when the input voltage is sufficiently lower than the output voltage)

Switching  $Q_3$  and  $Q_4$  shown in Fig. 3.1 enables boost mode.  $Q_3$  and  $Q_4$  operate in a complementary fashion and  $Q_4$  behave as a synchronous rectifier. At this time,  $Q_1$  is fixed to on and  $Q_2$  is fixed to off.

#### (3) Buck-Boost Mode (when input voltage $\approx$ output voltage)

If the input voltage  $\approx$  output voltage, the output voltage fluctuation becomes large in the stepdown mode or step-up mode. In the buck-boost mode, all Q<sub>1</sub> to Q<sub>4</sub> in Fig. 3.1 operate and correspond to the operation of the step-down mode and the step-up mode.

### 3.2. Operation of Each Mode

#### 3.2.1. Buck Mode

Fig. 3.2 shows the current path in buck mode. In buck operation,  $Q_1$  and  $Q_2$  are switched to control the voltage of SW1. At this time in the boost circuit,  $Q_3$  is fixed to off, and  $Q_4$  is fixed to on. The voltage of SW2 is  $V_{OUT}$ . When  $Q_1$  is on ( $Q_2$  is off), the current rises in the path of  $V_{IN}$ - $Q_1$ -Inductor L- $Q_4$ - $V_{OUT}$  to charge the L. When  $Q_1$  is off ( $Q_2$  is on), the stored energy in L is discharged along the path of GND- $Q_2$ -Inductor L- $Q_4$ - $V_{OUT}$  and the current is reduced. The waveforms of the current flowing through inductor L and the voltage across inductor L are shown in Fig. 3.3.



Fig. 3.2 Current Path in Buck Mode





The relationship between the input voltage and the output voltage is derived from the fact that the stored energy and the released energy of the inductor L are equal in Fig. 3.3. The following equation holds between the energy  $\Delta U_1$  accumulated in the inductor during  $Q_1$  on ( $Q_2$  off) period and the energy  $\Delta U_2$  (<0) released from the inductor during  $Q_1$  off ( $Q_2$  on) period:  $\Delta U_1 + \Delta U_2 = 0$ 

 $\Delta U_1$ ,  $\Delta U_2$  calculation is as follows; when the energy is accumulated in the inductor the current increases by  $\Delta i_{Q1}$ , and when the energy is released the current decreases by  $\Delta i_{Q2}$ ,  $Q_1$  on time is  $T_{on}$ , and the off time is  $T_{off}$ . (V<sub>IN</sub>-V<sub>OUT</sub> is applied when  $Q_1$  is ON and -V<sub>OUT</sub> is applied when  $Q_1$  is OFF)

$$\Delta U_1 = (V_{IN} - V_{OUT}) \cdot \Delta i_{Q1} \cdot T_{on}$$
$$\Delta U_2 = -V_{OUT} \cdot \Delta i_{Q2} \cdot T_{off}$$

From the above

 $(V_{IN}-V_{OUT}) \cdot \Delta i_{Q1} \cdot T_{on} - V_{OUT} \cdot \Delta i_{Q2} \cdot T_{off} = 0$ 

When a constant current is applied to the inductor,

$$\Delta i_{Q1} = \Delta i_{Q2}$$

Thus, it becomes

$$V_{OUT} = \frac{T_{on}}{T_{on} + T_{off}} V_{IN}$$
$$= \frac{T_{on}}{T} V_{IN}$$

Assuming that the ratio of  $T_{on}$  in the switching period T of  $Q_1$  is duty D,

$$V_{OUT} = D \cdot V_{IN}$$

If the switching frequency is  $f_{sw}$ , D is expressed by the following equation.

$$D = \frac{T_{on}}{T} = \frac{T_{on}}{T_{on} + T_{off}} = T_{on} \times f_{sw}$$

© 2023 Toshiba Electronic Devices & Storage Corporation

#### 3.2.2. Boost Mode

Fig. 3.4 shows the current path in boost mode. In boost operation,  $Q_3$  and  $Q_4$  are switched to control the voltage of SW2. At this time in the buck circuit,  $Q_1$  is fixed to on and  $Q_2$  is fixed to off. Thus, the voltage of SW1 is  $V_{IN}$ . When  $Q_3$  is on ( $Q_4$  is off), the current rises along the path of  $V_{IN}$ - $Q_1$ -Inductor L- $Q_3$ -GND to charge the Inductor L. When  $Q_3$  is off ( $Q_4$  is on), current flows through the path of  $V_{IN}$ - $Q_1$ -inductor L- $Q_4$ - $V_{OUT}$  based on the stored energy in the inductor L. The difference between the input voltage and the output voltage is applied to inductor L. The waveforms of the current flowing through inductor L and the voltage across inductor L are shown in Fig. 3.5.



Fig. 3.4 Current Path in Boost Mode



Fig. 3.5 Operation Waveforms in Boost Mode

The relationship between the input voltage and the output voltage is derived from the fact that the stored energy and the released energy of the inductor L are equal in Fig. 3.5. The following equation holds between the energy  $\Delta U_3$  accumulated in the inductor during Q<sub>3</sub> on (Q<sub>4</sub> off) period and the energy  $\Delta U_4$  (<0) released from the inductor during Q<sub>3</sub> off (Q<sub>4</sub> on) period:  $\Delta U_3 + \Delta U_4 = 0$ 

 $\Delta U_3$ ,  $\Delta U_4$  are calculated as follows; when the energy is accumulated in the inductor the current increase is  $\Delta i_{Q3}$ , and when the energy is released from the inductor the current decrease is  $\Delta i_{Q4}$ ,  $Q_3$  on time is  $T_{on}$ ', and the off time is  $T_{off}$ '. (V<sub>IN</sub> is applied when  $Q_3$  is ON and V<sub>IN</sub>-V<sub>OUT</sub> is applied when  $Q_3$  is OFF)

$$\Delta U_3 = V_{IN} \cdot \Delta i_{Q3} \cdot T_{on}'$$
$$\Delta U_4 = (V_{IN} \cdot V_{OUT}) \cdot \Delta i_{Q4} \cdot T_{off}'$$

From the above

 $V_{IN} \cdot \Delta i_{Q3} \cdot T_{on}' + (V_{IN} \cdot V_{OUT}) \cdot \Delta i_{Q4} \cdot T_{off}' = 0$ 

When a constant current is applied to the inductor,

 $\Delta i_{Q3} = \Delta i_{Q4}$ 

Thus, it becomes

$$V_{OUT} = \frac{T_{on'} + T_{off'}}{T_{off'}} V_{IN}$$
$$= \frac{T}{T_{off'}} V_{IN}$$

Assuming that the duty D' is the ratio of  $T_{\text{on}}{}^{\prime}$  in  $Q_3$  switching period T

$$V_{OUT} = \frac{1}{1 - D'} V_{IN}$$

If the switching frequency is  $f_{sw}$ , D is expressed by the following equation.

$$D' = \frac{T_{on}'}{T} = \frac{T_{on}'}{T_{on}' + T_{off}'} = T_{on}' \times f_{sw}$$

#### 3.2.3. Buck-Boost Mode

In order to achieve the input voltage  $\approx$  output voltage, particularly the voltage ratio 1 in the buck mode and boost mode, in buck mode from the I/O voltage relation expression V<sub>OUT</sub> = D · V<sub>IN</sub>, Q<sub>1</sub> duty needs to be D=1, and in the boost mode from the I/O voltage relation expression V<sub>OUT</sub>=1/ (1-D') V<sub>IN</sub>, Q<sub>3</sub> duty needs to be D'=0. However, since such switching is not realistic, the IC operates in the buck-boost mode when input voltage  $\approx$  output voltage.

As described above, the relationship between the input voltage and the output voltage in the buck mode is as follows.

$$V_{OUT} = \frac{T_{on}}{T_{on} + T_{off}} V_{IN}$$
$$= \frac{T_{on}}{T} V_{IN}$$

( $T_{on}$ : Buck switch  $Q_1$  on time,  $T_{off}$ : Buck switch  $Q_1$  off time)

The relationship between the input voltage and the output voltage in boost mode is shown below.

$$V_{OUT} = \frac{T}{T_{off}} V_{IN}$$

( $T_{on}$ ': Boost switch  $Q_3$  on time,  $T_{off}$ ': Boost switch  $Q_3$  off time)

In the buck-boost mode, the operation is such that the output on the buck circuit side becomes the input of the boost circuit side. Therefore, the relationship between the input voltage and the output voltage is expressed by the following equation.

$$V_{OUT} = V_{IN} \frac{T_{on}}{T} \times \frac{T}{T_{off}}$$

When  $V_{IN}$ ,  $V_{OUT}$  or T (switching period) is determined for the buck mode or boost mode, the requirements of the switching elements are determined in one way. However, even if  $V_{IN}$  and  $V_{OUT}$  are determined, both the switching element  $Q_1$  on the buck side and the switching element  $Q_3$  on the boost side can be operated in various ways. There may also be cases where T (switching period) differs between the buck circuit side and the boost circuit side, or where the switching period fluctuates.

## 4. Circuit Design

This section describes the gist of the circuit design. This power supply uses a MAX25432 (hereafter referred to as this controller) manufactured by Analog Devices as a controller IC. Refer to MAX25432 data sheet and related documentation for detailed information on component circuit design.

Refer to RD227-SCHEMATIC1 (Option 1) or RD227-SCHEMATIC2 (Option 2) for schematic diagrams and to RD227-BOM1 (Option 1) or RD227-BOM2 (Option 2) for bill of materials. Fig. 4.1 shows the block diagram of this power supply.



Fig. 4.1 Block Diagram of Automotive Buck-Boost DC-DC Converter for USB PD

#### 4.1. Buck-Boost DC-DC Converter

Fig. 4.2 shows the basic circuit of the buck-boost DC-DC converter.



Fig. 4.2 Basic Circuit of Buck-Boost DC-DC converter

#### 4.1.1. Bootstrap Circuit

The high-side MOSFET of the buck-boost H-bridge,  $Q_1$  and  $Q_4$  gate-drive supplies are generated by a capacitor-diode bootstrap. Fig. 4.3 shows the bootstrap circuit. The capacitor  $C_1$  is MOSFET  $Q_1$ gate drive power supply (BST1) and the capacitor  $C_2$  is MOSFET  $Q_4$  gate drive power (BST2). When  $Q_2$  is on,  $C_1$  is charged via  $V_{CC}$ - $D_{B1}$ - $C_1$ - $Q_2$  path relative to  $Q_1$  source (LX1). Similarly, when  $Q_3$ is on,  $C_2$  is charged via  $V_{CC}$ - $D_{B2}$ - $C_2$ - $Q_3$  path relative to LX2 of  $Q_4$  source (LX2).



Fig. 4.3 Bootstrap Circuit

#### 4.1.2. Buck Mode Operation

In Fig. 4.2,  $Q_1$  and  $Q_2$  are switched to perform the buck-mode operation.  $Q_1$  and  $Q_2$  operate in a complementary fashion, and  $Q_2$  performs synchronous rectification.  $Q_4$  of the boost circuit is fixed to ON, and  $Q_3$  is fixed to OFF, so the operation is the same as that of the buck DC-DC converter circuit. Fig. 4.4 shows  $Q_1$  to  $Q_4$  gate signal control in buck-mode operation.



#### Fig. 4.4 Gate Signal Control Example in Buck Mode Operation

If  $Q_1$  on time is  $T_{on}$  and the off time is  $T_{off}$ , the input voltage  $V_{IN}$  and output voltage  $V_{OUT}$  are related as follows.

$$V_{OUT} = \frac{T_{on}}{T_{on} + T_{off}} V_{IN}$$
$$= \frac{T_{on}}{T} V_{IN}$$
$$= D \cdot V_{IN}$$

(T: Q<sub>1</sub>, Q<sub>2</sub> switching period, D: On duty of Q<sub>1</sub>)

#### 4.1.3. Boost Mode Operation

In Fig. 4.2,  $Q_3$  and  $Q_4$  can be switched for boost mode operation.  $Q_3$  and  $Q_4$  operate in a complementary fashion and  $Q_4$  behave as a synchronous rectifier.  $Q_1$  of the buck circuit is fixed to on, and  $Q_2$  is fixed to off. This operation is similar to that of the boost DC-DC converter circuit. Fig. 4.5 shows  $Q_1$  to  $Q_4$  gate signal control in boost mode.





When  $Q_3$  on time is  $T_{on}$ ' and the off time is  $T_{off}$ ', the input voltage  $V_{IN}$  and output voltage  $V_{OUT}$  are related as follows.

$$V_{OUT} = \frac{T_{on}' + T_{off}'}{T_{off}'} V_{IN}$$
$$= \frac{T}{T_{off}'} V_{IN}$$
$$= \frac{1}{1 - D'} V_{IN}$$

(T: Q<sub>3</sub>, Q<sub>4</sub> switching period, D': On duty of Q<sub>3</sub>)

#### 4.1.4. Buck-Boost Mode Operation

When the input voltage  $V_{IN} \approx$  output voltage  $V_{OUT}$ , buck-boost mode operation is performed, and boost mode operation and buck mode operation are alternately performed to stabilize the output voltage. Fig. 4.6 shows  $Q_1$  to  $Q_4$  gate-signal control in Buck-Boost mode. In the Fig. 4.6, when  $Q_3$ is off and  $Q_4$  is on,  $Q_1$  and  $Q_2$  are switched, and when,  $Q_1$  is on and  $Q_2$  is off,  $Q_3$  and  $Q_4$  are switched.



Fig. 4.6 Gate Signal Control Example in Buck-Boost Mode Operation

#### 4.2. Power Switch and Reverse Connection Protection Circuit

Fig. 4.7 shows the power switch and reverse connection protection circuit. In the power supply input section, two MOSFETs with their sources connected in common are connected in two stages (back-to-back connection), the first stage acts as a power switch and the second stage acts as a reverse connection protection switch. These MOSFETs are driven by the high-side gate driver TPD7104AF, and when the power is normally supplied, the gates are driven and these two MOSFET are turned on to supply the power to the buck-boost DC-DC converter circuit. However, in case of reverse connection of power supply, the gates of these two MOSFETs are not turned on, and since the body diodes of these two MOSFETs are connected in reverse (because of back-to-back connection), the overall switch is turned off, thus protecting the buck-boost DC-DC converter circuit from the reverse voltage.



Fig. 4.7 Power Switch and Reverse Connection Protection Circuit

### 4.3. Shield Short Circuit Protection Circuit

The battery shield short protection circuit is shown in Fig. 4.8. It protects the circuit from shortcircuit of the shield and battery power supply if the shield at the end of USB Type-C<sup>®</sup> cable touches the cigarette lighter socket. As shown in Fig. 4.8, the negative terminal of the Power Out connector is connected via a shielded short-circuit protective MOSFET rather than directly to ground within the power supply. The negative terminal (shield potential) of the power connector is monitored by the SHLD\_SNS (shield sense) pin of this controller. When the voltage at the connector shield is detected, the shield short-circuit protective MOSFET is turned off by GDRV signal. This prevents a short circuit between the shield and the battery.



Fig. 4.8 Shield Short Circuit Protection Circuit

### 5. Performance

#### 5.1. Switching MOSFET Characteristics

MOSFET used in the buck-boost DC-DC converter circuit of Option 1 and Option 2 of this power supply are shown in Table 5.1.

		Option 1	Option 2			
	Equipped MOSFET	XPN7R104NC	SSM6K804R			
Dackage	Name	TSON Advance(WF)	TSOP6F			
Package	Size	3.1 x 3.6 mm	2.9 x 2.8 mm			
	Rated drain-source voltage	40 V	40 V			
CS	Rated channel temperature	175 ℃	175 °C			
Characteristics	Drain-source on-resistance (Max.)	14.2 mΩ @V <sub>GS</sub> = 4.5 V	18 mΩ @V <sub>GS</sub> = 4.5 V			
Chara	Total gate charge (Typ.)	10 nC @V <sub>DD</sub> = 32 V V <sub>GS</sub> = 4.5 V $I_D$ = 20 A	7.5 nC @V <sub>DD</sub> = 20 V V <sub>GS</sub> = 4.5 V $I_D$ = 12 A			

#### Table 5.1 Characteristics of Switching MOSFET Used in Each Option

#### **5.2.** Power Supply Efficiency

The power supply efficiency varies depending on the load conditions and I/O voltage conditions. Fig. 5.1 shows the example of measured efficiency curves under each I/O voltage condition.

Generally, in the light load region (output current is small), the conduction loss of the switching element is small, and the percentage of the switching loss of each element is high. In the light load region, Option 2 tends to be more efficient than Option 1 because it uses a smaller-gate-inputcharge MOSFET. On the other hand, in the heavy load region (where the output current is large), the conduction loss in proportion to the current due to the on-resistance of the switching element accounts for a large percentage of the total loss. Therefore, under heavy loads, Option 1 tends to be more efficient as it uses a MOSFET with a smaller on-resistance.



Fig. 5.1 Power Supply Efficiency Example in Each Condition

Operation environment : Convection cooling

#### 5.3. Temperature Rise

Fig. 5.2 shows the measurement results of MOSFET surface temperature rise  $\Delta T$  under various input/output voltage conditions.

The maximum rated MOSFET channel temperature is 175 °C, and after derating it by 80% it becomes 140 °C. Considering the maximum ambient temperature of 85 °C, the allowable temperature rise becomes 55 °C (140 °C - 85 °C). The measured temperature rise shown in Fig. 5.2 has a considerable margin compared to the 55 °C.

Boost Mode 10.5 V ➡ 15 V/3 A (45 W)



TYPE1 (15 W) TYPE2 (15 W) Buck-side Low-side MOSFET



0 °r





- \* USB Type-C<sup>®</sup>, USB-C<sup>®</sup> are registered trademarks of USB Implementers Forum.
- X Company names, product names, and service names may be trademarks of their respective

#### companies.

#### Terms of Use

This terms of use is made between Toshiba Electronic Devices and Storage Corporation ("We") and customers who use documents and data that are consulted to design electronics applications on which our semiconductor devices are mounted ("this Reference Design"). Customers shall comply with this terms of use. Please note that it is assumed that customers agree to any and all this terms of use if customers download this Reference Design. We may, at its sole and exclusive discretion, change, alter, modify, add, and/or remove any part of this terms of use at any time without any prior notice. We may terminate this terms of use at any time and for any reason. Upon termination of this terms of use, customers shall destroy this Reference Design. In the event of any breach thereof by customers, customers shall destroy this Reference Design, and furnish us a written confirmation to prove such destruction.

#### 1. Restrictions on usage

1. This Reference Design is provided solely as reference data for designing electronics applications. Customers shall not use this Reference Design for any other purpose, including without limitation, verification of reliability.

2. This Reference Design is for customer's own use and not for sale, lease or other transfer.

3. Customers shall not use this Reference Design for evaluation in high or low temperature, high humidity, or high electromagnetic environments.

4. This Reference Design shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.

#### 2. Limitations

1. We reserve the right to make changes to this Reference Design without notice.

2. This Reference Design should be treated as a reference only. We are not responsible for any incorrect or incomplete data and information.

3. Semiconductor devices can malfunction or fail. When designing electronics applications by referring to this Reference Design, customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of semiconductor devices could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Customers must also refer to and comply with the latest versions of all relevant our information, including without limitation, specifications, data sheets and application notes for semiconductor devices, as well as the precautions and conditions set forth in the "Semiconductor Reliability Handbook".

4. When designing electronics applications by referring to this Reference Design, customers must evaluate the whole system adequately. Customers are solely responsible for all aspects of their own product design or applications. WE ASSUME NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.

5. No responsibility is assumed by us for any infringement of patents or any other intellectual property rights of third parties that may result from the use of this Reference Design. No license to any intellectual property right is granted by this terms of use, whether express or implied, by estoppel or otherwise.

6. THIS REFERENCE DESIGN IS PROVIDED "AS IS". WE (a) ASSUME NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (b) DISCLAIM ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO THIS REFERENCE DESIGN, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.

#### 3. Export Control

Customers shall not use or otherwise make available this Reference Design for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). This Reference Design may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of this Reference Design are strictly prohibited except in compliance with all applicable export laws and regulations.

#### 4. Governing Laws

This terms of use shall be governed and construed by laws of Japan.