TPD7106F
Application Note

Description

TPD7106F is a high-side gate driver IC for N-channel MOSFET with 12 V power. MOSFET used is driven by an internal charge-pump circuit (externally connected to a capacitor). By selecting the most suitable MOSFET for your application, you can configure the most suitable high-side switch from small to large currents. This IC has a built-in protection function for reverse-connection of the power supply in addition to the charge pump voltage drop detection function and diagnostic output function, which contributes to improved system safety. In addition, a rapid off command can be received to turn off the external MOSFET.

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1. Product overview

Mechanical relays have long been widely known as switches that cut off and connect the power supply line from a battery or other power source to the load. However, mechanical relays have problems in durability because they mechanically open and connect contacts repeatedly, and semiconductor relays using semiconductor elements are becoming increasingly popular in applications where long-term reliability is required. With the increasing number of systems, the current capability required of semiconductor relays is increasing year by year, and it is desirable to realize high-current semiconductor relays with low-loss and low heat generation by using load switch circuits using discrete N-channel MOSFET with low on-resistance.

TPD7106F is an N-channel MOSFET gate driver for 1-output high-side switches with a built-in charge pump circuitry. Combined with an external discrete N-channel MOSFET, high-side switches for high-current applications can be configured. In addition, unlike mechanical relays, the configuration of this semiconductor relay has no contact wear, so maintenance-free operation can be realized. In the event of an error, the microcontroller controls the turn-off function independently of the microcontroller using the I/O pins that rapidly control turn-off to protect MOSFET, thereby ensuring safe operation.

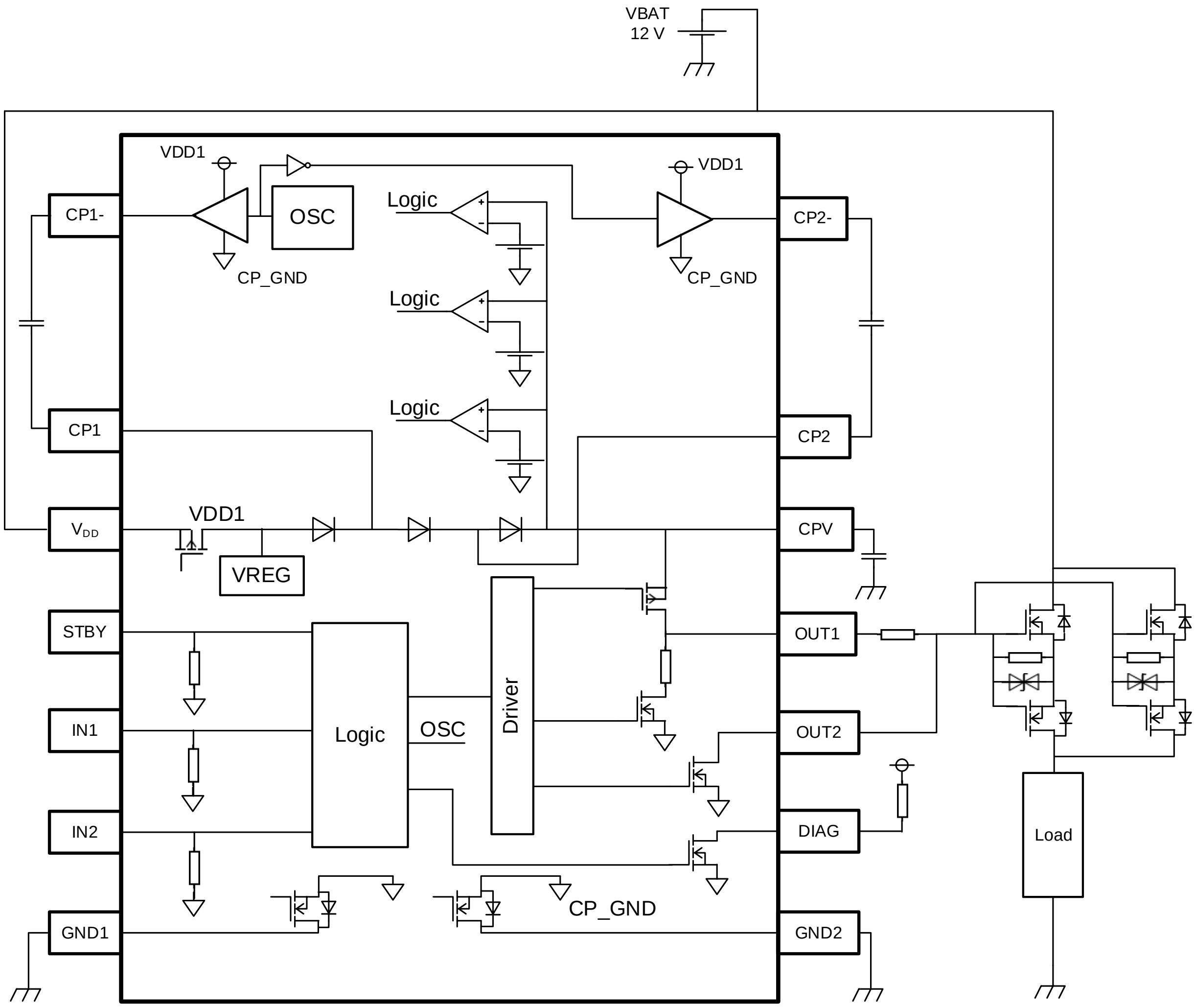


Fig. 1.1 TPD7106F and driving MOSFET group

1.1. I/O pins of TPD7106F

Table 1.1 Pin Description

Pin No	Symbol	Description
1	CP1-	The terminal for charge pump capacitor connection.
2	TEST	The terminal for and internal circuit test. Normal operation = connect to Ground.
3	CP1	The terminal for charge pump capacitor connection.
4	V_{DD}	Power supply pin.
5	STBY	Standby mode control pin.
6	IN1	Input pin. Built in pull down resistor. (for Normal operation)
7	IN2	Input pin. Built in pull down resistor. (for rapid off)
8	GND1	Ground pin.
9	GND2	Ground pin.
10	DIAG	Diagnostic output (Open drain).
11	OUT2	Output pin for an external N-channel MOSFET drive (for rapid off)
12	OUT1	Output pin for an external N-channel MOSFET drive (for Normal switching)
13	CPV	Output of charge pump voltage.
14	CP2	The terminal for charge pump capacitor connection.
15	N.C	No-Connect pin.
16	CP2-	The terminal for charge pump capacitor connection.

1.2. Compare products (TPD7104AF, TPD7106F, TPD7107F)

The following table shows the main differences between our 1-channel high-side N-channel MOSFET gate driver ICs. Depending on the product, highly safe protection functions such as power supply reverse connection protection and GND disconnection protection are built in. The TPD7106F features an output source current of 10 mA, an output sink current of 0.4 A, and the ability to turn on/off parallel-connected MOSFETs. Also, the method of controlling the external MOSFET during protection operation differs depending on the product, so consider these points when selecting an appropriate product.

Table 1.2 Product comparison

Item	TPD7104AF	TPD7106F	TPD7107F
Wafer process	BiCD0.13 µm	BiCD0.13 µm	BiCD0.13 µm
Power Supply Voltage (DC)	24 V	27 V	26 V
Power Supply Voltage (Pulse)	40 V (t≤300 ms)	40 V (t≤500 ms)	36 V (t≤400 ms)
Output source current	100 µA	10 mA	100 µA
Output sink current	5 mA	0.4 A	5 mA / 230 mA (Note2)
Reverse Battery protection method (Note1)	MOSFET OFF	MOSFET OFF	MOSFET ON
GND open protection.	-	-	✓
Package.	PS-8	SSOP16	WSON10A

Note1: Difference in external MOSFET operation when the power is reversed.

MOSFET ON: To reduce losses, the MOSFET is turned on and current flows.

MOSFET OFF: MOSFET and apply current to the MOSFET body diodes. To interrupt the current, connect an additional driver IC+ MOSFET so that the drain and drain are connected.

Note2: Switches to rapid off operation when an abnormality is detected.

2. Product features

The functions of TPD7106F include on/off control and quick off control of external MOSFET by input signal. It also has a built-in charge pump circuit (a capacitor is provided externally). It has a built-in charge pump voltage low voltage detection function, diagnostic output, and protection against reverse power supply connection.

2.1. Control of external MOSFET

The charge pump and the driving circuitry operate upon receiving the external N-channel MOSFET control signal from the input pin IN1. Drive the transistor M1 shown in Fig. 2.1 (M2 is off) to turn on MOSFET (Q1, Q2 (@V_{IN1}=V_{IH}) with enough gate-voltage (V_{OUT1}=V_{DD}+12 V (typ.)). By driving M2 (M1 is off), MOSFET is turned off (driver on resistance = 630 Ω (typ.) (@V_{IN1}=V_{IL}).

V_{IN1}: Input voltage of IN1 pin
V_{IH}: High-level input voltage
V_{IL}: Low-level input voltage
V_{OUT1}: Output voltage of OUT1 pin

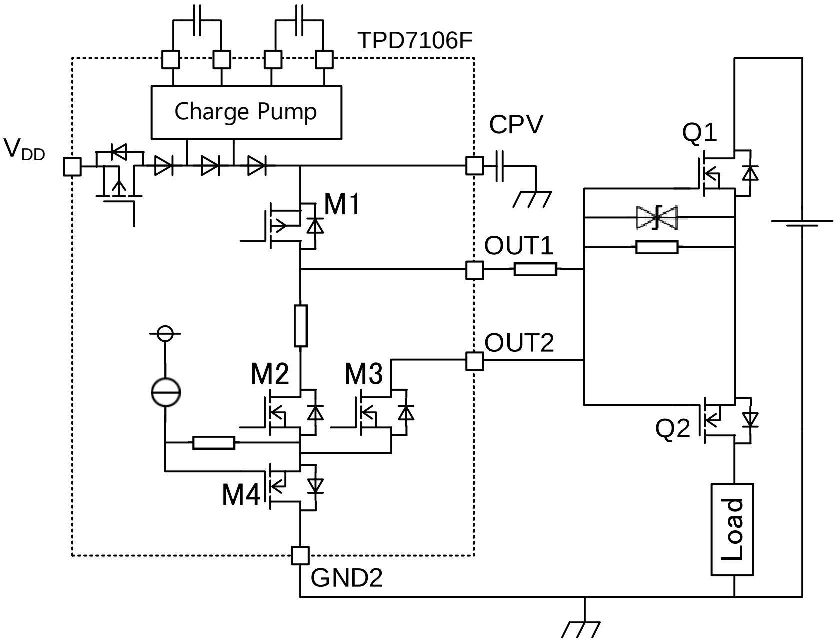
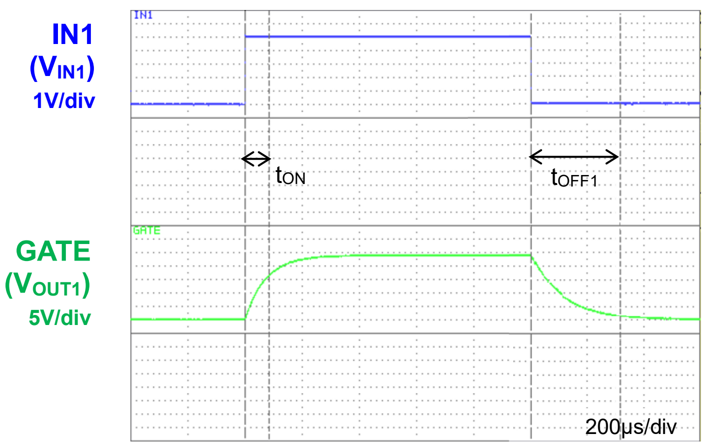


Fig. 2.1 Control of external MOSFET



t_{ON}, t_{OFF1}
Switching time

Fig. 2.2 I/O waveform

2.2. Function to quickly turn off external MOSFET

To turn off the external MOSFET immediately, use the input pin IN2. Connect OUT2 to OUT1 output path (Fig. 2.1). Drive M3 (M1 is off) to quickly lower the gate-voltage and turn off the external MOSFET (Q1, Q2) (@V_{IN2}=V_{IH}).

V_{IN2}: Input voltage of IN2 pin
V_{OUT2}: Output voltage of OUT2 pin

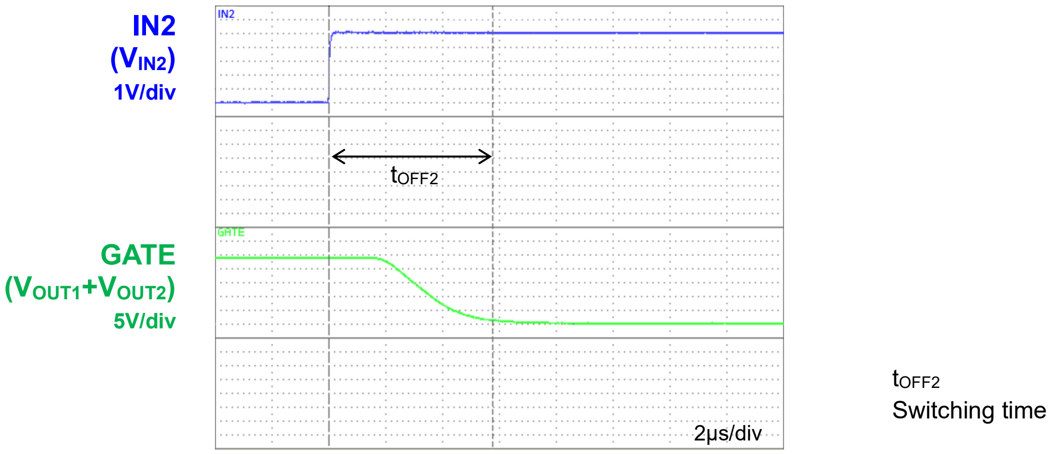


Fig. 2.3 Rapid off control waveform

Table 2.1 Truth table

IN1	IN2	STBY	OUT1	OUT2	Condition
X (Note 1)	X	L	Hiz (Note 2)	Hiz	Standby mode
L	L	H	L	Hiz	Normal operation
H	L	H	H	Hiz	
L	H	H	L	L	Rapid Off Mode
H	H	H	L	L	

Note 1: Don't care.
Note 2: High impedance.

2.3. Charge pump circuit

The charge pump circuit is a step-up power supply circuit for generating the external N-channel MOSFET gate-drive voltage. For the high-side switch, the source potential is approximately equal to the supply voltage when the N-channel MOSFET is turned on. To maintain the on-state, a voltage equal to the supply voltage + 10 to 15 V and higher than the supply voltage must be applied to the gate. A charge pump circuit is a circuit that generates a voltage equal to or greater than this power supply voltage inside IC.

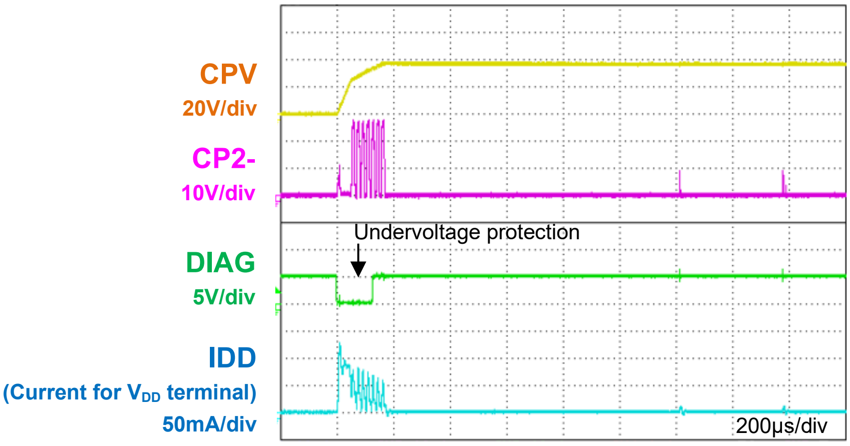


Fig. 2.4 Rising of charge pump voltage (V_{CPV}) after releasing standby

2.4. Low voltage detection function of charge pump voltage

TPD7106F monitors CPV terminal voltage and detects a charge pump voltage drop. When the voltage falls below the charge-pump low judgment voltage V_{CPL} (V_{DD}+4.7V (typ.)), DIAG pin becomes L state. Output pin OUT1, OUT2 keeps operating. When STBY pin is set to the L state, the charge pump is stopped because the IC is in the standby mode.

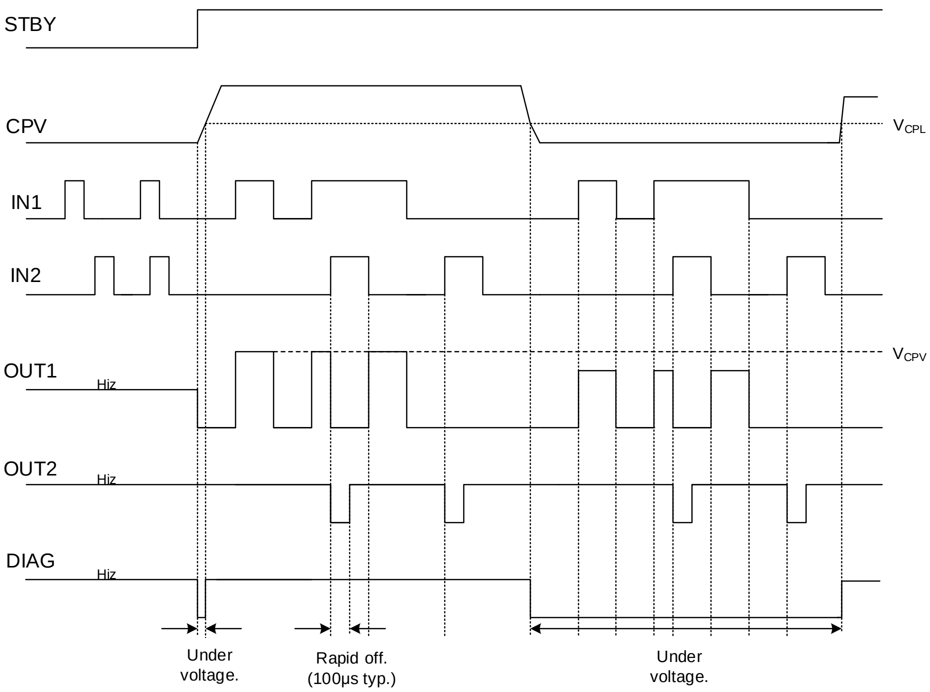


Fig. 2.5 Low voltage detection function of charge pump voltage

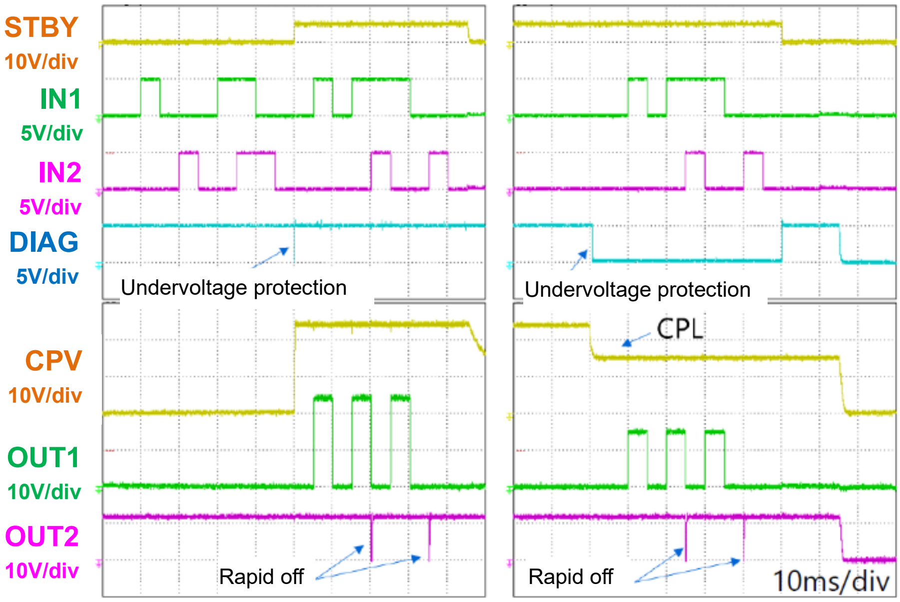


Fig. 2.6 Low voltage detection waveform

2.5. Power reverse connection protection function

When the power supply is connected in the reverse-polarity, M1 and M2 are turned off, the current from GND terminal is cut off by M4, M5, and the external MOSFET is turned off.

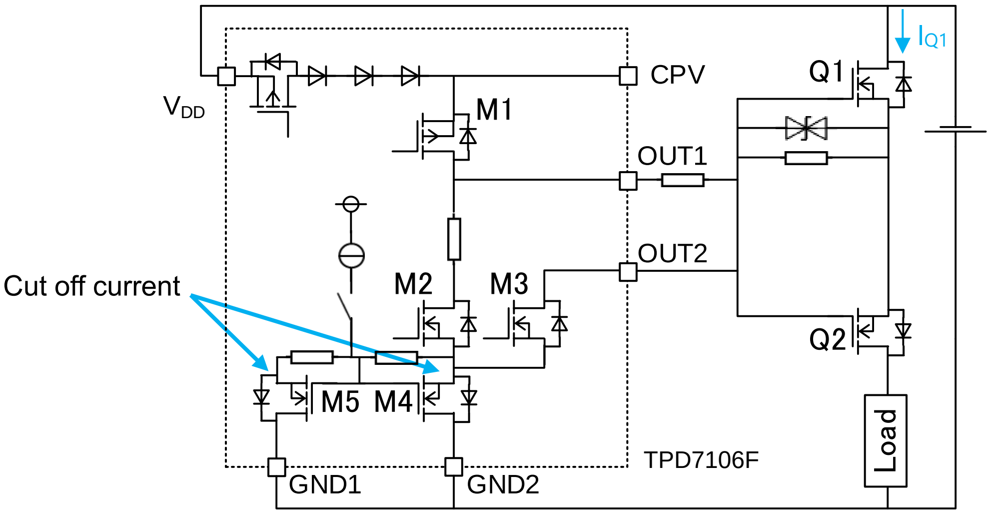


Fig. 2.7 Behavior of power reverse connection

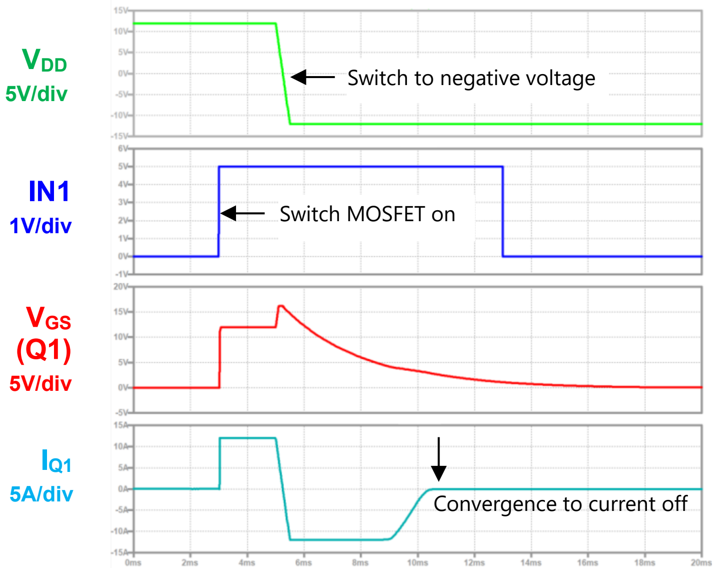


Fig. 2.8 Behavior of power reverse connection (simulation)

3. Electrical characteristics measurement circuit diagram

3.1. Switching time measuring circuit 1 (t_{ON}, t_{OFF1})

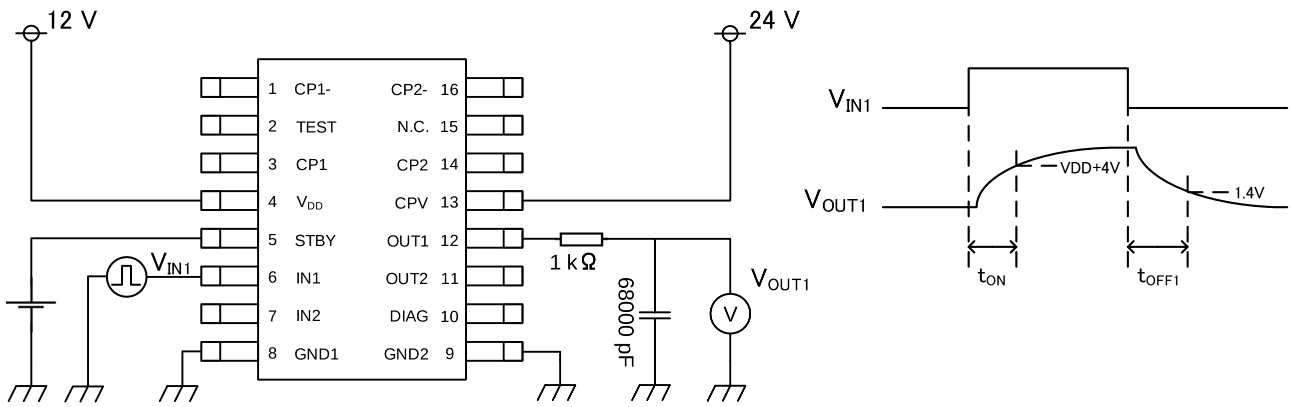


Fig. 3.1 Switching time measurement circuit 1

The switching time of the TPD7106F is affected by the load capacitance it drives. When using this product to switch the power supply path (cut one power supply path and then connect the other power supply path), take these into consideration. As a reference, when the load condition (CL=68000 pF) circuit in Fig. 3.1 is simulated with a simple SPICE model (typ. conditions), the switching time: rising t_{ON} is 0.15 ms, and falling t_{OFF1} is 0.4 ms. Consider these switching times when designing so that different power supply paths are not short-circuited during switching.

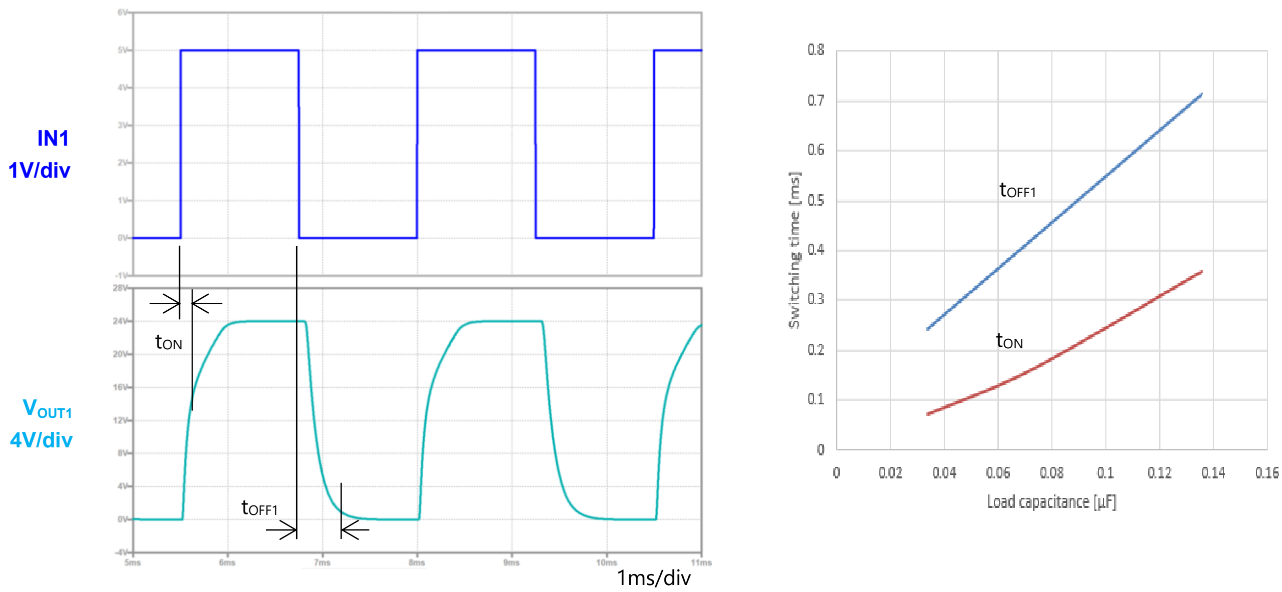


Fig. 3.2 Switching time and load capacitance (simulation)

3.2. Switching time measuring circuit 2 (t_{OFF2})

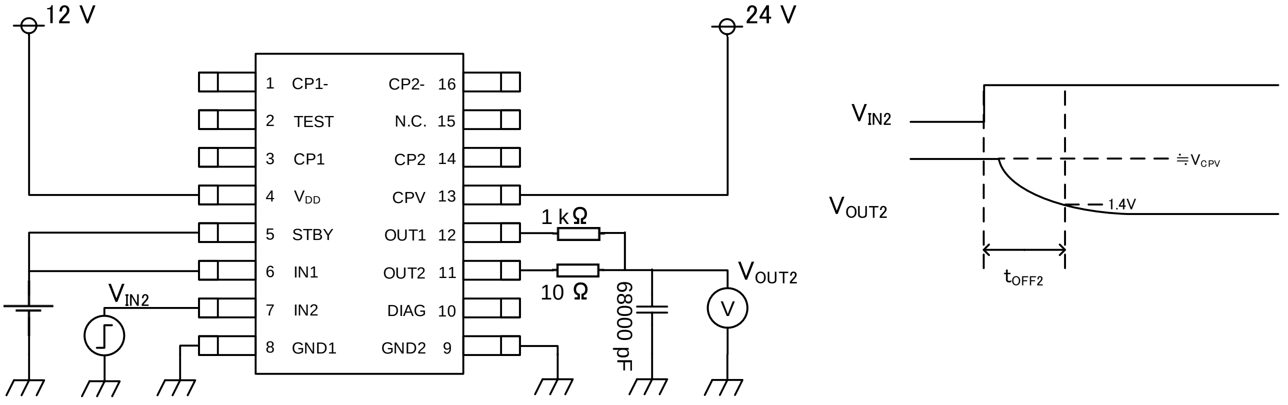


Fig. 3.3 Switching time measurement circuit 2

3.3. Output current measurement circuit with power reverse connection

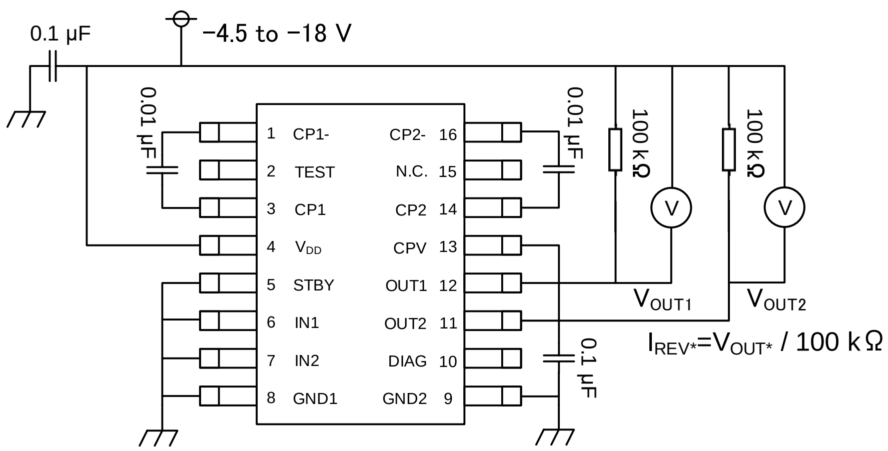


Fig. 3.4 Output current measurement circuit with power reverse connection

4. Terminal equivalent circuit diagram

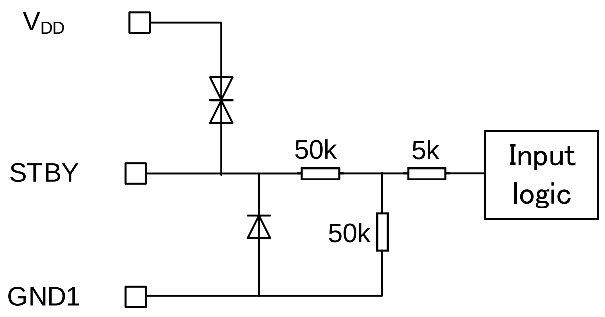


Fig. 4.1 STBY terminal equivalent circuit

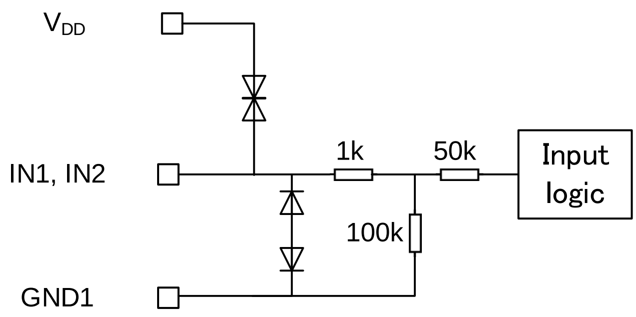


Fig. 4.2 IN1, IN2 terminal equivalent circuit

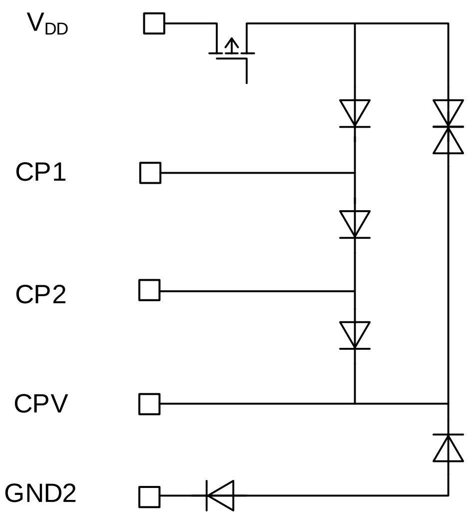


Fig. 4.3 CP1, CP2, CPV terminal equivalent circuit

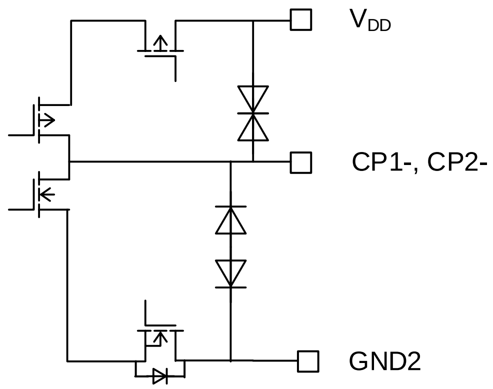


Fig. 4.4 CP1-, CP2- terminal equivalent circuit

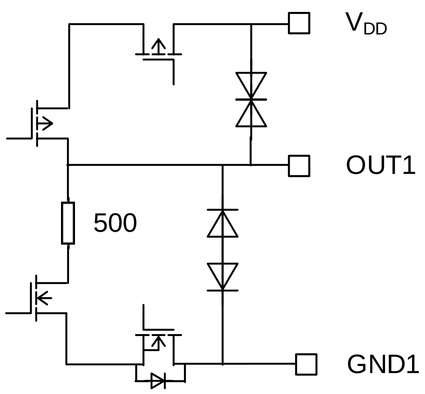


Fig. 4.5 OUT1 terminal equivalent circuit

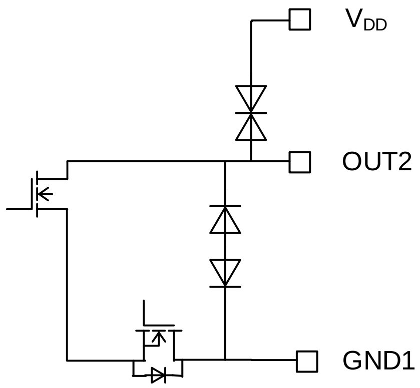


Fig. 4.6 OUT2 terminal equivalent circuit

*) Resistance unit: [Ω]

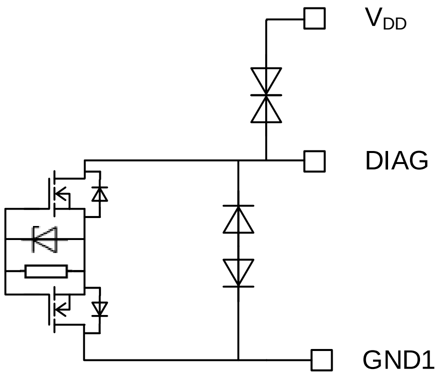


Fig. 4.7 DIAG terminal equivalent circuit

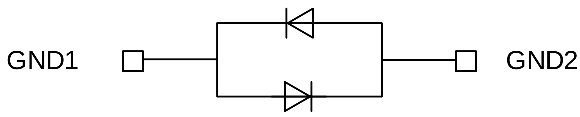
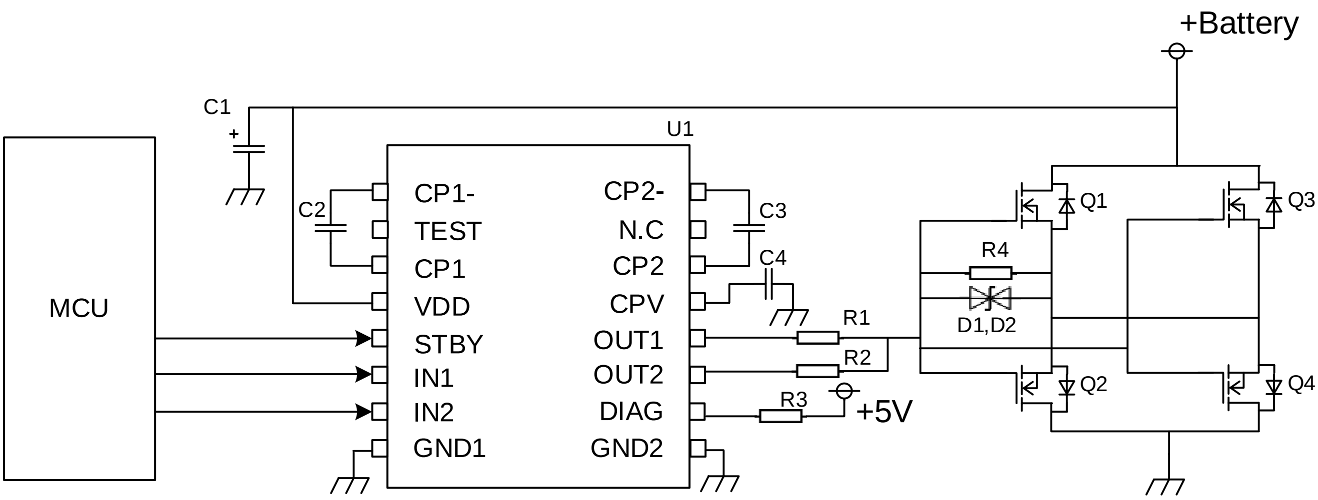


Fig. 4.8 GND1, GND2 equivalent circuit

5. Application circuit example (When 2 MOSFETs are connected in parallel)



U1:	TPD7106F
Q1, Q2, Q3, Q4:	Nch MOSFET / 40 V
D1, D2:	CRZ16
R1:	1 kΩ
R2:	10 Ω
R3:	10 kΩ
R4:	200 kΩ
C1:	10 µF / 50 V
C2, C3:	0.1 µF / 50 V
C4:	1 µF / 50 V

Note: Capacitors for the power supply lines should be connected as close to the IC as possible.

Fig. 5.1 Application circuit example

6. Explanation of terms

6.1. Absolute maximum rating

Table 6.1 Absolute maximum ratings

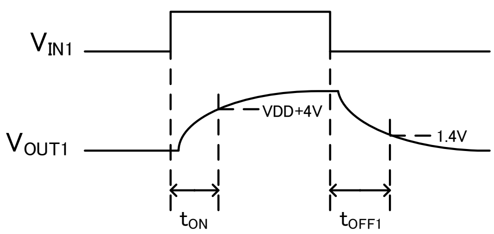
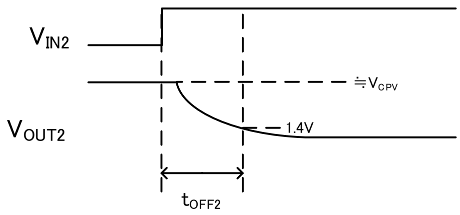
Term	Symbol	Descripition
Line voltage (DC)	$V_{DD\ (1)}$	DC-voltage rating that does not cause breakdown, property degradation, or reliability degradation of IC when applied to V_{DD} terminals.
Power supply voltage (pulse)	$V_{DD\ (2)}$	Pulse-voltage rating that does not cause breakdown, property degradation, or reliability degradation of IC when applied to V_{DD} terminals.
Input voltage (1)	V_{STBY}	The voltage-rating at which IC does not break, deteriorate properties, or degrade reliability when applied to STBY terminals.
Input voltage (2)	V_{IN1}, V_{IN2}	The voltage-rating at which IC does not break, deteriorate properties, or degrade reliability when applied to IN1, IN2 terminals.
CPV power	V_{CPV}	The voltage-rating at which IC does not break, deteriorate properties, or degrade reliability when applied to CPV terminals.
TEST terminal voltage	V_{TEST}	The voltage-rating at which IC does not break, deteriorate properties, or degrade reliability when applied to TEST terminals.
Output current (source)	$I_{OUT1\ (1)}$	The current rating at which IC can flow out of the output terminals that will not cause breakdown, property degradation, or reliability degradation.
Output current (sink)	$I_{OUT1\ (2)}$	The current rating that a IC can draw from its output terminals that will not destroy, degrade properties, or degrade reliability.
Output current (sink)	I_{OUT2}	The current rating that a IC can draw from its output terminals that will not destroy, degrade properties, or degrade reliability.
Diagnostic output voltage	V_{DIAG}	The voltage-rating at which IC does not break, deteriorate properties, or degrade reliability when applied to DIAG terminals.
Diagnostic output current	I_{DIAG}	The current rating at which IC can flow to DIAG terminals that will not cause breakdown, property degradation, or reliability degradation.
Power dissipation	P_D	Max allowable power dissipation for the entire operating area without IC corruption, etc.
Operating temperature	T_{opr}	Ambient temperature-range for normal operation of IC.
Junction temperature	T_j	Max junction temp. allowed for IC operation.
Storage temperature	T_{stg}	Ambient temperature range that can be stored or transported without applying voltage.

6.2. Electrical characteristics

Table 6.2 Electrical characteristics 1

Term	Symbol	Description
Power voltage for driving	V_{DD}	Supply voltage range for guaranteed normal operation and electric properties of IC at the preset junction temperature range.
Current consumption	$I_{DD\ (1)}$	At a junction temperature of 25°C, the current flowing to V_{DD} terminal (12 V) when the input voltage V_{STBY} is kept at a voltage lower than V_{IL} and IC is switched off.
Current consumption	$I_{DD\ (2)}$	Current flowing at V_{DD} terminal when IC is switched off by keeping the input voltage V_{STBY} higher than V_{IH} and V_{IN1}, V_{IN2} lower than V_{IL} at the default junction temperature. The capacitance elements to be placed between the terminal CP1/CP1-and CP2/CP2-shall be 0.01 µF, respectively.
Current consumption	$I_{DD\ (3)}$	The current flowing into V_{DD} terminal when IC is activated, keeping the input voltage V_{IN} above V_{IH} at the default junction temperature. The capacitance elements to be placed between the pin CP1/CP1-and CP2/CP2-shall be 0.01 µF and the pin OUT1, OUT2 shall be open, respectively.
High-level input voltage	V_{IH}	Minimum-voltage on the input-terminal IN1, IN2, STBY that ensures that the internal control circuitry operates normally and that the external N-channel MOSFET is activated at the specified junction temperature.
Low-level input voltage	V_{IL}	Max voltage on the input-terminal IN1, IN2 that ensures that the internal control circuitry operates normally and shuts off the external N-channel MOSFET at the specified junction temperature. Or, the max voltage of the input-pin STBY that ensures that the internal circuitry is in standby.
Input current	I_{IH}	Current that flows into each terminal when a voltage specified in the measurement condition is applied to the input terminal IN1, IN2, STBY at the specified junction temperature range.
Input current	I_{IL}	Current that flows out of each terminal when a voltage specified by the measurement condition is applied to the input terminal IN1, IN2, STBY at a specified junction temperature range.
High level output voltage	V_{OH1} V_{OH2} V_{OH3}	Voltage value that is output to the output terminal OUT1 when voltage and current specified by the measuring conditions are applied at the preset junction temperature range.
Output clamp voltage	V_{OCL}	Voltage clamping value of OUT1 at the output terminal when the specified voltage is applied at the specified junction temperature.
Low level output voltage	V_{OL1} V_{OL2}	The output voltage of the output terminal OUT1 and OUT2 when the voltage and current specified in the measuring conditions are applied at the specified junction temperature range.
Diagnostic output leakage current	I_{DIAGH}	Leakage current flowing through the diagnostic output-pin DIAG when the specified voltage is applied at the specified junction temperature.
Diagnostic output voltage	V_{DIAGL}	On-state voltage of the diagnostic output-pin DIAG when the specified voltage and current are applied at the specified junction temperature.

Table 6.3 Electrical characteristics 2

Term	Symbol	Description
Charge pump oscillation frequency	f_{OSC}	Oscillation frequency value of the oscillator that drives the charge pump when a voltage specified by the measurement conditions is applied at a predetermined junction temperature range.
Charge pump low judgement voltage (detection)	V_{CPL}	Detect voltage value that determines the voltage drop in the charge pump voltage V_{CPV} when a voltage specified in the measurement conditions is applied in the specified junction temperature range.
Charge pump decrease threshold voltage (hysteresis)	ΔV_{CPL}	The difference between the detection voltage value for determining a voltage drop in the charge pump voltage V_{CPV} when a voltage specified in the measurement conditions is applied in the predetermined junction temperature range and the detection voltage value for releasing the determination of a voltage drop.
Power driver on-resistance	R_{ONH} R_{ONL1} R_{ONL2}	The on-resistance of the diagnostic output-pin OUT1, OUT2 when the specified voltage and current are applied at the specified junction temperature.
Switching time	t_{ON} t_{OFF1}	The rising V_{DD} of the input voltage (50 %) to the rising 4 V of the output voltage plus the delay between 50 % of the falling edge of the input voltage and the falling 1.4 V of the output voltage. 
Switching time	t_{OFF2}	The delay between the rising edge of the line voltage (50 %) and the falling 1.4 V of the line voltage. 
Rapid off-drive operating time	t_{O2ON}	The elapsed time from when OUT2 output pin is turned V_{CPV} (pull-up 100 kΩ) to the potential (24 V) equivalent to the charge pump voltage, when IN2 pin is turned on, when the output voltage V_{OUT2} drops below 50% of 24 V, to when the voltage again rises above 50% of 24 V.
Output current at reverse connection of power supply	I_{REV1} I_{REV2}	Current flowing to OUT1, OUT2 of the OUTPUT terminal when the specified voltage is applied at the specified junction temperature.

7. Evaluation board

This product is used for semiconductor relays that control between various power supply systems, such as batteries, and devices that are driven. Evaluation boards with peripheral devices are prepared so that the functions can be confirmed. Switching operation and function under actual load can be checked.

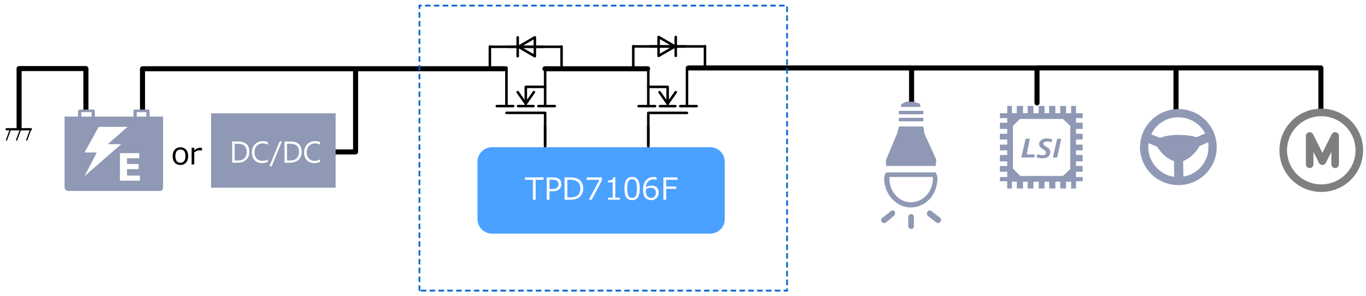
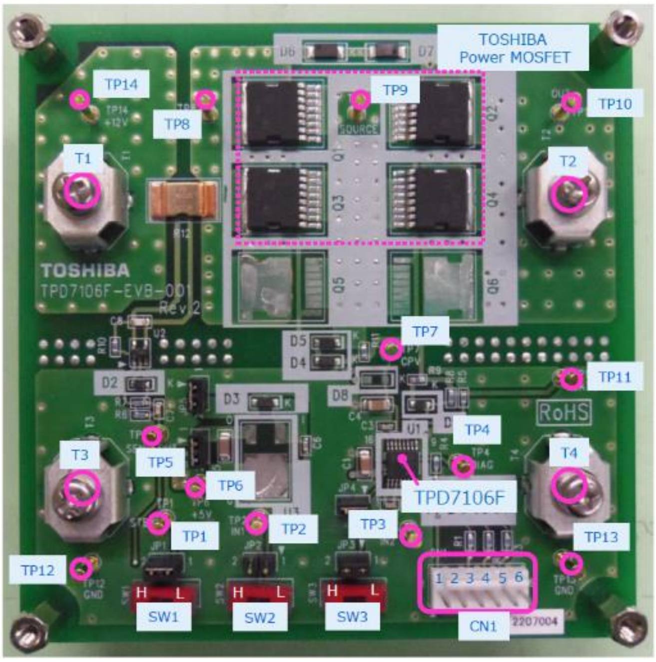


Fig. 7.1 Applications of TPD7106F

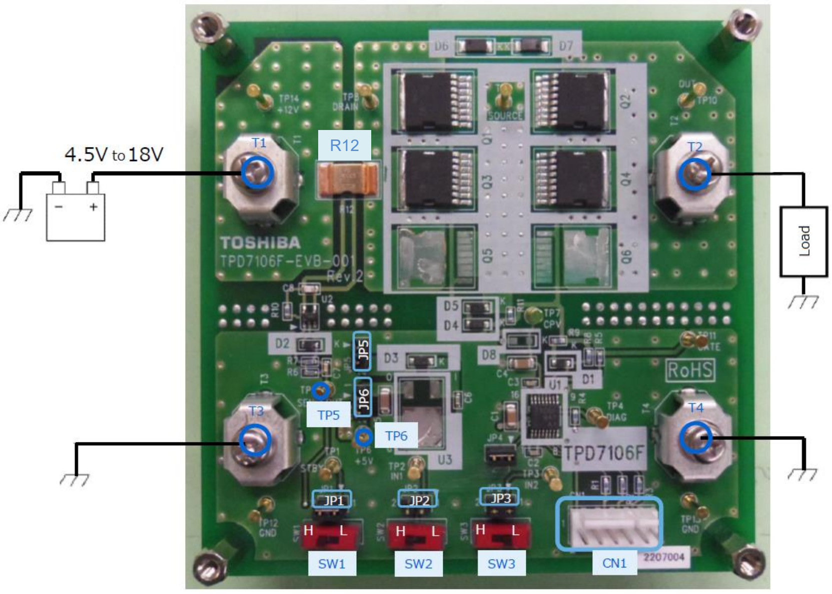
7.1. Appearance of evaluation board



pin name	Location	purpose	Absolute maximum ratings
DIAG	CN1-1	Diagnosis output for U1	-0.3 to 27V
SENSE OUT	CN1-2	Current sense output for U3	-0.3 to 6V
STBY	CN1-3	Standby mode control input for U1	-0.3 to 27V
IN1	CN1-4	Input for U1	-0.3 to 6V
IN2	CN1-5	Input for U1	-0.3 to 6V
GND	CN1-6	GND terminal	
+12V	T1	Power supply pin	-18 to 27V
VOUT	T2	Output pin	-18 to 27V
PGND	T3	GND terminal	
PGND	T4	GND terminal	
STBY	TP1	Monitor pin for U1	-0.3 to 27V
IN1	TP2	Monitor pin for U1	-0.3 to 6V
IN2	TP3	Monitor pin for U1	-0.3 to 6V
DIAG	TP4	Monitor pin for Diagnosis output for IC1	-0.3 to 27V
SENSE OUT	TP5	Monitor pin for U3	-0.3 to 6V
+5V	TP6	Monitor pin for U2	4.25 to 5.25V
CPV	TP7	Monitor pin for U1	40V max
DRAIN(Q1,Q3,Q5)	TP8	Monitor pin for drain of Q1,Q3,and Q5.	40V max
SOURCE	TP9	Monitor pin for source of FETs.	-0.3V to VDD
DRAIN(Q2,Q4,Q6)	TP10	Monitor pin for drain of Q2,Q4,and Q6.	40V max
GATE	TP11	Monitor pin for gate of FETs.	±16V
PGND	TP12	GND pin.	
PGND	TP13	GND pin.	
+12V	TP14	Power supply pin	-0.3V to 27V
STBY	SW1	5V(H-state)/0V (L-state) Selection switch	
IN1	SW2	5V(H-state)/0V (L-state) Selection switch	
IN2	SW3	5V(H-state)/0V (L-state) Selection switch	

Fig. 7.2 TPD7106F evaluation board appearance and terminal description

7.2. Method of use for TPD7106F evaluation board



[Method of use]

1. Set SW1,2,3 to "L". ($V_{STBY}=V_{IN1}=V_{IN2}=0$ V)
2. Apply power to T1. (Be sure to do after step 1.)
3. Apply 5 V to TP6.
4. Set SW1 connection to "H". (Cancel standby mode)
5. Set SW2 connection to "H". (VIN1=5V)
6. By setting the SW3 connection to "H" in the state of step 4, the driving MOSFET is rapidly turned off.
7. SENSEOUT(TP5) outputs the current detected by R12 with a differential amplifier.

[Usage Precautions]

1. JP1, JP2, JP3 should be open when inputting the control signal with CN1.
2. Load current is up to 70A. (without heat sink case).
3. JP5 and JP6 should be open.

Fig. 7.3 Method of use for TPD7106F evaluation board

7.3. Evaluation board circuit diagram

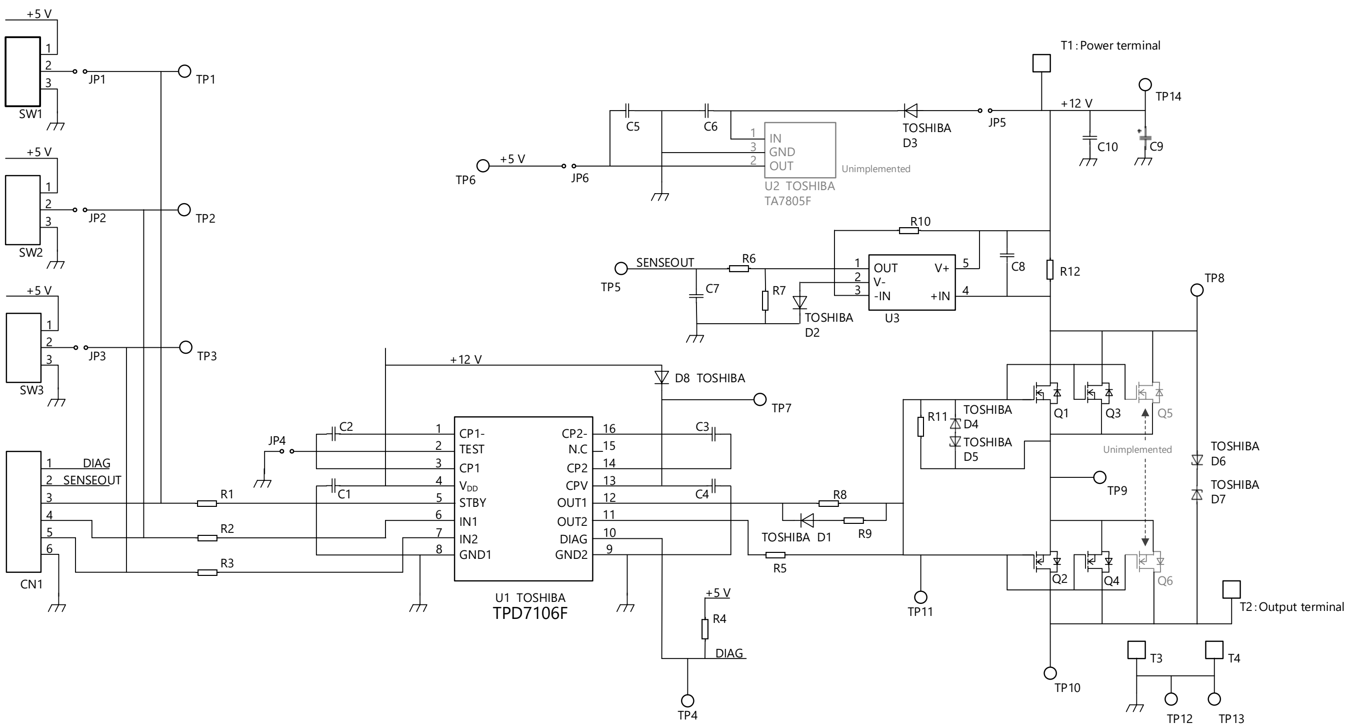


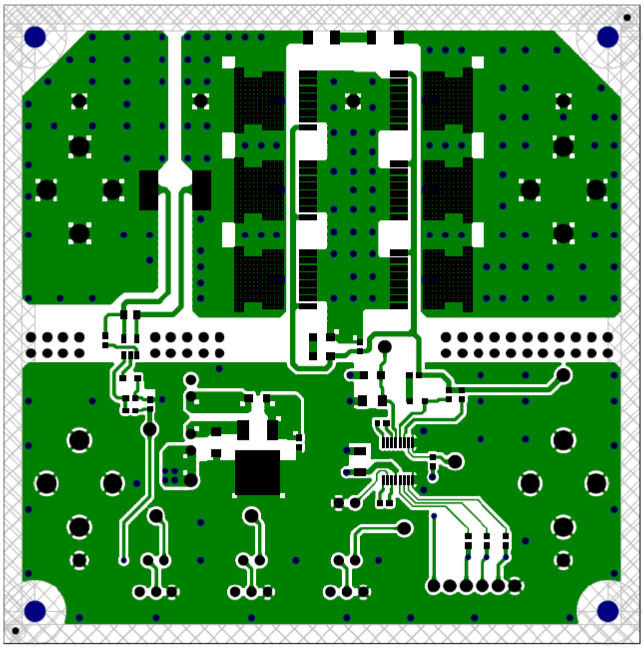
Fig. 7.4 TPD7106F evaluation board circuit diagram

7.4. Bill of materials

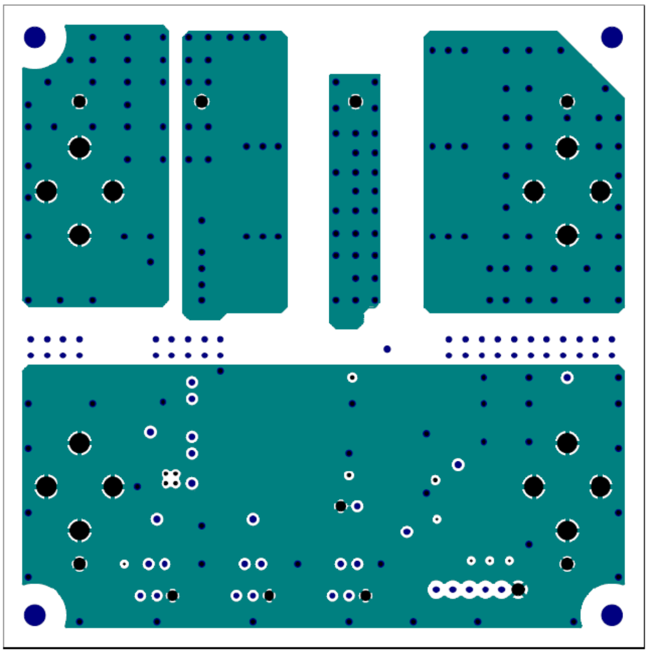
Table 7.1 BOM list

parts number	pcs	product number	spec.	maker	description	PKG	size (mm)	
IC1	1	TPD7106F	–	TOSHIBA	Power MOSFET Gate Driver	SSOP-16	6.4 x 5.5	
IC2	1	TA7805F	–	TOSHIBA	Voltage Regulator 5V	HSOP-3	6.5 x 9.5	Unimplemented
IC3	1	LTC6101BCS5	–	Analog Devices	Current Sense Amplifier	TSOT-23	2.9 x 2.8	
Q1,Q2,Q3,Q4	4	XPQR3004PB	–	TOSHIBA	Power MOSFET	L-TOGL	8.45 x 9.9	
D1,D2	2	1SS352	–	TOSHIBA	Switching Diode	USC	2.5 x 1.25	
D3,D8	2	CRG09A	–	TOSHIBA	Rectifier Diode	S-FLAT	3.5 x 1.6	
D4,D5	2	CRZ16	–	TOSHIBA	Zener Diode	S-FLAT	3.5 x 1.6	
D6,D7	2	CMZ27	–	TOSHIBA	Zener Diode	M-FLAT	4.7 x 2.4	
R1,R2,R3,R4,R7	5	–	10k	–	Resistor	–	1.6 x 0.8 (1608)	
R5	1	–	10	–	Resistor	–	1.6 x 0.8 (1608)	
R6	1	–	47k	–	Resistor	–	1.6 x 0.8 (1608)	
R8	1	–	1k	–	Resistor	–	1.6 x 0.8 (1608)	
R9	1	–	100	–	Resistor	–	1.6 x 0.8 (1608)	
R10	1	–	200	–	Resistor	–	1.6 x 0.8 (1608)	
R11	1	–	200k	–	Resistor	–	1.6 x 0.8 (1608)	
R12	1	BVS-M-R0005	0.5mΩ/5W	Isabellenhuette	Shunt Resistor	–	10 x 5.2	
C1,C4	1	–	1.0uF/50V	–	Ceramic Capacitor	–	3.2 x 1.6 (3216)	
C2,C3,C6	2	–	0.1uF/50V	–	Ceramic Capacitor	–	1.6 x 0.8 (1608)	
C5	1	–	10uF/50V	–	Ceramic Capacitor	–	3.2 x 1.6 (3216)	
C7	1	–	1000pF/50V	–	Ceramic Capacitor	–	1.6 x 0.8 (1608)	
C8	1	–	15pF/50V	–	Ceramic Capacitor	–	2.0 x 1.2 (2012)	
C9	1	–	2.2uF/25V	–	Ceramic Capacitor	–	–	
C10	1	–	100uF/25V	–	Aluminum electric field capacitor	–	–	

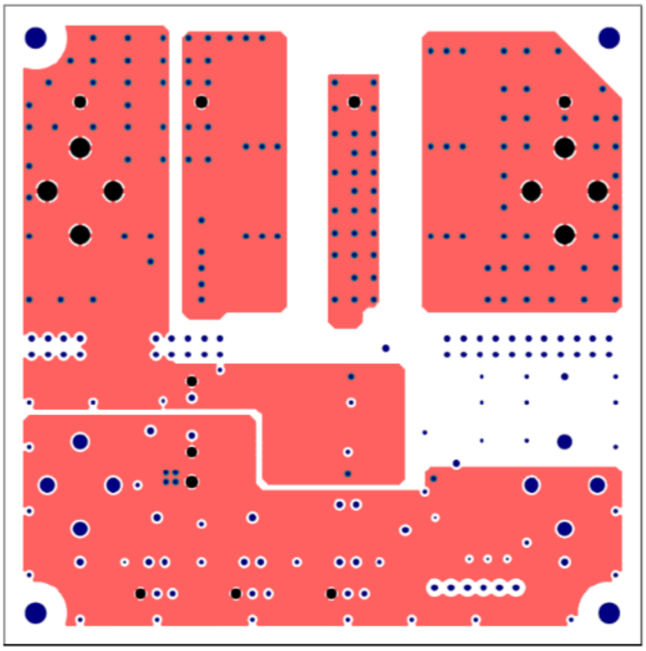
7.5. Evaluation board layout



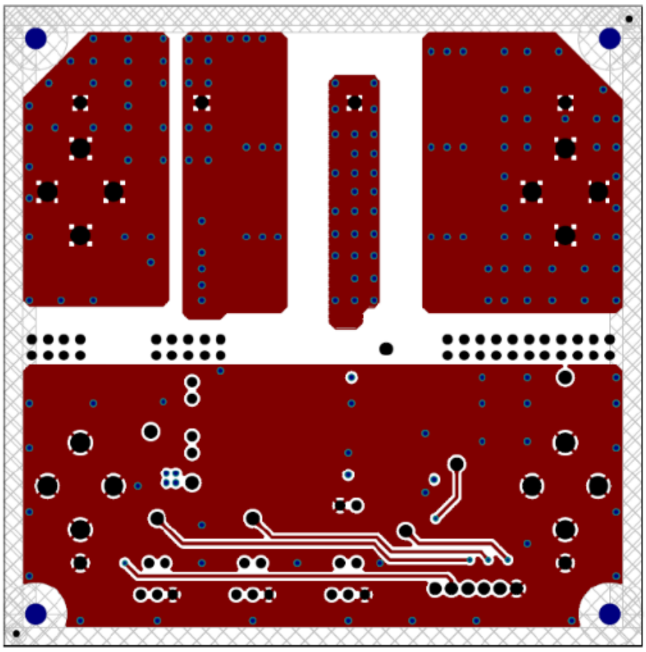
1st Layer



2nd Layer



3rd Layer



4th Layer

Fig. 7.5 TPD7106F evaluation board layout

Notes on contents

1. **Block diagrams**
   Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. **Equivalent circuits**
   The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

IC usage considerations

Notes on handling of ICs

The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Exceeding the maximum rating may cause destruction, damage and deterioration, and may result in injury due to explosion or burning.

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