1 kW Non-Isolated Buck-Boost DC-DC Converter for Telecommunication Equipment

Design guide

RD211-DGUIDE-01

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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1. Introduction

This Design Guide describes how to design various types of circuit for 1 kW Non-Isolated Buck-Boost DC-DC Converter (hereafter referred to as this Power Supply) for Telecommunication Equipment. Refer to the Reference Guide for detailed specifications, use, and characteristic data of this power supply.

If a component is indicated as "Not Mounted" in the bill of materials, then it is not mounted on the PCB even if its part number is indicated in the circuit diagram. Mounting locations are provided on the PCB for adjustment of the constant values at the time of circuit design.

1.1. Buck-Boost DC-DC Converter

The buck-boost DC-DC converter can step the voltage both up and down. Typical non-isolated buck-boost converters consist of a single-switch (MOSFET Q) with the characteristic "input-output inversion." Fig.1.1 shows the basic circuit.

Fig. 1.1 (a) shows the circuit when the input voltage is positive and (b) shows the circuit when the input voltage is negative.

In the circuit shown in Fig. 1.1 (a), energy is stored in the inductor while Q is on. Now if Q is turned off, the inductor will continue to attempt to draw current. The current in this inductor charges output capacitor C to a negative voltage relative to the positive input voltage. On the other hand, the circuit shown in Fig.1.1 (b) consists of a step-up/down converter from the negative input voltage to the positive output voltage. The current flowing through the inductor is in the opposite direction of Fig. 1.1 (a), and the output capacitor C is charged to a positive voltage with respect to the negative input voltage.

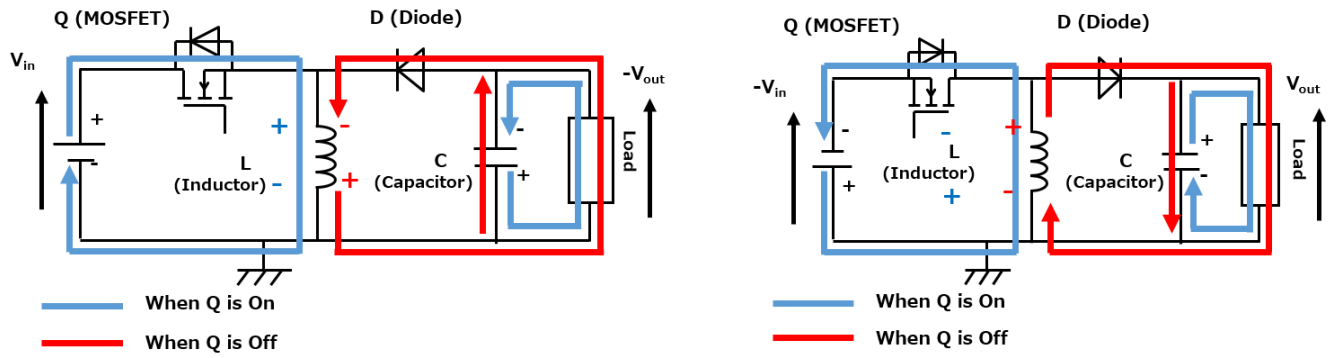


Fig. 1.1 Basic Circuit of Buck-Boost DC-DC Converter

1.2. Circuit Operation

This section explains the case of the circuit shown in Fig. 1.1 (b) (where the input is a negative voltage, and the output is a positive voltage). Fig. 1.2 shows the current path and current and voltage waveforms when MOSFET Q is on and off.

MOSFET On-Period

When MOSFET is turned on, a voltage V_{in} is applied to the inductor L in the direction shown in Fig. 1.2 (a), causing the current i_Q shown in Fig. 1.2 (a) to flow. Inductor current increases by the slope of $di_L/dt = V_{in}/L$. Energy is stored in L during this period. At this time, the voltage V_{in} is applied to the inductor L and the inverse voltage $V_{in}+V_{out}$ is applied to the diode D.

MOSFET Off-Period

When MOSFET is switched off and there is no more power available, the current will continue to flow due to the release of the energy stored in L.

Fig. 1.2 (b) shows the current path at this time. With this current, the output capacitor C is charged to the positive voltage inverted from the input voltage. Therefore, the output voltage V_{out} is a positive voltage. Inductor current decreases with the slope of $di_L/dt=-V_{out}/L$. At this time, the voltage $-V_{out}$ is applied to the inductor L and $V_{in}+V_{out}$ voltage is applied between the drain sources of the MOSFET Q.

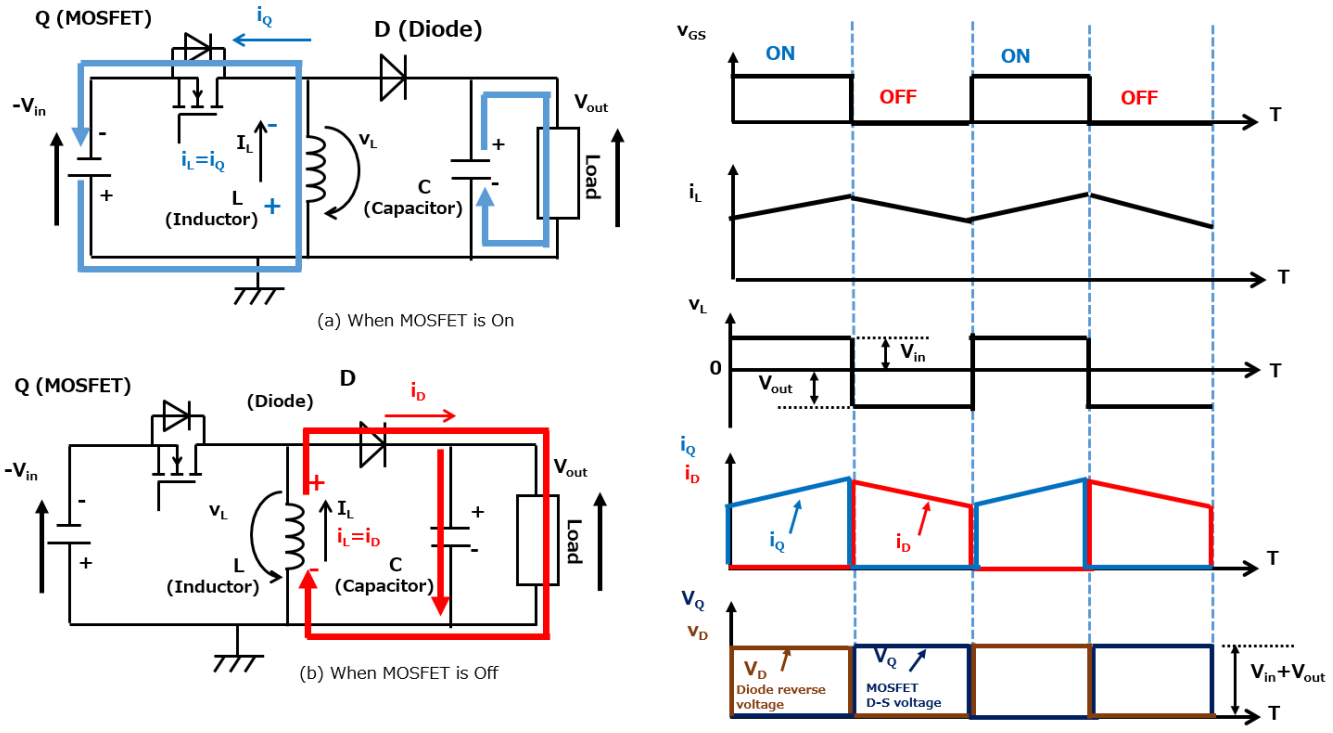


Fig. 1.2 Current Path and Voltage/Current Waveform when MOSFET is On/Off

1.3. Buck-Boost DC-DC Converter Output Voltage

The following equation holds for the energy ΔU_1 accumulated in L during the period in Fig. 1.2 (a) and the energy ΔU_2 (<0) released during the period in Fig. 1.2 (b):

$$\Delta U_1 + \Delta U_2 = 0 \quad \cdots\cdots(1)$$

When the average current at the time of accumulating energy ΔU_1 is i_1, the average current at the time of releasing energy ΔU_2 is i_2, the on time of Q (MOSFET) is t_{on} and the off time is t_{off}, then:

$$\Delta U_1 = V_{in} \times i_1 \times t_{on} \qquad \Delta U_2 = V_{out} \times i_2 \times t_{off} \quad \cdots\cdots(2)$$

Equations (1) and (2) provide the following equation:

$$V_{in} \times i_1 \times t_{on} + V_{out} \times i_2 \times t_{off} = 0$$

When the current flowing into L is stable, then $i_1 = i_2$ and the following is obtained from above equation.

$$V_{in} \times t_{on} + V_{out} \times t_{off} = 0 \quad \cdots\cdots(3)$$

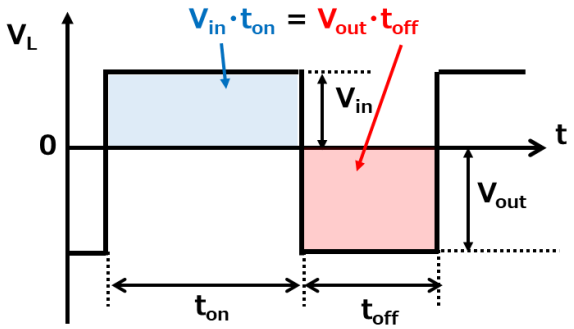


Fig. 1.3 Inductor Voltage Picture when MOSFET is ON and OFF

From equation (3)

$$V_{out} = -\frac{t_{on}}{t_{off}} \times V_{in}$$

Let D be the ratio duty of t_{on} for one period T (= t_{on}+t_{off}) of Q (MOSFET)

$$V_{out} = -\frac{D}{(1-D)} \times V_{in} \cdots\cdots(4)$$

D is expressed by the following equation when the switching frequency is f_{sw}.

$$\mathrm{D} = \frac{t_{on}}{T} = \frac{t_{on}}{(t_{on} + t_{off})} = t_{on} \times f_{sw}$$

As shown in Equation (4), the buck-boost DC-DC converter is a boost circuit when the duty D is greater than 0.5 and a buck circuit when it is lower.

2. Outline of 1 kW Non-Isolated Buck-Boost Converter

2.1. Basic Circuit

As shown in the circuit block in Fig. 2.1, this power supply adopts a two-phase interleave configuration. Interleave operation is a method in which each phase is connected in parallel as shown in Fig. 2.1, and by intentionally shifting the switching phase, current changes in the output capacitor are cancelled and the ripple is reduced. In this two-phase interleaving design, the ripple can be suppressed most by shifting the phase by 180 degrees. Here MOSFETs are used as switching elements and MOSFETs are also used as synchronous rectifier elements to improve efficiency. The MOSFET for switching and the MOSFET for synchronous rectification are switched alternately.

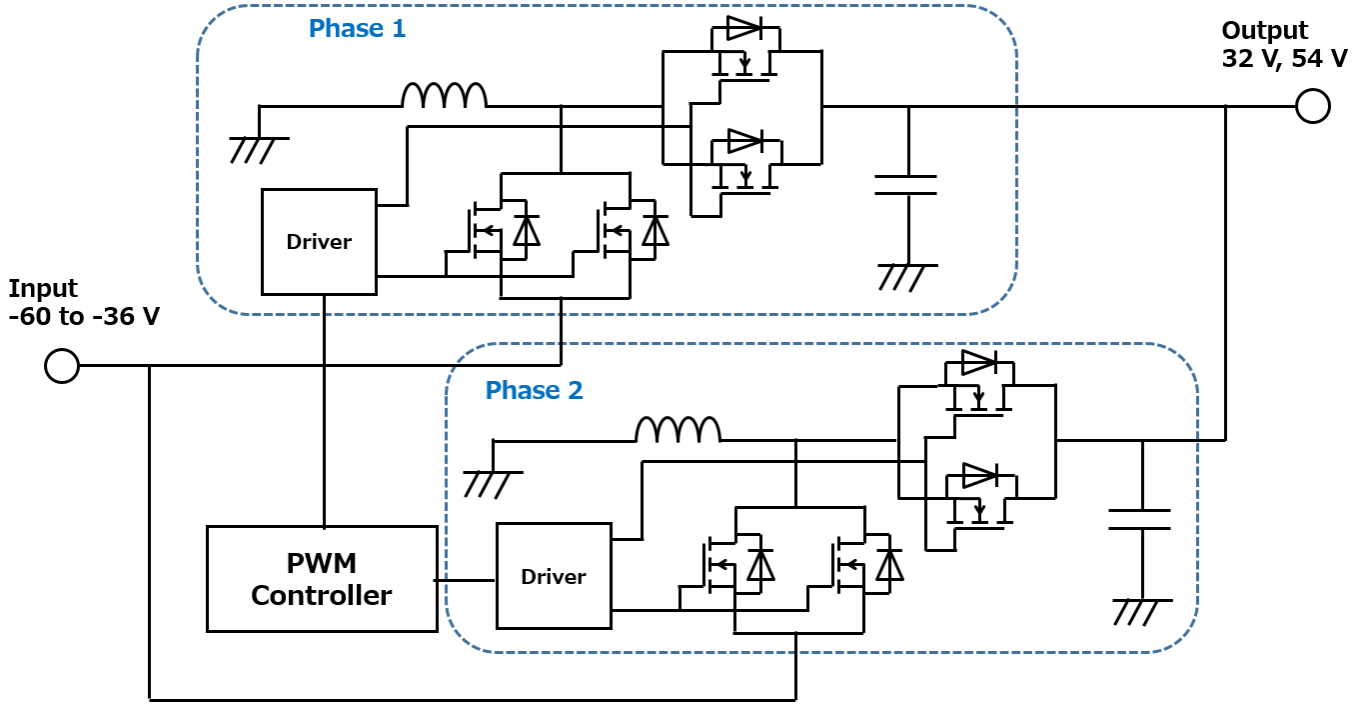


Fig. 2.1 1 kW Non-Isolated Buck-Boost DC-DC Converter Circuit Block Diagram

2.2. Overview

Input: DC -48 V (Range DC -60 to -36 V)
Output: DC +32 V/+54 V
Maximum Output Power: 1 kW
Chopping Frequency: 150 kHz fixed frequency
Ripple Voltage: + 320 mV @ Output +32 V, +520 mV @ Output +52 V

2.3. On-Board Power MOSFETs

TPH9R00CQH

Mounted on the low side (switch section)

V_{DSS} = 150 V, $R_{DS(ON)}$@V_{GS} = 10 V (Max.) = 9.0 mΩ, SOP Advance package

Latest U-MOSX-H process product with superior performance (Figure of Merit) for switching applications.

TPH9R00CQ5

Mounted on the high side (synchronous rectifier)

V_{DSS} = 150 V, $R_{DS(ON)}$@V_{GS} = 10 V (Max.) = 9.0 mΩ, SOP Advance package

Latest U-MOSX-H process product with built-in high-speed diodes. Reduced power dissipation in synchronous commutation operation.

Supplement: 2-Phase Interleave System

In the two-phase interleaving method, two sets of circuits are connected in parallel, and the circuit phases to drive them are shifted by 180 degrees. And the switches turning On/Off makes each inductor current a triangular waveform. At the output triangular inductor current overlaps. As a result, the ripple current is reduced, and the effective frequency is doubled. Fig. 2.3 shows the gate signal waveform of Q_{SW1} and Q_{SW2} (shown in Fig. 2.2), the current waveform of each inductor (L_1 and L_2), and the output current waveform (sum of current L_1 and L_2). The interleaving method uses two sets of switches, which distributes the switching loss and reduces the load on one switch, making thermal design easier. The filter size can be reduced because the ripple is small, and the effective frequency is doubled.

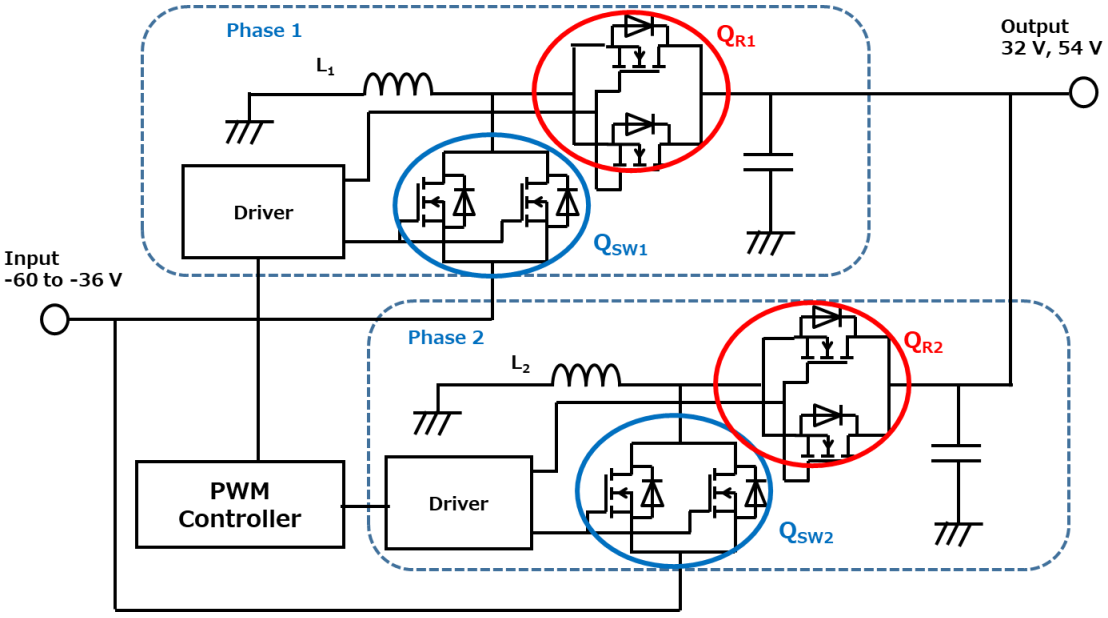


Fig. 2.2 Two-Phase Interleave Buck-Boost Converter Circuit

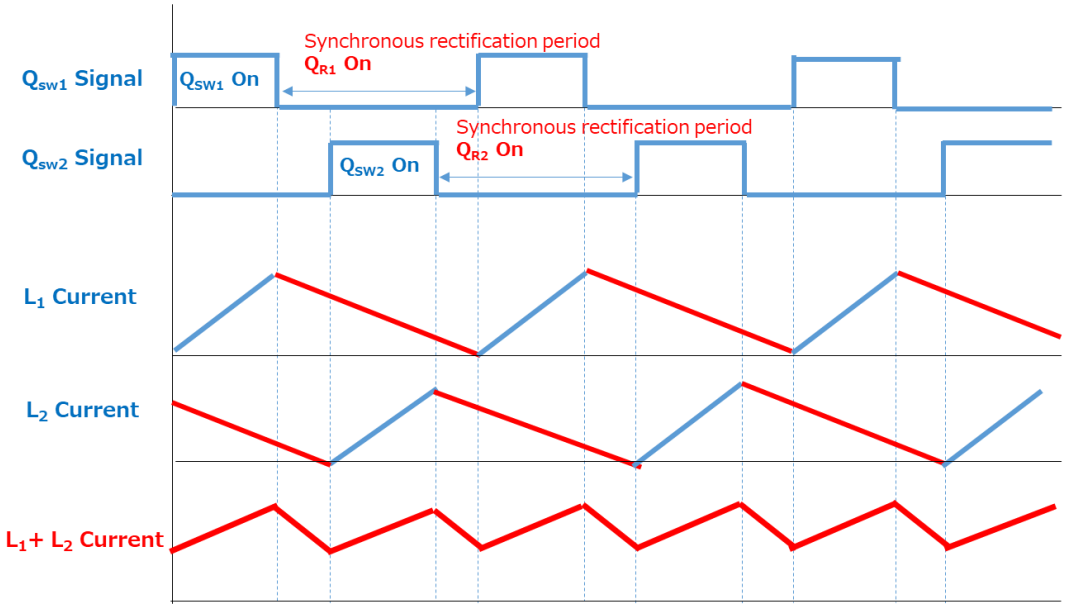


Fig. 2.3 Two-Phase Interleave Operation

3. Circuit Design

This power supply generates +32 V/+54 V output using non-isolated buck-boost converter circuit. The non-isolated buck-boost converter circuit system consists of an inductor, a high-side MOSFET, and a low-side MOSFET to form a main circuit. The on/off duty of the high-side and low-side MOSFETs controls the time-ratio for storing energy in the inductor to enable step-up and step-down operations. The output capacity of this power supply is 1 kW and two-phase interleave design is used to implement it.

Maxim's controller IC MAX15158 (hereafter refered to as controller IC) is used to control this power supply. Refer to MAX15158 datasheet and related documents for details of design around the controller IC.

Fig. 3.1 shows the main circuit of this power supply and the current limiter setting circuit (1 and 2) section.

Fig.3.2 shows the enlarged view of the MOSFET for switching, the MOSFET for synchronous rectification and their circuit configuration shown in Fig. 3.1.

Fig.3.3 shows the controller IC, IC power supply circuit, and output voltage switching circuit. It also shows the output voltage setting and switching circuit, switching frequency setting circuit, and current limiter setting circuit (3).

The following section describes how to set the constants of each circuit, and how to select inductors and output capacitors.

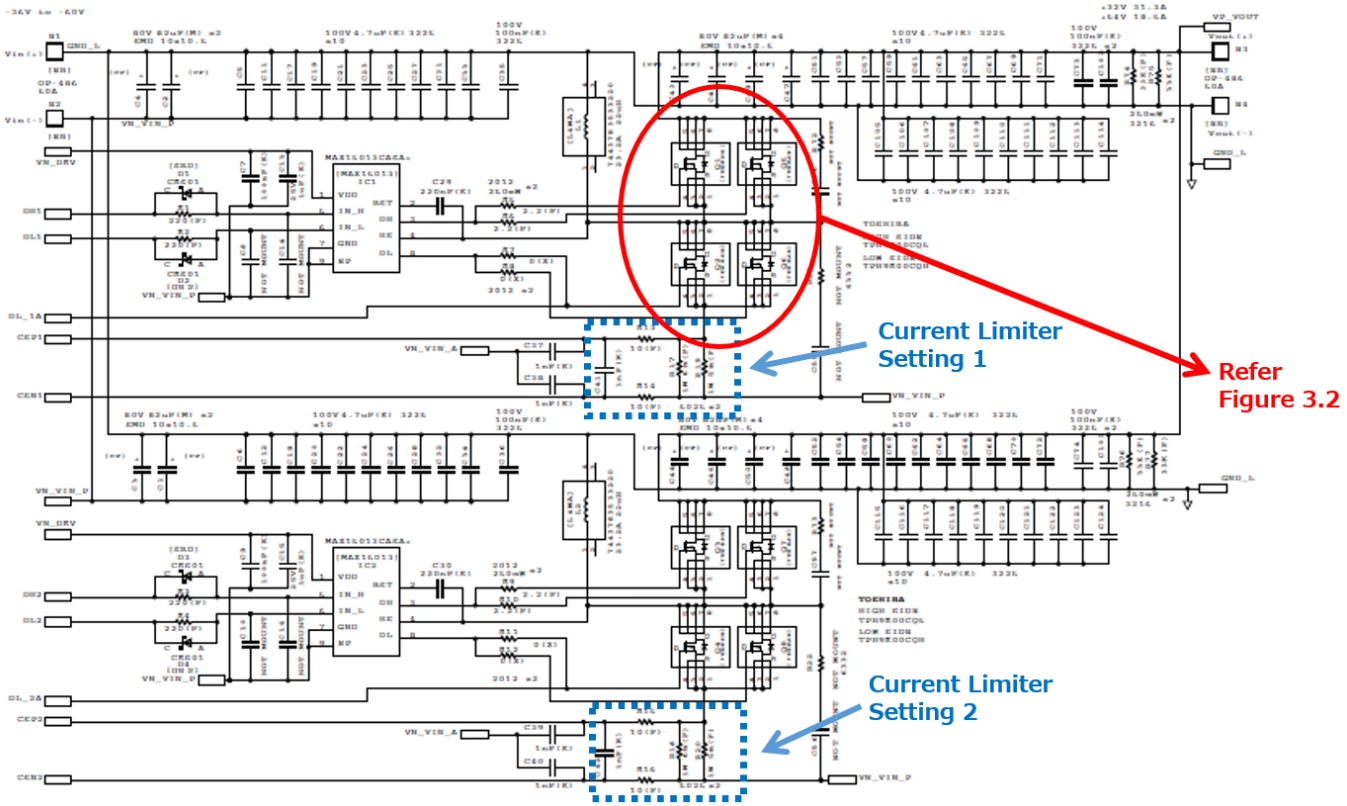


Fig. 3.1 Main Circuit Diagram

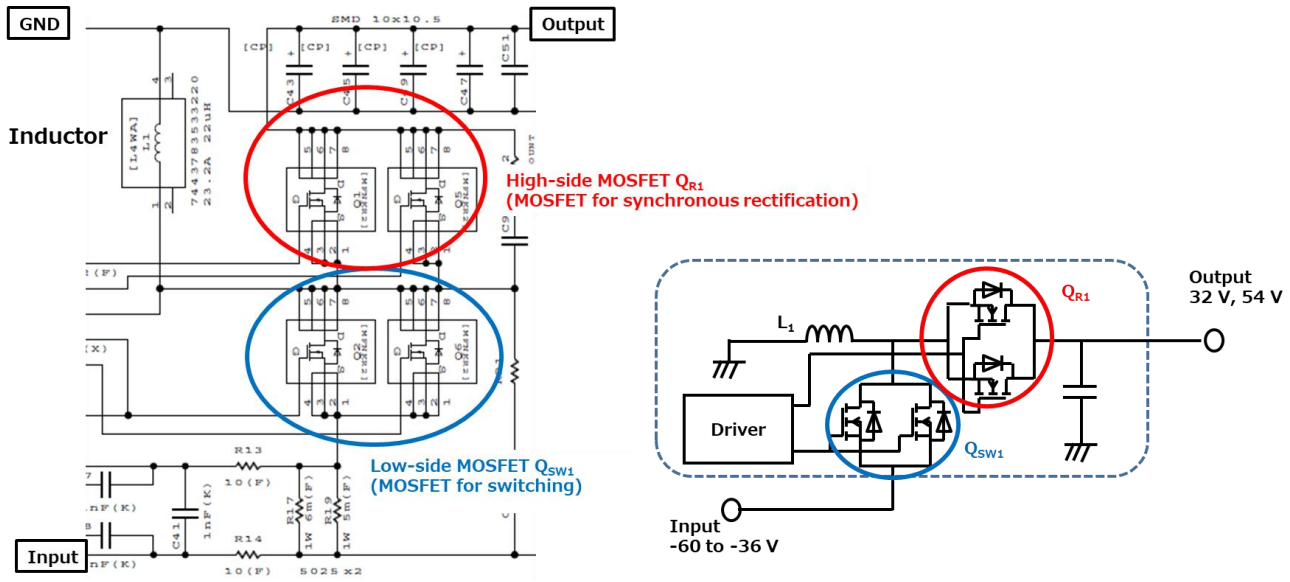


Fig. 3.2 Circuit Configuration of the MOSFET for Switching and the MOSFET for Synchronous Rectifier

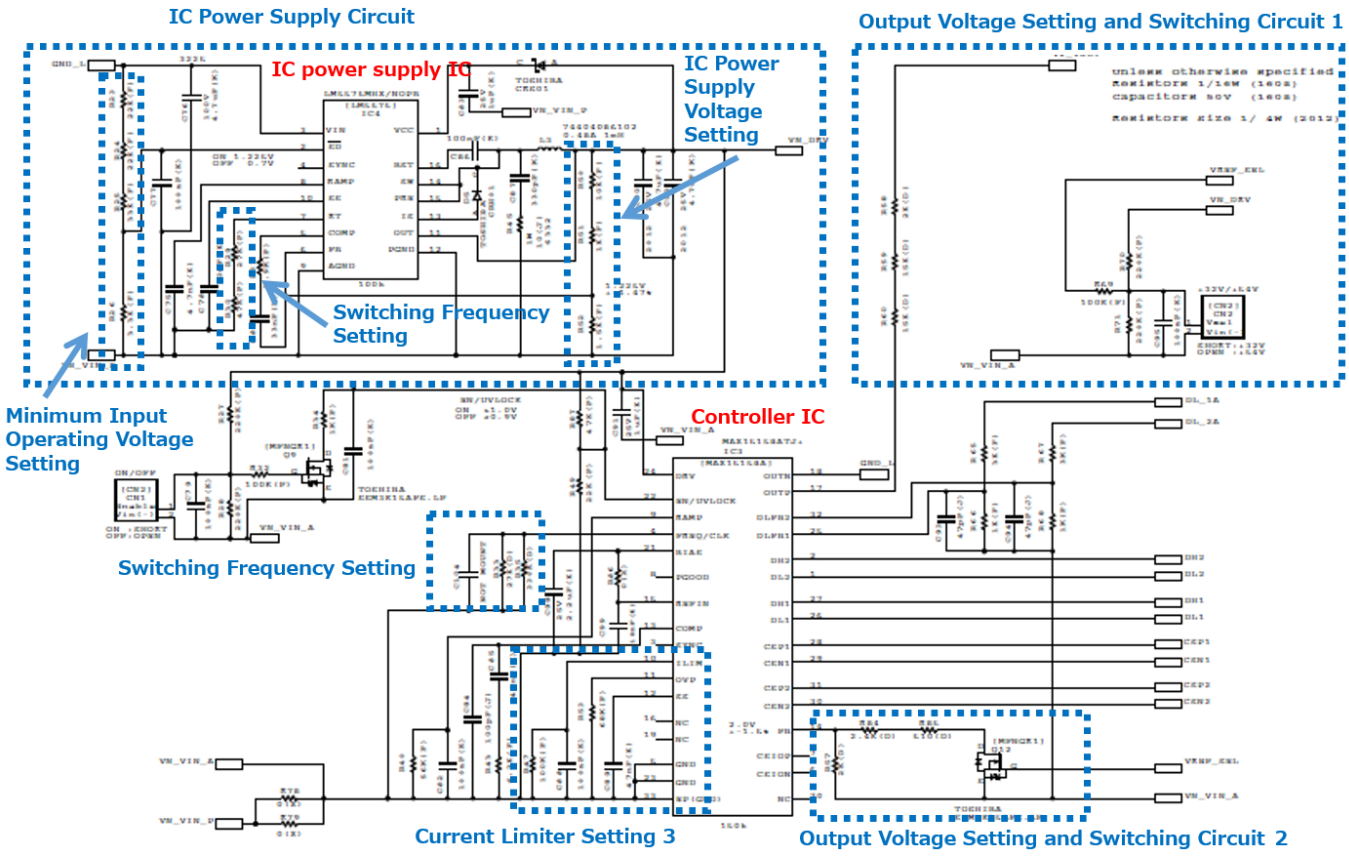


Fig. 3.3 Controller IC, IC Power Supply Circuit, and Output Voltage Setting and Switching Circuit

3.1. Minimum Input Operating Voltage Setting

Fig. 3.4 shows the minimum input operating voltage setting circuit. The minimum input operating voltage (V_{in}_min_on) is set by dividing the input voltage with external resistors (R23, R24, R25, R26) and sending it to SD (pin 2) of the switching regulator LM5575MHX (hereinafter referred to as switching regulator) manufactured by Texas Instruments Corporation, which constitutes the power supply circuit of the controller IC. Refer to LM5575MHX datasheet and related documents for detailed circuit designs around the switching regulator.

The switching regulator is supplying power to the controller IC. Therefore, if the switching regulator does not operate, the power cannot be supplied to the controller IC, and this power supply cannot operate.

When SD pin voltage exceeds 1.225 V, the switching regulator starts operating. The minimum input operating voltage (V_{in}_min_on) is the voltage when SD pin voltage obtained by dividing the input voltage by the external resistor R23+R24+R25 and R26 becomes 1.225 V.

After starting operation, the threshold voltages for shutdown and standby each have 0.1 V hysteresis. SD pin voltage must not exceed 14 V.

Calculate the operating voltage lower limit (V_{in}_min_on) using the following formula from Fig. 3.4.

$$\frac{(R23+R24+R25)}{R26}=\frac{V_{in}\_min\_on-1.225}{1.225}$$

$$V_{in}\_min\_on=\frac{1.225\times(R23+R24+R25)}{R26}+1.225$$

In the current circuit, 22 kΩ is selected for the resistor R23, 22 kΩ for the resistor R24, 33 kΩ for the resistor R25, and 3.3 kΩ for the resistor R26, as shown in Fig. 3.4.

Although V_{in}_min_on is 29.8 V from the above equation, it is -29.8 V because the input voltage is negative input in this power supply.

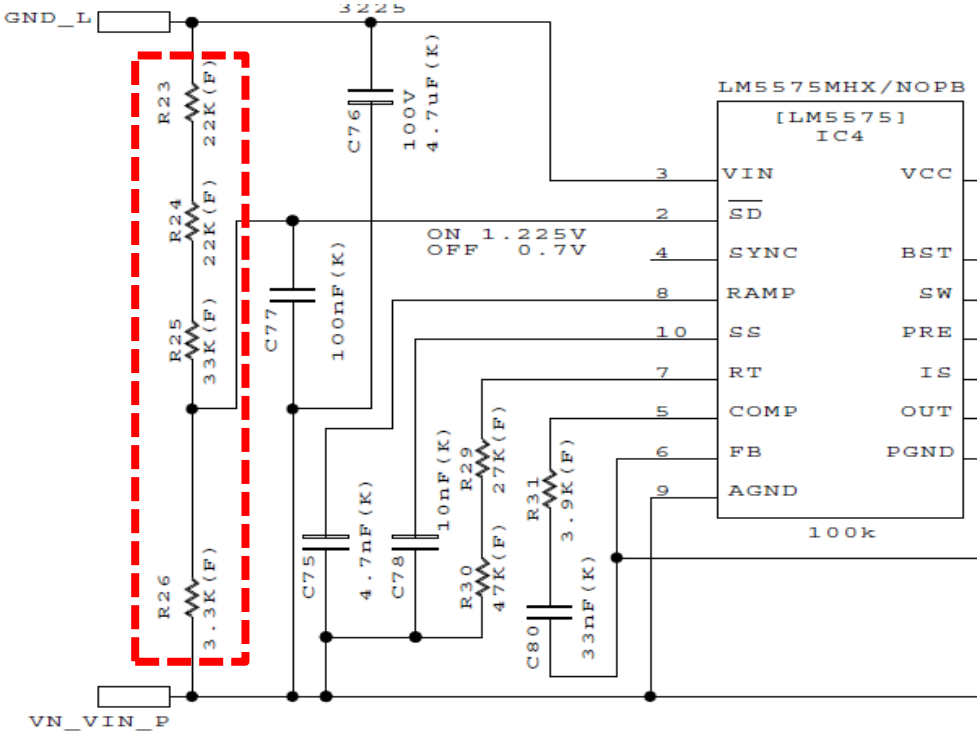


Fig. 3.4 Minimum Input Operating Voltage Setting Circuit

3.2. Switching Frequency Setting of the Controller's IC Power Supply Circuit

Fig. 3.5 shows the switching-frequency setting circuit of the controller IC power-supply circuit. The switching frequency (f_{LM5575}) of the switching regulator is calculated by the external resistor R_T (R29, R30) between RT (pin 7) and AGND (pin 9) using the following equation.

$$R_T = \frac{\frac{1}{F_{LM5575}} - 580 \times 10^{-9}}{135 \times 10^{-12}}$$

$$R_T = R29 + R30$$

Twist

$$F_{LM5575}(Hz) = \frac{1}{(R29 + R30) \times 135 \times 10^{-12} + 580 \times 10^{-9}}$$

In this power supply, the target setting of the switching frequency (f_{LM5575}) of the switching regulator is 100 kHz, thus 27 kΩ is selected for the resistor R29 and 47 kΩ is selected for the resistor R30 as shown in Fig. 3.5. 94.6 kHz is calculated using these parameters.

The switching frequency (f_{LM5575}) of the switching regulator must be set at least 10% apart from switching frequency (f_{PWM}) of the controller IC. If f_{LM5575} frequency is within ±10 % of f_{PWM}, interference may occur, resulting in abnormal oscillation. The selectable range of f_{LM5575} is 50 kHz to 500 kHz.

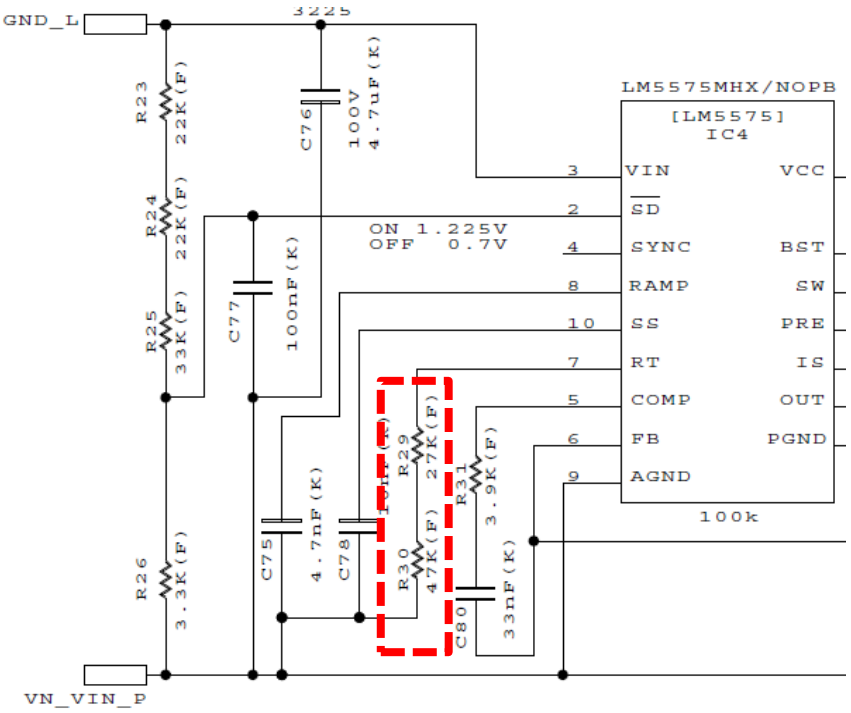


Fig. 3.5 Switching Frequency Setting Circuit of the Controller IC Power Supply

3.3. Controller IC Power Supply Voltage Setting (Switching Regulator Output Voltage)

Fig. 3.6 shows the circuit for setting the output voltage of the switching regulator. Set the output-voltage (V_{P10VP}) by adjusting the external resistor (R50, R51, R52) so that FB (pin 6) is 1.225 V. The relation between (R50+R51), R52 and voltage V_{P10VP} is expressed by the following equation.

$$\frac{(R50 + R51)}{R52} = \frac{V_{P10VP} - 1.225}{1.225}$$

From the above equation

$$V_{P10VP}(V) = \frac{1.225 \times (R50 + R51)}{R52} + 1.225$$

In this power supply, the target setting of the switching regulator's output voltage is 10 V, thus 10 kΩ is selected for the resistor R50, 1 kΩ is selected for the resistor R51, and 1.5 kΩ is selected for the resistor R52, as shown in Fig. 3.6. Calculating with these constants result in 10.2 V.
The tolerance of internal reference voltage 1.225 V is ±1.5 %.

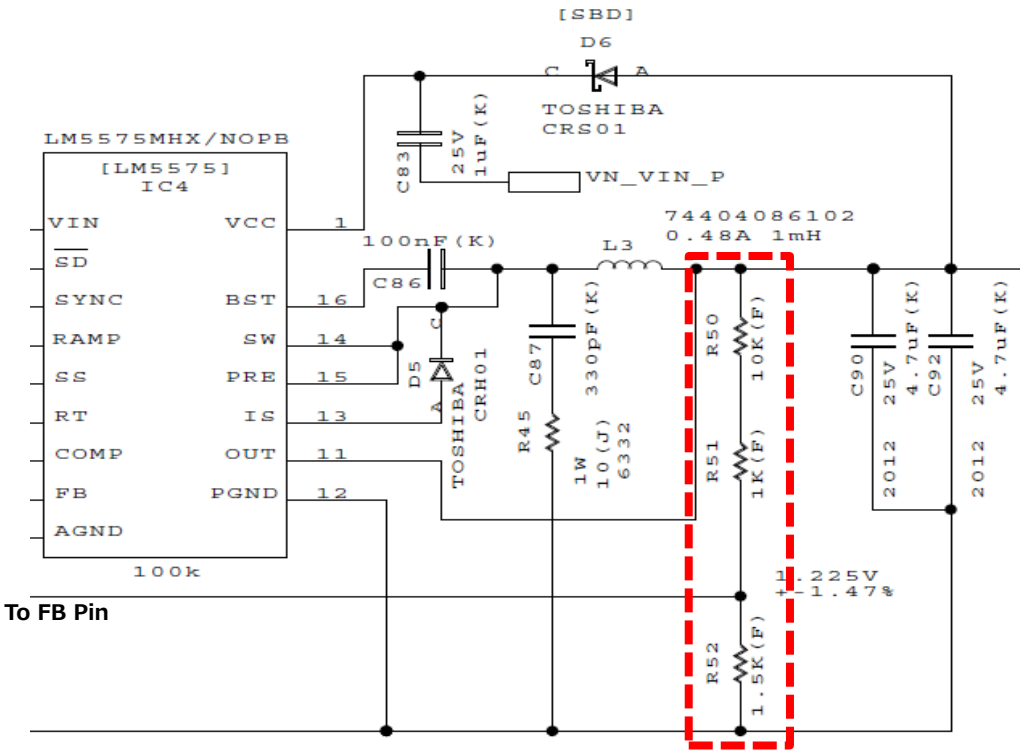


Fig. 3.6 Switching Regulator Output Voltage Setting Circuit

3.4. Current Limiter Setting

Fig. 3.7 shows the circuits (1, 2 and 3) used for current limiter setting. The controller IC controls the operation and limits the inductor current for each phase by using the current sense signals CSP1/CSN1 and CSP2/CSN2 for each phase and detecting the voltage across the current sense resistor between the low-side MOSFET (MOSFET for switching) and the input-side ground. This section explains how to set the current limit.

The current limiter level (I_limit) of each phase is set with the resistor R47 connected to ILIM (pin 10) on the controller IC and the current sense resistors R17//R19 and R18//R20.

The overcurrent setting V_{OCP} is set by the external resistor R_{ILIM} (R47) of ILIM pin. A source current of 10 μA flows into the resistor and the generated voltage is multiplied by a factor of 0.10 to get V_{OCP}.

$$V_{OCP} = 0.10 \times 10\ \mu A \times R_{ILIM}$$

The current limiter level (I_limit) is calculated by V_{OCP} and the current sensing resistor R_{SENSE} (R17//R19 as shown in Fig. 3.7 (a) and R18 //R20 as shown in Fig. 3.7 (b)) as follows:

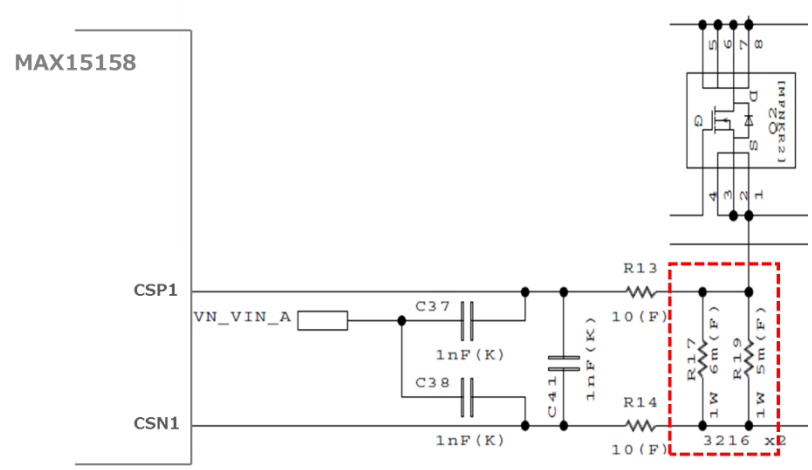
For phase 1:

$$I\_limt = \frac{V_{OCP}}{R_{SENSE}} = \frac{0.1 \times 10\mu \times R47}{R17//R19}$$

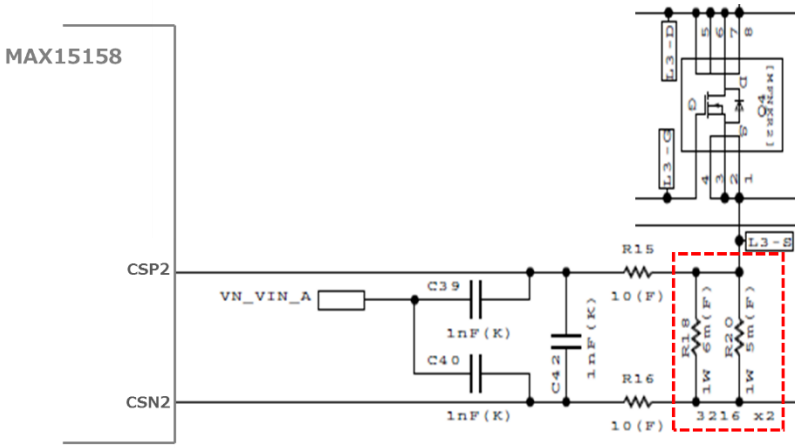
For phase 2:

$$I\_limt = \frac{V_{OCP}}{R_{SENSE}} = \frac{0.1 \times 10\mu \times R47}{R18//R20}$$

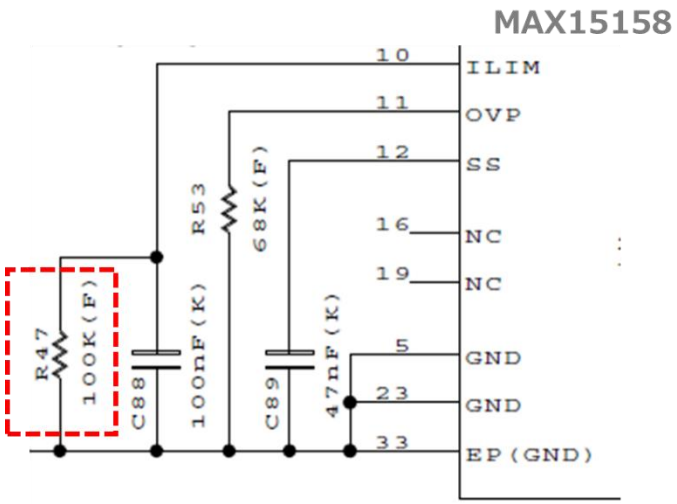
In this power supply, 6 mΩ is selected for R17 and R18, 5mΩ is selected for R19 and R20, and 100 kΩ is selected for R47, which sets I_limit to 36.5 A. I_limit is set same for both phase 1 and phase 2.



(a) Current Limiter Circuit 1



(b) Current Limiter Circuit 2



(c) Current Limiter Circuit 3

Fig. 3.7 Current Limiter Setting Circuit

3.5. Switching Frequency Setting

Fig. 3.8 shows the switching frequency setting circuit. The switching-frequency f_{PWM} of the non-isolated buck-boost converter circuit is set by connecting an external resistor between the FREQ/CLK (pin 4) of the controller IC and GND. f_{PWM} is calculated as follows:

$$f_{PWM}(Hz) = \frac{R_{FREQ}}{100k} \times 600k = \frac{R33//R35}{100k} \times 600k$$

As shown in Fig. 3.8, 27 kΩ is selected for the resistance R33 and 330 kΩ for the resistance R35, which sets the switching-frequency f_{PWM} to approx. 150 kHz.

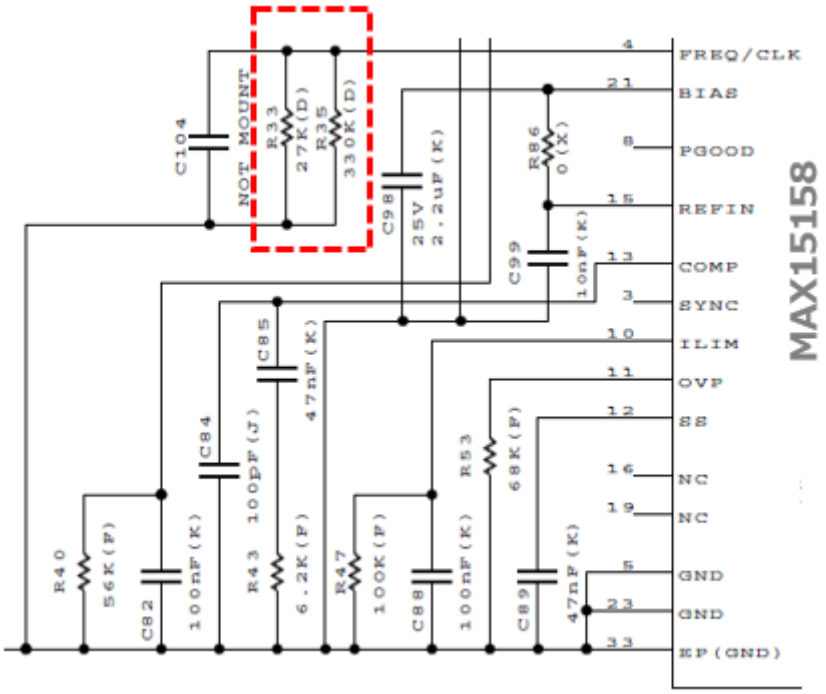


Fig. 3.8 Switching Frequency Setting Circuit

3.6. Output Voltage Setting & Switching

This section explains how to switch the output voltage. In the picture to the right in Fig. 3.9, when MOSFET (Q12) is turned off, the controller IC's FB (pin 14) is connected to VN_VIN_A (the controller IC's GND) via R57 (2 kΩ).
When MOSFET (Q12 is activated, R84 and R85 are also connected to the controller IC's GND, so the resistance across FB pin and GND becomes 1.18 kΩ with a combined resistance of R57 (2 kΩ) and R84 (2.4 kΩ) + R85 (510 Ω). Therefore, the resistance between FB (pin 14) and GND can changed by turning the MOSFET (Q12) on/off. The following explains how to calculate the output voltage setting.

Output Voltage Setting

Set the output voltage (V_{OUT}) of the power supply using the external resistors (R58, R59, R60, R57, R84, R85). To set the output voltage to 32 V/54 V, use the following equation to calculate the output voltage (V_{OUT}).

Output Voltage (32V): Q12 off

$$V_{OUT}(V) = \left(\frac{R58 + R59 + R60}{R57}\right) \times V_{REF}$$

Output Voltage (54V): Q12 on

$$V_{OUT}(V) = \left(\frac{R58 + R59 + R60}{R57 // (R84 + R85)}\right) \times V_{REF}$$

In this power supply, V_{REF} is set to 2 V, which is the internal default reference voltage of the controller IC.

As shown in Fig. 3.9, 2 kΩ is selected for R58, 15 kΩ is selected for R59, R60, 2 kΩ is selected for R57, 2.4 kΩ is selected for R84, and 510 Ω is selected for R85, thus the output voltage V_{OUT} setting becomes 32 V/54 V. Resistance tolerance ±0.5 % is used to suppress fluctuation range of output voltage. However, the tolerance of internal reference voltage of the controller IC is ±1.5 %.

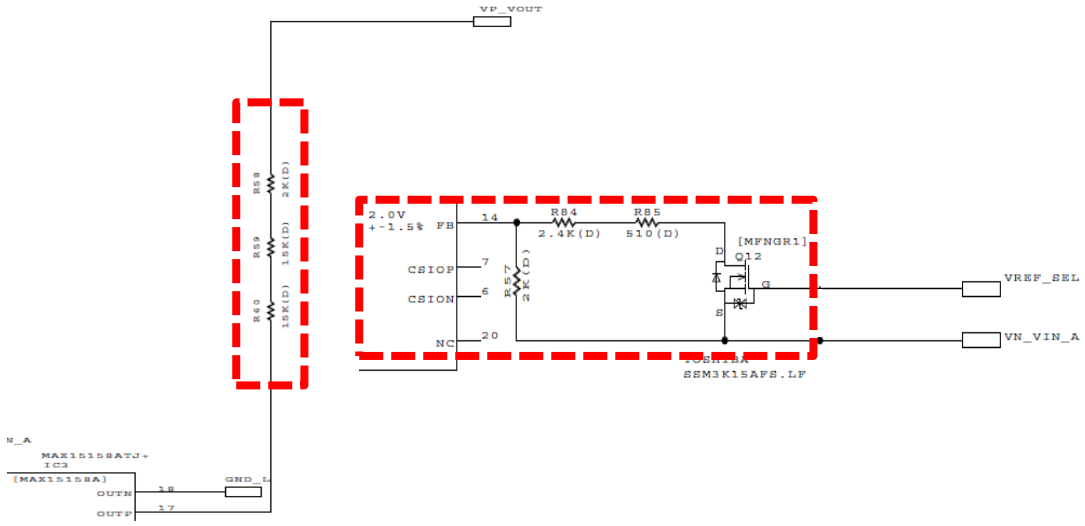


Fig. 3.9 Output Voltage Setting and Switching Circuit

3.7. Inductor Selection

Increasing the inductance value L decreases the inductor ripple current and core loss. However, the larger the inductance value, the larger the physical size. Calculate the minimum required inductance value L using the following equation.

Here, assuming that V_{in}max = -36 V, f_{PWM} = 150 kHz, V_{OUT}min = 32 V, V_{in}min = -60 V, and Pmax = 1 kW, and the assumed inductor ripple current is half of the inductor current I_L, then L_{min} can be calculated by the following equation.

$$L_{min} = D \times \frac{V_{IN}max}{f_{PWM} \times I_L/2}$$

The lowest duty D_{min},

$$D_{min} = \frac{V_{OUT}min}{-V_{IN}min + V_{OUT}min}$$

And the inductor current I_L is

$$I_L = \frac{I_{OUT}max}{(1 - D_{min}) \times N}$$

Here N denotes the number of phases. For this power supply, N is 2.

The maximum output current I_{OUT}max is

$$I_{OUT}max = \frac{Pmax}{V_{OUT}min}$$

From the above equation, inductance value per phase L_{min} = 12.75 μH, and the maximum current per phase is half of I_{OUT}max = 31.25 A which is 15.625 A. Select an inductor with inductance greater than or equal to this calculated value.

In this power supply, inductors of specification 23.2 A and 22 μH are selected as L1, L2.

3.8. Output Capacitor Selection

The output ripple V_{ripple} must be set to meet the required specifications using the capacitance C_{OUT} of the output capacitor.

Calculate the ripple voltage using the following equation.

$$V_{ripple}(V) = \frac{D \times I_{OUT}max}{N \times C_{OUT} \times f_{PWM}}$$

D = 0.47, I_{OUT}max = 1000 W/32 V = 31.3 A (whole), N = 2 phases, f_{PWM} = 150 kHz.

In order to keep V_{ripple} under 150 mV, C_{OUT} is set as 328 µF. Four capacitors of 82 µF are used for C_{OUT} (4 x 82 µF = 328 µF).

ESR, ESL of the output capacitor can be omitted because these are very small and does not affect the result.

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