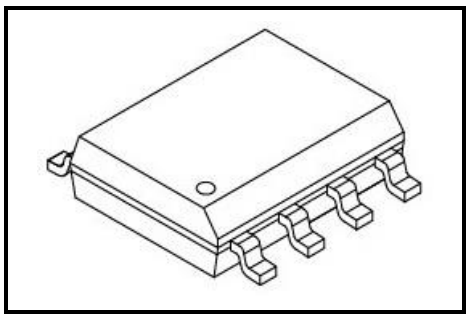
CDMOS Linear Integrated Circuits Silicon Monolithic

TB9032FNG

Automotive CXPI communication driver receiver IC

1. INTRODUCTION

TB9032FNG is a driver receiver IC that is compliant with ISO 20794-4 for the CXPI (Clock Extension Peripheral Interface) communication. It can switch between commander and responder nodes using the external pin. When in Sleep Mode, it enters a standby state with low power consumption.
In addition, it is equipped with fault detection functions including overheat detection and low voltage detection, and stops output when an abnormality is detected.



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2. APPLICATIONS

- Automotive body system applications such as steering switches, meter cluster switches, light switches, door locks, and door mirror control
- Interfaces of zone ECUs

3. FEATURES AND BENEFITS

- CXPI communication driver receiver IC
- Physical layer interface conforming to CXPI (Clock Extension Peripheral Interface) automotive communication protocol standard
- Operating voltage VBAT: 7 to 18 V
- Microcomputer interface: 4.5 to 5.5 V
- Operating temperature range (Ta): -40 to 125 ℃
- Junction temperature (Tj): 150 ℃ (max)
- Package: SOP8
- Sleep Mode
- Wake-up Transmission Mode
- Dominant timeout detection function
- Overheat detection function
- Undervoltage detection function (BAT, VIO)
- Communication speed: 20 kbps (max)
- To conform to AEC-Q100, AEC-Q006 (planned)

This material is for reference only. Do not use this for final equipment design.

4. BLOCK DIAGRAM

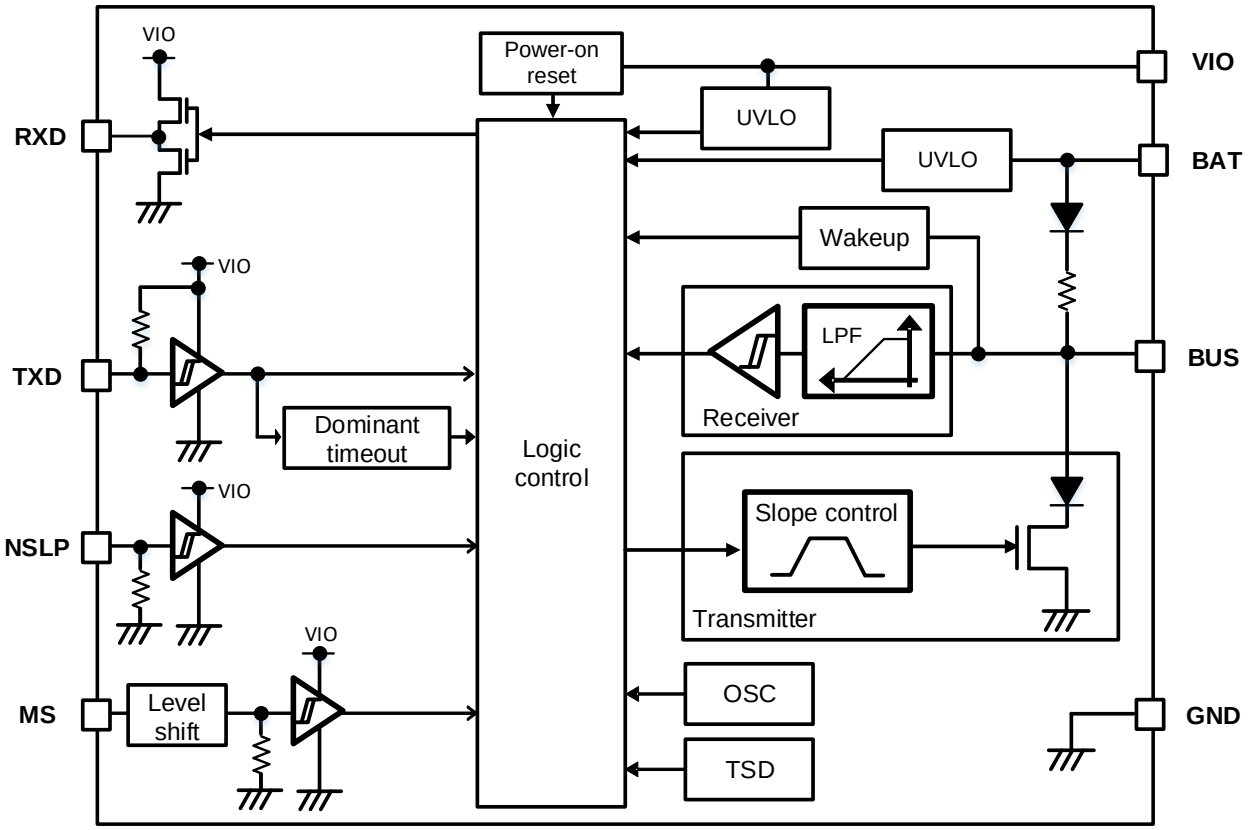


Figure 4 Block Diagram

5. INFORMATION ON PINS

5.1. Pin Assignment (Top view)

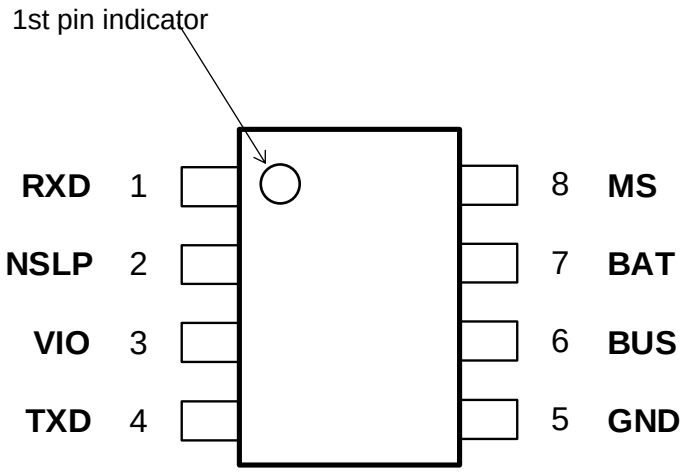


Figure 5.1 Pin Assignment

5.2. Pin Arrangement and Function Description

Table 5.2 Pin Arrangement and Function Description

No.	Name	Device Type	Withstand Voltage (V)	I/O	Pull-up/ Pull-down	Description
1	RXD	CMOS	6	Output	-	Output pin of CXPI signals received from BUS
2	NSLP	CMOS	6	Input	Pull-down	In Normal Mode: High input In Sleep Mode or Wakeup Transmission Mode: Low input
3	VIO	CMOS	6	Power source	-	5 V Interface
4	TXD	CMOS	6	Input	Pull-up	Input pin of CXPI signals to be transmitted to BUS
5	GND	CMOS	-	-	-	GND
6	BUS	DMOS	40	I/O	-	CXPI communication BUS pin
7	BAT	DMOS	40	Power source	-	Connected to the battery
8	MS	DMOS	40	Input	-	Commander node: High input Responder node: Low input

All parts should be correctly mounted and electrically connected before using the IC. The IC may experience abnormal operation, operate differently from the settings, or not operate when adjacent pins are short-circuited or a pin is open, though it may work normally even in such cases.

5.3. Equivalent Circuits around Pins

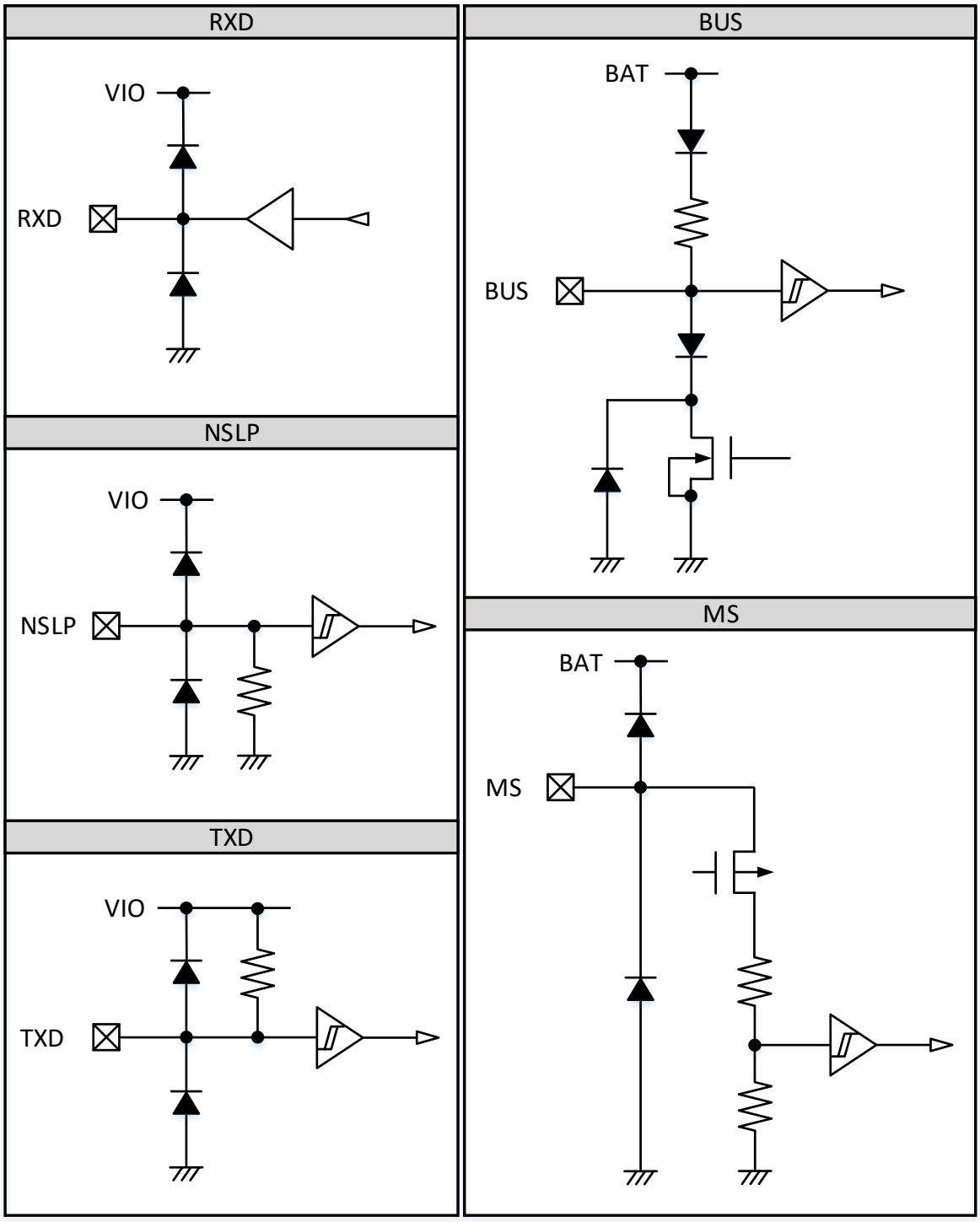
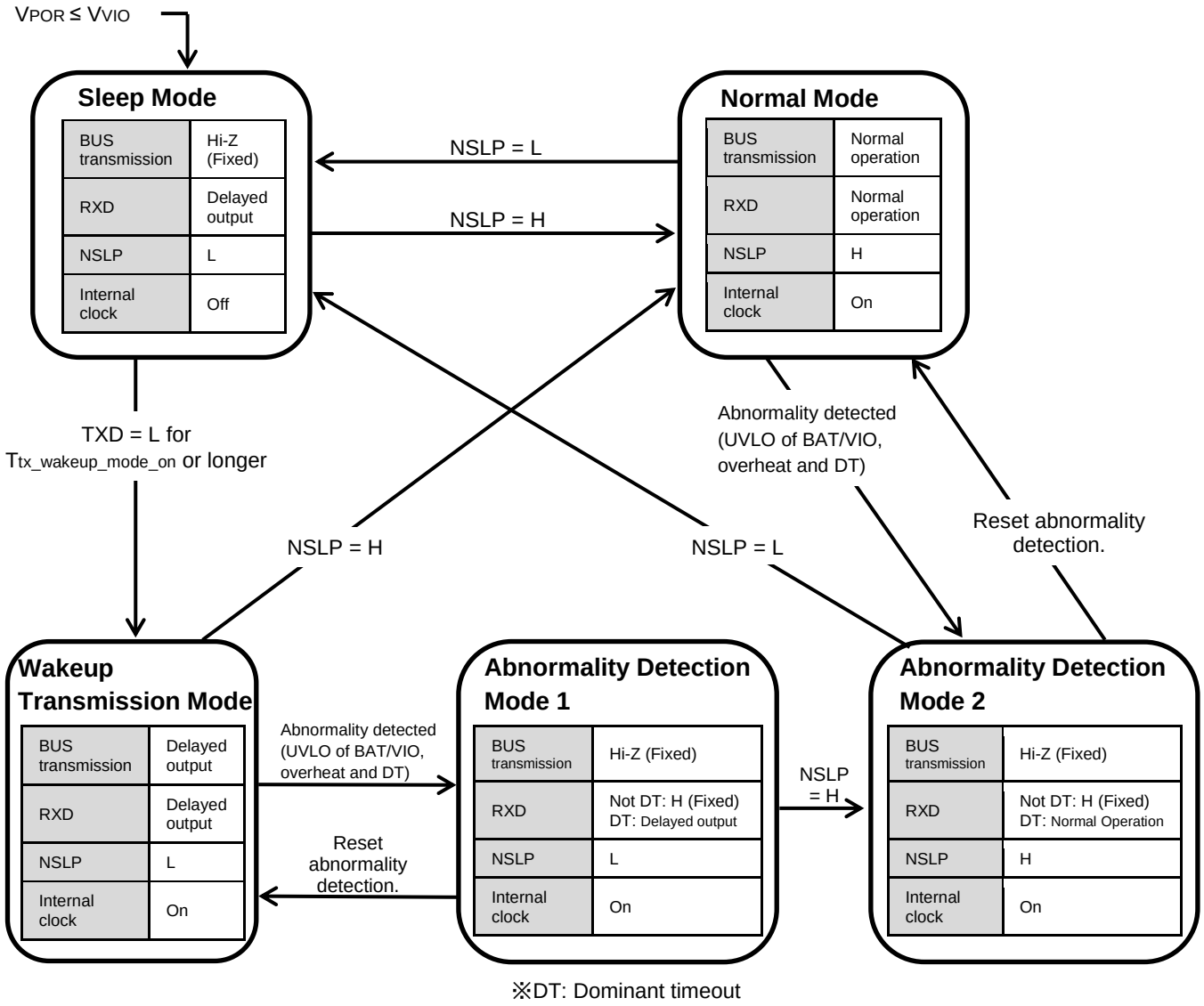


Figure 5.3 Equivalent Circuits around Pins

6. STATE TRANSITION

State transition of this IC is shown below.



Reset when V_{VIO} ＜ V_{POR}. This applies to all modes.

Figure 6 State Transition

6.1. Transition to Sleep Mode

When the V_{VIO} power is turned on, the IC enters Sleep Mode. Additionally, if NSLP = L is input from an MCU during Normal Mode, the IC will transition to Sleep Mode within a certain time period, Tsleep.

6.2. Transition to Wakeup Transmission Mode

The IC will transition to Wakeup Transmission Mode if it receives “TXD = L” from an MCU for a period of Ttx_wakeup_mode_on or longer when in Sleep Mode. In Wakeup Transmission Mode, TXD signal received from an MCU can be transmitted from BUS as a wake-up pulse for the responder node trigger. Please refer to "7.2.3.1 Responder Node" for information on wakeup pulses for the responder node trigger.
According to the CXPI standards, transmission of wakeup pulse in the responder node trigger is part of operational sequence initiated by a responder node. Please refer to “7.2.2.1. Commander Node” for information on wakeup pulses for the commander node trigger.

6.3. Transition to Normal Mode

When this IC is in sleep mode, both commander node and responder node transition to normal mode when NSLP = H has been received from MCU.
When this IC is in wakeup transmission mode, it transmits a wakeup pulse triggered by a responder node and then transitions to normal mode by receiving “NSLP = H” from MCU.
CXPI communication can be conducted normally in normal mode. Also, a commander node transmits a wakeup pulse.

6.4. Transition to Abnormality Detection Mode 1

When the state is wakeup transmission mode and abnormality is detected, the state transitions to abnormality detection mode 1. For types of abnormality detection and conditions for detection and resetting, refer to “7.1 Abnormality Detection Functions.” Note that the state transitions to wakeup transmission mode when abnormality detection has been reset. In addition, when NSLP = H is received from MCU, the state transitions to abnormality detection mode 2.

6.5. Transition to Abnormality Detection Mode 2

When the state is normal mode and abnormality is detected, the state transitions to abnormality detection mode 2. For types of abnormality detection and conditions for detection and resetting, refer to “7.1 Abnormality Detection Functions”. Note that the state transitions to normal mode when abnormality detection has been reset. In addition, when NSLP = L is received from MCU, the state transitions to sleep mode.

7. OPERATIONS

7.1. Abnormality Detection Functions

As abnormality detection functions, this IC is equipped with detection functions for TXD dominant timeout, overheat, and undervoltage of BAT and VIO. Each detection function works as follows.

Table 7.1 Abnormality Detection Functions

Abnormality Detection Function	Description	BUS Output	RXD Output
BAT undervoltage (UVLO of BAT)	Detects by $V_{BAT} \leq V_{BAT\_UV}$. Resets by $V_{BAT} \geq V_{BAT\_UV}$.	Hi-Z(H) Fixed	High Fixed
VIO undervoltage (UVLO of VIO)	Detects by $V_{VIO} \leq V_{VIO\_UV}$. Resets when $V_{VIO} \geq V_{VIO\_UV}$.	Hi-Z(H) Fixed	High Fixed
VIO undervoltage (POR)	Detects by $V_{VIO} \leq V_{POR}$ and resets.	Hi-Z(H) Fixed	High Fixed
Dominant timeout	Detects by TXD = Low for T_{DTC} or longer. Resets when TXD input = High.	Hi-Z(H) Fixed	Delayed output or normal operation
Overheat (TSD)	Detects by $T_{TSD} \leq T_J$. Resets when T_{HYS} is low and $T_J < 150$℃.	Hi-Z(H) Fixed	High Fixed

7.1.1. BAT Undervoltage Detection (UVLO of BAT)

When the power source voltage (V_{BAT}) is V_{BAT_UV} or lower, undervoltage is detected, and BUS output and RXD output are stopped. When the power source voltage recovers to V_{BAT_UV} or higher, abnormality detection is reset.

7.1.2. VIO Undervoltage Detection (UVLO of VIO)

When the power source voltage (V_{VIO}) is V_{VIO_UV} or lower, undervoltage is detected, and BUS output and RXD output are stopped. When the power source voltage is recovered to V_{VIO_UV} or higher, abnormality detection is reset.

7.1.3. VIO Undervoltage Detection (POR)

When the power source voltage (V_{VIO}) is V_{POR} or lower, undervoltage is detected, and the IC is reset. This operation applies to all modes defined in “6. State Transition.”

7.1.4. Overheat Detection (TSD)

When the IC’s Tj temperature has exceeded T_{TSD}, overheat is detected, and BUS output and RXD output are stopped. After that, when the temperature decreases from the detected overheat temperature by about T_{HYS} or Tj < 150℃ is observed, the abnormality detection is reset.
Note that the overheat detection function is not tested at mass production shipment, but an alternative test is conducted.

7.1.5. Dominant Timeout

When “Low” time of TXD input from the microcomputer is long and dominant time of BUS output has exceeded T_{DTC}, this timeout is detected, BUS output is stopped and is set to Hi-Z (H). RXD outputs delayed output in abnormality detection mode 1 and operates normally in abnormality detection mode 2, and when any other abnormality is detected simultaneously, the other abnormality detection is given priority and RXD becomes High (Fixed).
When TXD input becomes High, abnormality detection is reset.

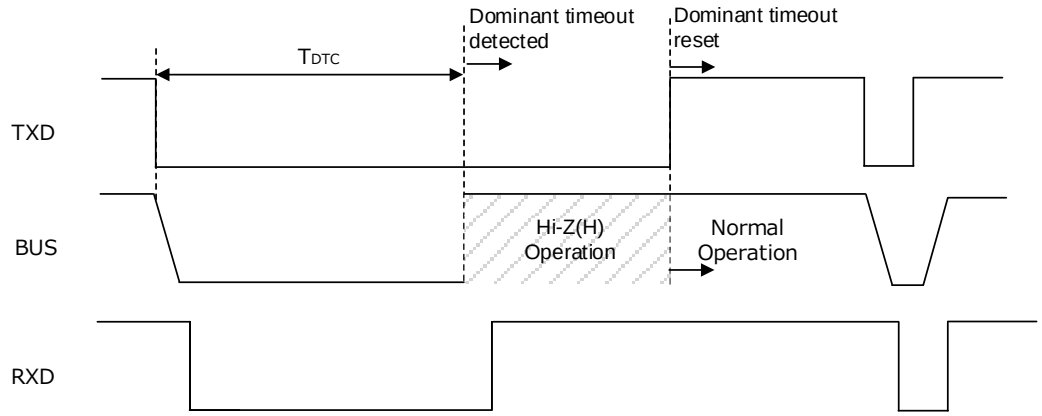


Figure 7.1.5 Sequence of Dominant Timeout

7.2. Operation Sequences

7.2.1. Sleep Mode and Power-off Sequence

7.2.1.1. Commander Node

When the state transitions to sleep mode and power is turned off, the operation sequence of commander node is as shown below.

(MS Pin = High)

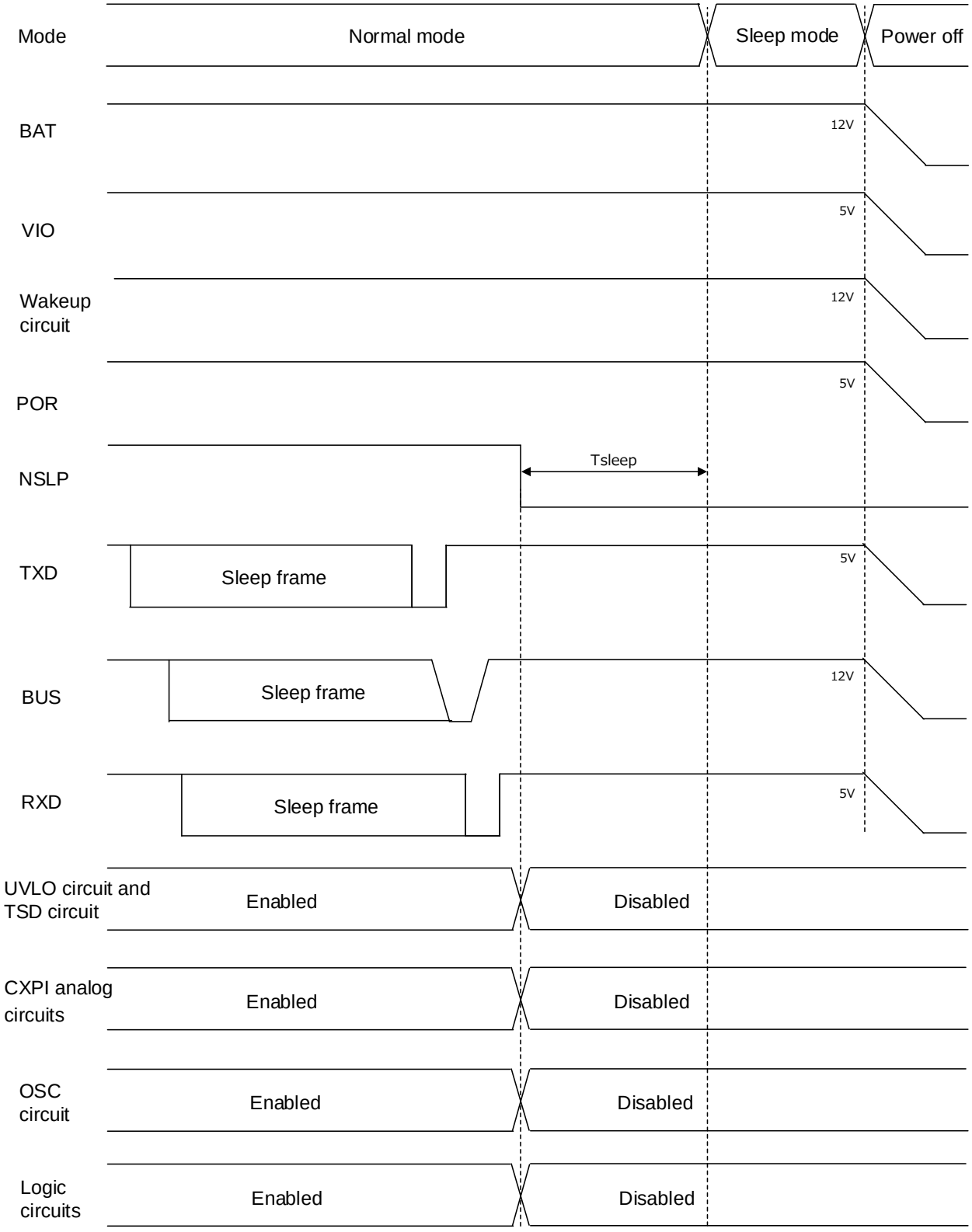


Figure 7.2.1.1 Sleep Mode and Power-off Sequence (Commander Node)

1. Sleep Frame from MCU is transmitted to BUS.
2. NSLP = L is received from MCU, which triggers to turn off UVLO, TSD, OSC, analog circuits (transceiver circuit and receiver circuit).
3. When OSC is turned off, the digital logic is also turned off.
4. Operations in 2 and 3 above are completed during Tsleep, and the IC then operates in sleep mode.
5. When the voltage of BAT and VIO become low, the wakeup circuit is turned off. Also, $V_{VIO} < V_{POR}$ is observed and power is turned off.

Supplementary information:

Sleep Frame is not directly related to the operation of TB9032FNG. Sleep Frame transmission at a commander node related to sleep mode transition is described as reference information.

7.2.1.2. Responder Node

When the state transitions to sleep mode and power is turned off, the operation sequence of a responder node is as shown below.

(MS Pin = Low)

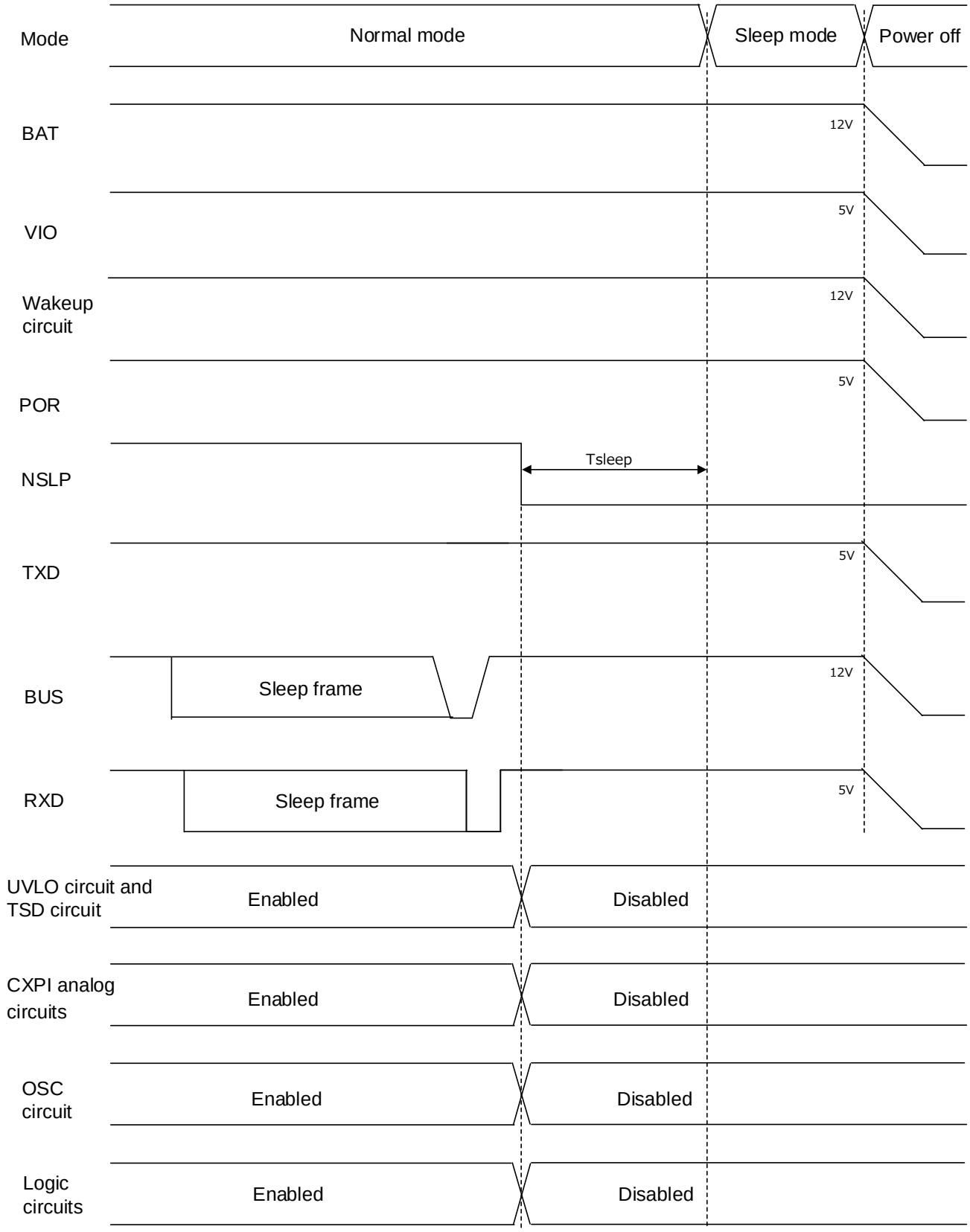


Figure 7.2.1.2 Sleep Mode and Power-off Sequence (Responder Node)

1. Sleep Frame is received from BUS.
2. NSLP = L is received from MCU, which triggers to turn off UVLO, TSD, OSC, analog circuits (transceiver circuit and receiver circuit).
3. When OSC is turned off, digital logic is also turned off.
4. Operations in 2 and 3 are completed during Tsleep, and the IC operates in the sleep mode.
5. When the voltage of BAT and VIO become low, the wakeup circuit is turned off. In addition, $V_{VIO} < V_{POR}$ is observed and power is turned off.

Supplementary information:

Sleep Frame is not directly related to the operation of TB9032. Sleep Frame reception at a responder node related to sleep mode transition is described as reference information.

7.2.2. Power-on and Wakeup Sequence (Triggered by a Commander Node)

7.2.2.1. Commander Node

When a wakeup is caused by a commander node, the operation sequence of the commander node is as shown below.

(MS Pin = High)

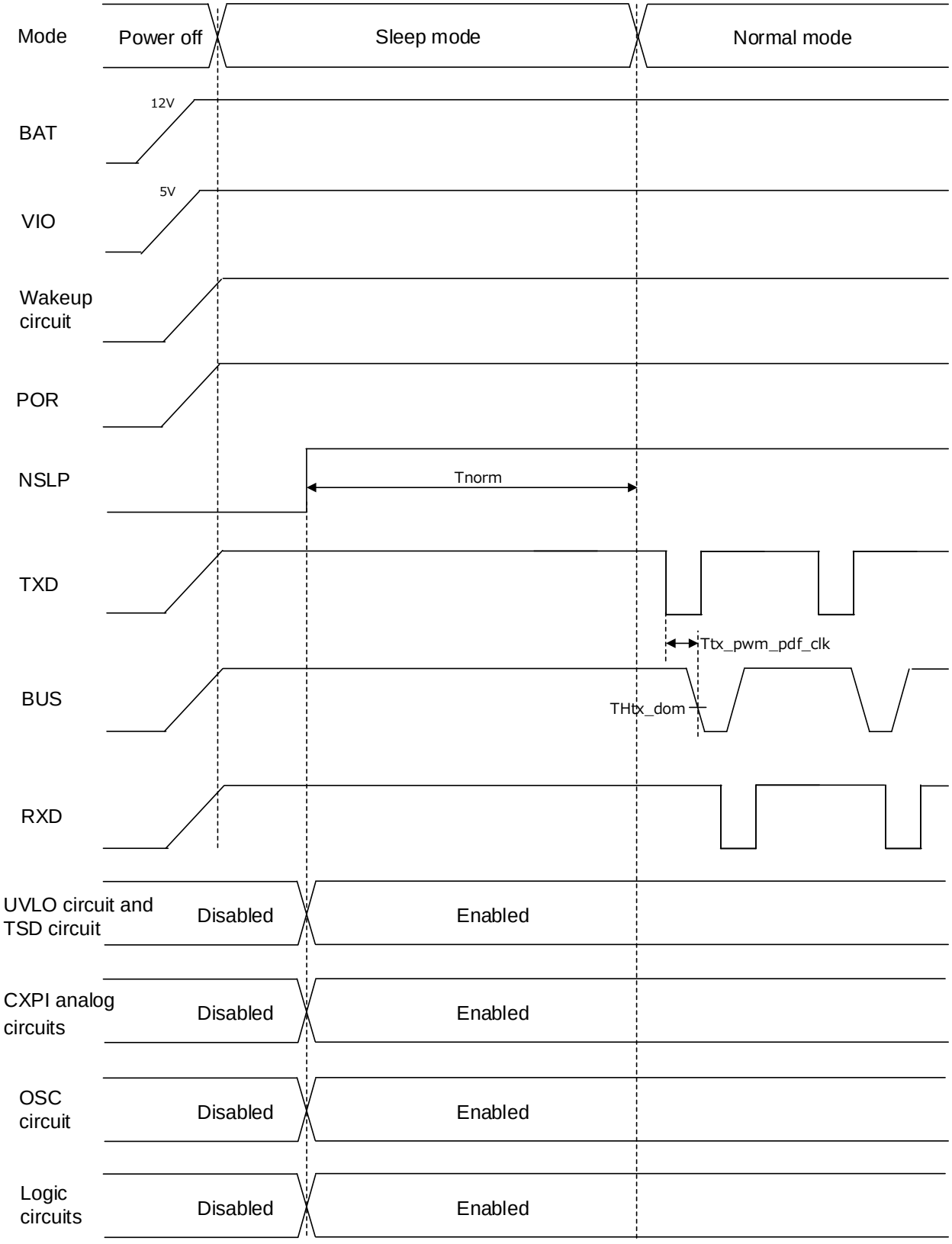


Figure 7.2.2.1 Wakeup Sequence Triggered by a Commander Node (Commander Node)

1. When the power sources of BAT and VIO are turned on, the wakeup circuit and POR circuit are turned on.
2. Pins of TXD, BUS and RXD are fixed at High, and the IC operates in this state in sleep mode.
3. When NSLP = H is received from MCU, it triggers to turn on UVLO, TSD, OSC and analog circuits (transceiver circuit and receiver circuit).
4. OSC starts normal operation.
5. The digital logic is turned on triggered by NSLP = H and starts normal operation using OSC as reference.
6. Operations in 3 to 5 above are completed during Tnorm, and the IC then starts operation in the normal mode. By receiving TXD = L from MCU and transmitting BUS = L for a certain period or longer, a wakeup pulse triggered by the commander node is transmitted.

Supplementary explanation:
When NSLP = H is input with the power sources of BAT and VIO off, Internal circuitry doesn't work. After that, when the power sources of BAT and VIO are turned on, operations from 3 to 6 above are conducted triggered by NSLP = H, and the state transitions to normal mode.

7.2.2.2. Responder Node

When a wakeup is caused by a commander node, the operation sequence of the responder node is as shown below.

(MS Pin = Low)

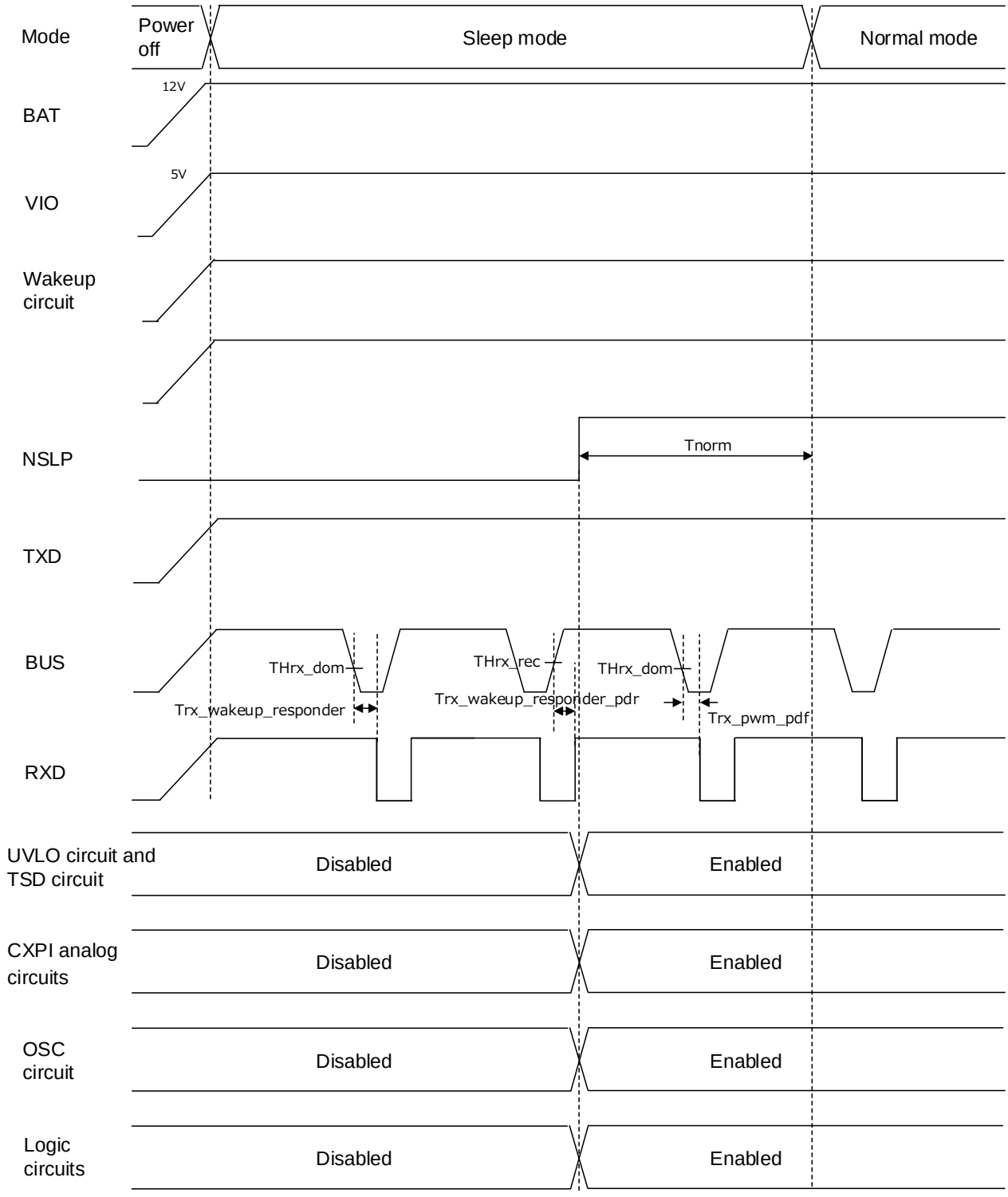


Figure 7.2.2.2 Wakeup Sequence Triggered by a Commander Node (Responder Node)

1. When the power sources of BAT and VIO are turned on, the wake-up circuit and POR circuit are turned on.
2. Pins of TXD, BUS and RXD are fixed at High, and in this state, the IC operates in sleep mode.
3. ”Low” width (a wake-up pulse triggered by the commander node) for over Trx_wakeup_responder is received from BUS, and is output to RXD.
4. When NSLP = H is received from MCU, it triggers to turn on UVLO, TSD, OSC and analog circuits (transceiver circuit and receiver circuit).
5. OSC starts normal operation.
6. The digital logic is turned on triggered by NSLP = H, and starts normal operation using OSC as reference.
7. Operations in 4 to 6 above are completed during Tnorm, the IC then works in the normal mode.

Notes:

1. Request regarding use for microcomputers:
   When the state transitions to normal mode, do not make judgment between logic 0 and logic 1 based on RXD value before Tnorm has passed.
   When the state changes from sleep mode to normal mode, the delay time of RXD changes as described below.
   When RXD is output in the wakeup circuit with NSLP = L, the fall (TF) delay time from BUS to RXD is Trx_wakeup_responder: 5 μs (max), and the rise time (TR) is also Trx_wakeup_responder_pdr: 5 μs (max). After, when NSLP = H occurs and CXPI analog circuits have been turned on, the fall (TF) delay time from BUS to RXD changes to Trx_pwm_pdf: 2.1 μs (max) and rise time (TR) is also Trx_pwm_pdr: 2.1 μs (max).
2. In the wakeup sequence, the timing when RXD value becomes valid is 0.5 ms after the power sources of BAT and VIO have been turned on, so it should be taken into consideration.

7.2.3. Power-on and Wakeup Sequence (Triggered by a Responder Node)

7.2.3.1. Responder Node

When a wakeup is caused by a responder node, the operation sequence of the responder node is as shown below.

(MS Pin = Low)

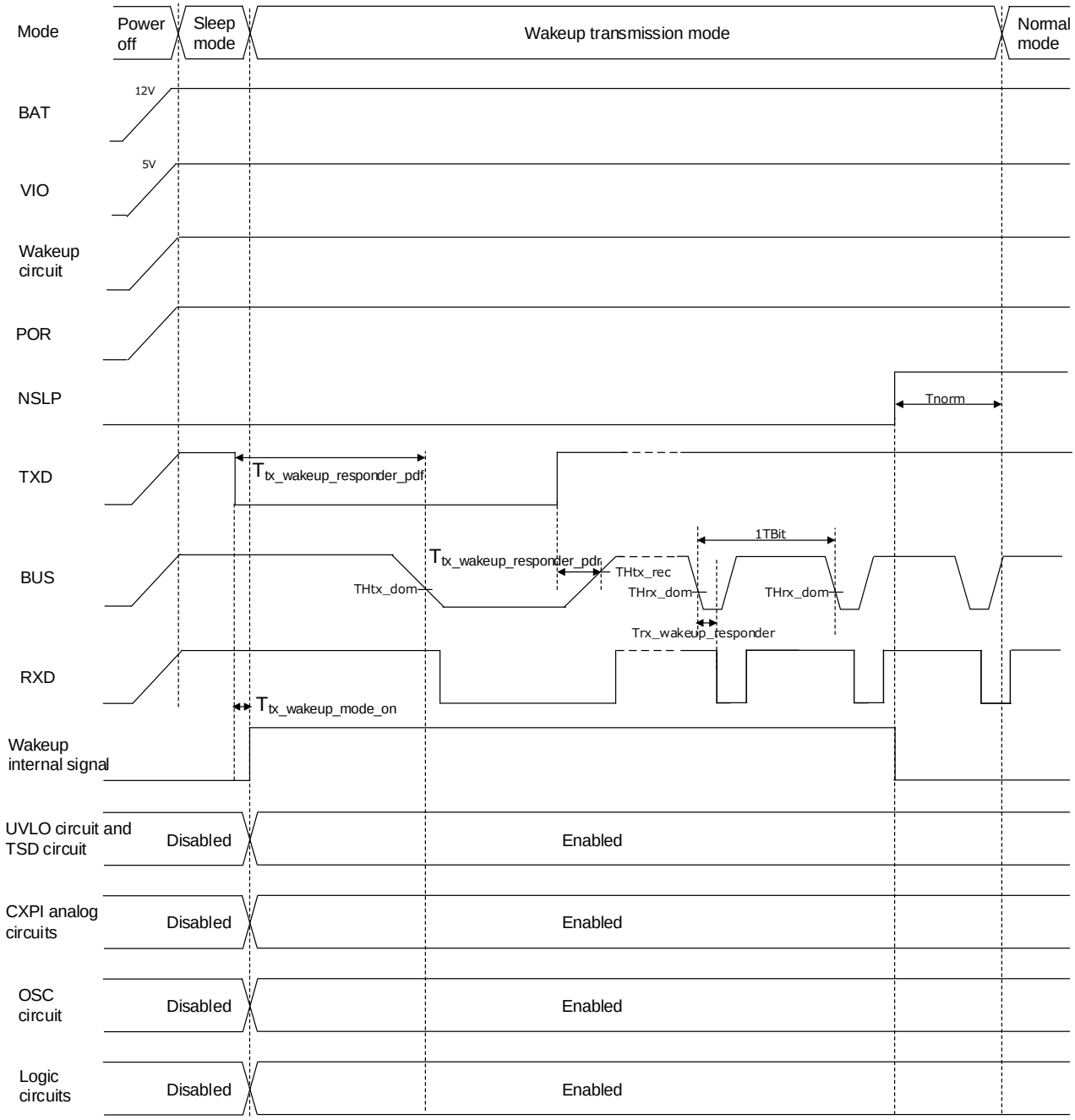


Figure 7.2.3.1 Wakeup Sequence Triggered by a Responder Node (Responder Node)

1. When the power sources of BAT and VIO are turned on, the wakeup circuit and POR circuit are turned on.
2. Pins of TXD, BUS and RXD are fixed to High (Note 1), and in this state, the IC works in sleep mode.
3. When TXD = L is received from MCU for a period (Trx_wakeup_mode) or longer, the wakeup internal signal is fixed to High.
4. Triggered by the wakeup internal signal, UVLO, TSD and analog circuits (transceiver circuit and receiver circuit) are turned on. (Wakeup transmission mode starts.)
5. In addition, OSC and Logic are turned on, and BUS = L is output.

Supplementary explanation 1:
The BUS = L output here works as a wakeup pulse triggered by the responder node.
Supplementary explanation 2:
The delay time from TXD = L to BUS = L is Ttx_wakeup_responder_pdf.

6. After, when Low width (wakeup pulse from the commander node) for the period of Trx_wakeup_responder or longer from BUS is detected, it is output to RXD.
7. When NSLP = H is received from MCU, it makes the wakeup internal signal Low.
8. OSC starts normal operation.
9. The digital logic starts normal operation using OSC as reference.
10. Operations 7 to 9 are completed during Tnorm, and the IC then works in normal mode.

Supplementary explanation 3:
Even if TXD = H happens before BUS = L is output after the wakeup internal signal becomes High, the wakeup internal signal is fixed at High, and circuits (BGR, UVLO, TSD, analog circuits, OSC and logic) are turned on. However, after that, BUS = L (wakeup pulse triggered by the responder node) is not output.

Note 1:
When TXD = L is externally set while the power sources are being turned on, the state does not transition to sleep mode and wakeup transmission mode starts. In wakeup transmission mode, the consumption current is equivalent to that in normal mode.

7.2.3.2. Commander Node [RS-OP-01232]

When a wakeup is caused by a responder node, the operation sequence of the commander node is as shown below.

(MS Pin = High)

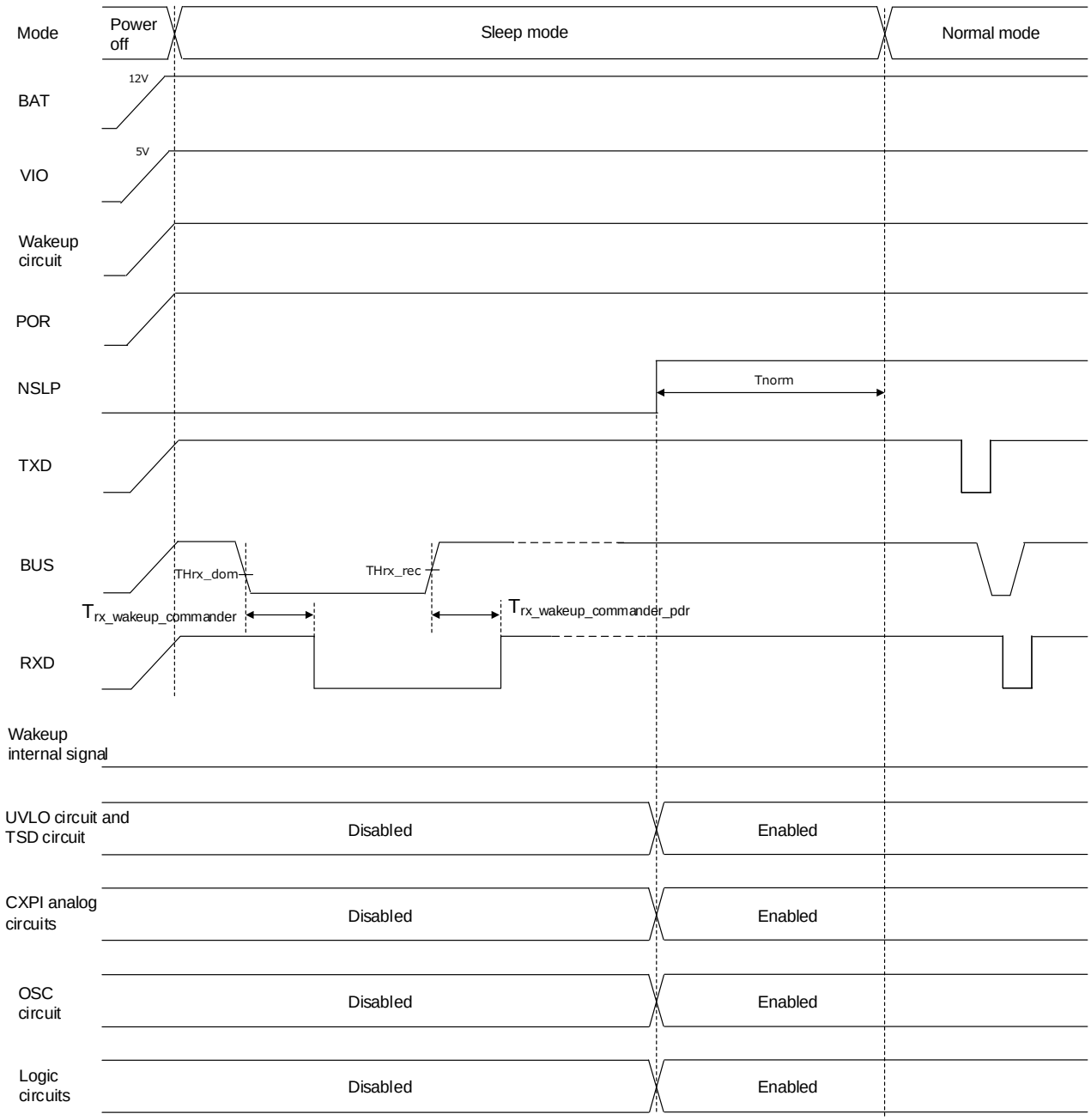


Figure 7.2.3.2 Wakeup Sequence Triggered by a Responder Node (Commander Node)

1. When the power sources of BAT and VIO are turned on, the wakeup circuit and POR circuit are turned on.
2. Pins of TXD, BUS and RXD are fixed to High, and in this state, the IC works in sleep mode.
3. When “Low” width (a wakeup pulse triggered by the responder node) for the period of Trx_wakeup_commander or longer from BUS is detected, it is output to RXD.
4. When NSLP = H is received from MCU, it triggers to turn on UVLO, TSD, OSC and analog circuits (transceiver circuit and receiver circuit).
5. OSC starts normal operation.
6. The digital logic is turned on triggered by NSLP = H, and starts normal operation using OSC as reference.
7. Operations 4 to 6 above are completed during Tnorm, and the IC then works in normal mode.

7.2.4. Delay Time in BUS Transmission

When TXD = L is received from MCU and BUS = L is output in normal mode, the delay time differs between a commander node and a responder node.

7.2.4.1. Commander Node

To transmit clock to BUS, a commander node operates with the same delay time from TXD to BUS for both rise and fall (Ttx_pwm_pdf_clk = Ttx_pwm_pdr = 16.9 µs (max)). The slope of the BUS is 8 µs (max) (Ttx_pwm_slope_clk) from the fall of the BUS to the dominant (THtx_dom = 0.3 × VBAT).

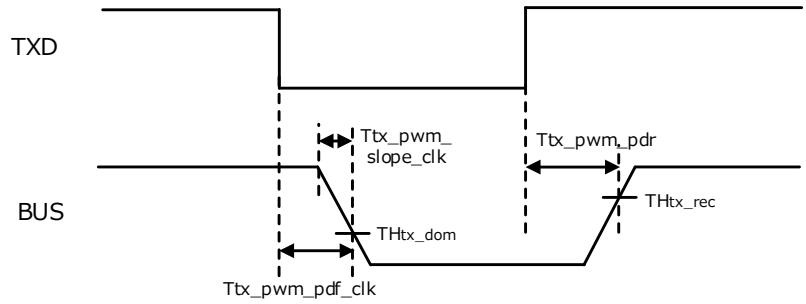


Figure 7.2.4.1 Delay Time in BUS Transmission (Commander Node)

7.2.4.2. Responder Node

As a responder node receives BUS clock from the commander node and transmits a BUS waveform of logic 0, the fall delay time of the BUS is short. The delay time from TXD to BUS fall is 2.9 µs (max) (Ttx_pwm_pdf). For the BUS rise, however, the delay time is the same as that of a commander node (Ttx_pwm_pdr = 16.9 µs (max)).

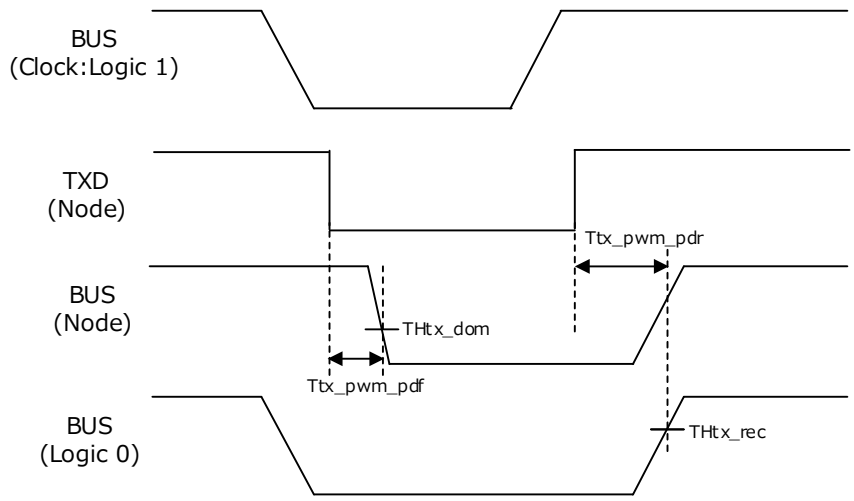


Figure 7.2.4.2 Delay Time in BUS Transmission (Responder Node)

8. ABSOLUTE MAXIMUM RATINGS

Table 8 Absolute Maximum Ratings

(Ta = -40 to 125 °C unless otherwise specified)

Item	Symbol	Pin	Test Conditions	Rating	Unit
Power source voltage 1	V_{BAT}	BAT	Voltage between BAT and GND pin	- 0.3 to 40	V
Power source voltage 2	V_{VIO}	VIO	Voltage between VIO and GND pin	- 0.3 to 6	V
Input withstand voltage 1	V_{MS}	MS	$V_{MS} \leq V_{BAT}$	- 0.3 to V_{BAT}	V
Input withstand voltage 2	V_{TXD}、V_{NSLP}	TXD, NSLP	-	- 0.3 to V_{VIO} + 0.3 and -0.3 to 6	V
Output withstand voltage	V_{RXD}	RXD	-	- 0.3 to V_{VIO} + 0.3 and - 0.3 to 6	V
I/O withstand voltage	V_{BUS}	BUS	7 V $\leq V_{BAT} \leq$ 18 V	- 27 to 40	V
Output current	I_{BUS}	BUS	-	200	mA
Junction temperature	Tj	-	-	150	℃
Storage temperature range	Tstg	-	-	- 55 to 150	℃

The absolute maximum ratings are standard values that must not be exceeded even momentarily. When any absolute maximum rating is exceeded, it may cause destruction, degradation, or damage to the IC and/or other parts. Design systems so that absolute maximum ratings are not exceeded in any operating condition.
Please use this IC within the operating ranges described above.

8.1. Thermal Resistance

・Thermal resistance values that include the below board

- Θ_{JA} ・・・ Between junction and ambient temperature
  Θ_{JA} = 147.9 ℃/W

- Ψ_{JT} ・・・ Between junction and package upper surface center
  Ψ_{JT} = 5.6 ℃/W

・Board conditions

- 1-layer board
- Board size (FR-4) 114.3 mm × 76.2 mm × 1.57 mm t
  1st layer Copper foil thickness: 70 μm
  Copper foil area: 1L land pattern area：Cu 50 %, lead wires area：Cu 25 %
  (Area of land pattern and lead wires is assumed.)

9. OPERATING RANGES

Table 9 Operating Ranges

Item	Symbol	Pin	Operating Range	Unit	Remark
BAT normal operation range	V_{BAT}	BAT	7 to 18	V	-
Function operation (BAT high voltage)	V_{BAT}	BAT	18 to 27	V	Function operation only (Note 1), (Note 2)
Function operation (BAT low voltage)	V_{BAT}	BAT	V_{BAT_UV} to 7	V	Function operation only (Note 1), (Note 2)
VIO normal operation range	V_{VIO}	VIO	4.5 to 5.5	V	Supports 5 V power source of microcomputer
Function operation (VIO low voltage)	V_{VIO}	VIO	V_{VIO_UV} to 4.5	V	Function operation only (Note 1), (Note 2)
Operating temperature range	Ta	-	- 40 to 125	℃	-

Note 1) Details of the function operation are as shown below.

1. Receives BUS recessive and maintains RXD = H.
2. Transmits RXD = L when TXD = L is received.
   Load condition: RL = 500 Ω
3. Maintains the state without being shut down.
4. Electrical characteristics during function operation follow “10.2. Characteristics of RXD and TXD”.
5. During BAT function operation, VIO is assumed to be within the normal operation range.
6. During VIO function operation, BAT is assumed to be within the normal operation range.
7. Except the function operation following 1 to 6 above, each item in the electrical characteristics table is not guaranteed.

Note 2) The operating ranges and operating conditions are design guidelines to obtain expected performance. As each item is an independent guideline, specified values in the electrical characteristics table and so on must also be checked when designing.

10. ELECTRICAL CHARACTERISTICS

10.1. IC Overall

Table 10.1 IC Characteristics

(V_{VIO} = 4.5 to 5.5 V, VBAT = 7 to 18 V, Ta = -40 to 125 °C unless otherwise specified)

Characteristics	Symbol	Test Conditions	Min	Typ.	Max	Unit
BAT						
Consumption current (Sleep)	I_{BAT_SLP}	NSLP = L, TXD = H, BUS = V_{BAT}	-	5	-	μA
Consumption current (Normal)	I_{BAT_NORM}	NSLP = H	-	-	2	mA
BAT undervoltage detection	V_{BAT_UV}	Function operation only during V_{BAT_UV} detection by VBAT < 7 V (Note 1)	5.0	-	6.7	V
BAT undervoltage detection hysteresis	V_{BAT_HYS}	-	-	0.5	-	V
BAT slew rate while power source rising	T_{BAT_SLPOE}	-	0.01	-	2	V/μs
VIO						
Consumption current (Sleep)	I_{VIO_SLP}	NSLP = L	-	3	-	μA
Consumption current (Normal)	I_{VIO_NORM}	NSLP = H	-	-	10	mA
VIO undervoltage detection	V_{VIO_UV}	Function operation only during V_{VIO_UV} detection by VVIO < 4.5 V (Note 1)	3.7	-	4.5	V
VIO undervoltage detection hysteresis	V_{VIO_HYS}	-	-	0.5	-	V
POR detection	V_{POR}	-	1.5	2.5	3.5	V
POR detection hysteresis	V_{POR_HYS}	-	-	0.2	-	V
VIO slew rate while power source rising	T_{VIO_SLPOE}	-	0.01	-	0.5	V/μs
NSLP						
Input High voltage	V_{IH_NSLP}	-	0.8 × V_{VIO}	-	-	V
Input Low voltage	V_{IL_NSLP}	-	-	-	0.2 × V_{VIO}	V
Input hysteresis	V_{NSLP_HYS}	-	0.032 × V_{VIO}	0.065 × V_{VIO}	0.13 × V_{VIO}	V
Pull-down resistance	R_{NSLP}	NSLP = 5 V	50	100	200	kΩ
MS						
Input High voltage	V_{IH_MS}	-	3.0	-	-	V
Input Low voltage	V_{IL_MS}	-	-	-	2.0	V
Input hysteresis	V_{MS_HYS}	-	-	0.5	-	V
Input High current	I_{IH_MS}	MS = V_{BAT} = 12 V	-	3	-	μA
Input Low current	I_{IL_MS}	MS = 0 V	-	0	-	μA
Oscillator						
Frequency	OSC	-	-	8	-	MHz

Note 1: Not included in the shipping inspection items.

10.2. Characteristics of RXD and TXD

Table 10.2 Characteristics of RXD and TXD

(V_{VIO} = 4.5 to 5.5 V, VBAT = 7 to 18 V, Ta = -40 to 125 °C unless otherwise specified)

Characteristics	Symbol	Test Conditions	Min	Typ.	Max	Unit
RXD						
Output High voltage	V_{OH_RXD}	Load Current =-1 mA Function operation period supported as well	V_{VIO}-0.5	-	-	V
Output Low voltage	V_{OL_RXD}	Load Current = 1 mA Function operation period supported as well	-	-	0.5	V
TXD						
Input High voltage	V_{IH_TXD}	Function operation period supported as well	0.8 × V_{VIO}	-	-	V
Input Low voltage	V_{IL_TXD}	Function operation period supported as well	-	-	0.2 × V_{VIO}	V
Hysteresis	V_{HYS_TXD}		0.032 × V_{VIO}	0.065 × V_{VIO}	0.13 × V_{VIO}	V
Pull-up resistance	R_{TXL}	TXD = 0 V	50	100	200	kΩ
Loop characteristics						
Loop delay time during function operation	$T_{LOOP\_FUNC\_PDF}$	Time between TXD = L input and RXD = L output	-	-	100	μs

10.3. BUS (DC Characteristics)

Table 10.3 BUS (DC Characteristics)

(V_{VIO} = 4.5 to 5.5 V, VBAT = 7 to 18 V, Ta = -40 to 125 °C unless otherwise specified)

Characteristics	Symbol	Test conditions	Min	Typ.	Max	Unit
BUS dominant output voltage	V_{OL_BUS}	V_{TXD} = 0 V、R_L(Note 1) = 500 Ω V_{BAT} = 7.3 V	-	-	1.2	V
		V_{TxD} = 0 V, R_L = 500 Ω 7.3 V ≤ V_{BAT} ≤ 10 V	-	-	0.2 × V_{BAT}	V
		V_{TxD} = 0 V, R_L = 500 Ω 10 V ≤ V_{BAT} ≤ 18 V	-	-	2.0	V
BUS recessive output voltage	V_{OH_BUS}	TXD = H	0.8 × V_{BAT}	-	V_{BAT}	V
Current when BUS is short-circuited (DC)	I_{BUS_LIM}	V_{BUS} = V_{BAT} = 18 V	40	-	200	mA
Leak current when BUS dominant	$I_{BUS\_PAS\_dom}$	V_{BUS} = 0 V、V_{BAT} = 12 V	-1	-	-	mA
Leak current when BUS recessive	$I_{BUS\_PAS\_rec}$	8 V < V_{BAT} < 18 V, 8 V < V_{BUS} < 18 V, V_{BAT} < V_{BUS}	-	-	20	μA
Leak current when ground disconnected	$I_{BUS\_NO\_GND}$	GND= V_{BAT}, 0 < V_{BUS} < 18 V, V_{BAT} = 12 V	-1	-	1	mA
Leak current when power is off	$I_{BUS\_NO\_BAT}$	V_{BAT} = 0 V、0 V < V_{BUS} < 18 V	-	-	100	μA
Dominant threshold voltage when receiving	V_{BUSdom}	Voltage by which receiving node judged as L level	-	-	0.423 × V_{BAT}	V
Recessive threshold voltage when receiving	V_{BUSrec}	Voltage by which receiving node judged as H level	0.556 × V_{BAT}	-	-	V
Center voltage when receiving	V_{BUSCNT}	-	0.475 × V_{BAT}	0.5 × V_{BAT}	0.525 × V_{BAT}	V
Hysteresis	V_{BUShys}	-	-	-	0.133 × V_{BAT}	V

Note1: R_L is a pull-up resistance between BAT and BUS externally connected to the IC.

10.4. BUS (AC Characteristics)

Table 10.4 BUS (AC Characteristics)

(V_{VIO} = 4.5 to 5.5 V, V_{BAT} = 7 to 18 V, Ta = -40 to 125 °C, 1 Tbit = 50 µs unless otherwise specified)

Characteristics	Symbol	Test conditions	Min	Typ.	Max	Unit
Dominant detection time when receiving wake-up (commander node)	$T_{rx\_wakeup\_commander}$	TH_{rx_dom} = 0.423 × V_{BAT} (Figure 7.2.3.2.)	30	90	150	µs
Shutoff pulse width at wakeup (commander node)	$T_{rx\_wakeup\_commander}$	All pulses with dominant 30 µs or less are shut off (Note 1).	-	-	30	µs
Pass-through (recognized) pulse width at wakeup (commander node)	$T_{rx\_wakeup\_commander}$	All pulses with dominant 100 to 2600 µs are passed through (recognized) (Note 1).	100	200	2600	µs
Rise delay when receiving wakeup (commander node)	$T_{rx\_wakeup\_commander\_pdr}$	TH_{rx_rec} = 0.6 × V_{BAT} (Figure 7.2.3.2.)	30	90	150	µs
Dominant detection time when receiving wake-up (responder node)	$T_{rx\_wakeup\_responder}$	TH_{rx_dom} = 0.423 × V_{BAT} (Figure 7.2.2.2.)	0.5	2.75	5	µs
Shut-out pulse width at wakeup (responder node)	$T_{rx\_wakeup\_responder}$	All pulses with dominant 0.5 µs or less are shut out (Note 1).	-	-	0.5	µs
Pass-through (recognized) pulse width at wakeup (responder node)	$T_{rx\_wakeup\_responder}$	All pulses with dominant 3~2600 µs are passed through (recognized) (Note 1).	3	6	2600	µs
Rise delay when receiving wakeup (responder node)	$T_{rx\_wakeup\_responder\_pdr}$	TH_{rx_rec} = 0.6 × V_{BAT} (Figure 7.2.2.2.)	0.5	2.75	5	µs
Fall delay when transmitting wakeup (responder node) TXD⇒BUS	$T_{tx\_wakeup\_responder\_pdf}$	C_{BUS} = 10 nF, R_{BUS} = 500 Ω	-	-	195	µs
Rise delay when transmitting wake-up (responder node) TXD⇒BUS	$T_{tx\_wakeup\_responder\_pdr}$	C_{BUS} = 10 nF, R_{BUS} = 500 Ω	-	-	26.6	µs
Rise delay of wakeup internal signal (responder node)	$T_{tx\_wakeup\_mode\_on}$	Pulses of min. or less are ignored.	3	-	10	µs
Transition time to normal mode	T_{norm}	-	-	-	1	ms
Transition time to sleep mode	T_{sleep}	-	-	-	1	ms
Difference in bit widths (Figure 10.4.1)	ΔT_{bit_driver}	Difference from Tbit_ref, bit width of reference communication speed, TH = 50 %	-0.5	-	+0.5	%
Fall delay when receiving BUS (Figure 10.4.2) BUS ⇒RXD	$T_{rx\_pwm\_pdf}$	C_{BUS} = 1 nF, R_{BUS} = 1 kΩ V_{th_dom} = 0.423 × V_{BAT}	-	-	2.1	µs
Rise delay when receiving BUS (Figure 10.4.2) BUS⇒ RXD	$T_{rx\_pwm\_pdr}$	C_{BUS} = 1 nF, R_{BUS} = 1 kΩ V_{th_rec} = 0.556 × V_{BAT}	-	-	2.1	µs
RXD delay time difference when receiving BUS (Figure 10.4.2)	T_{RX_SYM}	(T_{rx_sym} = $T_{rx\_pwm\_pdf}$–$T_{rx\_pwm\_pdr}$) C_{BUS} = 1 nF, R_{BUS} = 1 kΩ	-2	-	2	µs

Note 1: Not included in shipping inspection items.

(V_{VIO} = 4.5 to 5.5 V, V_{BAT} = 7 to 18 V, Ta = -40 to 125 °C, 1 Tbit = 50 µs unless otherwise specified)

Characteristics	Symbol	Test conditions	Min	Typ.	Max	Unit
Slope in BUS transmission (commander node) (Figure 7.2.4.1)	$T_{tx\_pwm\_slope\_clk}$	C_{BUS} = 10 nF, R_{BUS} = 500 Ω TH_{tx_dom} = 0.3 × V_{BAT}	-	-	8	µs
Fall delay in BUS transmission (commander node) TXD⇒ BUS (Figure 7.2.4.1)	$T_{tx\_pwm\_pdf\_clk}$	C_{BUS} = 10 nF, R_{BUS} = 500 Ω TH_{tx_dom} = 0.3 × V_{BAT}	-	-	16.9	µs
Rise delay in BUS transmission TXD⇒BUS (Figure 7.2.4.1, Figure 7.2.4.2)	$T_{tx\_pwm\_pdr}$	C_{BUS} = 10 nF, R_{BUS} = 500 Ω TH_{tx_rec} = 0.7 × V_{BAT}	-	-	16.9	µs
Fall delay in BUS transmission (responder node) TXD⇒BUS (Figure 7.2.4.2)	$T_{tx\_pwm\_pdf}$	C_{BUS} = 10 nF, R_{BUS} = 500 Ω TH_{tx_dom} = 0.3 × V_{BAT}	-	-	2.9	µs
BUS dominant time for Logic 1 (Figure 10.4.3)	$T_{tx\_1\_lo\_dom}$	C_{BUS} = 1 nF, R_{BUS} = 1 kΩ TH_{tx_dom} = 0.3 × V_{BAT} Ttxpwm_lo = 13.75 µs	5.5	-	-	µs
BUS recessive time for Logic 1 (Figure 10.4.3)	$T_{tx\_1\_lo\_rec}$	C_{BUS} = 10 nF, R_{BUS} = 500 Ω TH_{tx_rec} = 0.7 × V_{BAT} Ttxpwm_lo = 11.25 µs	-	-	22.5	µs
BUS dominant time for Logic 0 (Figure 10.4.4)	$T_{tx\_0\_lo\_dom}$	C_{BUS} = 1 nF, R_{BUS} = 1 kΩ TH_{tx_dom} = 0.3 × V_{BAT} Ttxpwm_lo = 16.75 µs	8.5	-	-	µs
BUS dominant time difference between Logic 1 and Logic 0	T_{TX_dif}	$T_{tx\_0\_lo\_dom} - T_{tx\_1\_lo\_dom}$ C_{BUS} = 10nF, R_{BUS} = 500 Ω Ttxpwm_lo = 12.5 µs (Logic 1) Ttxpwm_lo = 35 µs (Logic 0)	3	-	-	µs

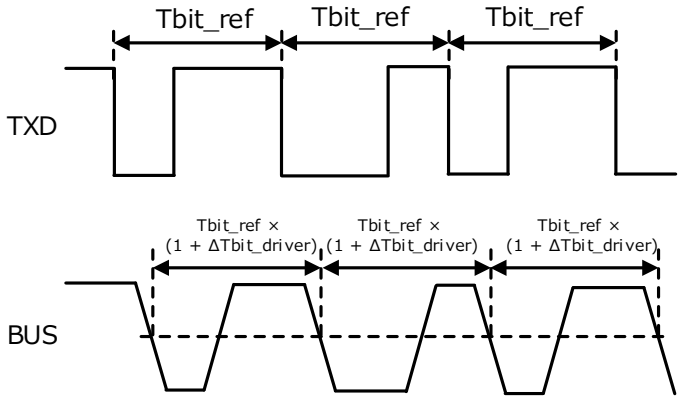


Figure 10.4.1 Difference in Bit Widths

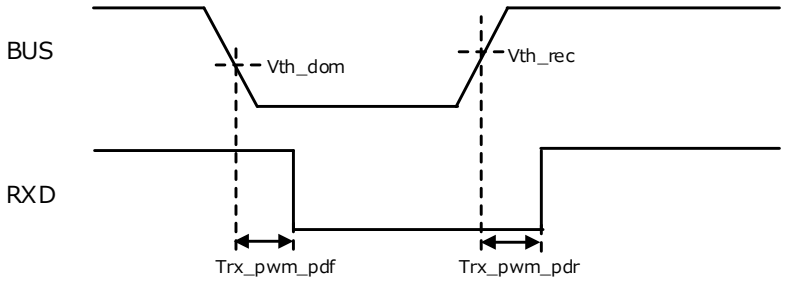


Figure 10.4.2 Delay Time when Receiving BUS

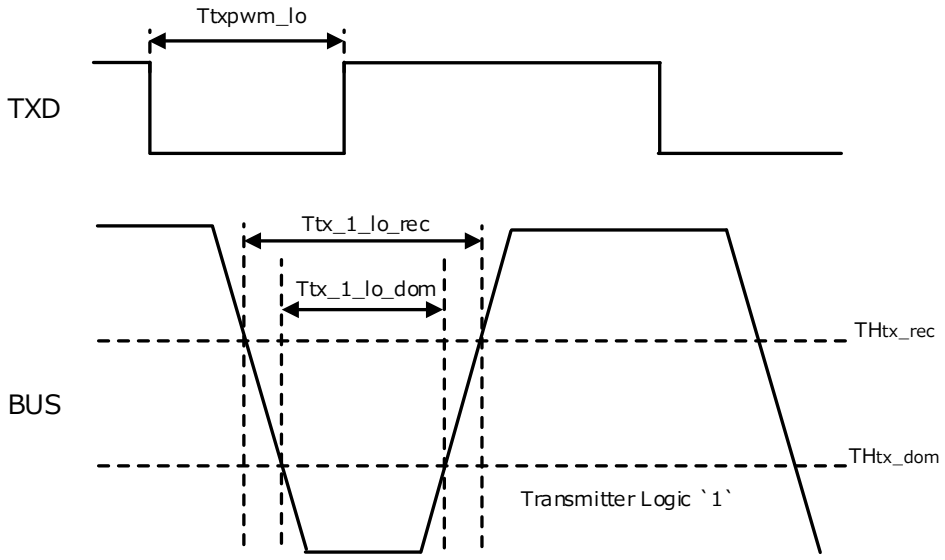


Figure 10.4.3 BUS Width for Logic 1

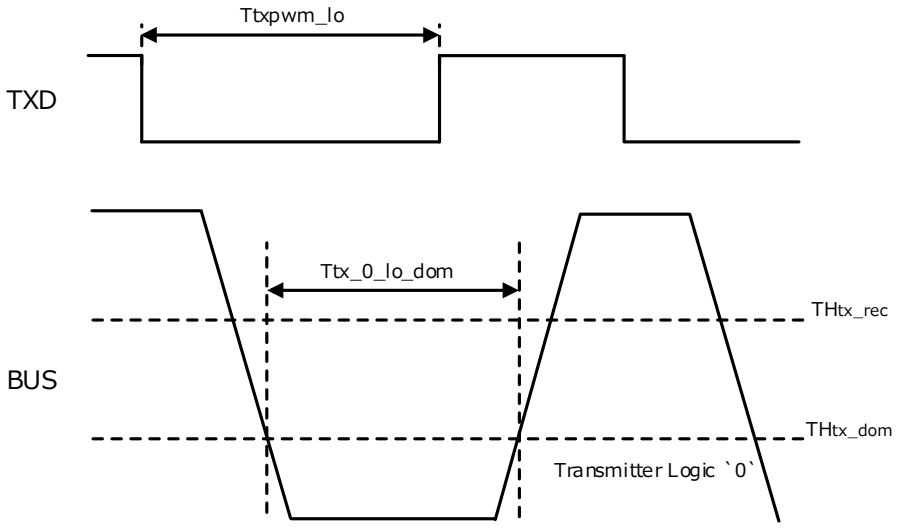


Figure 10.4.4 BUS Width for Logic 0

10.5. Others

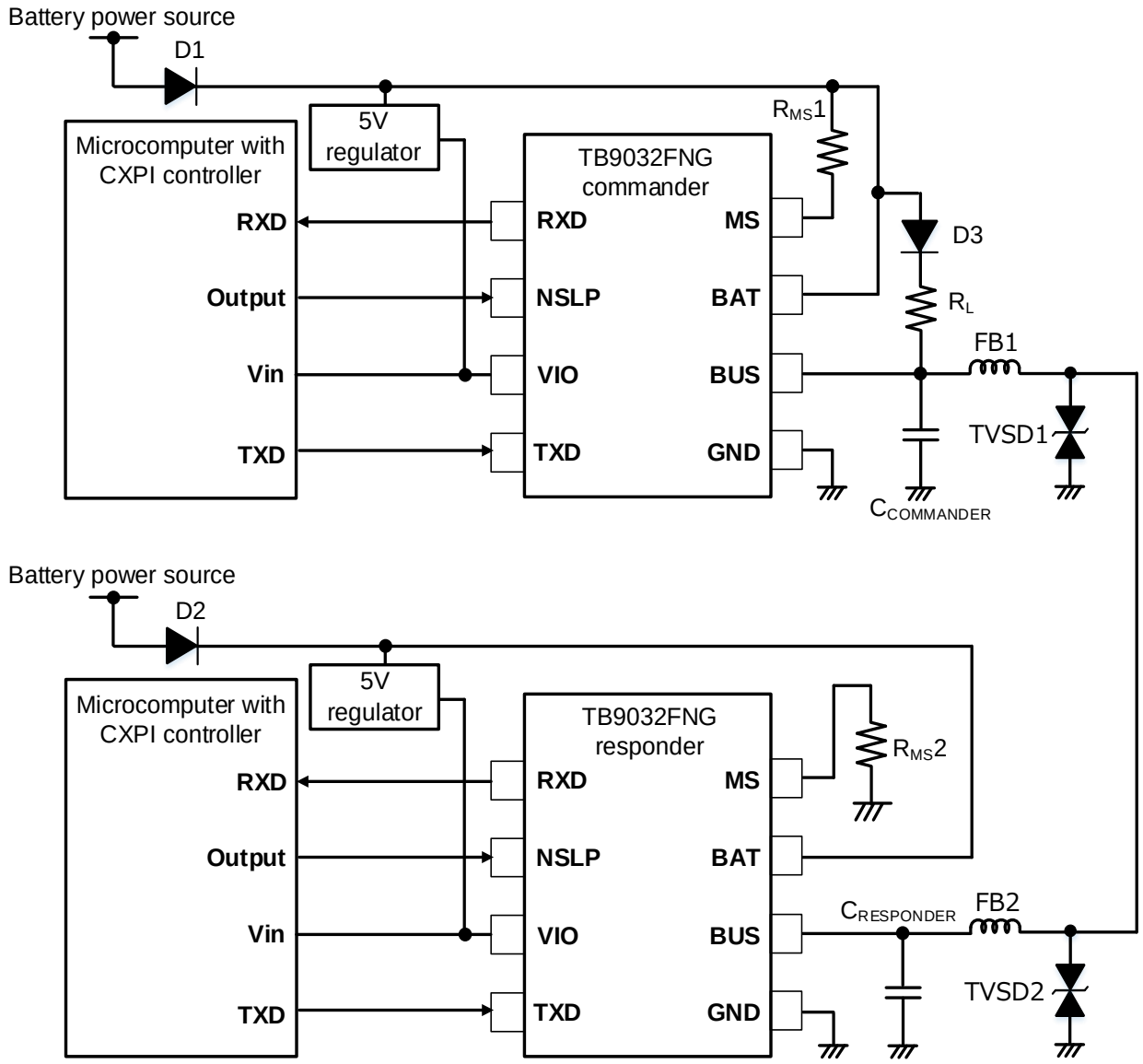
Table 10.5 Other Characteristics

(VBAT = 7 to 18 V, Ta = -40 to 125 °C unless otherwise specified)

Characteristics	Symbol	Test conditions	Min	Typ.	Max	Unit
Others						
BUS external resistance (commander node)	R_L	External resistance between BAT and BUS of a commander node	900	1000	1100	Ω
BUS internal resistance (responder node)	$R_{RESPONDER}$	Internal specification	20	30	60	kΩ
BUS external diode voltage drop	V_F	External diode between BAT and BUS	0.4	0.7	1.0	V
MS pin external resistance	R_{MS}	-	-	10	-	kΩ
Allowable capacitance of commander node side	$C_{COMMANDER}$	-	-	220	-	pF
Allowable capacitance of responder side	$C_{RESPONDER}$	-	-	220	250	pF
BUS allowable capacitance 1	C_{BUS}	R_L = 1 kΩ	-	-	1	nF
BUS allowable capacitance 2	C_{BUS}	R_L = 660 Ω	-	-	4	nF
BUS allowable capacitance 3	C_{BUS}	R_L = 500 Ω	-	-	10	nF
Dominant timeout	T_{DTC}	-	2.6	6	15	ms
Overheat detection temperature (TSD)	T_{TSD}	-	150	175	200	℃
Hysteresis after overheat detection reset	T_{HYS}	-	-	10	-	℃

11. APPLICATION CIRCUIT EXAMPLE

11.1. Application Circuit Diagram



The above is just one example of application circuits, therefore, it can't be guaranteed as a design for a mass-produced product.
External parts are examples. Other external part other than those shown in the above figure can also be chosen."

Figure 11.1 Application Circuit Diagram

11.2. Reference value for parts

Table 11.2 Reference value for parts

Symbol	Reference part and reference value	Remarks
D1	CRG09A	-
D2	CRG09A	-
D3	LL4148 $V_F \leq 1.0V$	Refer to Table 10.5
$R_{MS}1$	10kΩ	Refer to Table 10.5
$R_{MS}2$	10kΩ	Refer to Table 10.5
R_L	1kΩ	Refer to Table 10.5
$C_{COMMANDER}$	220pF	Refer to Table 10.5
$C_{RESPONDER}$	220pF	Refer to Table 10.5
FB1	BLM18AG601SH1	-
FB2	BLM18AG601SH1	-
TVSD1	DF2B29FU	-
TVSD2	DF2B29FU	-

External parts values are examples. External part values other than those listed above can also be chosen.

12. NOTES ON CONTENTS

12.1. Notes on Contents

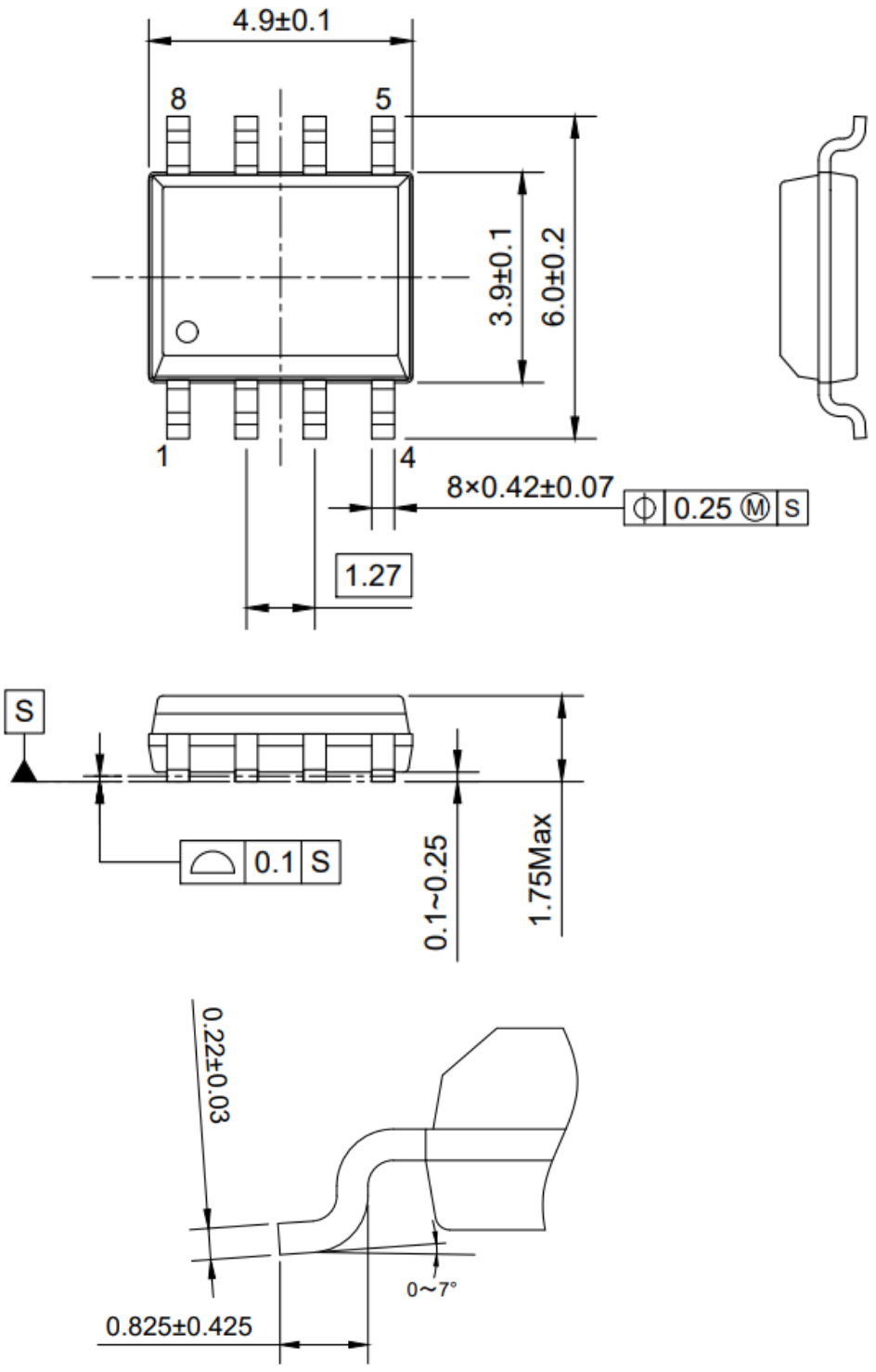
(1) Some of the functional blocks, circuits, or constants in the block diagrams may be omitted or simplified for explanatory purposes.
(2) The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.
(3) Timing charts may be simplified or partially omitted for explanatory purposes.
(4) The application circuits shown in this document are provided for reference purposes only. Components in the application circuit examples are not guaranteed to prevent malfunction or failure in the application circuits. Thorough evaluation of the application is required in selecting your components, especially at mass production design stage. Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.
(5) Components in the test circuits and test conditions are used only to obtain and confirm device characteristics. They are not guaranteed to prevent malfunction or failure in application equipment.

13. OUTLINE DRAWING

13.1. External Dimensions

P-SOP8-0405-1.27-002

(Unit: mm)



Mass: 0.08 g (typ.)

Figure 13.1 External Dimensions

13.2. Labeling Diagram

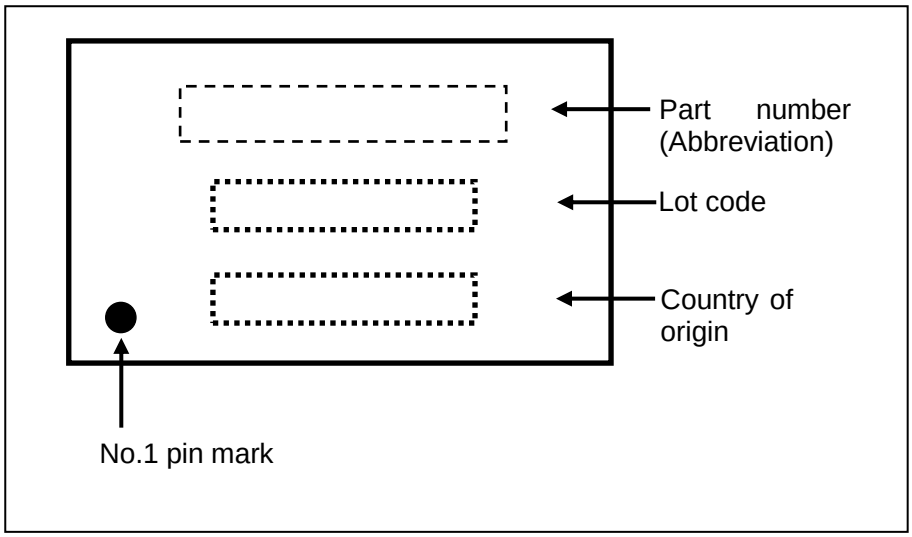
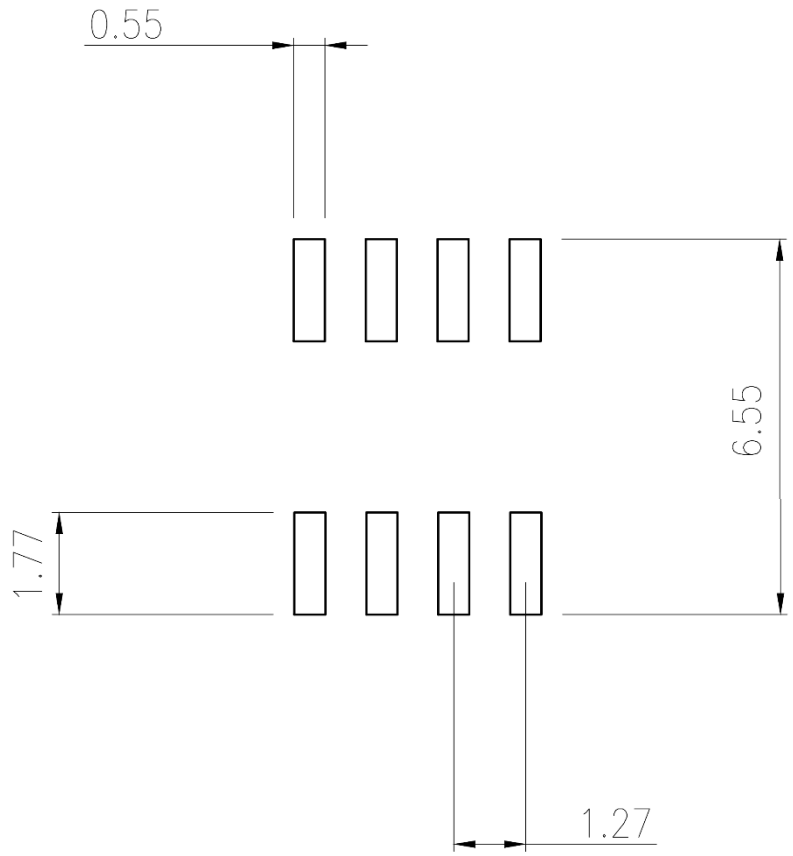


Figure 13.2 Labeling Diagram

13.3. Land Pattern Dimensions (for reference only)

Unit : mm



Notes

- All linear dimensions are given in millimeters unless otherwise specified.
- This drawing is based on JEITA ET-7501 Level3 and should be treated as a reference only.
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Figure 13. 3 Land Pattern Dimensions (for reference only)

14. IC USAGE CONSIDERATIONS

14.1. Notes on Handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even momentarily.
Do not exceed any of these ratings.
Exceeding rating(s) may cause device breakdown, damage, or deterioration, and may result in injury by explosion or combustion. In your design, make sure that absolute maximum ratings are not exceeded in any operating conditions. Use the product within described operating ranges.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over-current and/or IC failure. The IC may fully break down when used under conditions exceeding absolute maximum ratings, when wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and breakdown can lead smoke or combustion. To minimize effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

(3) Do not insert devices in the wrong orientation or incorrectly. Ensure that positive and negative pins of power supplies are connected properly. Otherwise, current or power consumption may exceed the absolute maximum rating and exceeding the rating(s) may cause the device breakdown, damage, or deterioration, and may result in injury by explosion or combustion. Also, do not ever use any device that was applied the current with inserting in the wrong orientation or incorrectly.

14.2. Reminders on Handling of ICs

(1) Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If thermal shutdown circuits operate against over temperature, clear the heat generation status immediately. Depending on the method of use and usage conditions, exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation. Thermal shutdown circuits temporarily detect or avoid abnormality and are not guaranteed to prevent ICs from breaking down. In addition, when the IC is not working within the guaranteed operating ranges, such functions may not work, leading to IC breakdown.

(2) Design the board so that heat is appropriately radiated, not to exceed specified junction temperature (Tj) at any time or condition. ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, design the device taking into consideration the effect of IC heat radiation on components used around the IC.

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