Single-Output High-Side N-Channel Power MOSFET Gate Driver Application and Circuit of the TPD7106F

Reference Guide

RD178-RGUIDE-01

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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1. Overview

Mechanical relays are widely known as switches that cut off and connect power supply lines from power sources such as batteries to loads. However, because mechanical relays mechanically open and connect contacts repeatedly, there is a problem with durability, and in applications where long-term reliability is required, semiconductor relays using semiconductor elements are becoming increasingly popular. Furthermore, with the increasing number of systems, the current capacitor required for semiconductor relays is increasing year by year, and by using a load switch circuit using a discrete N-channel power MOSFET with low on-resistance, a high-current semiconductor relay with low-loss and low heat generation can be realized.

TPD7106F is an N-channel power MOSFET gate driver for a single-output high-side switch with a built-in charge pump circuit. When combined with an external discrete N-channel MOSFET, a high-side switch can be configured for high-current applications. In addition, semiconductor relays have no contact wear unlike mechanical relays, so maintenance-free operation can be achieved. There are I/O terminals that control turn-off rapidly to protect MOSFET when an abnormality occurs, and they are independently controlled from the microcomputer to achieve safe operation.

This reference guide explains, the operation at the power supply reverse connection, which is important for the safe operation of the system including the high current load switch, and the application of the charge pump circuit.

Please refer to the datasheet for TPD7106F functions and detailed information.

Download TPD7106F datasheets from here → Click Here

1.1 Target Application

- Automotive junction box
- On-board power distribution module
- Semiconductor relay

Application circuit example

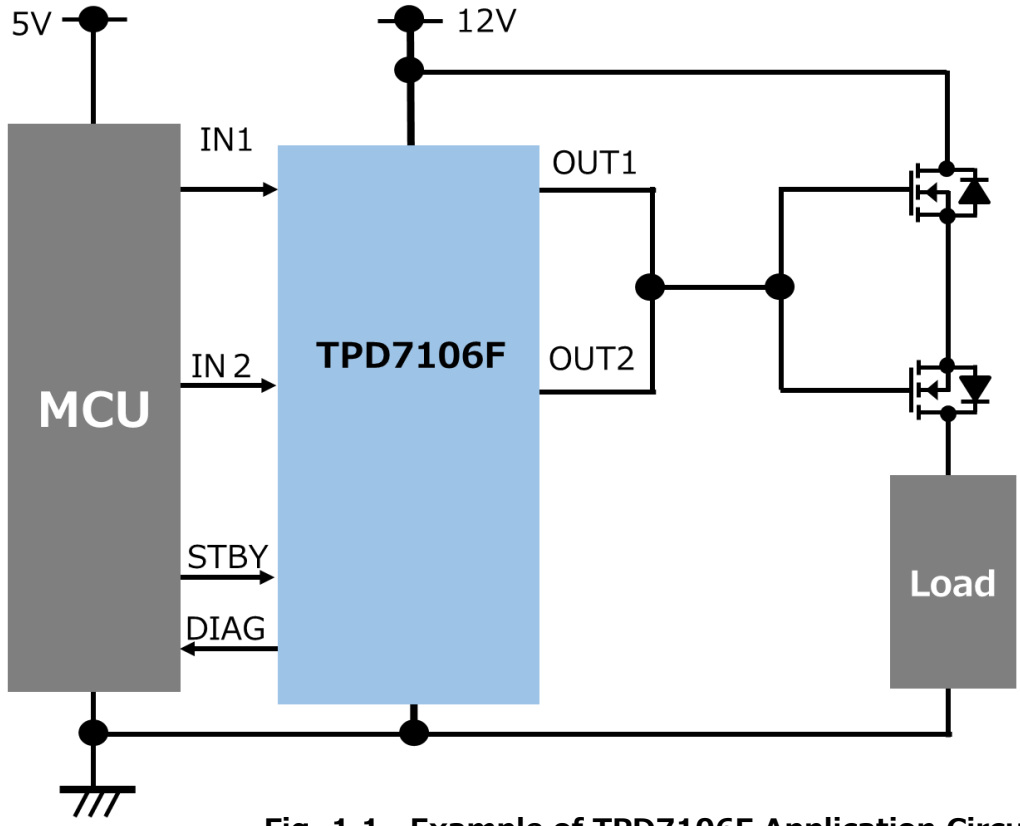

Fig. 1.1 Example of TPD7106F Application Circuit

2. Application Circuit Diagram

Fig. 2.1 is an application circuit diagram of a semiconductor-relay block composed of TPD7106F and TKR74F04PB (N-channel 40 V, 0.74 mΩ).

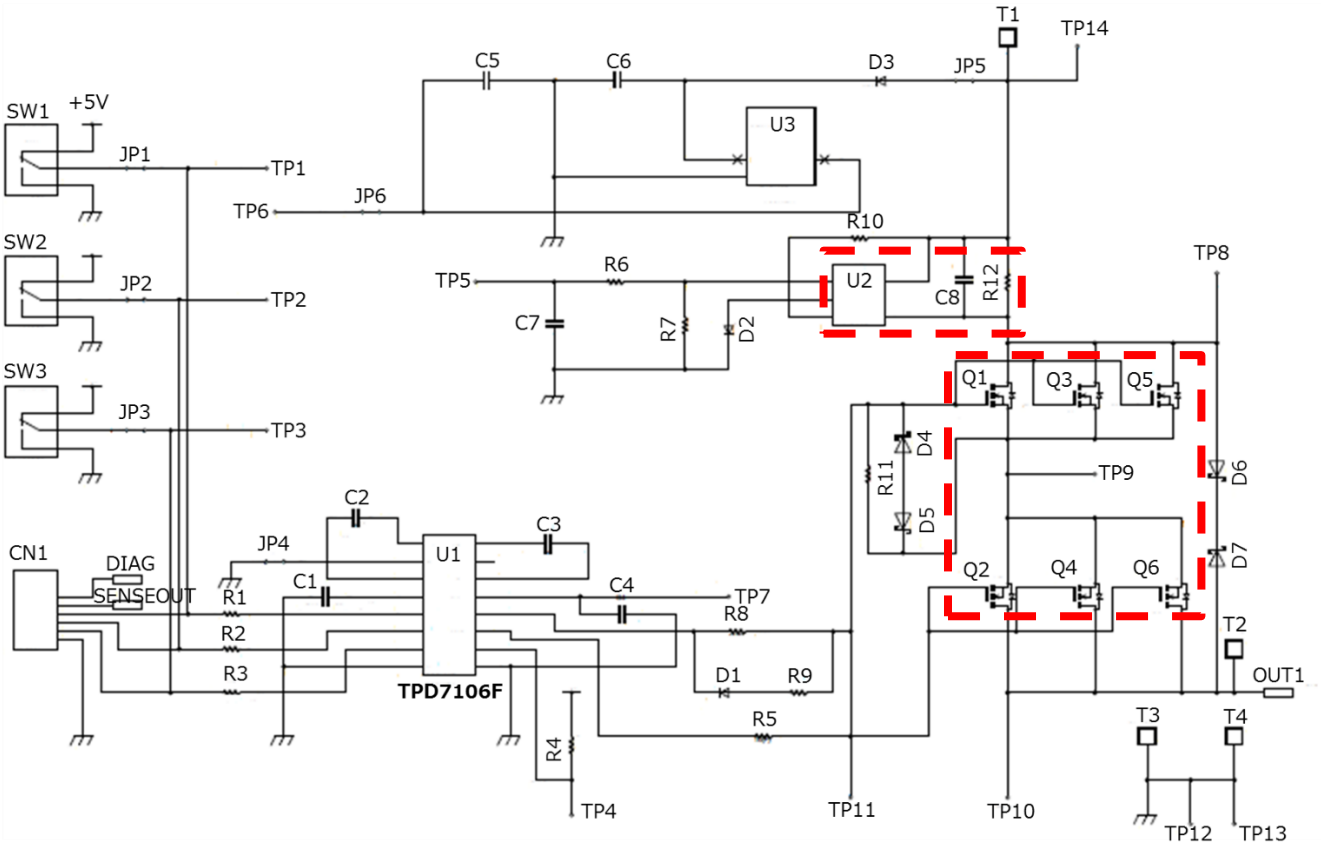

Fig. 2.1 Application Circuit Diagram (Semiconductor Relay)

MOSFET is a three-parallel connection of the source common, so TPD7106F are driving six MOSFET. The maximum load current is targeted at 200 A. The current sense amplifier uses a shunt resistor (R12) and a low-offset current sense amplifier (U2) for voltage conversion. The gate drive of the TPD7106F is described in Chapter 4.1.

The typical gate-source breakdown voltage of MOSFET is ±20 V.

D4 and D5, a zener diode of 16 V is inserted to protect the gate-source of MOSFET. The switching time adjustment is described in Chapter 4.2.

TPD7106F has a function to keep Q_1 to Q_6 off-state at the power supply reverse connection. Chapter 4.3 describes the operation.

TPD7106F has a built-in charge pump circuitry that is combined with an external capacitance so that it can drive an external discrete N-channel MOSFET with a low on-resistance. Therefore, the capacitor is required as an external component. For capacitors C2 and C3, 0.1 μF is selected. The selection method is described in Chapter 4.4.

TPD7106F has a built-in charge pump voltage drop detection function to check that the proper gate voltage is applied to MOSFET. The operation is described in chapter 4.5.

Please refer to the overall schematic as it is published in (RD178-SCHEMATIC-01).

The overall schematic is shown in this → Click Here

Download TKR74F04PB datasheet from here → Click Here

For more information about MOSFET, go here to → Click Here

3. Bill of Materials

Table 3.1 is a bill of materials in Application Circuit Diagram.

Table 3.1 Bill of Materials for Semiconductor Relay Circuits

No.	Ref.	Q'ty	Value	Part Number	Manufacturer	Description	Package Name	Standard Dimensions in mm (inches)
1	U1	1		TPD7106F	TOSHIBA	IPD (Gate driver)	SSOP-16	5.5×6.4
2	U2	1		LTC6101BCS5	LT	Current sense amplifier	TSOT-23	2.9×2.8
3	U3	1		TA7805F	TOSHIBA	Regulator	HSOP-3	6.5×9.5
4	Q1,Q2,Q3,Q4,Q5,Q6	6		TKR74F04PB	TOSHIBA	MOSFET	TO-220SM(W)	10.0×13.0
5	D1,D2	2		1SS352	TOSHIBA	Switching diode	SOD-323	2.5×1.25
6	D3	1		CRG09A	TOSHIBA	Rectifier diode	S-FLAT	1.6×3.5
7	D4,D5	2		CRZ16	TOSHIBA	Zener diode	S-FLAT	1.6×3.5
8	D6,D7	2		CMZ27	TOSHIBA	Zener diode	M-FLAT	2.4×4.7
9	R1,R2,R3,R4,R7	5	10k			Chip resistor, ±1%	1608	1.6×0.8 (0603)
10	R5	1	10			Chip resistor, ±1%	1608	1.6×0.8 (0603)
11	R6	1	47k			Chip resistor, ±1%	1608	1.6×0.8 (0603)
12	R8	1	1k			Chip resistor, ±1%	1608	1.6×0.8 (0603)
13	R9	1	100			Chip resistor, ±1%	1608	1.6×0.8 (0603)
14	R10	1	200			Chip resistor, ±1%	1608	1.6×0.8 (0603)
15	R11	1	200k			Chip resistor, ±1%	1608	1.6×0.8 (0603)
16	R12	1	0.5m	BVS-M-R0005	isabellenhuette	Shunt resistance, ±1%		6.35×3.05
17	C1,C4	2	1.0uF			Ceramic, 50V, ±10%	3216	3.2×1.6 (1206)
18	C2,C3,C6	3	0.1uF			Ceramic, 50V, ±10%	1608	1.6×0.8 (0603)
19	C5	1	10uF			Ceramic, 50V, ±10%	3216	3.2×1.6 (1206)
20	C7	1	1000pF			Ceramic, 50V, ±10%	1608	1.6×0.8 (0603)
21	C8	1	15pF			Ceramic, 50V, ±10%	2012	2.0×1.25
22	CN1	1		22-23-2061	molex	6-pole 1-row connector		
23	SW1,SW2,SW3	3		SS-12SDP2	NKK	Switch		
24	T1,T2,T3,T4	4		OP-486	OSADA	Terminal		
25	JP1,JP2,JP3,JP4,JP5,JP6	6		XJ8B-0211	OMRON	Jumper		
26	TP1～TP14	14		ST-2-2	MAC8	Monitor pin		

4. Application Circuit Design Guide

In addition to normal operation, this chapter describes the "operation at the power supply reverse connection" and "charge pump circuit", which are the points in designing, in chapter 4.1 to 4.5, including verification by simulation.

4.1 Normal Operation (Gate Drive of Power MOSFET)

Table 4.1 lists the truth values. The input pin IN1 is a control pin in normal operation. The input pin IN2 is a control pin in quick off mode. The quick off mode by IN2 is used to shut down MOSFET in abnormal operation such as load short circuit.

Table 4.1 Truth Table

IN1	IN2	STBY	OUT1	OUT2	State
X	X	L	Hiz	Hiz	Standby mode
L	L	H	L	Hiz	Normal operation
H	L	H	H	Hiz	
L	H	H	L	L	Quick off mode
H	H	H	L	L	

4.1.1 Simulation Verification

Check the simulation for normal operation, switching waveform (turn-on, turn-off time) and quick-off operation. Fig. 4.1 to Fig. 4.5 show the simulation circuit. Simulation is performed under the conditions and procedures in Table 4.2.

Table 4.2 Simulation Conditions and Procedures

1	V_{DD12}	12 V
2	V_{DD5}	5 V
3	V_{IN1}	0 V
4	V_{IN2}	0 V
5	Start of simulation	
6	V_{STBY}	0 to 5 V (1 ms standby mode)
7	V_{IN1}	0 to 5 V (2 ms normal operation)
8	V_{IN2}	0 to 5 V (9 ms quick-off operation)

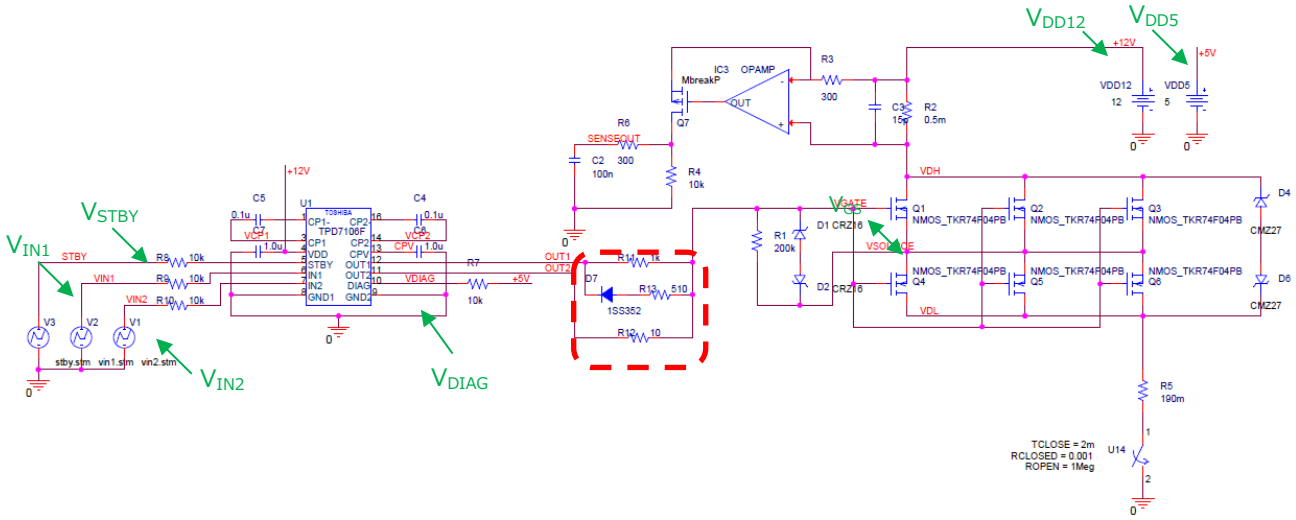

Fig. 4.1 Simulation Circuit (Normal Operation)

During the transition from standby mode to normal operation, V_{DIAG} is set to the L state (Fig. 4.2 ※1). This is because the charge pump voltage drop detection is activated. The charge pump voltage has reached the specified level and V_{DIAG} has returned to the H state. After 9 ms, V_{IN2} = L to H input causes a quick off, and MOSFET (Q_1 to Q_3) is turned off briefly. This quick-off takes precedence over V_{IN1}. The switching time is described in the next section. Adjust the switching speed in the simulation-circuit R11, R13, D7 by Fig. 4.1.

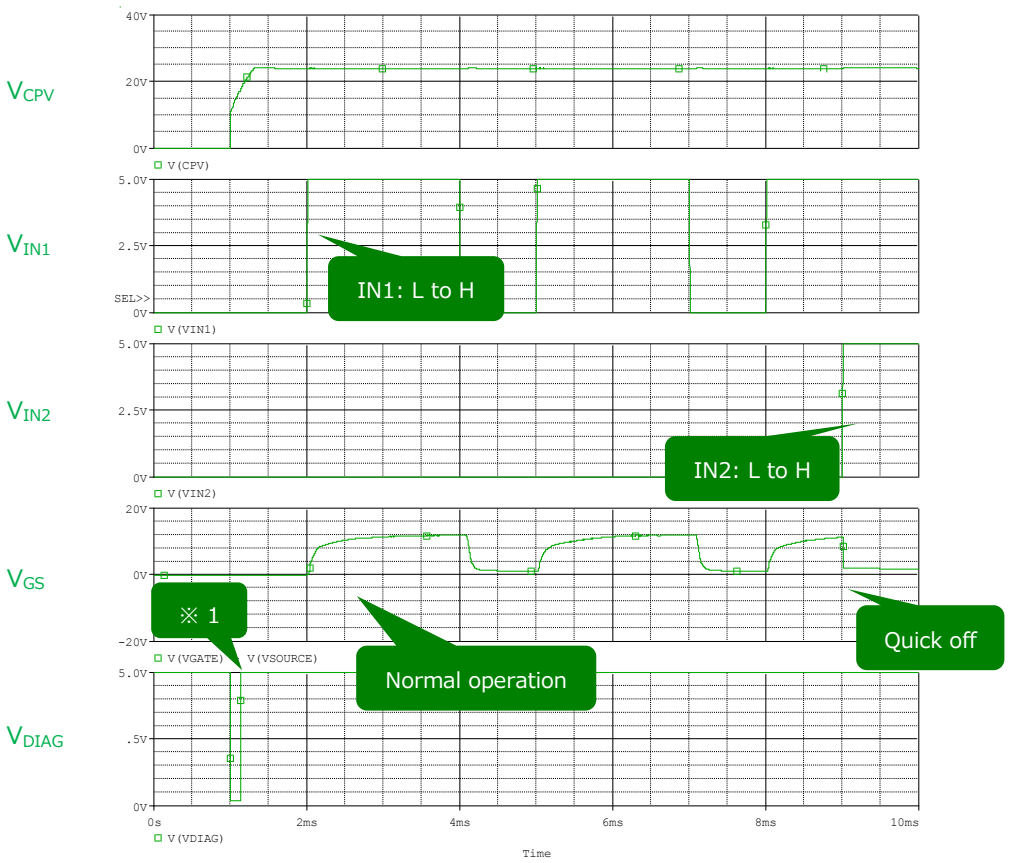

Fig. 4.2 Simulation Waveform (Normal Operation)

4.2 Switching Waveform

Fig. 4.3 to Fig. 4.5 show the switching waveforms. The simulation waveform V_{DS}, V_{GS} are waveform of six MOSFET because MOSFET Q_1 to Q_6 are connected in parallel. The turn-on time can be adjusted by changing R11 in Fig. 4.1. On the other hand, turn-off is adjusted with R13. Fig. 4.5 shows the turn-off waveform in quick off mode.

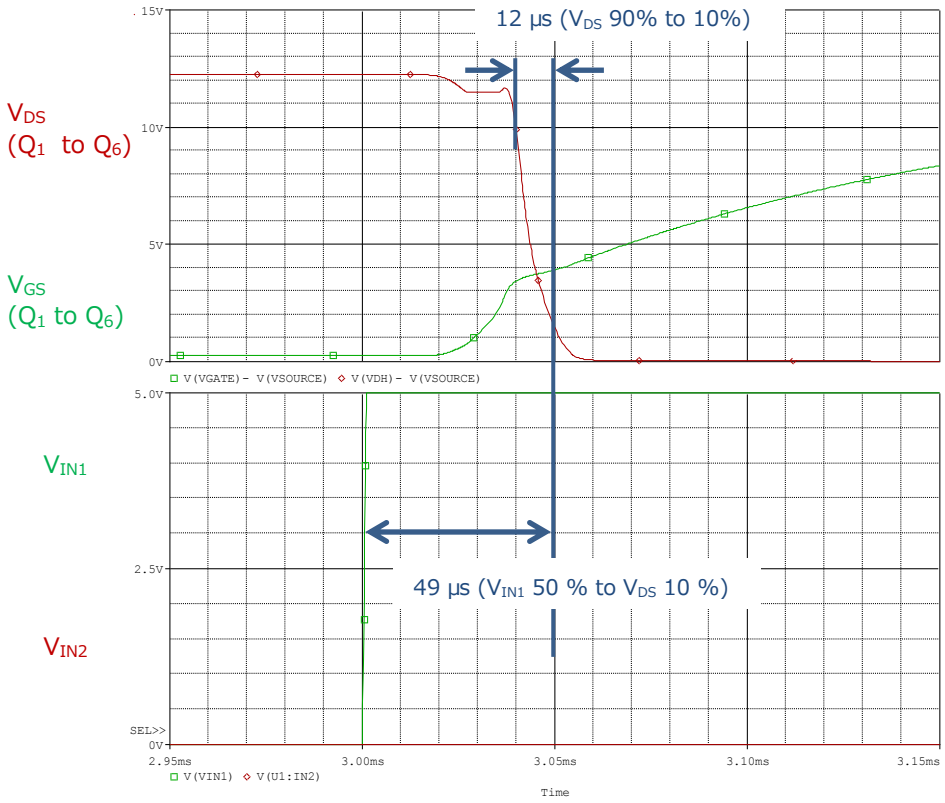

Fig. 4.3 Simulation Waveform (Turn-On)

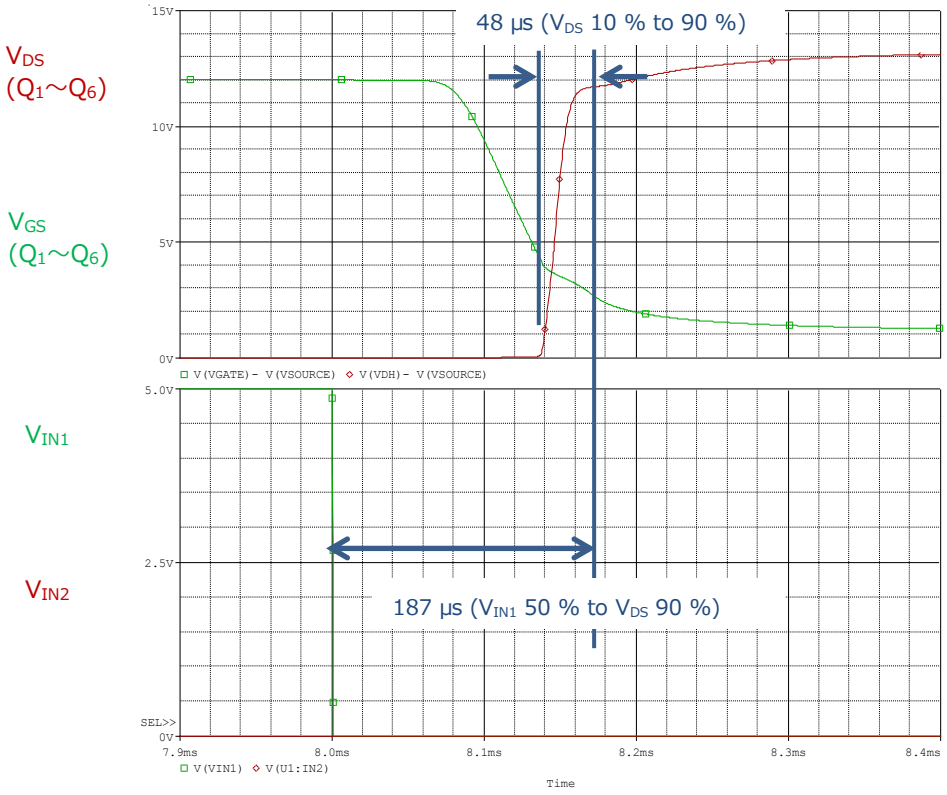

Fig. 4.4 Simulation Waveform (Turn-Off)

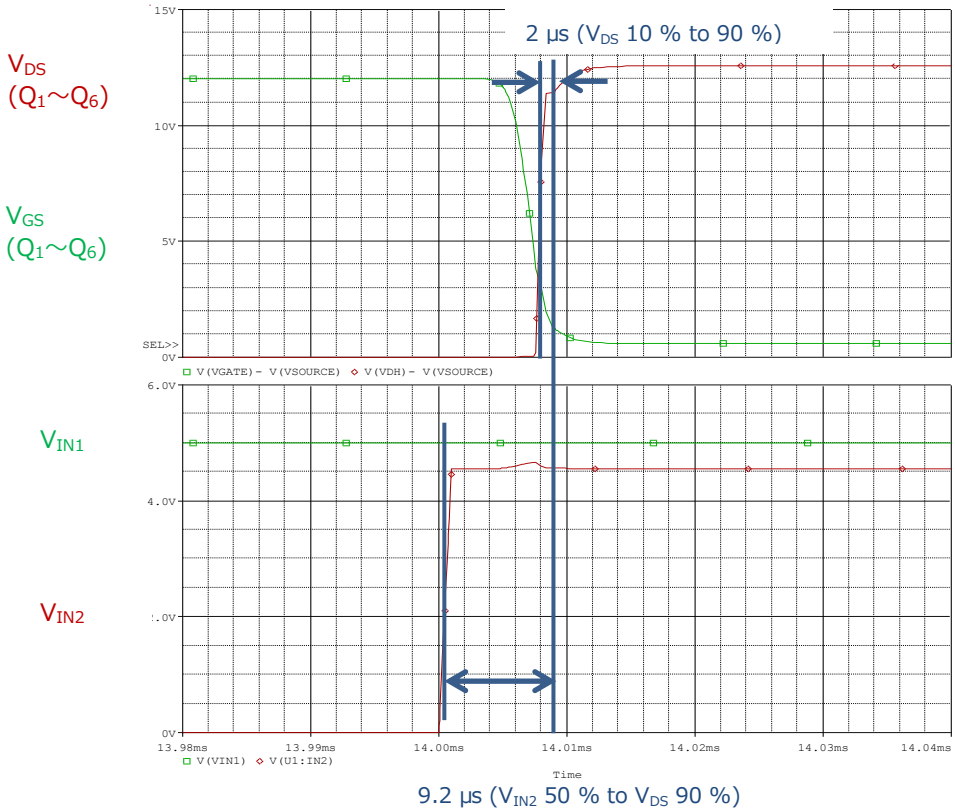

Fig. 4.5 Simulation Waveform (Quick Off)

4.3 Operation with the Power Supply Reverse Connection

The power supply reverse connection assumes reverse connection of the car battery.

The purpose of this application is to cut off the current generated when the power supply is connected in reverse. By using TPD7106F, MOSFET can be kept off and the current can be suppressed.

4.3.1 Simulation Verification

Check the operation of the power supply reverse connection by simulation. Fig. 4.6 shows the simulation circuit. Simulation is performed under the conditions and procedures in Table 4.3.

Table 4.3 Simulation Conditions and Procedures

1	V2	12 V
2	V_{DD5}	5 V
3	V_{IN1}	0 V
4	V_{IN2}	0 V
5	V_{STBY}	0 V
6	Start of simulation	
7	V2	12 V to -18 V (10 ms)

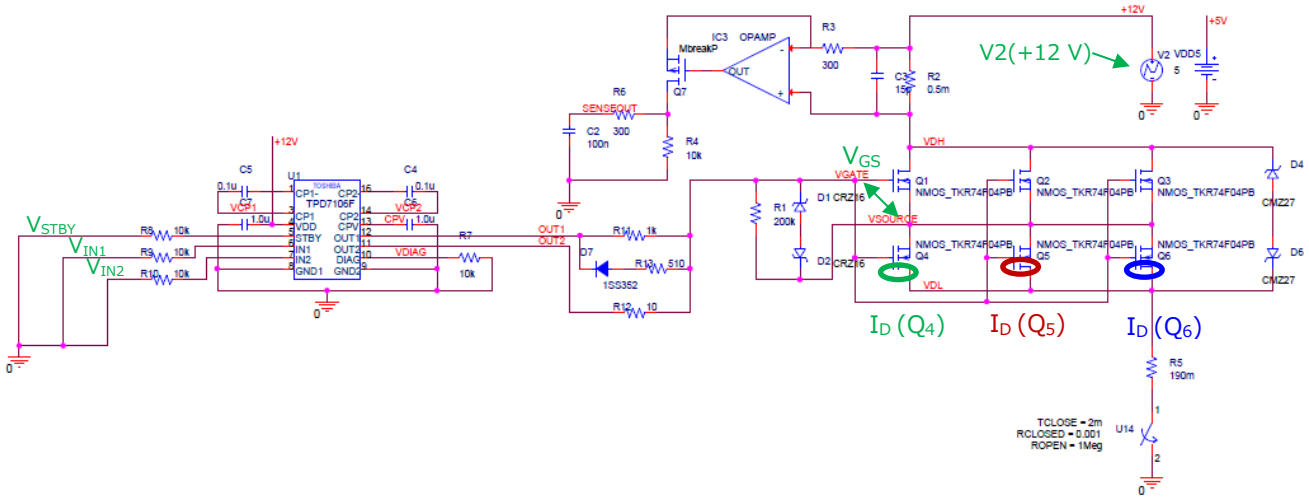

Fig. 4.6 Simulation Circuit (Power Supply Reverse Connection)

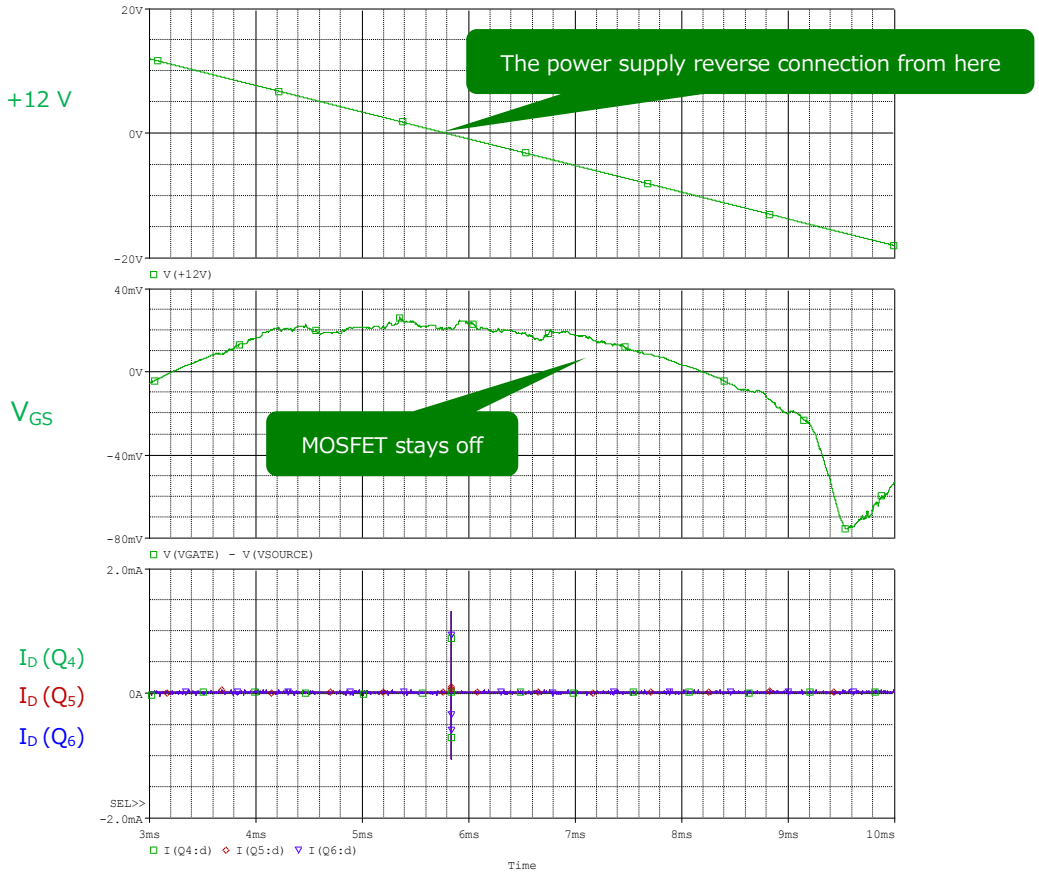

Fig. 4.7 Simulation Waveform (Power Supply Reverse Connection)

Fig. 4.7 shows the simulation waveform. A DC voltage source of +12 V is swept from 12 V to -18 V. The power supply reverse connection state is equivalent to the power supply voltage being at a negative potential. MOSFETQ_1 to Q_6 remains off as shown in V_{GS} waveform. Normally, a semiconductor device has a parasitic body diode. When the polarity of the power supply is reversed, current is generated from the GND. However, TPD7106F has a built-in switch that suppresses the current from the GND. When the power supply becomes negative, the switch is turned off. Therefore, the current output from OUT1, OUT2 pin are suppressed, and the external MOSFET can be kept off.

4.4 Charge Pump Capacitor Selection

Commonly used as non-isolated high-side gate drivers are the bootstrap method or the charge pump method. The bootstrap method requires periodic recharging of the bootstrapped capacitor, so operation close to 100 % duty is not possible. Therefore, the bootstrap method cannot be used for systems requiring high-duty operation, such as systems with low input voltages and high loads.

TPD7106F uses a charge pump system, so it can also be used in systems requiring high duty or DC energization. The current required for the charge pump circuitry can be obtained from V_{DD} terminal voltage, power supply voltage, and drive frequency of TPD7106F. Table 4.4 lists the conditions required for the charge pump circuit.

Table 4.4 Requirements for Charge Pump Circuits

MOSFET	TKR74F04PBx6
V_{DD} terminal voltage of TPD7106F	12 V
Power supply voltage	12 V
Drive Frequency (F_{sw})	100 Hz

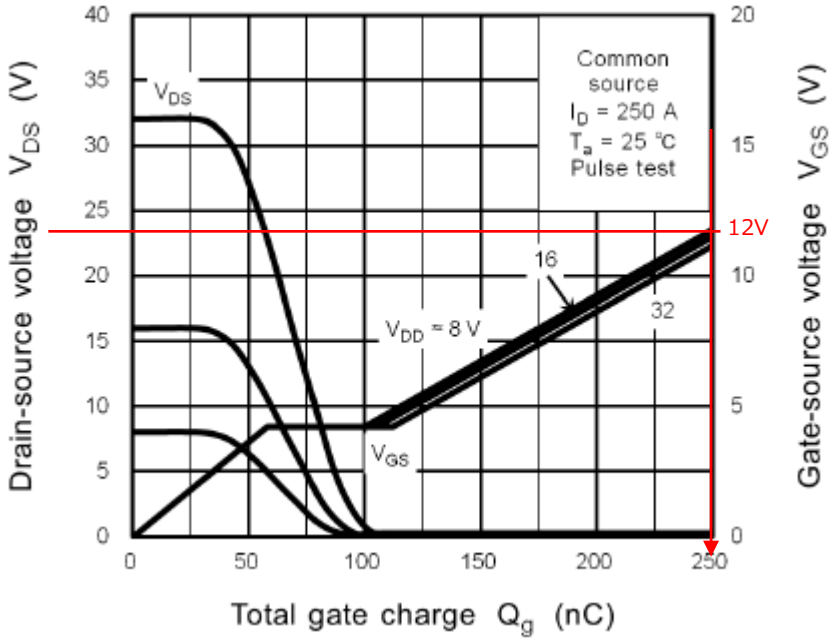

Fig. 4.8 TKR74F04PB Dynamic Input/Output Characteristics

MOSFET charge is approximately 250 nC from V_{DD} pin voltage condition (12 V) and gate-source voltage (12 V) shown in TPD7106F in Table 4.2, as shown in Fig. 4.8. Six MOSFET are connected. In this circuit, MOSFET is driven at the maximum. drive frequency (F_{sw}) = 100 Hz. Therefore, the output current of the charge pump circuit is calculated as follows.

$$I_{average} = Q_g \times F_{SW} = 1500\ (nC) \times 100\ (Hz) = 150\ (\mu A)$$

Considering the effects of the pull-down resistor of 200 kΩ and the internal impedance of the IC, it is necessary to ensure that the output current has a sufficient margin. Capacitor values can be easily estimated using the simulation shown in Fig. 4.9.

4.4.1 Simulation Verification

Verify by simulation to confirm charge pump capacitor selection. Fig. 4.9 shows the simulation circuit. Simulation conditions and procedures in Table 4.5 are used for the execution.

Table 4.5 Simulation Conditions and Procedures

1	V_{DD12}	12 V
2	V_{DD5}	5 V
3	V_{IN1}	0 V
4	V_{IN2}	0 V
5	V_{STBY}	5 V
6	Start of simulation	
7	I1	0 to 100 mA (1ms step.)
8	Monitoring V_{CPV} Voltage	

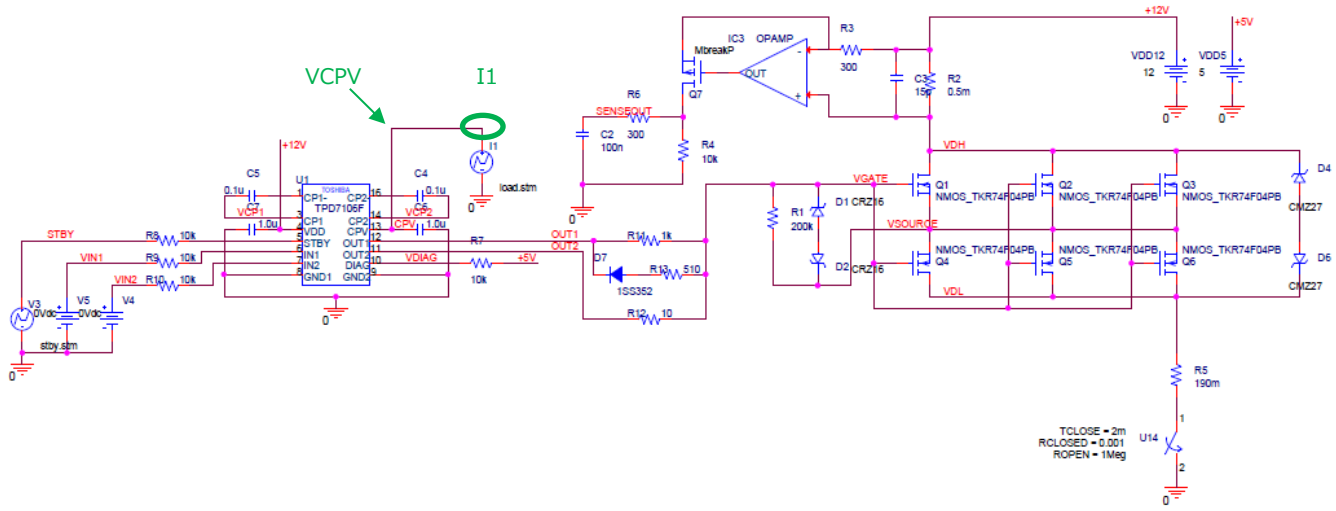

Fig. 4.9 Simulation Circuit (Charge Pump Capacitor Selection)

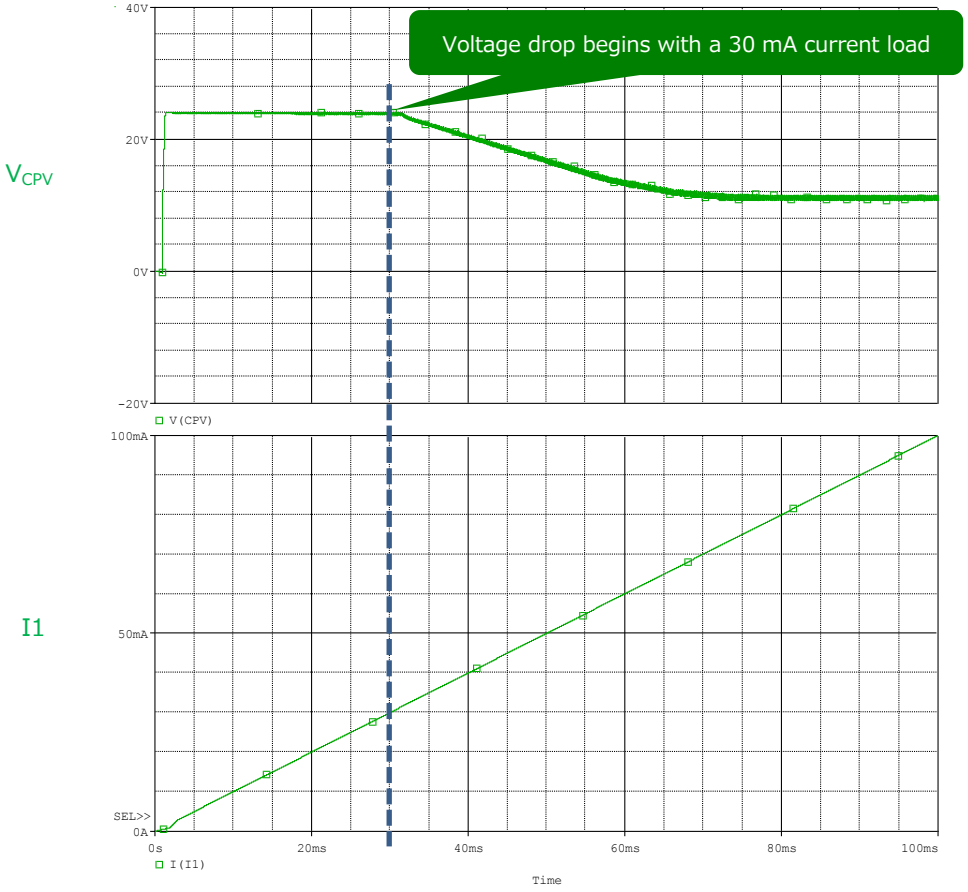

Fig. 4.10 Simulation Waveform (Charge Pump Capacitor Selection)

Fig. 4.11 shows the simulation results. Depending on the nature of MOSFET, V_{GS} typically requires at least 10 V. Therefore, the area where the CPV pin voltage is 22 V or less becomes an unstable area with bias application. The results also show that the output characteristics vary depending on the charge pump capacities C4 and C5. It is possible to estimate the selectable capacitor value from this result.

However, environmental temperatures, power supply voltage conditions, and characteristics of peripheral components such as diodes will also affect the product. Therefore, we recommend that you conduct actual measurements. 0.1 μF is selected for this circuit in consideration of sufficient margin for design. In addition, the capacitors in the charge pump circuitry of TPD7106F are supplied with voltages typically 12 V higher than V_{DD}, so care must be taken in withstanding voltage of the capacitors. In this circuit, the voltage at the VDH pin is boosted to 24 V for V_{DD} = 12 V. Therefore, a 50 V withstanding voltage product is selected.

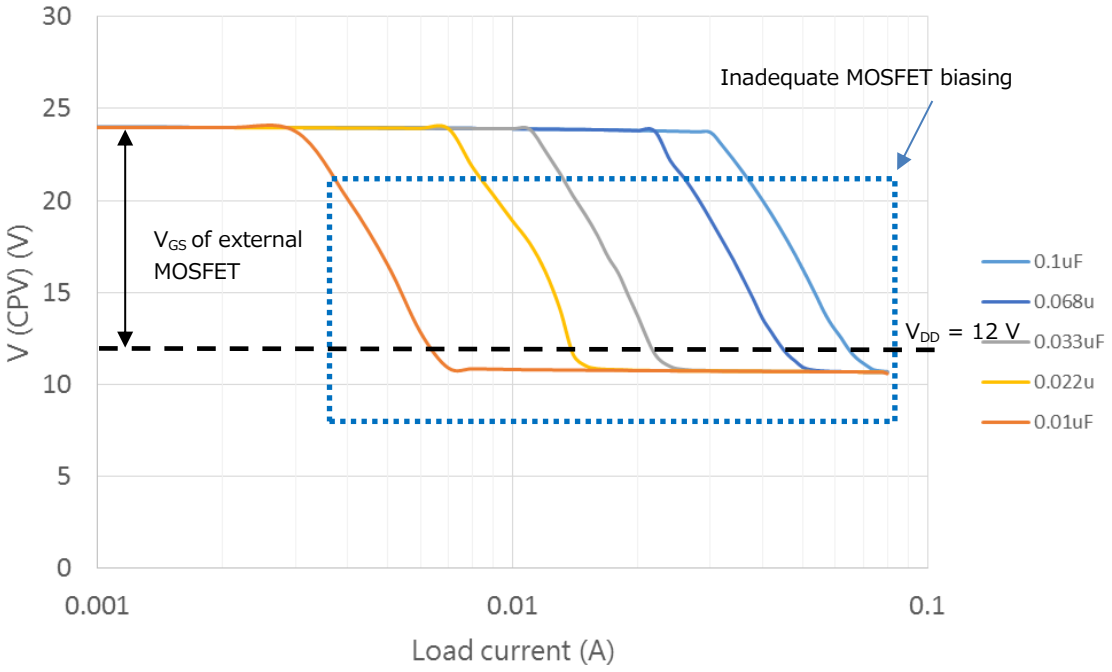

Fig. 4.11 Simulation Results (Charge Pump Capacitor Dependent)

4.5 Charge Pump Voltage Drop Detection

This product monitors the CPV terminal voltage and detects the charge pump voltage drop. DIAG pin enters the L state when the charge pump drops below the threshold voltage V_{CPL} (V_{DD}+4.7 V typical). The output pin OUT1,OUT2 maintains operation. Note that when STBY is set to the L state, the charge pump circuit is stopped because the unit enters the standby mode.

4.5.1 Simulation Verification

Verify by simulation to check charge pump voltage drop detection. Fig. 4.12 shows the simulation circuit. Simulation is performed under the conditions and procedures in Table 4.6.

Table 4.6 Simulation Conditions and Procedures

1	V_{DD12}	12 V
2	V_{DD5}	5 V
3	V_{IN1}	0 V
4	V_{IN2}	0 V
5	V_{STBY}	0 V
6	Start of simulation	
7	V_{STBY}	0 to 5 V (1 ms)
8	V_{IN1}	0 to 5 V (2 ms)
9	I1	0 to 200 mA (2 ms to 5 ms)
10	I1	200 mA to 0 (5 ms to 8 ms)

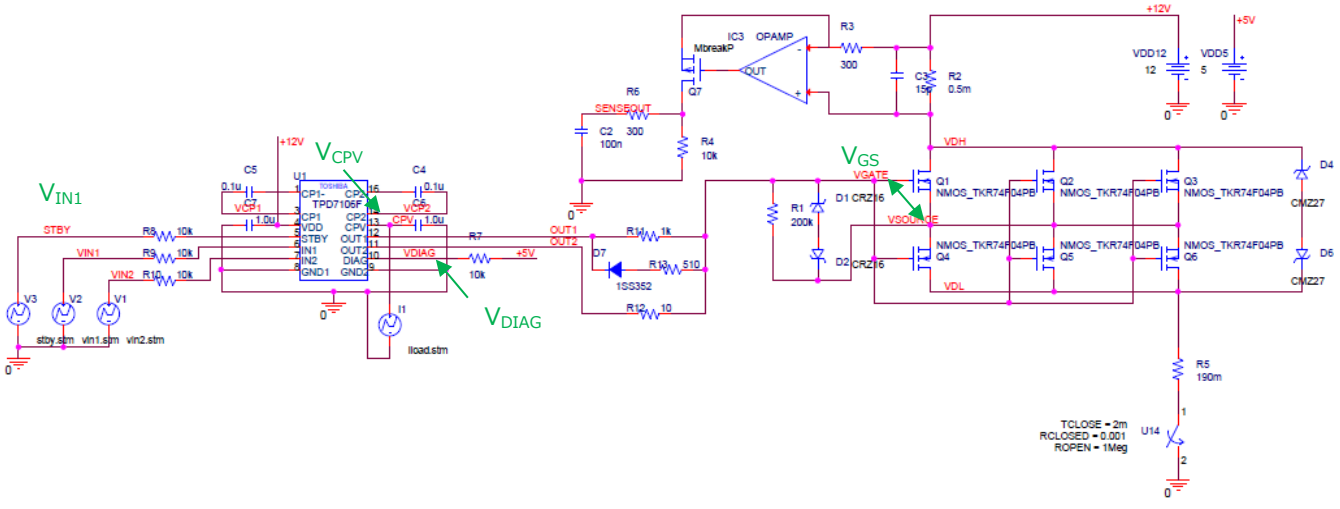

Fig. 4.12 Simulation Circuit (Charge Pump Voltage Drop Detection)

The charge pump voltage V_{CPV} is reduced by increasing the load current from the normal operating condition. If the charge pump voltage returns to normal without stopping the output, it can be confirmed that the diagnostic output also returns to the normal state.

The power control must be operated with IN1, IN2.

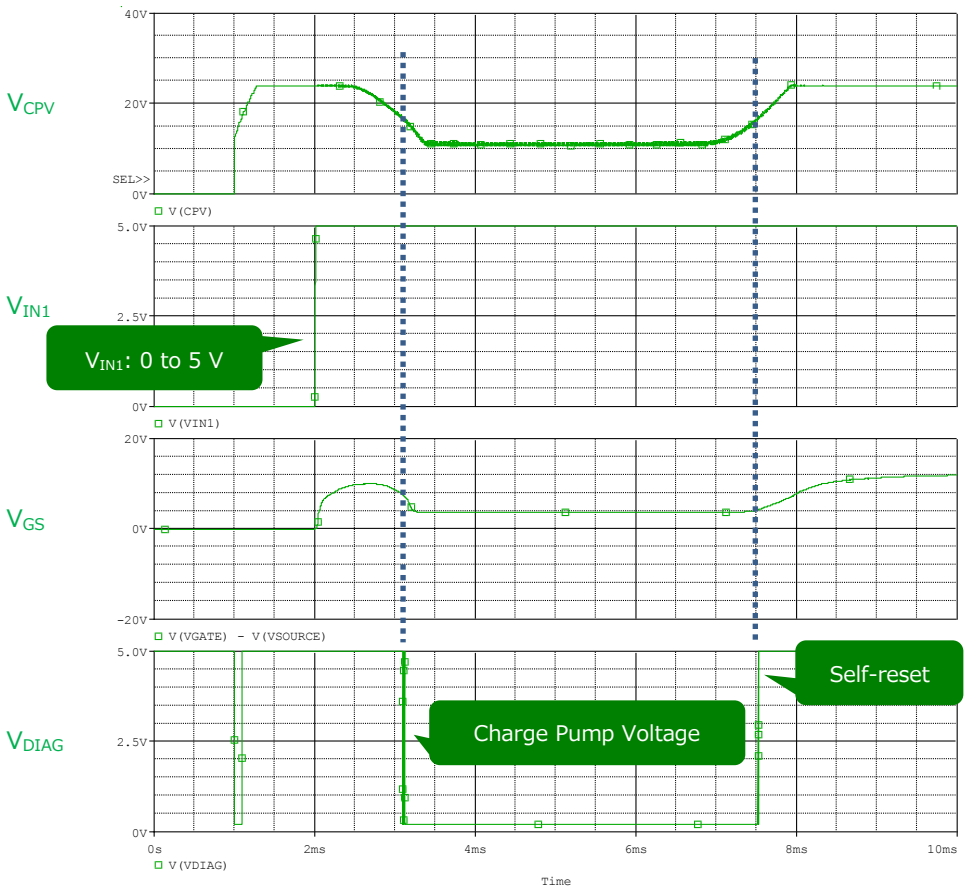

Fig. 4.13 Simulation Waveform (Charge Pump Voltage Drop Detection)

5. Product Overview

5.1 TPD7106F

5.1.1 Overview

TPD7016F is an N-channel power MOSFET gate driver for 1-channel high-side switches. A built-in charge pump circuit makes it easy to configure high-side switches for high-current applications.

- AEC-Q100 qualified products for automotive applications
- Output current of-10 mA/+400 mA allows gate-driving with parallel use of N-channel power MOSFET
- Built-in power supply reverse connection protection function
- Built-in charge pump circuit
- Small surface mount SSOP16 packaging

5.1.1 Appearance and Pin Assignment

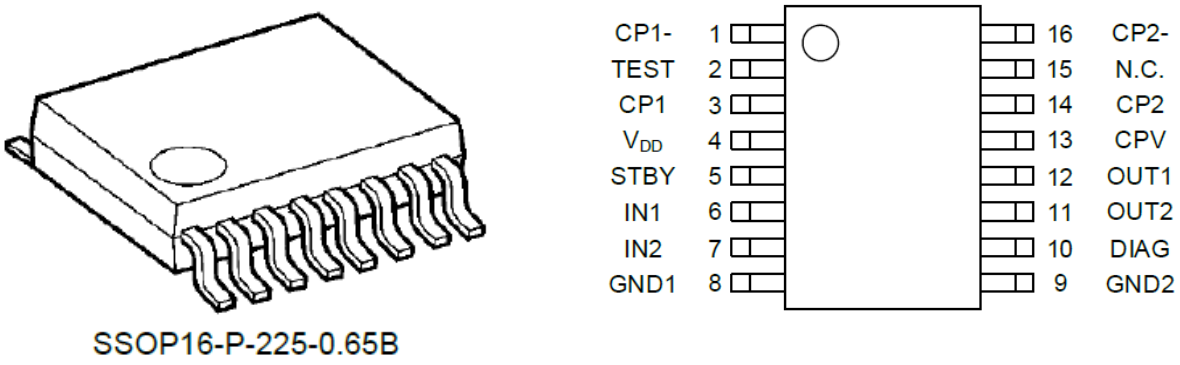

Fig. 5.1.2 Appearance and Pin Assignment 5.1.1

5.2 TKR74F04PB

5.2.1 Overview

TKR74F04PB uses our latest low-voltage MOSFET processing U-MOSIX-H to achieve low on-resistance and high current ratings.

- AEC-Q101 qualified products for automotive applications
- Low on-resistance: $R_{DS\ (ON)}$ = 0.6 mΩ (Typ.) (V_{GS} = 10 V)
- Low Leakage Current: I_{DSS} = 10 μA (Max.) (V_{DS} = 40 V)
- Easy-to-handle enhancement type: V_{th} = 2.0 to 3.0 V (V_{DS} = 10 V, I_D = 1 mA)
- Maximum current rating :I_D = 250 A (DC)
- Maximum voltage rating: V_{DSS} = 40 V
- Small TO-220SM (W) Packaging

5.2.2 Appearance and Pin Assignment

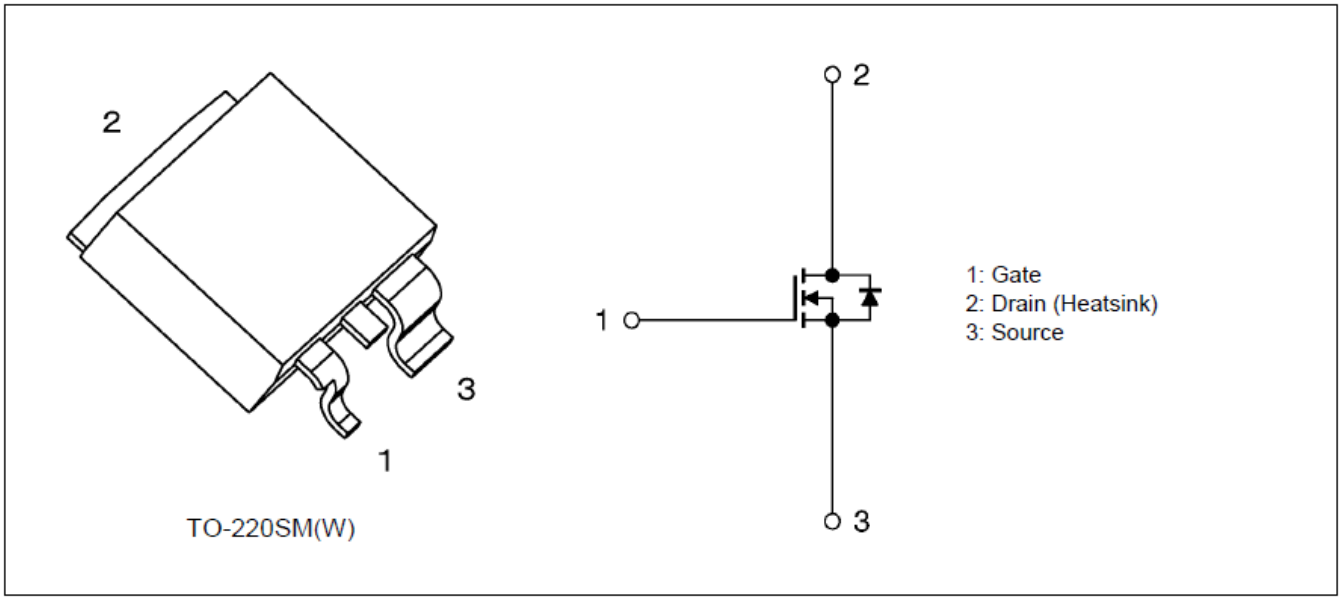

Fig. 5.2 Appearance and Pin Assignment

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