1.6 kW 48 V Output Telecommunication Equipment Power Supply

Design Guide

RD171-DGUIDE-01

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

Contents

1. Introduction

This Design Guide describes the circuit design and the layout of the 1.6 kW 48 V output telecommunication equipment power supply (this power supply). Refer to the Reference Guide for the specifications, operation, and performance of this power supply.

Components marked “Not Mounted” in the BOM are not used in this power supply even if component designators are shown in the circuit diagram. They are intended as reserved spaces for components necessary to modify circuit constants when designing an actual circuit.

1.1. Power MOSFET Used

Toshiba has the 600/650 V DTMOS series, which is suitable for the primary side (PFC/main switch) of AC-DC converters, and the low-voltage U-MOS series, which is suitable for the secondary side (synchronous rectifier and ORing). Both series offer an extensive lineup, allowing you to select the most suitable product according to the design specifications. The following is an introduction to the products used in this power supply.

TK25N60X

In the semi-bridgeless PFC circuit

V_{DSS} = 600 V, $R_{DS(ON)}$@V_{GS} = 10 V (max) = 125 mΩ, TO-247 package

DTMOSIV process: high-speed switching and reduced switching loss

TK25N60X5

In the primary side of the phase shift full-bridge (PSFB) circuit

V_{DSS} = 600 V, $R_{DS(ON)}$@V_{GS} = 10 V (max) = 140 mΩ, TO-247 package

DTMOSIV process with built-in high-speed diode: reduced loss during reverse recovery operation

TPH2900ENH

In the synchronous rectification circuit on the secondary side of the PSFB circuit

V_{DSS} = 200 V, $R_{DS(ON)}$@V_{GS} = 10 V (max) = 29 mΩ, SOP Advance package

U-MOSⅧ-H process: suitable for switching applications, reduced synchronous rectification loss

TPH2R408QM

In the output ORing circuit

V_{DSS} = 80 V, $R_{DS(ON)}$@V_{GS} = 10 V (max) = 2.43 mΩ, SOP Advance package

U-MOSX-H process: low on-resistance to reduce power dissipation in ORing circuit

2. Circuit Design

This section describes the points of circuit design of this power supply.

2.1. AC Line Circuit Design

Fig. 2.1 shows the AC line circuit and explains the basic design method.

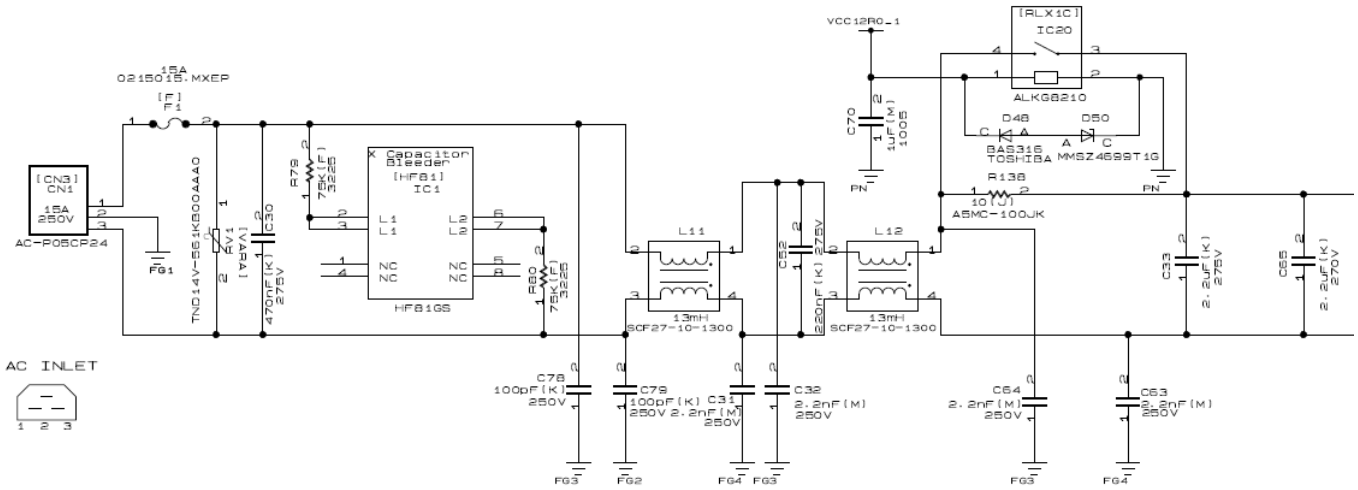

Fig. 2.1 AC Line Circuit

Fuse

A fuse (F1) is used to shut off the AC line when an excessive current flows through the AC line. Select a fuse from the maximum AC line current value. Using the maximum power, $Pout_{max}$, power supply efficiency, η, power factor, PF, and AC line voltage value, $VinAC_{min}$, calculate the maximum AC line current, $ACin_{peakrms}$ with the following equation.

$$ACin_{peakrms} = \frac{Pout_{max}}{\eta \times PF \times VinAC_{min}}$$

This power supply is designed for 1.6 kW output when the input is AC 200 V system and 800 W output when it is AC 100 V system. If the power supply efficiency of the PFC does not change depending on the input voltage, the maximum value of the AC line input current will be the same regardless of the input voltage. However, in general, the power supply efficiency of PFC is low when the input voltage is low. Therefore, when calculating the maximum current value of the AC line, the input voltage is assumed to be 90 V, which is the minimum value of the 100 V system.

Assuming that the AC input voltage (minimum) = 90 V, the maximum power = 800 W, the power supply efficiency = 93 %, and the power factor = 0.99, the maximum AC-line current value of this power supply is approximately 10 A. Select a 15A fuse with margins to this power supply. When selecting a fuse, it is necessary to consider the inrush current when the AC power is turned on, whether the product has obtained the safety standards to be complied with, etc., in addition to the above maximum current.

Varistor

A ceramic varistor (RV1) is installed to protect the circuitry when surge voltages due to lightning strike are applied to the AC line. Select a varistor using the voltage value of the AC line. Since the maximum AC line voltage of this power supply is 264 V and the maximum instantaneous voltage value is 373 V, a varistor with a maximum allowable circuit voltage of 350V (AC rms value) and a varistor voltage of 560V is used in addition to the margin.

Select the product considering not only the maximum allowable circuit voltage and varistor voltage, but also the surge current withstand capability and energy withstand capability. In addition, since a failure mode of varistor is short mode generally, insert a fuse to the front stage (input side of the AC line) of the varistor.

IC for the discharging of the X capacitors

After the AC input is disconnected, the charge stored in the X capacitor (C30, C33, C52, C65) must be discharged quickly to avoid the risk of electric shock hazard. In this power supply, a HF81 is mounted as an IC for discharging X capacitors. This IC realizes power saving of the system because the discharge path is cut off when AC power is supplied. The circuit consisting of this IC and external resistors (R79, R80) can discharge the charge stored in the X capacitors so that the voltage of the X capacitors are 37 % or less of the initial value within 1 second after the AC power supply is lost. This power supply contains tow external resistors (75 kΩ) necessary to discharge 5 μF capacitance, because the capacitance of the X capacitors totals approximately 5 μF. Note that when changing the X capacitor for noise suppression, etc., it may be necessary to change the external resistance value connected to this IC. It is also possible to change this IC to a discharge resistor for cost reduction. However, in this case, power loss due to the resistance for continuous discharge will occur when AC connection is made, so it is necessary to confirm whether the power saving requirements of the system are satisfied.

EMI countermeasure parts

Y capacitor (C31, C32, C78, C79, C63, C64) and common mode choke (L11, L12) are used as common mode noise suppression. X capacitors (C30, C33, C52, C65) are implemented as a countermeasure against differential noise. The noise level is affected by the board layout and enclosure design. Change, remove or add the above parts as necessary. Note that increasing the capacitance of the Y capacitor increases the leakage current, so it is necessary to confirm whether the system satisfies the required safety standards.

Inrush current countermeasures

A resistor with a built-in fuse (R138) and a relay (IC20) are mounted to suppress inrush current when the AC power is turned on. When this power supply is started in the correct procedure, the relay circuit is turned off when the AC power is turned on, and the current flows through the fuse built-in resistor (10 Ω), so inrush current can be suppressed. The relay circuit is designed to detect and turn on the primary 12 V power supply that is generated for operation/control of this power supply after the AC power is turned on. After the relay circuit is turned on, power loss during

operation can be reduced because current flows through relays with lower resistance. The conditions and timing for turning the relay on and off must be checked to see if the required specifications of the system are satisfied.

Primary 12V power supply, secondary 12V power supply

In this power supply, the primary 12V power supply and the secondary 12V power supply are generated by the flyback converter for operation/control. Depending on the requirements of the system, it is necessary to design a flyback converter that can supply the required current capacity when driving a cooling FAN.

2.2. Power Factor Correction (PFC) Circuit Design

This power supply employs a semi-bridgeless PFC circuit configuration using a controller UCC28070A (PFC controller) manufactured by Texas Instruments to make the PFC circuit highly efficient. The following describes the basic design items of the semi-bridgeless PFC circuit for this power supply. For detailed designs around the controller, refer to the datasheet and related documents of PFC controller. Fig. 2.2 shows the circuit around the controller, and Fig. 2.3 shows the circuit around the power MOSFET and inductor.

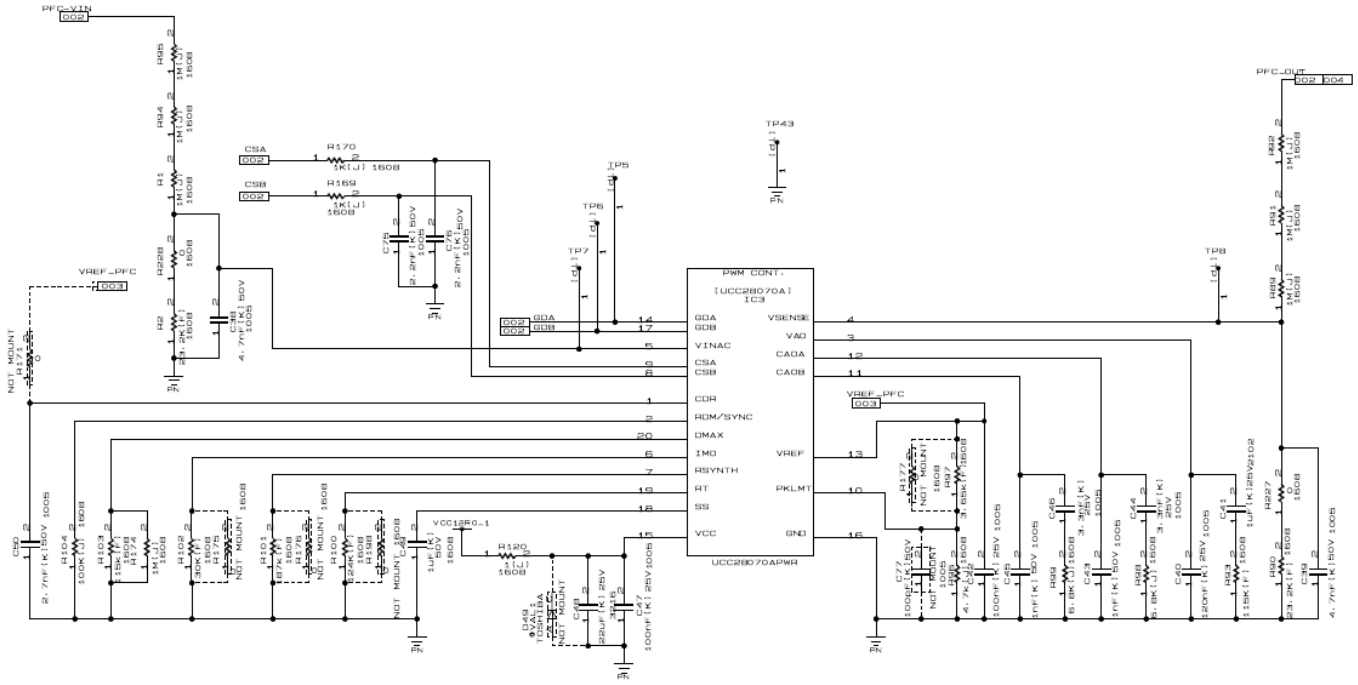

Fig. 2.2 PFC Circuit 1 (Around the Controller)

Output voltage

The output-voltage PFC_OUT of the PFC circuitry can be set by external resistors (R89, R90, R91, R92, R227). The output voltage is controlled by comparing the output pin sense voltage, VSENSE, divided by the above resistor with the internal referenced voltage (3.0 V) of the PFC controller. The output voltage setting value is calculated by the following equatio.

$$PFC\_OUT(V) = \frac{3.0 \times (R89+R91+R92+R90+R227)}{(R90+R227)}$$

When changing the output voltage of the PFC circuit, the resistor (R1, R2, R94, R95, R228) for measuring the AC-line voltage must also be changed to the same value. The initial setting for the PFC circuit output voltage is approximately 391V with R90 = R2 = 23.2 kΩ, R227 = R228 = 0 Ω, R1 = R89 = R91 = R92 = R94 = R95 = 1 MΩ. Change the above resistor values as necessary and set them to the desired output voltage value.

Switching frequency

The switching frequency of the PFC circuit, f_{PWM}, can be set by the external resistor R100. The switching frequency is calculated by the following equation.

$$f_{PWM}(kHz) = \frac{7500}{R100(k\Omega)}$$

The default switching frequency is approximately 60 kHz with R100 = 124 kΩ. Change the resistor value of R100 as required and set it to the desired frequency.

Soft start

The soft-start time of the PFC circuit can be set by the external capacitor C49. The setting value is calculated by the following equation.

$$T_{SS}(s) = C49 \times \frac{2.25(V)}{10(\mu A)}$$

The default soft start time is approximately 225 ms with C49 = 1 μF. Change the capacitance value of C49 as necessary and set it to the desired soft start time. It must be confirmed that the current limiter does not operate during the soft-start period and that the output voltage recovers to the normal range when restarting after the hold-up period.

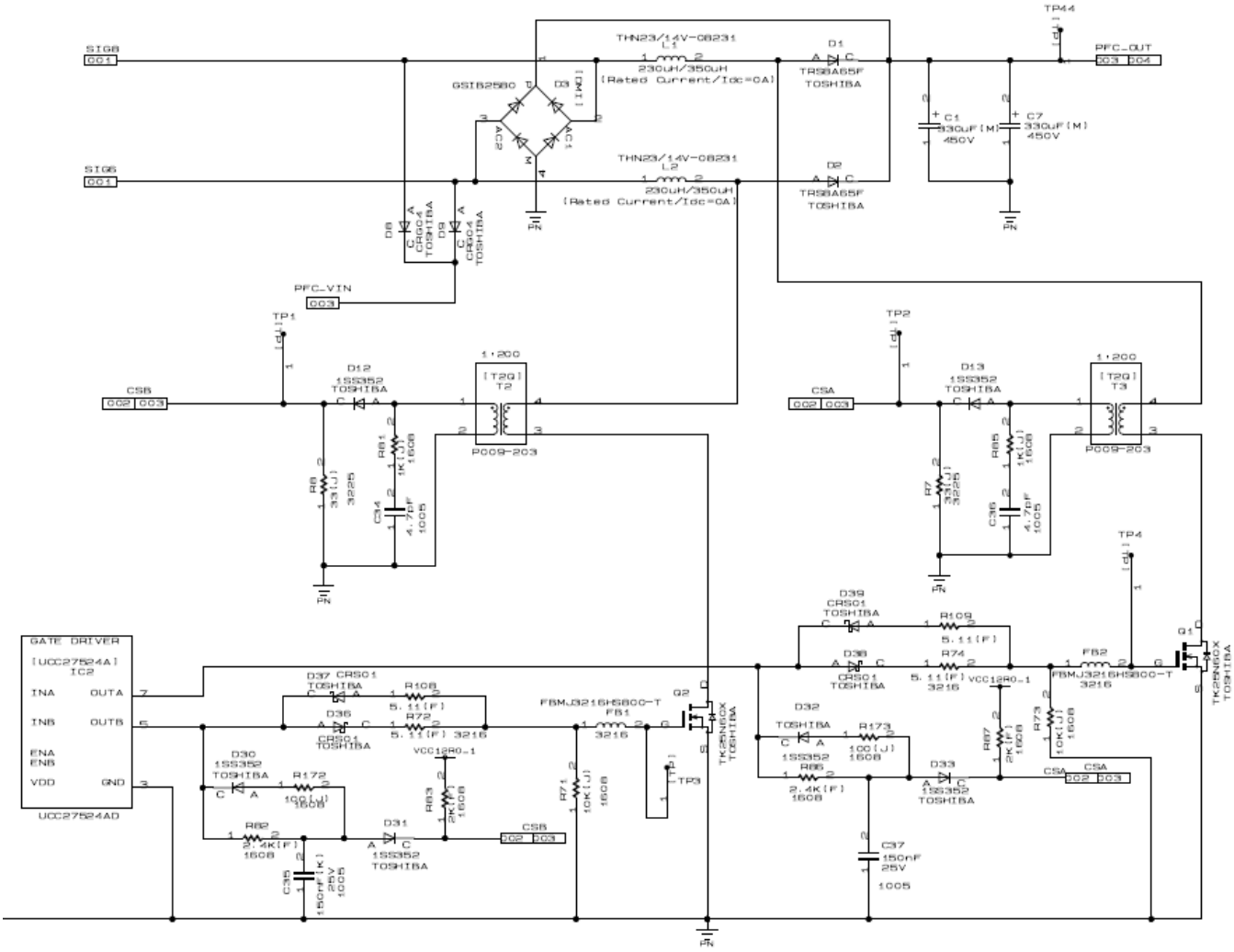

Fig. 2.3 PFC Circuit 2 (Around the Power MOSFET, Diode Bridge, and Inductor)

Current limiter

The current limiter of the PFC circuit can be set by the current transformer (T2, T3), current detection resistor (R7, R8), and threshold setting resistor (R96, R97). When the current reaches the threshold, the PFC controller turns Disable the gate-drive signals (GDA, GDB). The current limit level is calculated by the following equation.

$$I_{limit} = \frac{Vs \times Nct}{Rs}$$

Current limit threshold voltage: Vs, current transformer winding ratio: Nct = 200, PFC controller reference voltage: Vref = 6.0 V

$$Vs = \frac{R96}{R96 + R97} \times Vref$$

The default setting for the current limit level is 20.47 A.
On the other hand, the maximum current value flowing through the switching element of the PFC circuit is calculated by the following equation.

$$Ipeak = \left(\frac{POUT \times \sqrt{2}}{efficiency, \eta 1(\%) \times VinAC} + \frac{\Delta I}{2} \right) \times margin$$

When VinAC = 90 V, the maximum current flowing through the switching elements is 18.74 A assuming that POUT = 800W, PFC conversion efficiency η1 = 93 %, ΔI = 4.2 A, and margin = 1.2. Change the above values as necessary to set the desired current value.

Gate drive circuit

The design of the gate drive circuit affects power supply efficiency and EMI noise. Generally, power supply efficiency and EMI noise have a trade-off relationship, so it is necessary to design both in a balanced manner. If you need to reduce EMI noise, we recommend that you change the gate-series resistors (R72, R74, R108, R109) to a larger value to check for noise. The gate drive circuit of this power supply has a circuit configuration in which the turn-on speed and turn-off speed of the MOSFET can be individually adjusted. If the prior check shows that the noise source is occurring during the MOSFET turn-on or turn-off period, no change is required for all resistors. EMI noise may be reduced by changing R72 and R74 if noise at turn-on is a problem, or by changing R108 and R109 if noise at turn-off is a problem. Note that changing the gate series resistor to a large value reduces the switching speed of the MOSFET, so deterioration of the power supply efficiency becomes a concern. When changing the gate series resistor, it is necessary to confirm that the required power efficiency performance and heat dissipation performance of the system are satisfied. Also, if EMI noise suppression is possible with either turn-on or turn-off adjustment only, it may be possible to reduce the adverse effects on the power efficiency of the system compared to countermeasures that delay both.

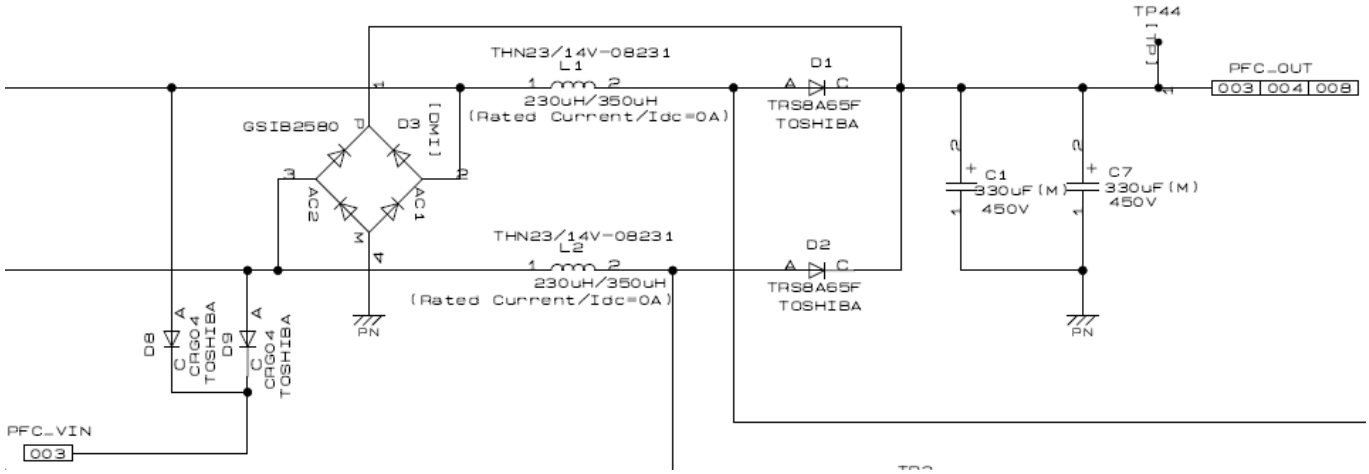

Fig. 2.4 PFC Circuit 3 (Around the Diode Bridge and Inductor)

Fig. 2.4 shows the circuits around the diode bridge and inductor.

Diode bridge

A bridge diode (D3) is used for the rectifier diode. Since this power supply has a semi-bridgeless PFC circuit configuration, the diode between 2-pin and 1-pin and the diode between 3-pin and 1-pin contribute only to rectifying operation when the power supply is started, and does not contribute to further operation. It is also possible to change this bridge diode (D3) to a half-bridge diode and a surface mount type diode. When using a surface mount type diode, you must select a product with a rating that can support inrush current.

Output Capacitor

The capacitance values of the output capacitors (C1, C7) are calculated based on the hold-up time requirements. The hold-up time Thold is calculated by the following equation, assuming that the capacitance of the output capacitor is Cout, the output voltage is Vout_PFC, the lower limit voltage of the output voltage is Vmin, and the maximum output power is Pout.

$$Thold = Cout \times \frac{(Vout\_PFC^2 - Vmin^2)}{2 \times Pout/\eta 2}$$

The default setting of hold-up time is 8.76ms with Cout = 660 μF, Vout_PFC = 390 V, Vmin = 328.42V, Pout = 1600 W, the power conversion efficiency of the PSFB, η2, = 96 %. Adjust the capacitance of the output capacitor to satisfy the hold-up time required for the system. In addition, when the output ripple specification is requested, the capacitance required to satisfy the output ripple specification should be calculated and compared with the capacitance that satisfies the hold-up time, and a large capacitance value should be used. In addition, tolerances and aging degradation must be considered when selecting a capacitor.

Inductor

The inductor (L1, L2) is selected by setting the ripple current ΔI of the inductor to 30 % of the peak input current value (ACin_peak) of the AC line. Assuming that the input voltage is VinAC, the

PFC output voltage is Vout_PFC, the switching frequency is F, the power conversion efficiency of the PFC is η1, and the power conversion efficiency of PSFB at the subsequent stage is η2, the inductor value can be calculated as follows.

$$ACin\_peak = \frac{(Pout/\eta 2) \times \sqrt{2}}{VinAC \times \eta 1}$$

$$\Delta I = ACin\_peak \times 30\%$$

$$L = \sqrt{2} \times VinAC \times \frac{(Vout\_PFC - VinAC)}{Vout\_PFC \times \Delta I \times F}$$

This power supply uses 350 μH because L = 386 μH if VinAC = 90 V, Vout_PFC = 390 V, F = 60 kHz, Pout = 800 W, η1 = 93 %, and η2 = 96 %.

Also, the peak current IL_peak flowing through the inductor can be calculated as follows.

$$IL\_peak = ACin\_peak + \frac{\Delta I}{2}$$

Since ACin_peak is 14.08 A and ΔI = 4.22 A, IL_peak = 16.19 A. Therefore, select an inductor that can flow more than 16.19 A.

2.3. Phase-Shift Full-Bridge (PSFB) Circuit Design

This power supply generates 48 V output after the semi-bridgeless PFC circuit. The controller UCC28950 (PSFB controller) manufactured by Texas Instruments, which enables Zero Volt Switching (ZVS) operation over a wide range of loads, is used to improve power supply efficiency. The following describes basic designs for PSFB circuitry of this power supply. For detailed designs around the controller, refer to the datasheet and related documents of PSFB controller. Fig. 2.5 shows the circuit around the controller.

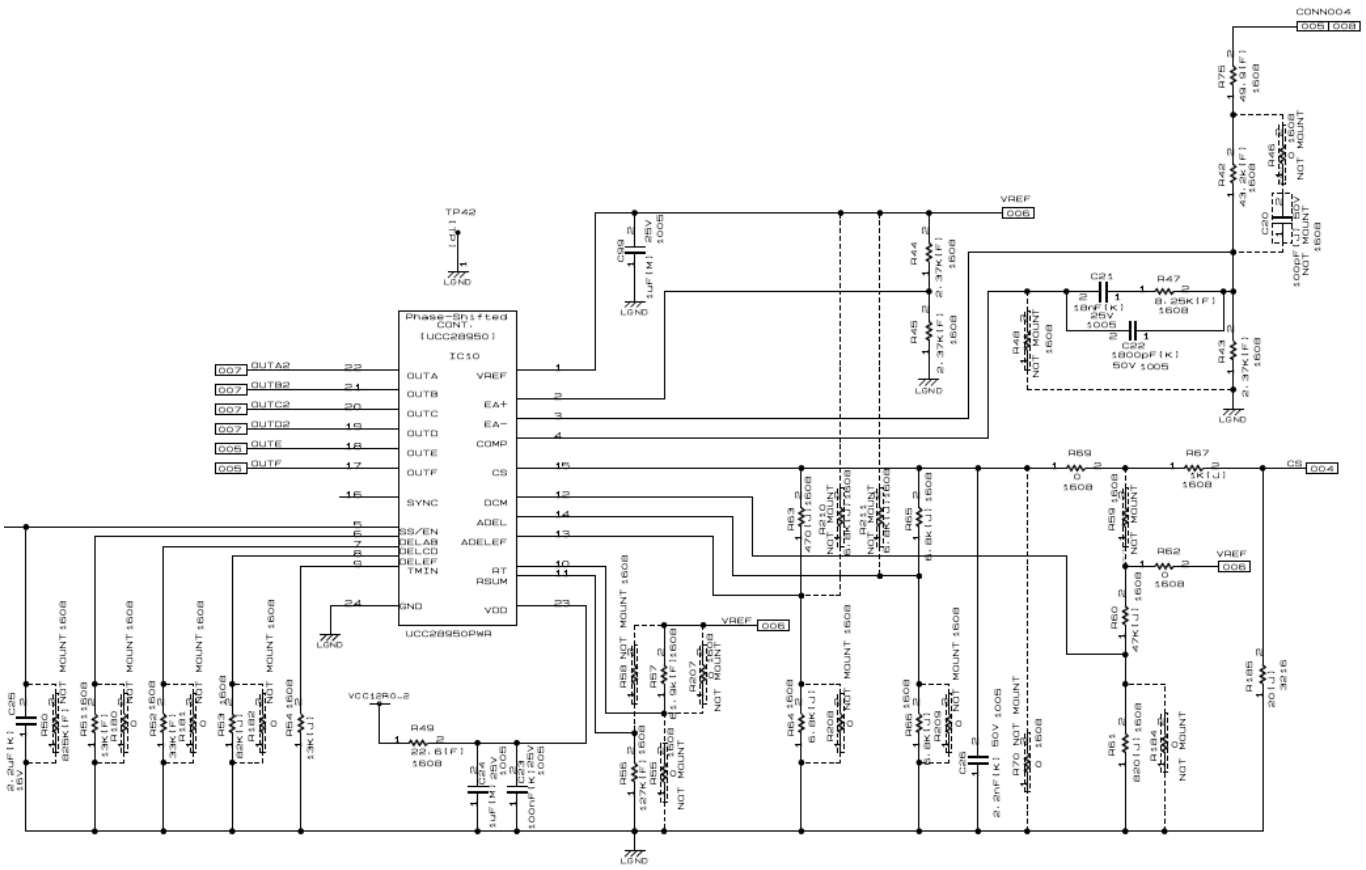

Fig. 2.5 PSFB Circuit 1 (Around the PSFB Controller)

Output voltage

The output-voltage of PSFB circuit, VOUT, can be set by external resistors (R42, R43, R44, R45, R75). The set value is calculated by the above resistors and the internal voltage for voltage setting (VREF=5.0 V) of the PFC controller using the following equation.

$$VOUT(V) = \frac{VREF(V) \times R45 \times (R43 + R42 + R75)}{(R44 + R45) \times R43}$$

The default setting is 48.12V with R42 = 43.2 kΩ, R43 = R44 = R45 = 2.37kΩ, and R75 = 49.9 Ω. Change the above resistor values as necessary and set them to the desired output voltage value.

Switching frequency

The switching-frequency of PSFB circuit, f_{PWM}, can be set by the external resistor R57. The switching frequency is calculated by the following equation.

$$f_{PWM}(kHz) = \frac{2.5 \times 10^3}{\left(\frac{R57(k\Omega)}{VREF(V) - 2.5} + 1\right)}$$

The default switching frequency is 97.05 kHz with R57 = 61.9kΩ. Change the above resistance value as necessary and set it to the desired frequency.

Soft start

The soft-start duration of PSFB circuit can be set by an external capacitor C25. The setting value can be calculated by the following equation.

$$T_{SS}(s) = \frac{C25(\mu F) \times \left(\frac{VREF(V) \times R45}{R44 + R45} + 0.55\right)}{25}$$

The default soft start time is 268.4ms with C25 = 2.2 μ. Change the capacitance value of C25 as necessary and set it to the desired soft start time. During the soft-start period, it must be checked that the current limiter does not operate.

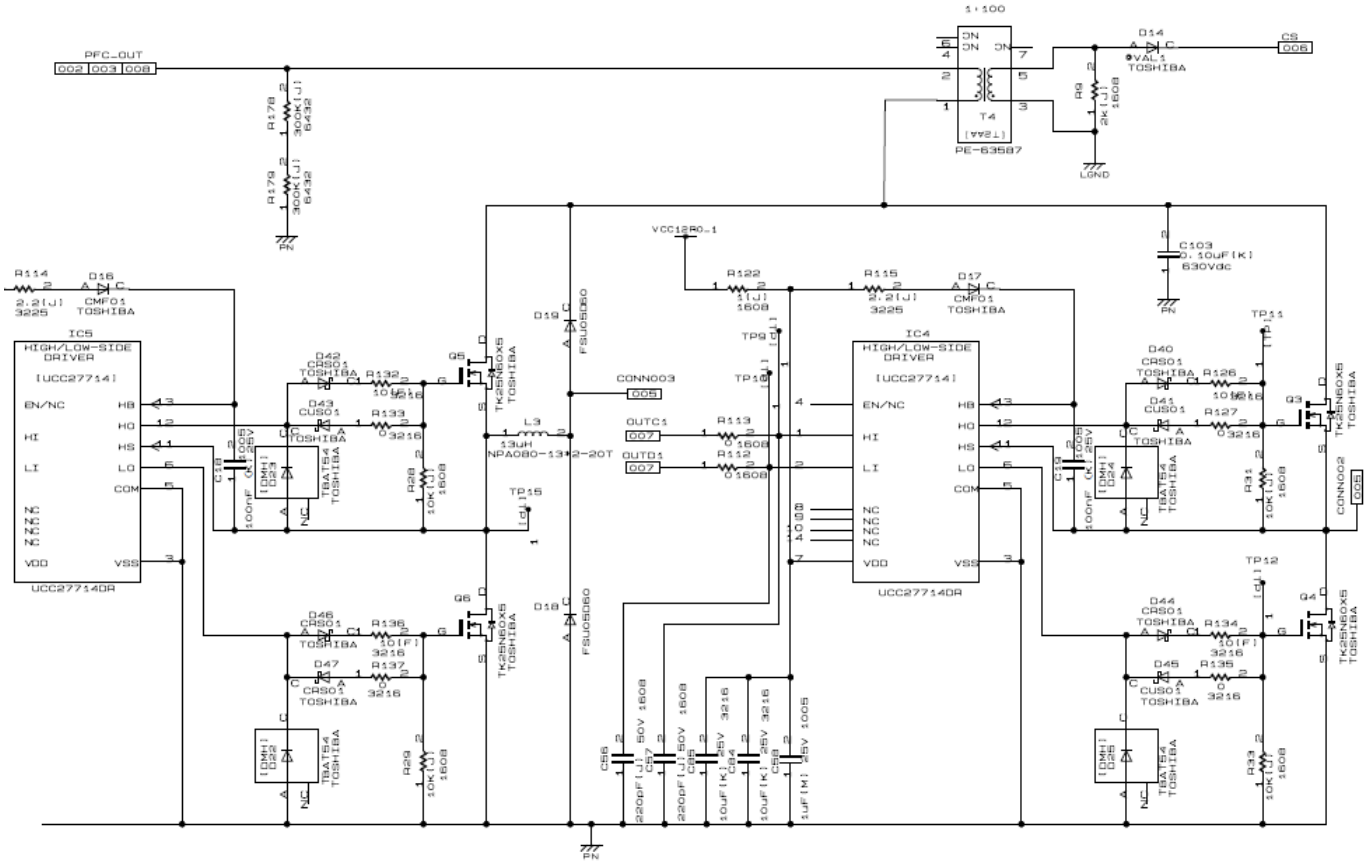

Fig. 2.6 PSFB Circuit 2 (Around the Primary-Side MOSFET)

Fig. 2.6 shows the circuit around the primary-side MOSFET.

Current limiter

The current limiter of PSFB circuit can be set by the current transformer (T4), current sense resistor (R185), and current limit threshold (2 V). When the current reaches the threshold, The PSFB controller limits the MOSFET drive for MOSFET control on the primary side to prevent abnormal current from flowing to the secondary side. The current limit level is calculated by the following equation.

$$I\_limit = \frac{2.0}{R185 \times transfomer\ \ turns\ \ ratio}$$

The default setting of the current limiter is 10A because R185 = 20 Ω and the number of turns is 100:1. Change the above values as necessary to set the desired current value.

Gate drive circuit

The design of the gate drive circuit affects power supply efficiency and EMI noise. Generally, power supply efficiency and EMI noise have a trade-off relationship, so it is necessary to design both in a balanced manner. Although PSFB has implemented Zero Volt Switching (ZVS), if there is a hard switching area and it is the source of EMI-noise, we recommend that you change the gate series resistors (R126, R127, R132 - R137) of the corresponding MOSFET (Q3 - Q5) to a large value for checking. If only one of these adjustments is available, the system's power supply

efficiency may be reduced because the circuit configuration is independently adjustable during turn-on and turn-off as with the gate drive circuit of the PFC.

Transformer

When On Duty of the synchronous rectifier is set to 85 % in the steady-state condition of PSFB circuit, a square wave of approximately 56 V is required on the secondary side because the output voltage is 48V. Since the PFC output voltage of this power supply is 390V, the turn ratio of the transformer (T5, T6) is selected to be 26:4:4 (center tap method). Thus, a square wave of 60V is generated in the output rectifier section on the secondary side. In addition, primary-secondary dielectric strength, winding temperature rise, magnetic flux saturation, core loss, etc. must be sufficiently considered. Please refer to the BOM for the specifications of the transformer used in this power supply. Note that the secondary synchronous rectifier MOSFET generates a square wave equivalent to two secondary windings, resulting in a 120V square wave that is twice as large as the secondary output rectifier. This power supply selects MOSFET of 200V withstand voltage for secondary-side synchronous rectification in view of derating.

In this power supply, Zero Volt Switching (ZVS) is performed using the leakage inductance of the transformer. If the resonance due to the leakage inductance is insufficient, ZVS cannot be realized, and problems such as a drop in power supply efficiency and an increase in EMI noise may occur. When changing the transformer, it is necessary to confirm that the ZVS is used in a wide range of load areas. If the resonance becomes insufficient due to transformer change and ZVS is not performed, mount a coil (L3) for resonance and adjust so that ZVS is achieved over a wide load range. In the initial state of this power supply, in order to achieve ZVS, an additional resonant coil of 13 μH is connected to L3 in addition to the leakage inductance of the transformer.

Output Capacitor

The output capacitor must be checked to ensure that the output voltage ripple is within the required range of the system. The output voltage ripple, Vripple, is the combined waveform of the ripple current ΔI generated by switching, and the respective voltages generated by the ESR, capacitance (Cap), and ESL of the output capacitor. Assuming that the switching voltage is Vsw, the output voltage is Vout, and the switching frequency is F, the voltages generated by ESR, Cap, and ESL are calculated by the following equation.

$$Vripple\_ESR = \Delta I \times ESR$$

$$Vripple\_Cap = \frac{\Delta I}{8 \times Cout \times F \times 2}$$

$$Vripple\_ESL = \frac{Vsw \times ESL}{L}$$

Here,

$$\Delta I = \frac{(Vsw - Vout) \times Vout}{Vsw \times F \times 2 \times L} \times 2(phases)$$

If Vsw = 60 V, Vout = 48 V, F = 97.05 kHz, L = 27 μH, the secondary output of PSFB is twice the primary SW output frequency, and the ripple current value is doubled for safety because the switching frequency is doubled and the phase difference is 180 degree. Then ΔI = 3.66 A. When Cout = 330 μF × 6 pcs, ESR = 40 mΩ, ESL = 5 nH, L = 27 μH, the default values of the output ripple voltages generated by the elements are Vripple_ESR = 146 mV, Vripple_Cap = 1.2 mV, and Vripple_ESL = 11.1 mV.

Since the voltage generated by Cap is out of phase with the voltage generated by ESR and ESL, a simple sum is not possible originally, but because the voltage generated by Cap is small, a simple sum can be used as a guideline. Adjust the capacitance of the output capacitor to satisfy the ripple voltage required for the system. It is also necessary to confirm that the undershoot and overshoot generated in the output when the load changes suddenly are within the specified voltage range, and that the allowable ripple current of the capacitor of the output is ensured.

2.4. ORing Circuit Design

This power supply is equipped with ORing circuit at 48 V output so that it can respond to demands for N+1 redundant operation. ORing circuit consists of a Texas Instruments controller LM74700 (ORing controller) and an on/off MOSFET (Q15 - Q18). When the output voltage of this power supply is higher than the output voltage of other power supplies with the output of this power supply and other power supplies connected in parallel, the ORing controller turns on the on/off MOSFET to supply current to the output. If the output voltage of this power supply is lower than the output voltage of other power supplies, the ORing controller turns off the on/off MOSFET to prevent the current from flowing back from other power supplies to this power supply. The following describes basic designs for ORing circuit of this power supply. For detailed designs around the controller, refer to the datasheet and related documnts of the ORing controller. The type and quantity of the on/off MOSFET must be determined so that the power loss due to the voltage drop and on-resistance is within the allowable range of the system when the maximum load (33 A) is applied. This power supply is equipped with a TPH2R408QM of 4 pcs. Since the on-resistance of the FET rises at high temperatures, it is necessary to select a component that considers the environmental temperature supported by the system and the temperature rise of the MOSFET at the maximum load.

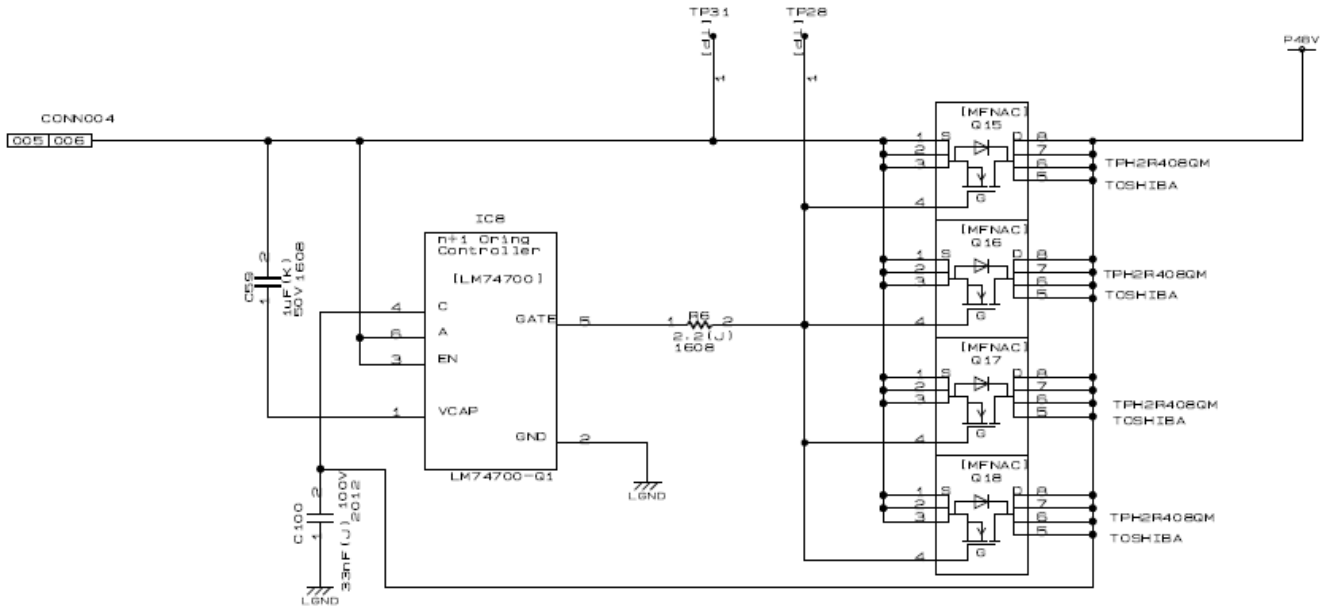

Fig. 2.7 ORing Circuit

3. PCB Design

This section describes considerations for designing the PCB of this power supply.

3.1. PCB Pattern Design

Creepage distance

Appropriate clearance and creepage distances must be ensured in accordance with the safety standards required for the system. This power supply ensures the following creepage distances. Since the required clearance and creepage distances vary depending on the environment in which the system is installed, the contamination of materials, humidity, altitude (atmospheric pressure), etc., sufficient consideration is required when setting the creepage distances.

Table 3.1 Design Minimum Creepage Distance

Line 1	Line 2	Creepage Distance Between Line 1 and Line 2
Primary side L	Primary side N	2.5 mm
PFC output	PN (primary side GND)	3.75 mm
All primary lines	FG	4 mm
Primary side (coupler)	Secondary side (coupler)	8.2 mm
Primary side (transformer section)	Secondary side (transformer section)	9 mm

Current capacity

Each pattern on the board must have a pattern width that does not cause any problems due to temperature rise or IR drop due to the pattern when the maximum current in each pattern is applied.

3.2. PFC Circuit Pattern Design

This section describes precautions for designing PCBs around PFC circuit. Please refer to the PFC controller datasheet and related documents for the layouts around the controller.

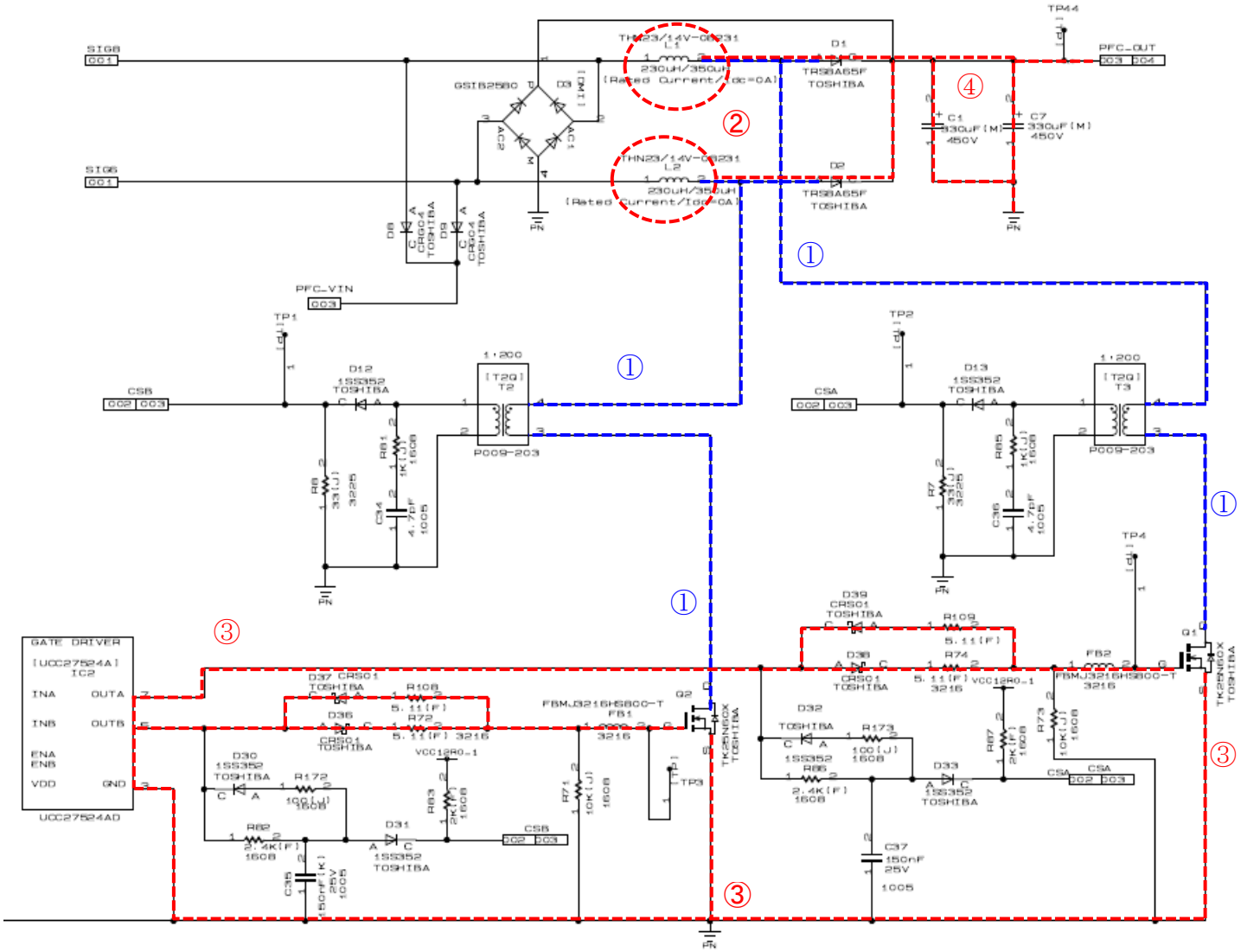

Fig. 3.1 PFC Circuit Pattern Design Considerations

1. Place the PFC controller (IC3) away from the following areas.

   Around the switching node: line between L1, Q1, and D1, line between L2, Q2, and D2 (① in the figure)

   Periphery of the PFC coil: within 2.5 cm from L1 and L2 (② in the figure)

   Driver output: IC2-Q1-GND (PN), IC2-Q2-GND looping (③ in the figure)

   PFC-output peripheral: L1-D1-C1/C7-GND (PN)-C33/C65, L2-D2-C1/C7-GND (PN)-C33/C65 loop (④ in the figure)

2. Arrange each component so that the area around the switching node with large voltage fluctuation (① in the figure) is as small as possible.

3. Keep the driver output line (③ in the figure) as short as possible. For this reason, IC2 and Q1, Q2 must be placed nearby. Also, ensure a pattern width that allows the driving current (maximum approximately 2 A) to flow.
4. When separating the drive current return path from the GND (PN) plain, separate it from the source terminal most recently in Q1 and Q2.
5. Place the boost diode (D1, D2) and the output capacitor (C1, C7) as close as possible.
6. The current detection lines (CSA and CSB) should be connected to GND (PN) in kelvin and fed back to IC3 through areas with low current fluctuations and voltage fluctuations.

The following is a layout diagram (Layer 1) of the power supply around the PFC circuits.

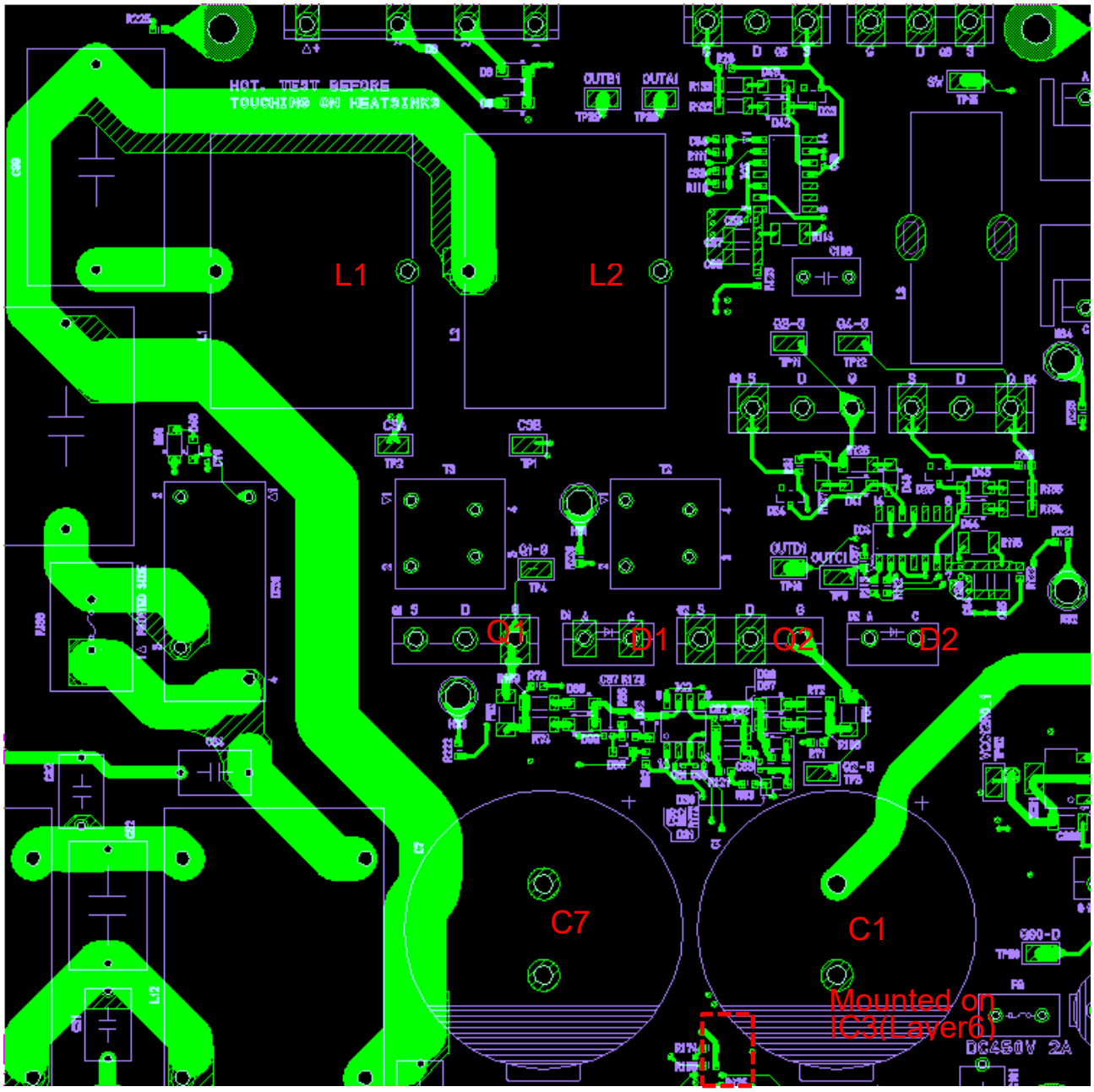

Fig. 3.2 PFC Circuit Pattern

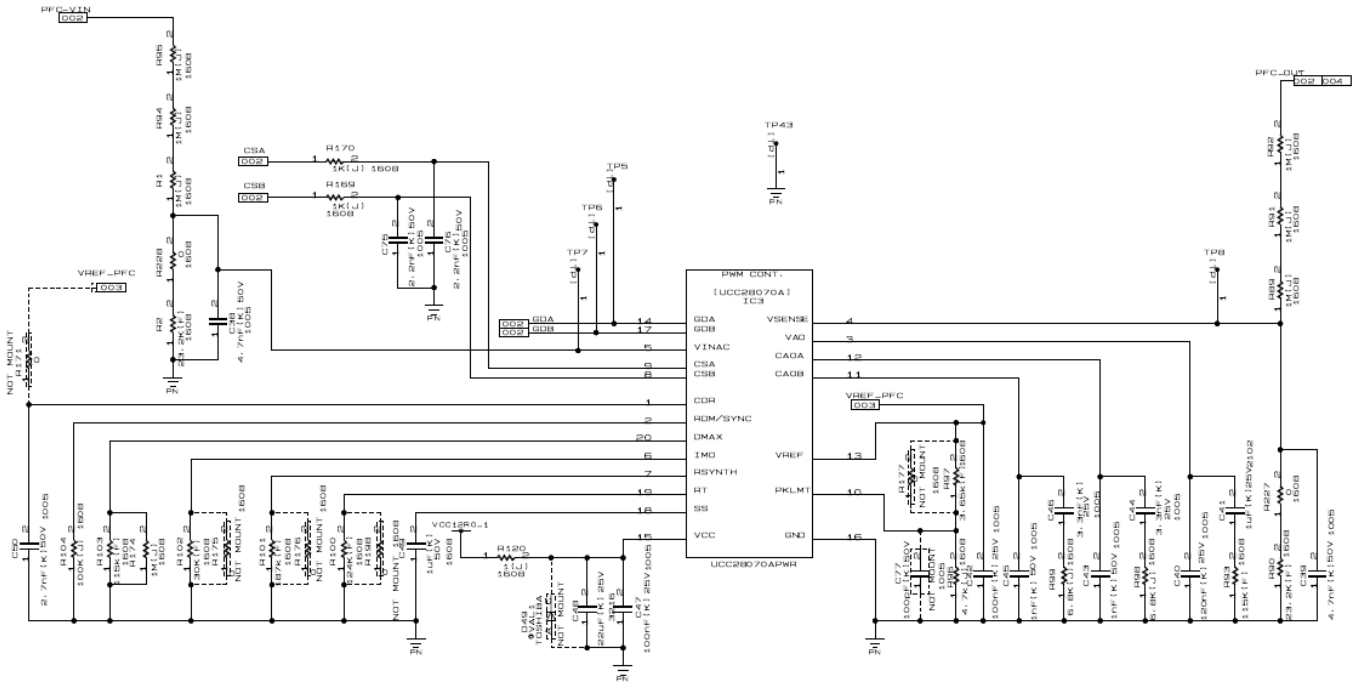

Fig. 3.3 PFC Circuit (Around the Controller)

1. All components listed in the above schematic should be mounted close to IC3.
2. Connect the GND (PN) to the GND pin of IC3 at one point. If all components can be placed close to IC3 and no switching current or driver current GND return paths exist near the components, they can also be connected to the GND (PN) plane in the immediate vicinity of the components.

3.3. PSFB Circuit Pattern Design

This section describes considerations for designing PCB around PSFB circuit. Please refer to the PSFB controller datasheet and related documents for the layout around the controller.

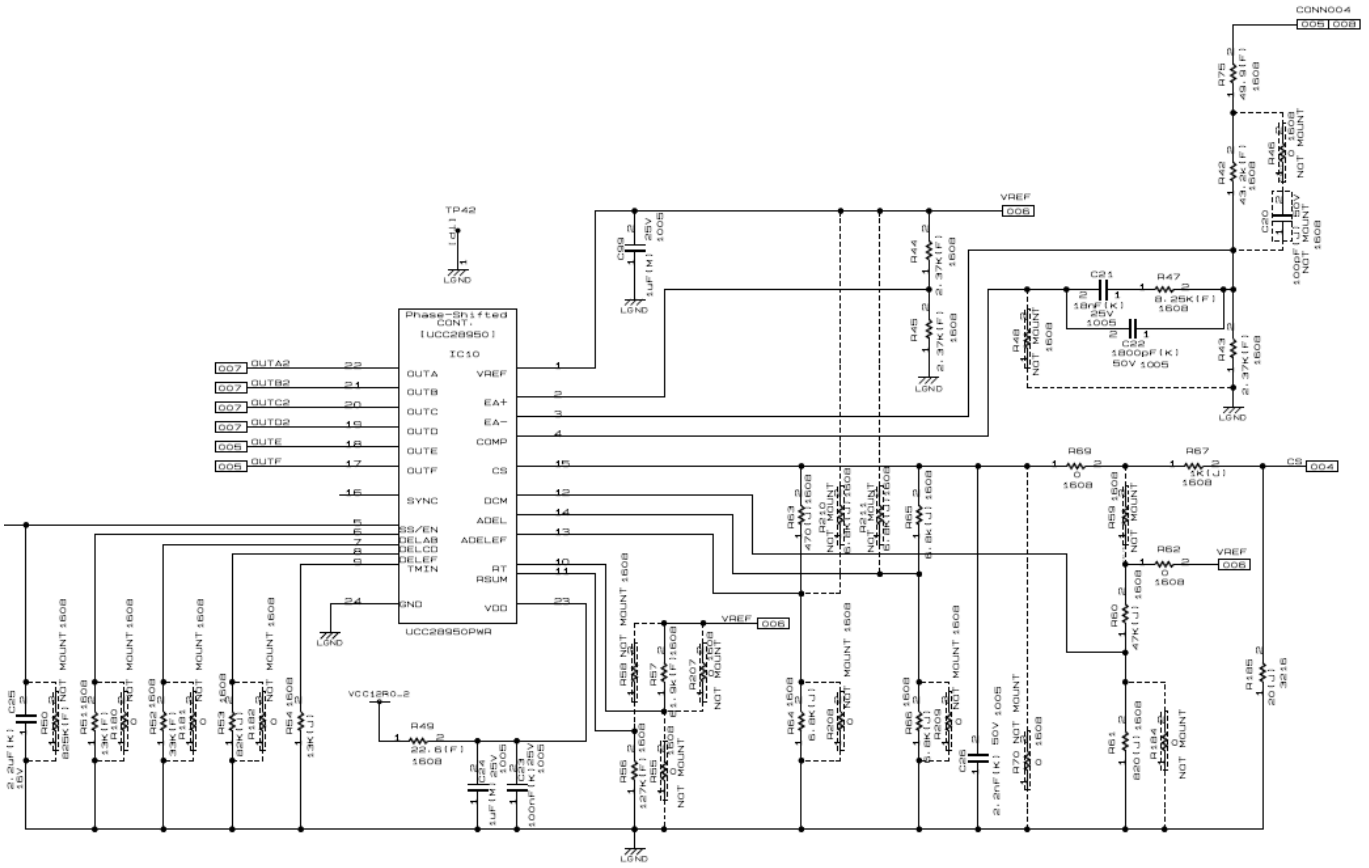

Fig. 3.4 PSFB Circuit (Around the Controller)

1. Place the PSFB controller (IC10) away from the secondary-side high-current switching circuit, transformers, and reactors.
2. All components listed in the above schematic should be mounted close to IC10.
3. Connect the GND (LGND in the circuit diagram) to the GND pin of IC10 at one point. If all components can be placed close to IC10 and no switching current or driver current GND return paths are present near the components, they can also be connected to the GND (LGND) plane in the immediate vicinity of the components.

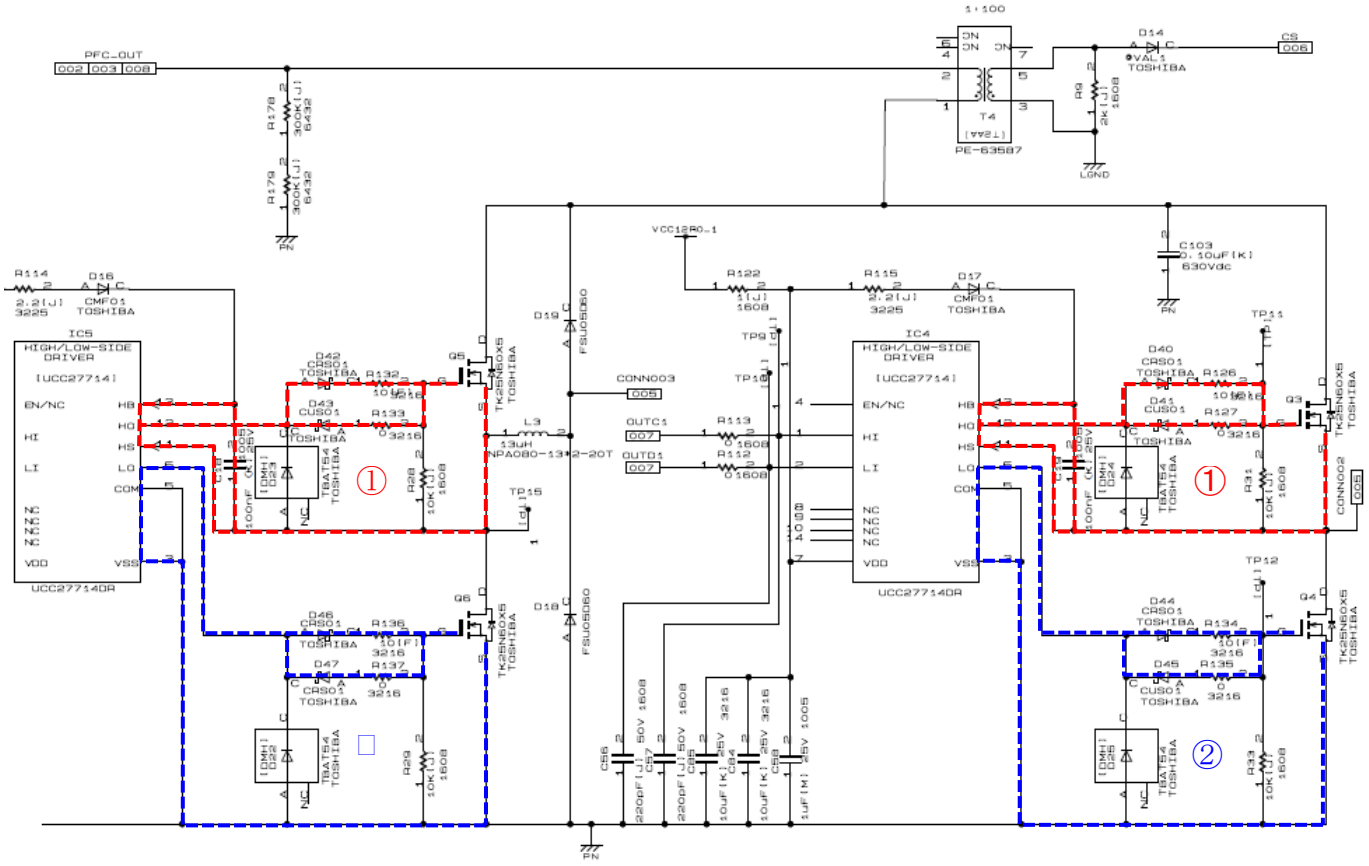

Fig. 3.5 Considerations on Designing PSFB Circuit Pattern 1

1. Arrange each component so that the area around the switching node with large voltage fluctuation (the line with the same potential fluctuation as ① and ① in the figure) is as small as possible.
2. Keep the driver output lines (① and ② in the figure) as short as possible. To do so, IC5 and Q5, Q6, and IC4 must be placed nearby Q3, Q4. Also, secure a pattern width that allows the driver output line to carry the maximum drive current.
3. Separate the return path of Q3 and Q5 drive currents from the nearest source pin.
4. When separating the return paths of the drive currents in Q4 and Q6 from the GND (PN) plane, separate them from the source terminals in Q4 and Q6 immediately.
5. The current detection line (CS) should be connected to the GND (LGND) in kelvin and fed back to IC10 through areas with little current fluctuation and voltage fluctuation.

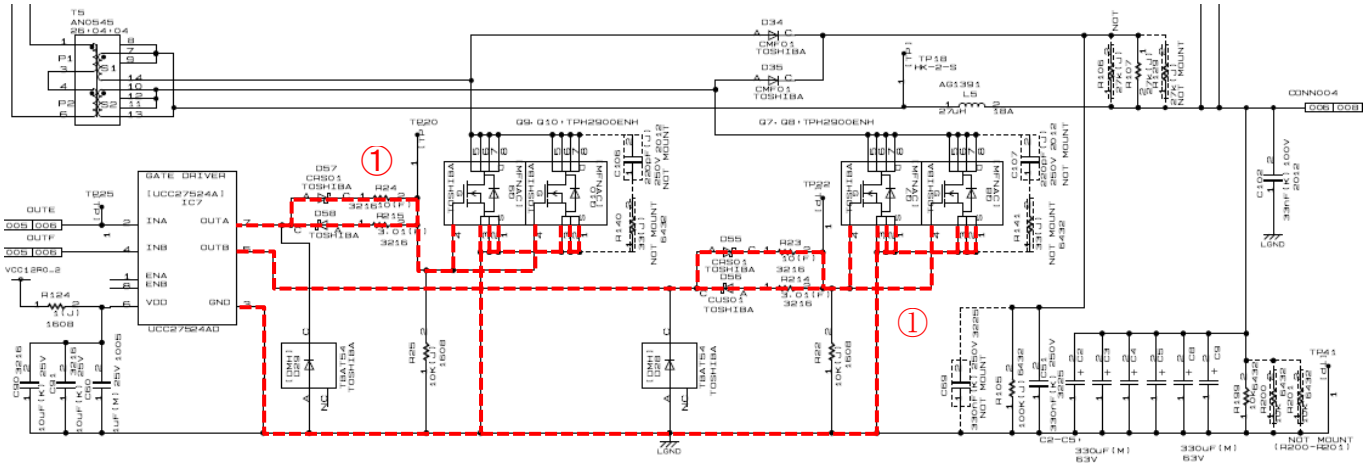

Fig. 3.6　Considerations on Designing PSFB Circuit Pattern 2

Keep the driver output line (① in the figure) as short as possible. To do so, IC7 and Q7-Q10 must be located nearby. Also, secure a pattern width that allows the driver output line to carry the maximum drive current. If the return path of the drive current is to be other than the GND (LGND) plane, isolate it from the immediate vicinity of the source pin of Q7-Q10.

The secondary side of PSFB of this power supply has a two-phase configuration. The same thing as above should be applied to the other phase as well.

The following is a layout diagram (Layer1) of the power supply around PSFB circuit.

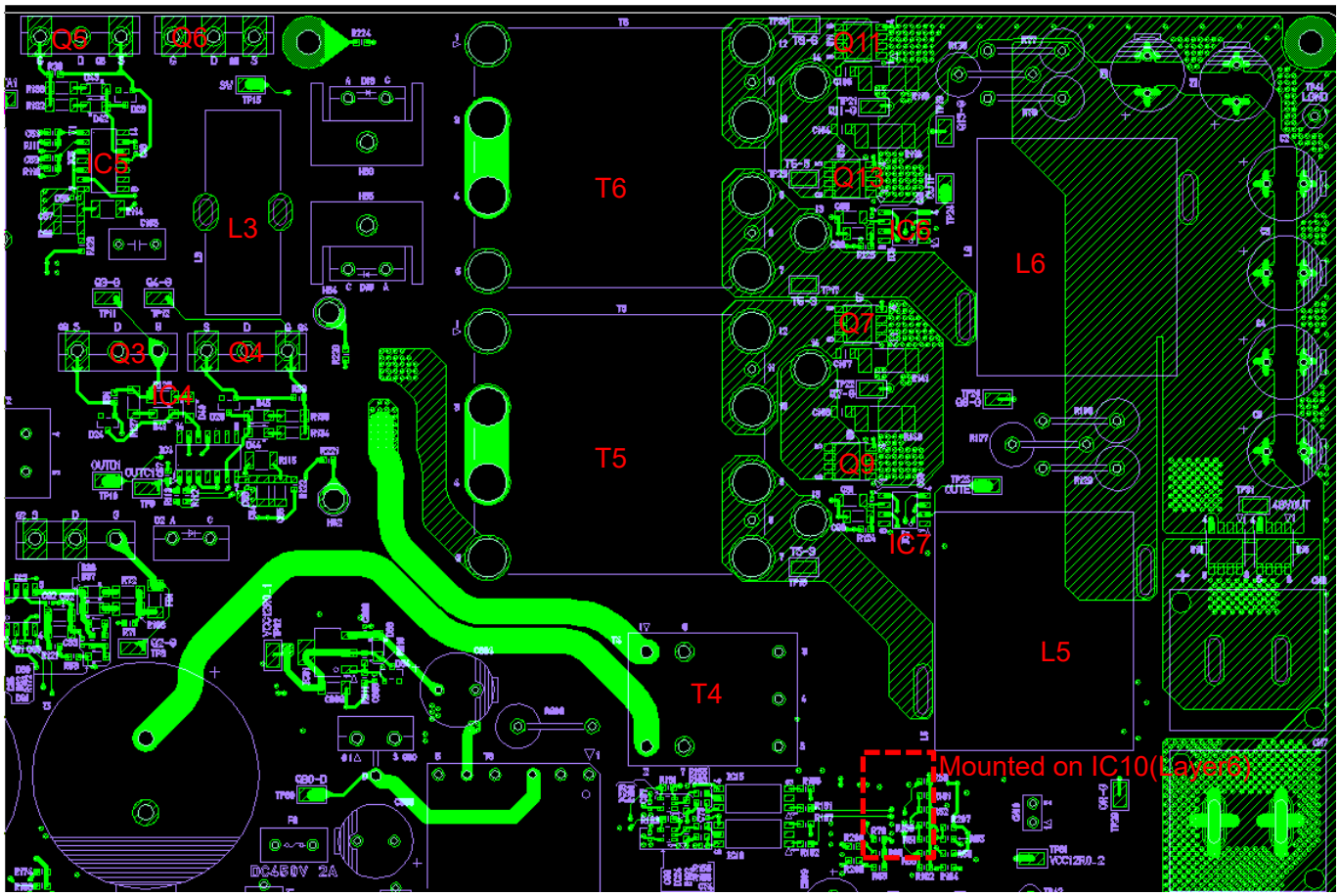

Fig. 3.7 PSFB Circuit Patterns

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