100 W LLC DC-DC Converter

Design Guide

RD165-DGUIDE-01

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

Table of Contents

1. Introduction

This Design Guide describes how to design various circuits and layouts for 100 W LLC DC-DC converter (hereafter referred to as the "Power Supply").
Refer to the reference guide for the specifications, use, and characteristic data of this power supply.

If a component is indicated as "Not Mounted" in the bill of materials, then it is not mounted on the PCB even if its part number is indicated in the circuit diagram. Mounting locations are provided on the PCB for adjustment of the constant values at the time of circuit design.

1.1. Onboard Power MOSFET

TPN7R504PL

Mounted on the primary-side main switch section.

V_{DSS} = 40 V, $R_{DS(ON)}$ (Max) = 7.5 mΩ@V_{GS} = 10 V, TSON Advance package

This MOSFET made with U-MOSIX-H process provides good balance between drive loss and conduction loss.

TPH1R204PL

Mounted on the secondary-side synchronous rectifier section.

V_{DSS} = 40 V, $R_{DS(ON)}$ (Max) = 1.24 mΩ@V_{GS} = 10 V, SOP Advance package

This MOSFET made with U-MOSIX-H process reduces loss in synchronous rectification operation.

2. Circuit Design

This section describes the key points of circuit design of this power supply.

2.1. LLC Circuit Design

This power supply generates 12 V output using the LLC resonance circuit method. The LLC-resonance circuit alternately turns on/off the high-side MOSFET and low-side MOSFET on the primary side (input side) at a duty of 50 %, and adjusts the frequency of turn on/off according to the load to control the output voltage. When the high-side MOSFET and low-side MOSFET are switched, a dead-time is provided to prevent shoot through phenomenon. However, during this time due to the resonance operation Zero Volt Switching (ZVSs) occurs in the MOSFET. ZVS reduces switching losses and enables a high-efficiency power supply. This power supply uses a controller UCC256000 manufactured by Texas Instruments (hereinafter referred to as the LLC controller) to form an LLC resonator. The following describes the basic design items of the LLC resonant circuit of this power supply. For detailed designs around the controller, refer to UCC256000 datasheets from Texas Instruments and related documents. Refer to the Reference Guide (RD165-RGUIDE-01_E) for detailed specifications of this power supply, RD165-SCHEMATIC-01 for circuit diagrams, and RD165-BOM-01 for bill of materials.

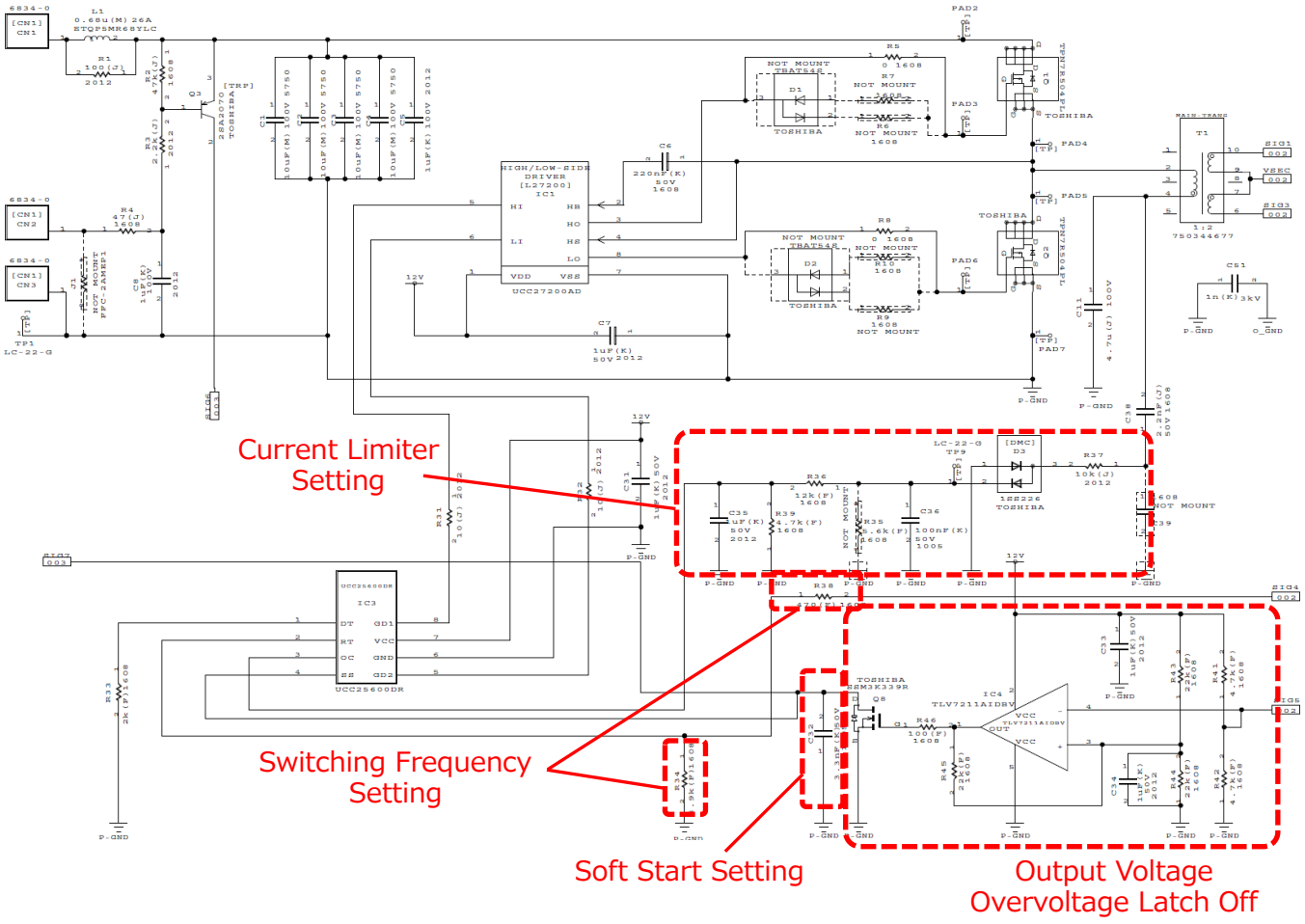

Fig. 2.1 LLC Circuit 1 (around Controller)

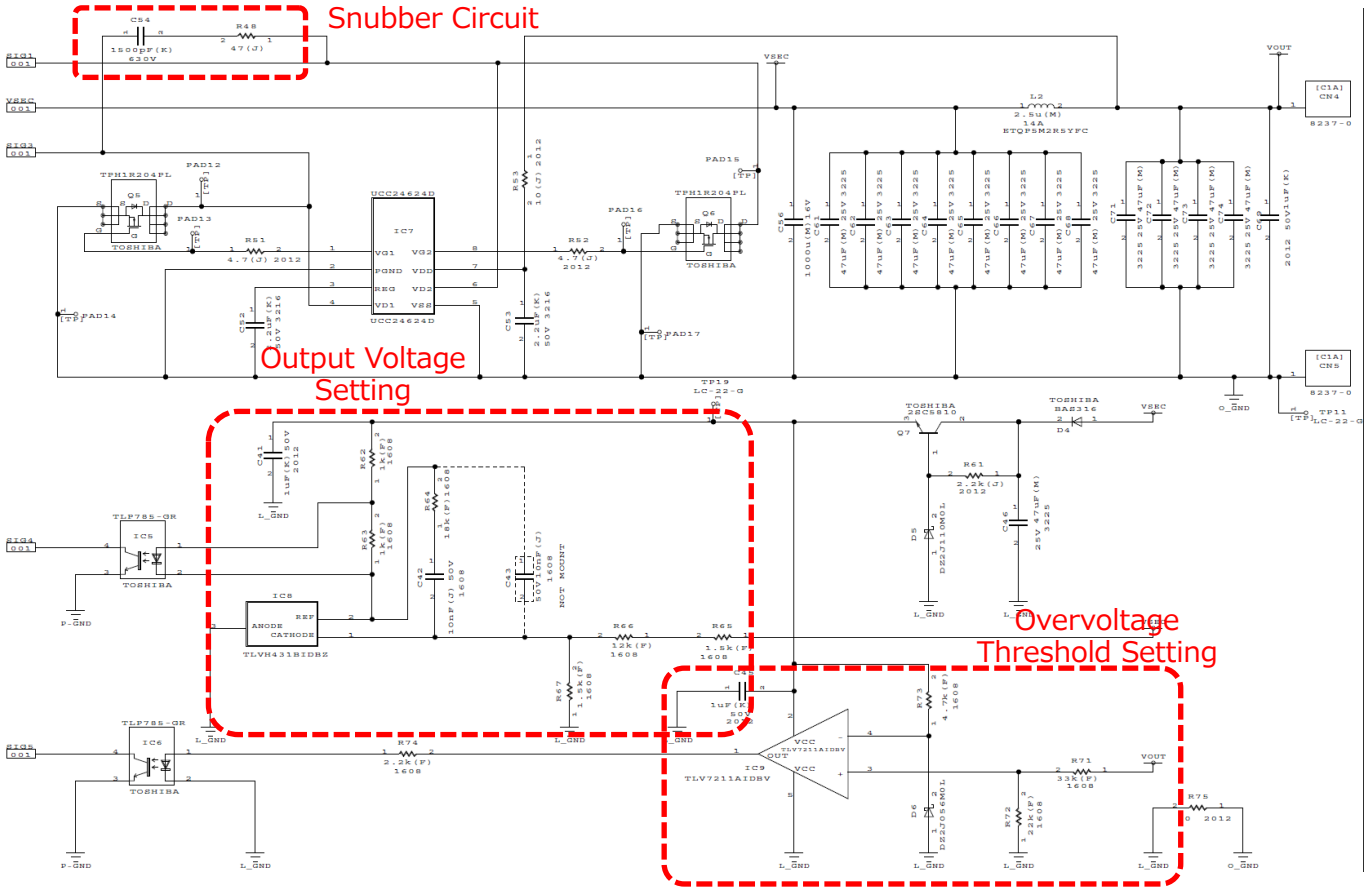

Fig. 2.2 LLC Circuit 2 (around Input-Side MOSFET)

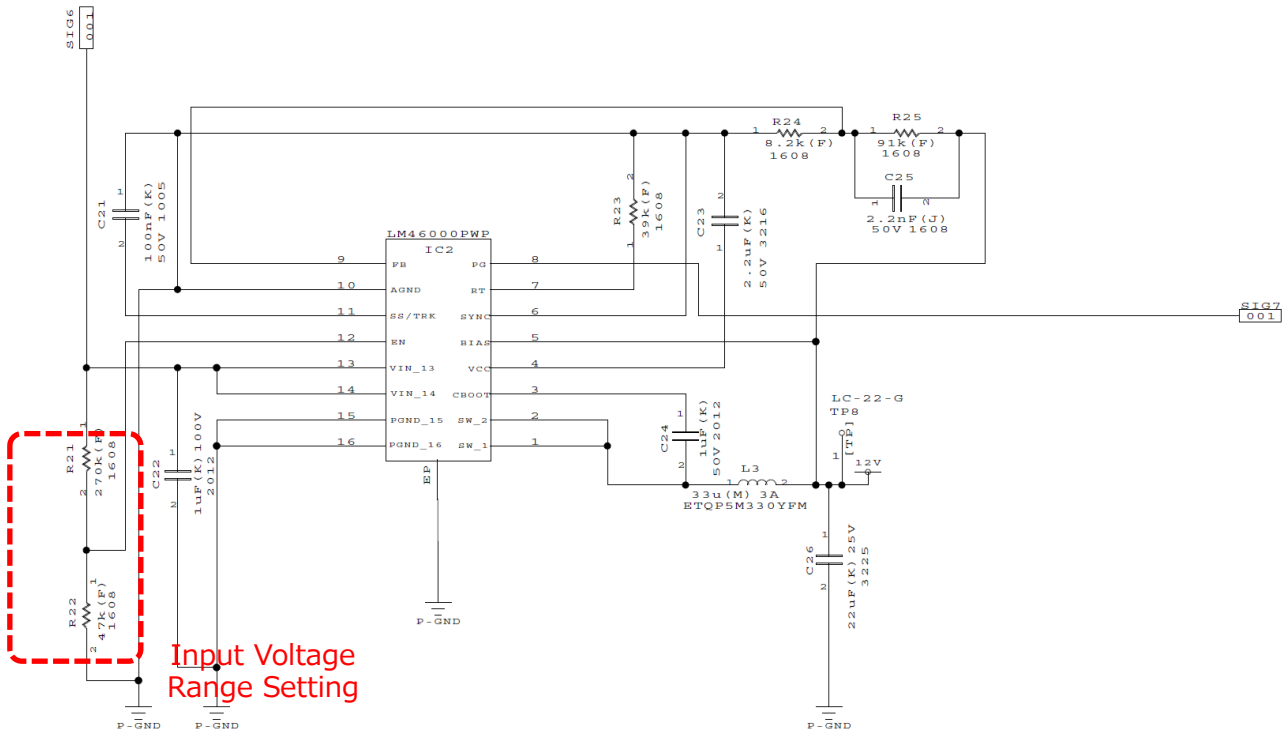

Fig. 2.3 LLC Circuit 3 (around Controller Power Supply)

Input Voltage Operation Range Setting (Lower Limit)

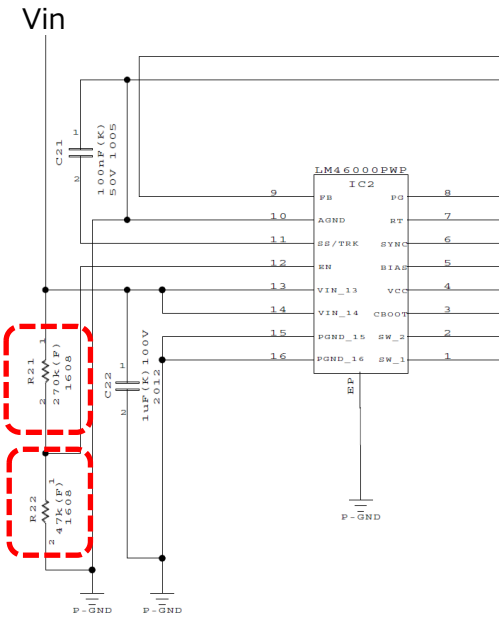

Fig. 2.4 Input Voltage Range Setting

The input voltage of this power supply is converted to 12V by the step-down converter LM46000. After that, this voltage is supplied to the LLC controller, which then starts the operation of this power supply. The input voltage range of this power supply is set by the resistance value of the external resistors (R21 and R22). The operating voltage lower limit ($V_{in\_min\_on}$, $V_{in\_min\_off}$) is set by dividing the input voltage V_{in} by resistors (R21, R22) and inputting it to the EN pin of DC-DC converter (IC2). DC-DC converter (IC2) starts switching operation when the EN pin voltage generated by the resistor division exceeds the threshold voltage (2.0 V). Since the EN pin has an internal hysteresis voltage (-305 mV), the switching stops again when the EN pin voltage drops from the threshold voltage by the amount of hysteresis voltage after switching starts.

Operating voltage lower limit ($V_{in\_min\_on}$, $V_{in\_min\_off}$) is calculated using the following equation.

$$\boldsymbol{V_{in\_min\_on}(V) = \ 2.0(V) \times \frac{(R21 + R22)}{R22}}$$

$$\boldsymbol{V_{in\_min\_off}(V) = 2.0(V) \times \frac{(R21 + R22)}{R22} \ - \ 305(mV)}$$

In this power supply, $V_{in\_min\_on}$ is set to 13.5 V, and $V_{in\_min\_off}$ is set to 13.2 V by setting the resistance value of (R21) as 270 kΩ and the resistance value (R22) as 47 kΩ, as shown in Fig. 2.4. Fig. 2.5 shows the relation between the input voltage V_{in} and the EN pin voltage and switching operation status.

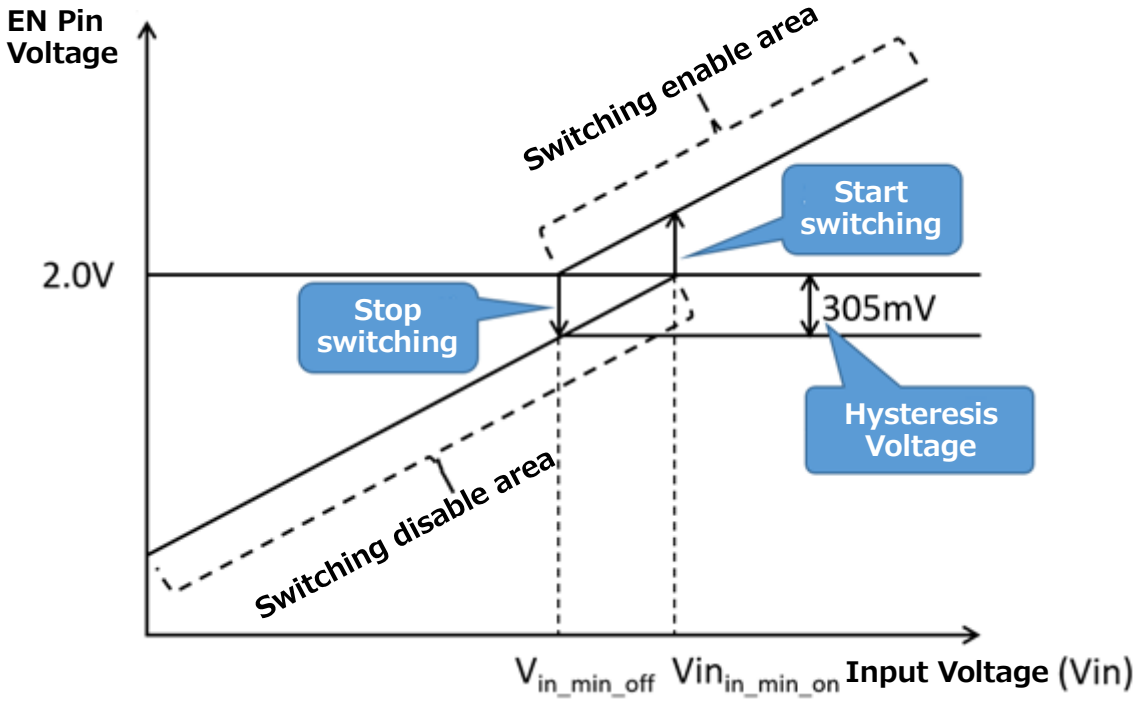

Fig. 2.5 Input Voltage vs EN Pin Voltage, Switching Operation Status

Output Voltage Setting (Phase Compensation)

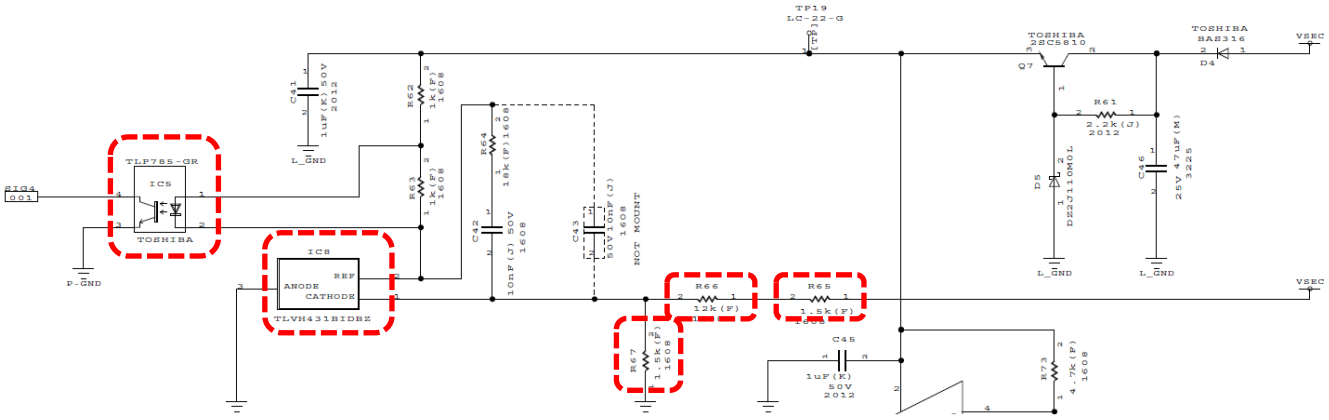

Fig. 2.6 Output Voltage Setting

Output-voltage V_{out} of this power supply is set using the external resistors (R65, R66, and R67) and the shunt regulator (IC8). The shunt regulator (TLVH431BIDBZ) controls the current of the photocoupler (IC5) so that the voltage obtained by dividing the output voltage of this power supply using resistor (R65, R66, R67) matchs the reference voltage (V_{REF} = 1.24 V). LLC controllers operates to keep the output voltage V_{out} constant according to the amount of current fed back from the photocoupler (IC5). Output voltage V_{out} is calculated using the following equation.

$$V_{out} \quad (V) = \frac{V_{REF}(V) \times (R65 + R66 + R67)}{R67}$$

In this power supply, the output voltage V_{out} is set to 12.40 V by setting the resistance value of (R65) as 1.5 kΩ, the resistance value of (R66) as 12 kΩ, and the resistance value of (R67) as 1.5 kΩ, as shown in Fig. 2.6.

Transformer (Resonance Design)

The following transformer is used in this power supply.

Winding ratio n = 1

Excitation inductance Lm = 6.97 μH

Parasitic inductance Lr = 0.78 μH

Resonant capacitance Cr = 4.7 μH

Fig. 2.7 shows the relation between switching frequency and voltage Gain when the above transformer is used.

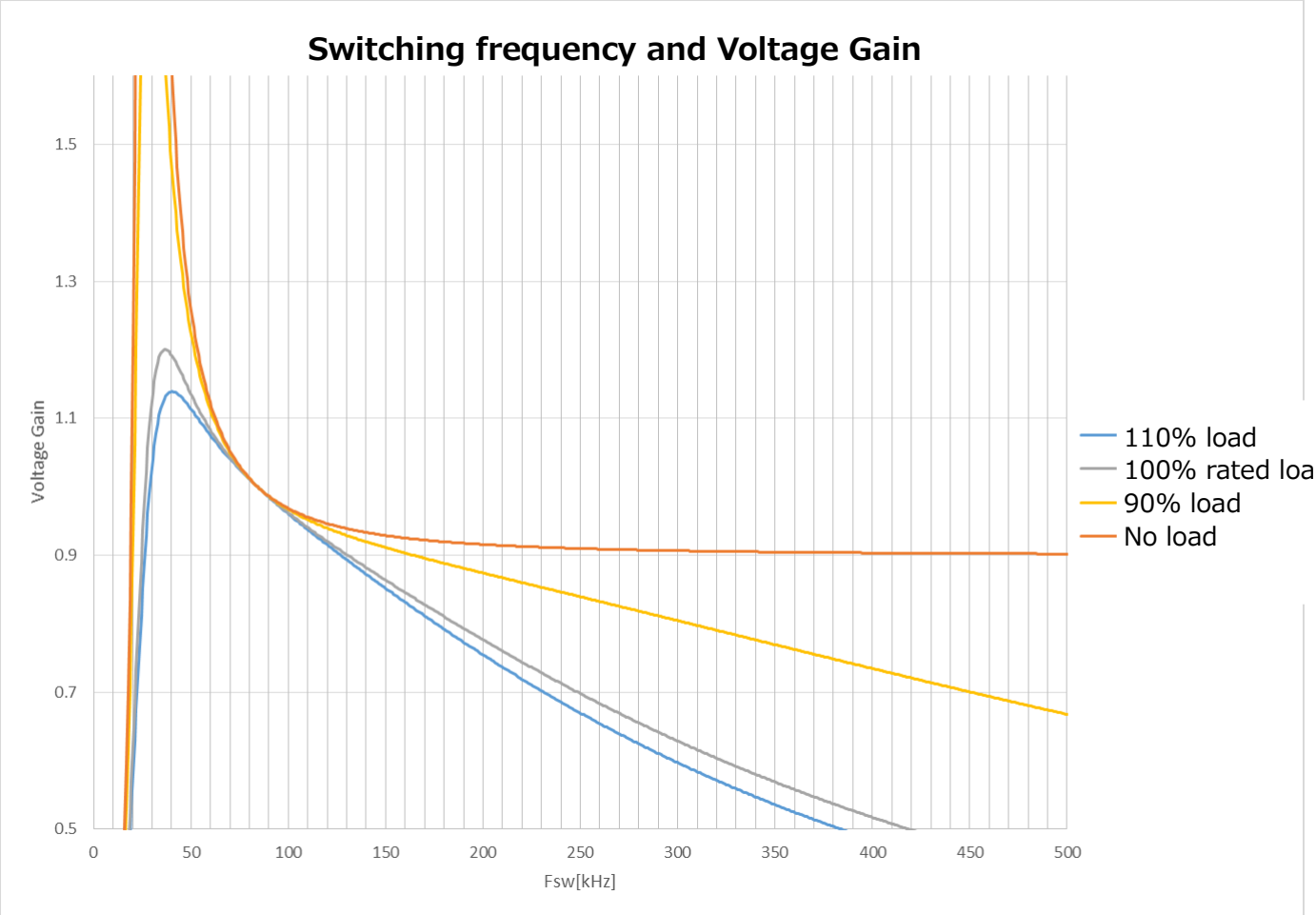

Fig. 2.7 Relation between Switching Frequency and Gain

Switching Frequency Setting (Upper/Lower Limit)

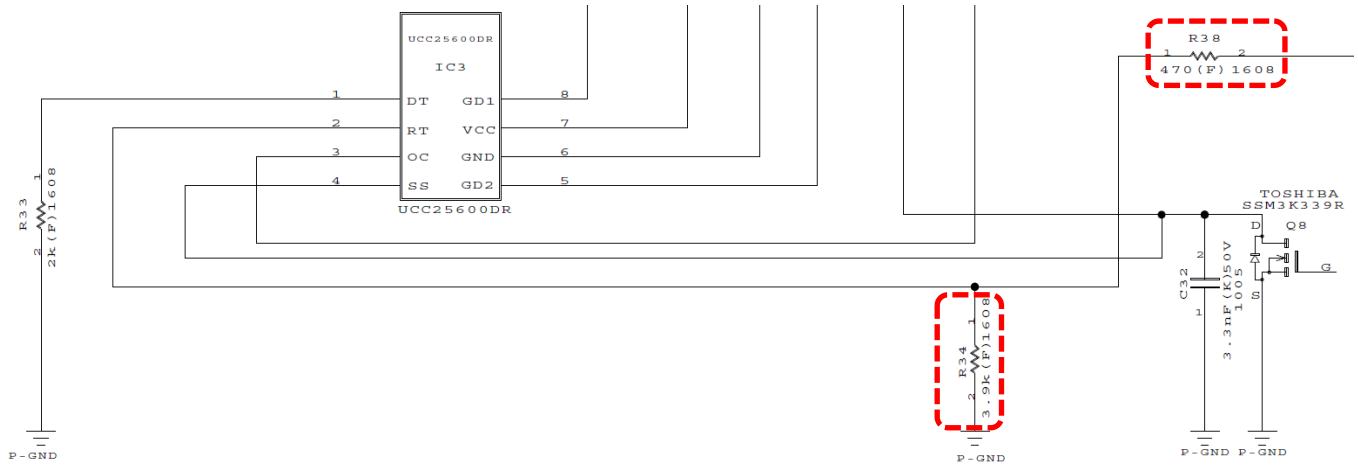

Fig. 2.8 Switching Frequency Setting

The switching frequency f_{PWM} of the LLC power supply is set using the external resistors (R34, R38). Switching frequency f_{PWM} is calculated using the following equation.

$$f_{PWM}(Hz) = \frac{1}{2} \times \frac{1}{\frac{6(ns) \times 1(A)}{I_{RT}} + 150(ns)}$$

$$I_{RT} = 2.5(V) \times \left(\frac{1}{R34} + \frac{1}{R38}\right)$$

The minimum switching frequency (f_{PWM_min}) is set using R34. For this power supply, the minimum switching frequency (f_{PWM_min}) is set to approximately 50 kHz, and 3.9 kΩ is selected as the resistance value (R34) as shown in Fig. 2.8. The maximum switching frequency (f_{PWM_max}) is set using R38. In this power supply, the maximum switching frequency (f_{PWM_max}) is set to approximately 430 kHz, and 470 Ω is selected as the resistance value (R38), as shown in Fig. 2.8.

Soft Start Setting

The soft start time (Tss) of the LLC power supply can be set by using an external capacitor (C32). The LLC controller performs soft start operation when the C32 voltage is between 1.2 V and 4 V. Just after the beginning of soft start, the frequency becomes higher than usual to reduce the inrush current, and then decreases gradually to become equal to normal frequency at the time of completion of soft start.

$$Tss(s) = C32 \times \frac{2.8(V)}{5(\mu A)}$$

In this power supply, the soft start time (Tss) is set to 1.8 ms by setting the external capacitor (C32) as 3.3 nF, as shown in Fig. 2.9. Adjust the soft start time by changing the capacitance as necessary.

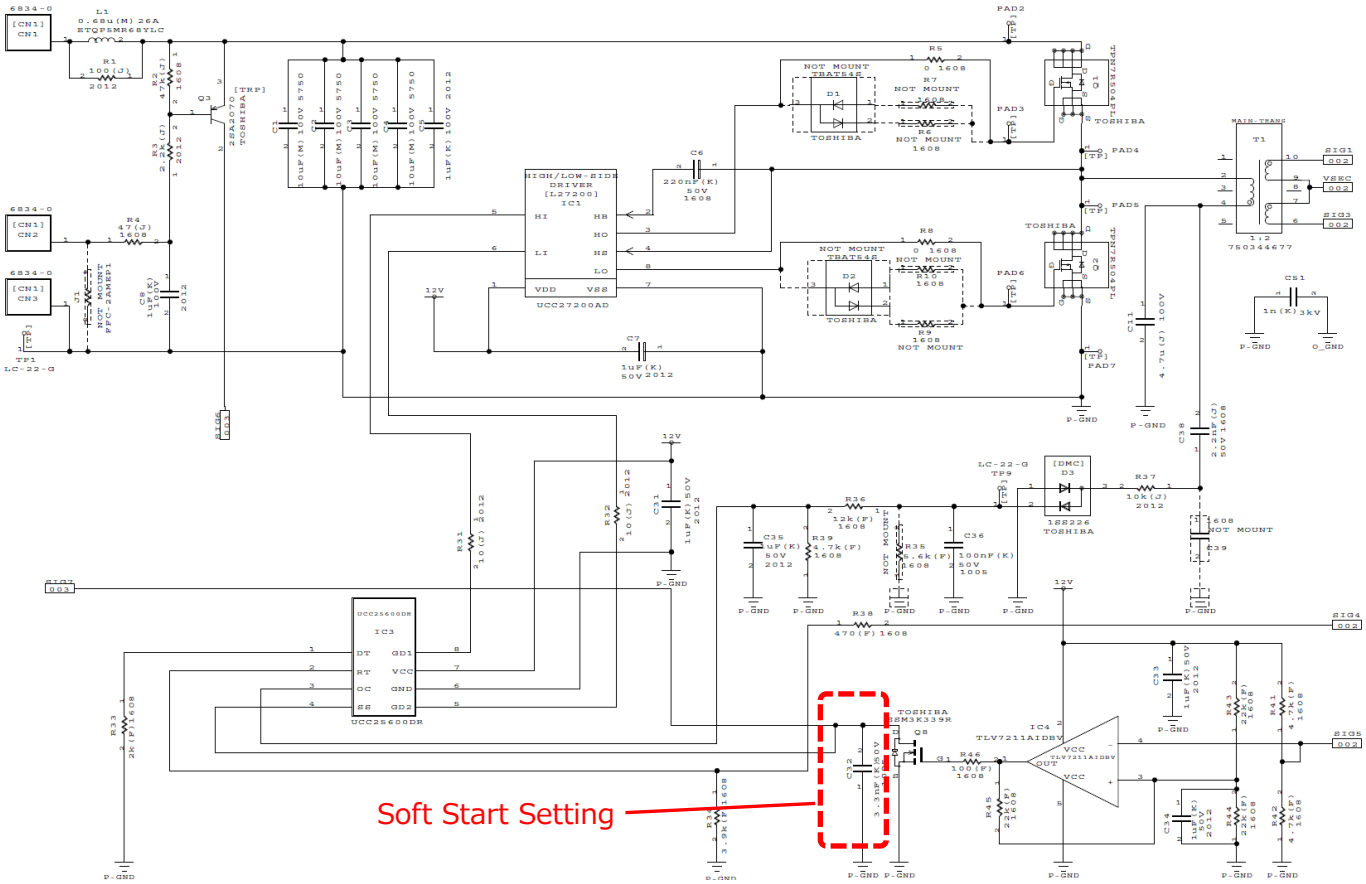

Fig. 2.9 Soft Start Setting

Gate Drive Circuit

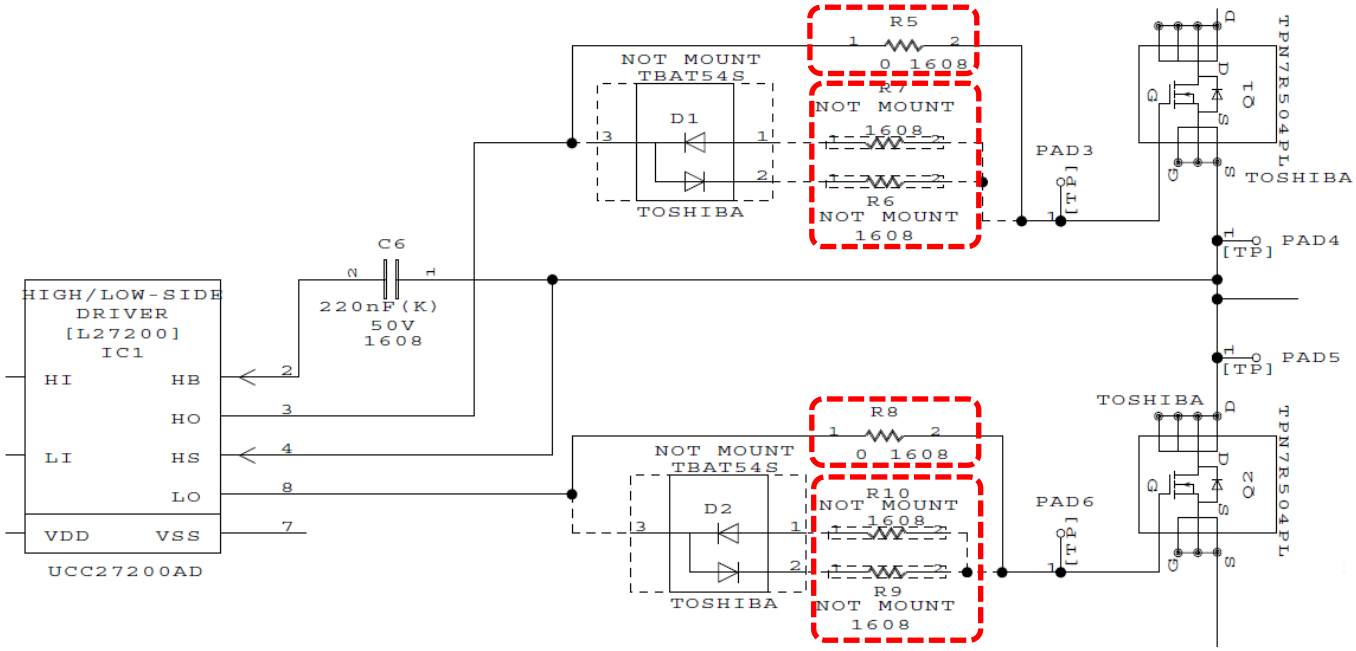

Fig. 2.11 Gate Drive Circuit

The design of the gate drive circuit affects power supply efficiency and EMI. Generally, there is a trade-off between power supply efficiency and EMI, and a balanced design is required for both. The LLC circuit has low EMI due to ZVS operation, but if switching noise seems to be the source of EMI issues, check the EMI by adjusting the resistor value (R5-R10) of the gated series resistors in MOSFET (Q1, Q2). Individual adjustments can be made for MOSFET turn on and turn off timing. As shown in Fig. 2.11, 0 Ω is selected for resistors R5 and R8, and the other resistors are not mounted.

Output Capacitor

Capacitance Value C_{out} of the output capacitor can be set to satisfy the requirements of the output ripple voltage (V_{ripple}) and the requirements of the Ripple Current.
If the output voltage ripple (V_{ripple}) is 100 mV and the maximum load is I_{max}, the ESR required for the output capacitors is calculated as follows:

$$ESR = \frac{V_{ripple}}{\frac{2 \times \pi}{4} \times I_{max}} = 7.6(m\Omega)$$

ESR is 7.6 mΩ as I_{max} is 8.4 A.

The RMS value (I_{C_rms}) of the ripple current that flows through the output capacitors is calculated by the following equation.

$$I_{C\_rms} = \sqrt{\left(\frac{\pi}{2\sqrt{2}} I_{out}\right)^2 - {I_{out}}^2} = 4.02(A)$$

Output capacitor must be selected to meet the ESR and (I_{C_rms}) specifications listed above.

Following points must also be checked:

1. The output terminal undershoot and overshoot that occur when the load changes suddenly fall is within the specified voltage range.
2. The allowable ripple current of the output capacitor is ensured.
3. Tolerances and aging of output capacitors are confirmed.

Synchronous Rectifier MOSFET Surge-Voltage Reduction Circuit

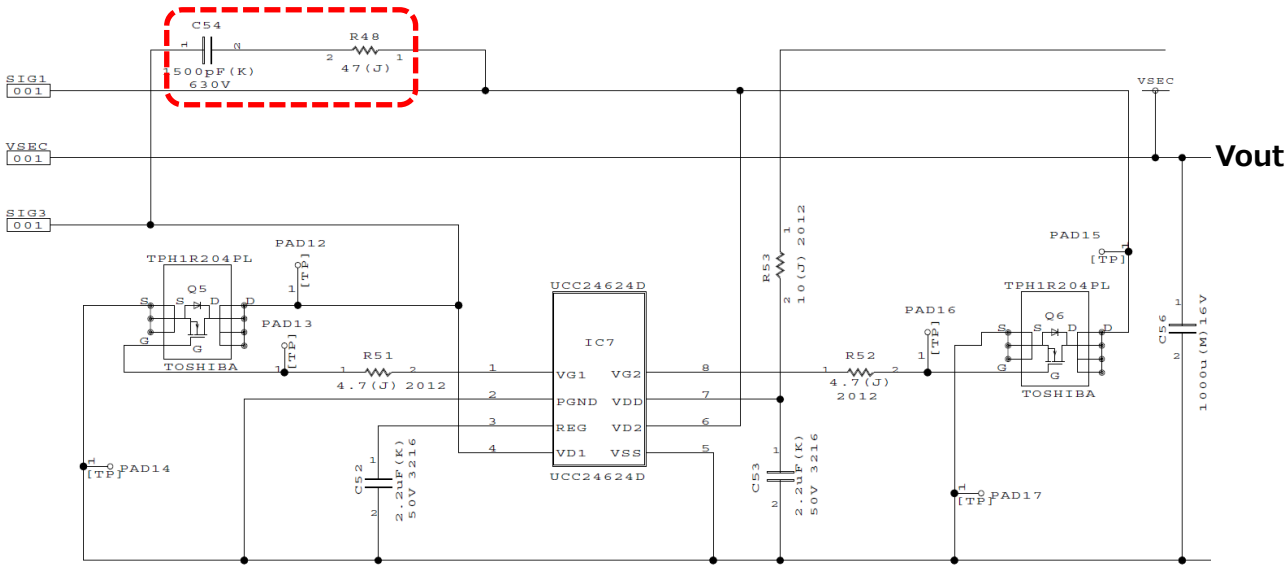

Fig. 2.12 Snubber Circuit

Snubber circuit is configured with R48 and C54 as shown in Fig. 2.12. Snubber circuit absorbs the surge-voltage (V_{srg}) generated in Q5 and Q6. At this time, the loss (P_{d_Rsnb}) generated by the resistor (R48) is as follows.

$$P_{d\_Rsnb} = C54 \times (V_{srg})^2 \times \left(\frac{f_{PWM}}{2}\right)$$

If the surge voltage (V_{srg}) is 30 V, C54 is 1500 pF, and f_{PWM} is 100 kHz, P_{d_Rsnb} is 68 mW. Adjust the constants and ratings of each element according to the actual surge voltage level.

Output Overvoltage Detection Circuit

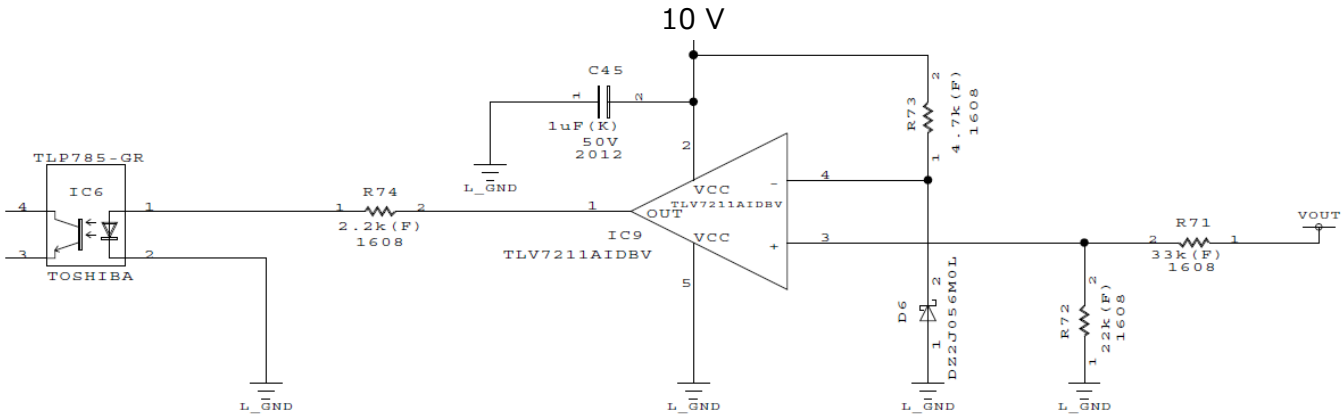

Fig. 2.13 Output Overvoltage Detection Circuit

Set the overvoltage detection value (V_{ovp}) of the output using the zener diode (D6), comparator (IC9), and external resistors (R71, R72). When the voltage obtained by dividing the output voltage using the resistance (R71, R72) exceeds the zener voltage (V_{Zener} = 5.6 V) of D6, the comparator (IC9) detects OVP and transmits an overvoltage signal to the input side. When an overvoltage signal is received, the input side circuit latches the SS pin of the LLC controller low to stop switching. The output overvoltage (V_{ovp}) is calculated using the following formula:

$$V_{ovp} = \frac{(V_{zener}) \times (R71 + R72)}{R72}$$

In this power supply, the overvoltage detection value (V_{ovp}) is set to 14.0 V by setting the resistance value of (R71) as 33 kΩ and the resistance value of (R72) as 22 kΩ, as shown in Fig. 2.13. To restart the switching operation stopped by overvoltage detection, Enable pin must be reset (open and connected to GND again).

3. PCB Design

This section describes precautions for designing the PCB of this power supply.

3.1. PCB Pattern Design

Creepage Distance

Adequate clearance and creepage distance must be ensured in accordance with the safety standards of the required specifications. Table 3.1 shows the creepage distances used for this power supply. Note that the required clearance and creepage distance vary depending on the installation environment, material, degree of contamination in the material, humidity, altitude (atmospheric pressure), and other factors. Therefore, careful consideration should be given to these factors.

Table 3.1 Required Minimum Creepage Distance

Line 1	Line 2	Creepage Distance between Line 1 and Line 2
Input (coupler)	**Output (Coupler)**	2.0 mm
Input (transformer)	**Output (transformer)**	2.0 mm

Current Capacity

Each pattern on the board must have sufficient pattern width to prevent problems due to temperature rise or IR drop caused by the pattern when maximum current is applied to each pattern.

3.2. LLC Circuit Pattern Design

This section explains precautions for PCB design around the LLC circuit. Fig. 3.1 shows the LLC circuit (around the controller), Fig. 3.3 shows LLC circuit pattern design note 1, and Fig. 3.4 shows LLC circuit pattern design note 2. For the layout around the controller, refer to the LLC controller data sheet, and related documents, etc.

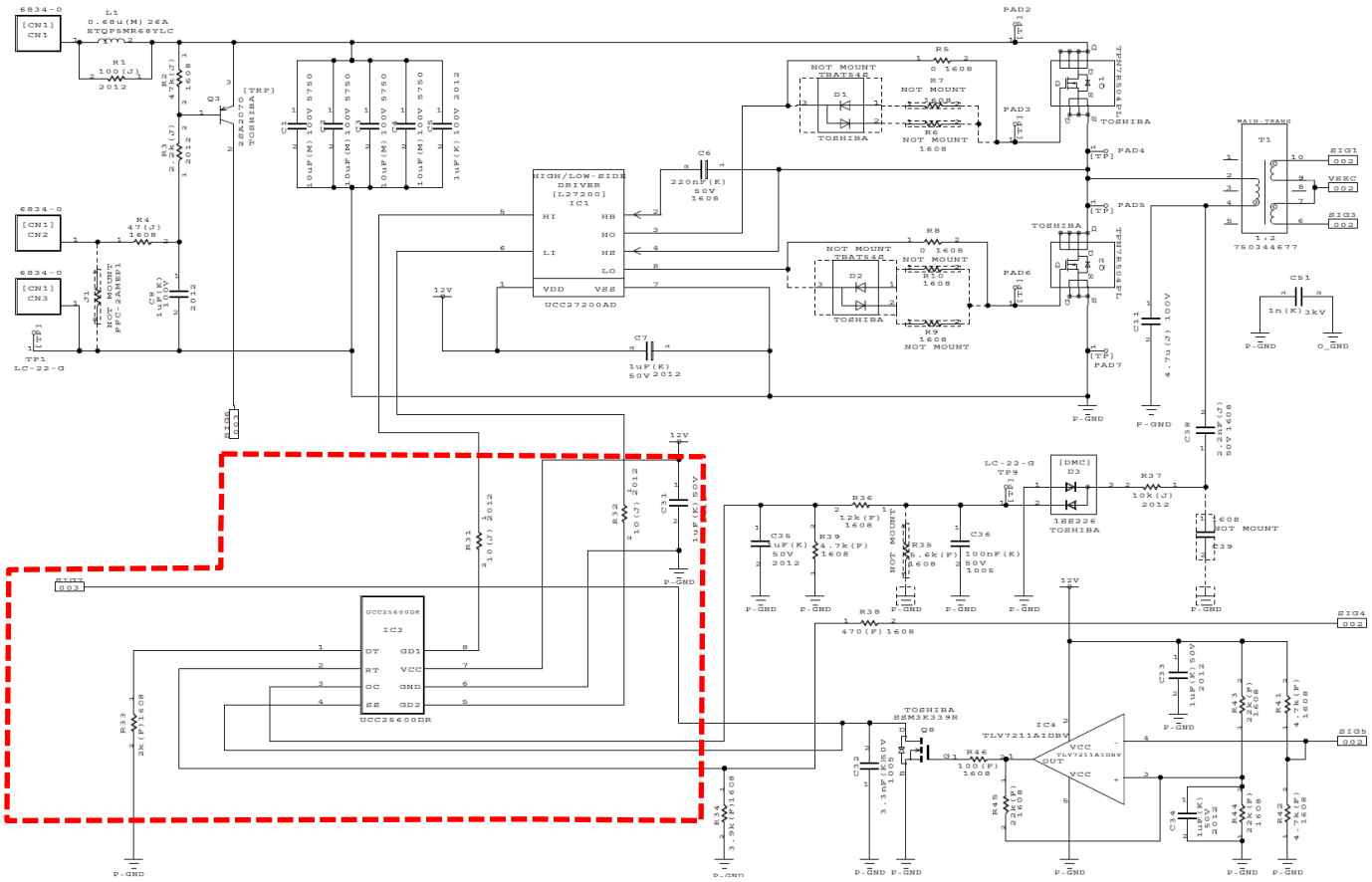

Fig. 3.1 LLC Circuit (around Controller)

1. Place the LLC-controller (IC3) away from the high-current switching circuit and transformer.
2. The components inside the red dotted line shown in Fig. 3.1 should be located near the LLC controller.
3. The GND (P-GND in the schematic) connects to the GND pin of the LLC controller in a path that does not have a common-impedance with the high-current path.

Fig. 3.2 shows the PCB front side layout. You can see that the area around the LLC controller surrounded by the broken line is located in accordance with the above precautions.

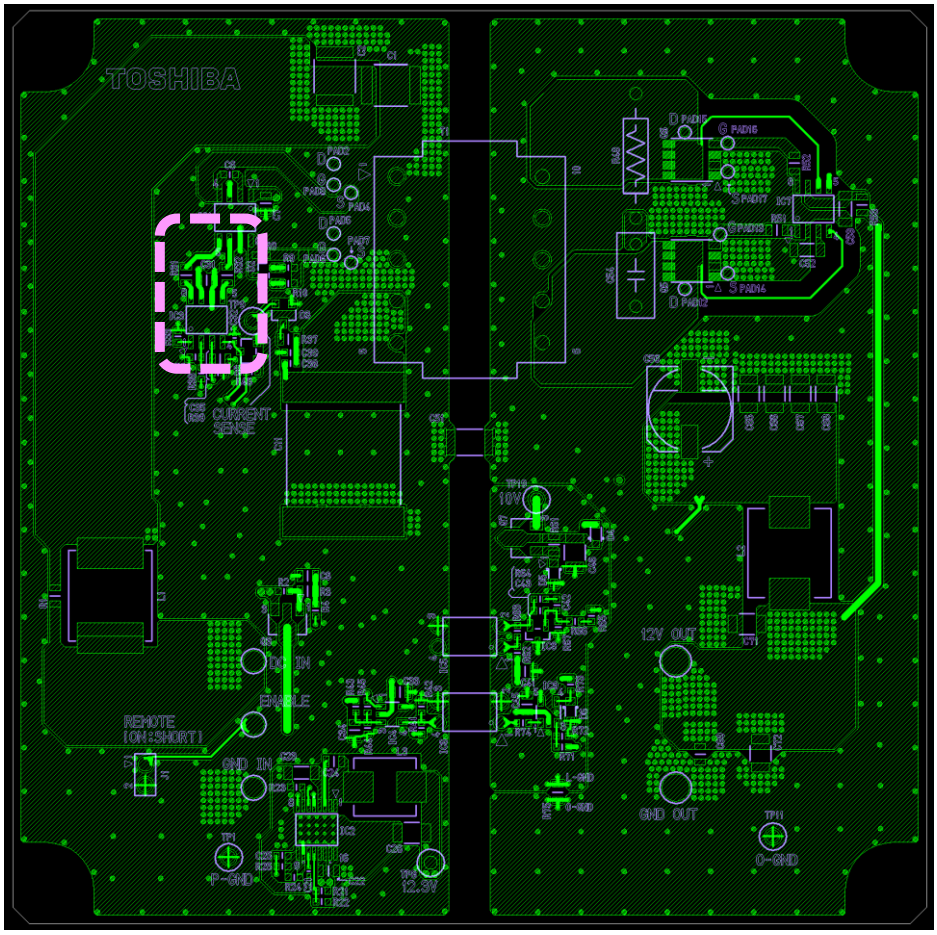

Fig. 3.2 PCB Front Side Layout (around Controller)

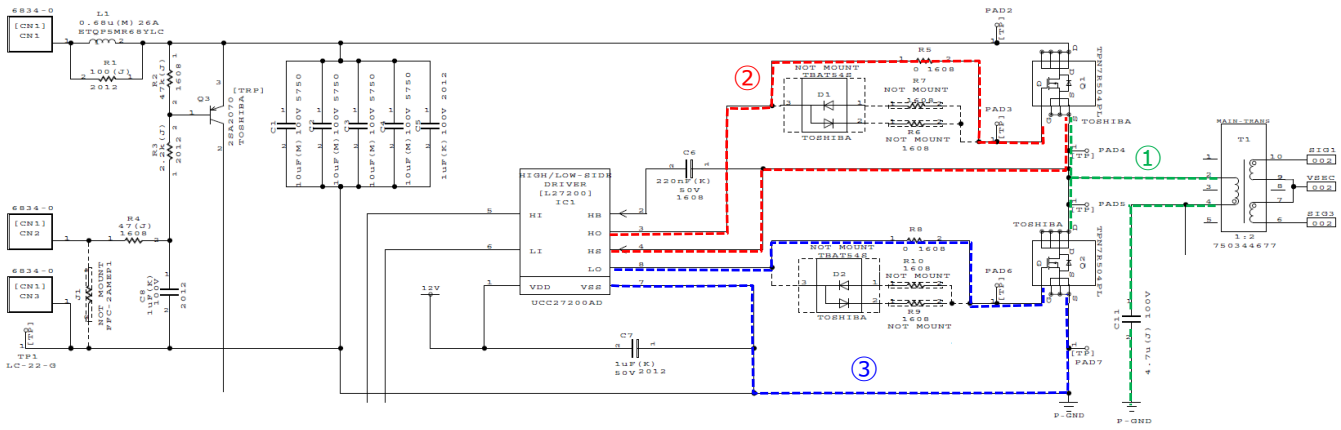

Fig. 3.3 LLC Circuit Pattern Design Note 1

1. Arrange the components so that the area around the switching node with large voltage fluctuation (the line with the same voltage fluctuation as ① and ① in the figure) is minimized.
2. Place IC1, Q1 and Q2 in the vicinity to shorten the driver output lines (in the figures ② and ③) as much as possible, ensuring a patternwidth that allows maximum drive current to flow.
3. Separate the return path of the Q1 drive current from the nearest source terminal.
4. If the return path of the Q2 drive current is to be separated from the GND (P-GND) plane, separate it from the nearest source terminal of Q1.
5. The current sensing line (pin-3 line on IC3) is sent to the LLC-controller through areas with low current and voltage variations.

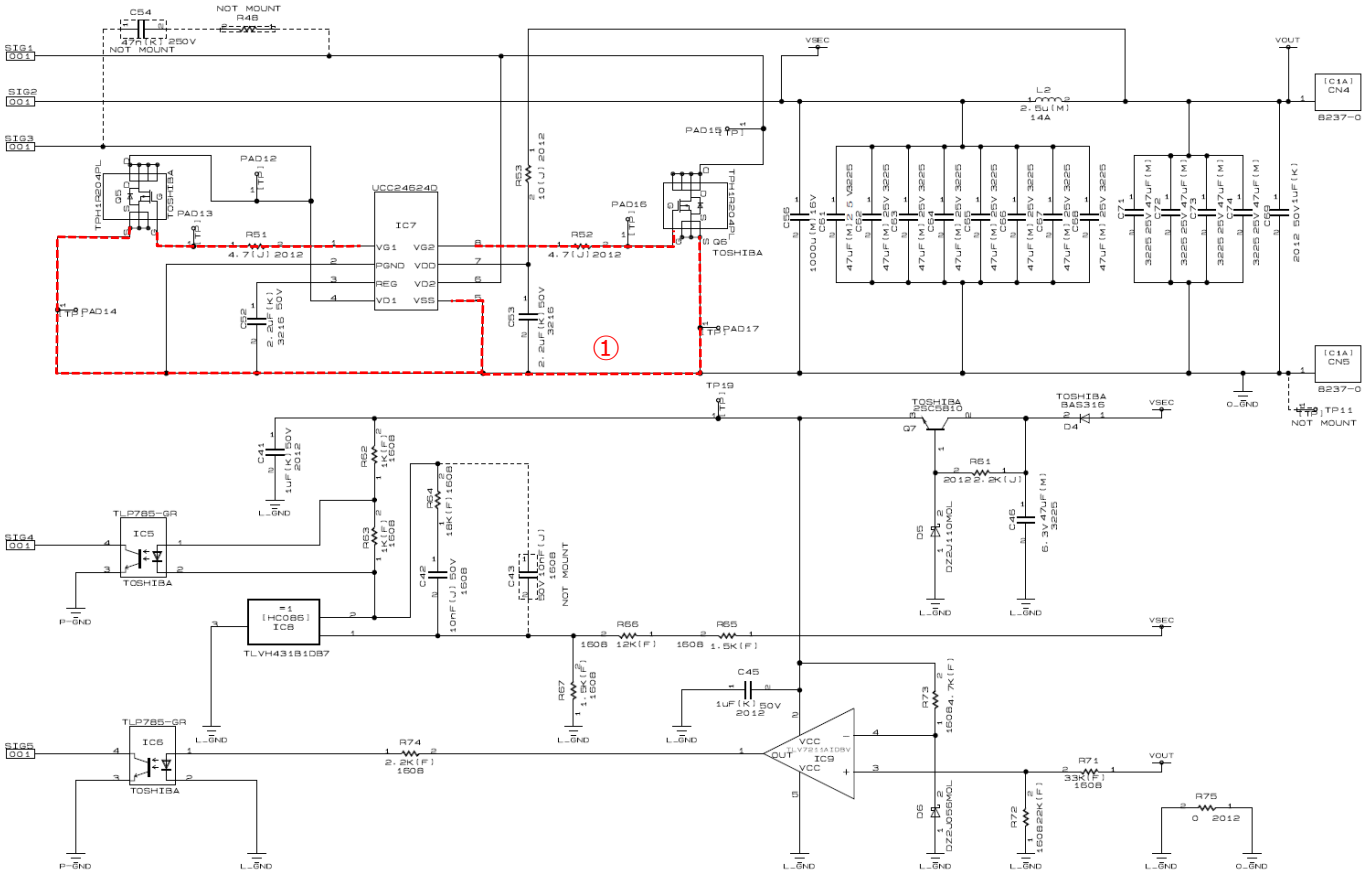

Fig. 3.4 LLC Circuit Pattern Design Note 2

1. The driver output line (in the pattern ①) is located with IC7, Q5 and Q6 in close proximity to each other in order to make it as short as possible. Ensure a patternwidth that allows the maximum drive current to flow.
2. If the return path of the drive current is to be other than the GND (O-GND) plane, isolate it from the immediate vicinity of the source terminals of Q5 and Q6.
3. Place Snubber circuit C54 and R48 close to Q5 and Q6 drain-source.
4. Place T1, Q5 and Q6 close to minimize the looping of the transformer and synchronous rectifier MOSFET.

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