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Active Clamp Forward DC-DC Power Supply Basic Simulation Circuit Reference Guide

RD158-RGUIDE-01

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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Table of Contents

1.	Introduction3
2.	Outline of Active Clamp Forward DC-DC Power Supply6
2.1	Power Supply Specifications
2.2	Circuit Configuration7
3.	Simulation Result10
4.	Product Overview17
4.1	TPN4R806PL17
4.2	TPCP8110
4.3	TPH2R003PL18
5	Using the Simulation Circuit19

1. Introduction

Most electrical equipment such as including information and telecommunications equipment and home appliances, operates with DC voltage.

Therefore, it is not possible to operate directly with commercial power supplied by AC voltage so it is necessary to convert from AC voltage to DC voltage.

Conversion from AC voltage to DC voltage is performed by AC-DC power supply. Depending on the power supply specifications of each load in the equipment, the DC voltage supplied by AC-DC power supply must be further converted to a DC voltage corresponding to that specification.

Fig. 1.1 shows an example of the configuration of the power supply line in the equipment. There are several power supply lines depending on the load, and the load may be connected directly to the output voltage supplied from AC-DC power supply, or the output voltage may be further converted to a different DC voltage by DC-DC power supply for connection. DC-DC power supply converts the DC voltage to a different DC voltage in this way.



Fig. 1.1 Example of the Configulation of the power supply Line

There are two types of conversion methods from DC voltage to DC voltage: the series regulating method and the switch regulating method (hereinafter referred to as "series-base" or "switch-base").

This document deals with switch-base, which are the mainstream in DC-DC power supplies. The switch-base regulates the on/off of the switching MOSFET to generate the desired voltage. The control circuit is more complicated than the series-base, but in general, the loss can be reduced than the series-base.

There are two way of switch-base: one is isolated DC-DC power supply, in which the input side and the output side are isolated by a transformer, and the other is non-isolated DC-DC power supply, in which the input side and the output side are not isolated. This document handles isolated DC-DC power supplies.

The isolated DC-DC power supply switches the input DC voltage at frequencies of several tens to several hundred kHz with a switching MOSFET, transmits the power to the secondary side through a transformer, rectifies, and smoothes to output the DC voltage. The final stage DC voltage is controlled by adjusting the switching MOSFET on/off period.

Fig. 1.2 shows examples of circuit blocks for isolated switch-base DC-DC power supply. It consists of two blocks: (1) DC-DC converters and (2) feedback circuits, as shown in the illustration. The functions of each block are shown below.





Fig. 1.2 Circuit Blocks for Isolated Switch-base DC-DC Power Supply

(1) DC-DC converters

Converts the input DC voltage to any DC voltage.

(2) Feedback circuit

The switching MOSFET is controlled so that the output voltage becomes a desired value.

There are a variety of topologies for DC-DC converters. Table 1.1 shows typical topologies and characteristics of DC-DC converters.

Circuitry of the DC-DC converter section		Power level	Advantages	Disadvantages
Flyback		< 200 W	• Small part count	 Reduction in efficiency at high power Large transformer
Forward		50 W~500 W	 Higher efficiency than a flyback circuit 	Transformer reset circuit required
Active clamp forward		50 W~500 W	 Higher Efficiency than a forward 	 There are many parts. Be difficult to control
Half bridge		100 W~1 kW	 High efficiency Low noise 	 Specially designed transformer is required. Be difficult to control
Resonant half bridge (LLC resonance)		100 W~1 kW	 High efficiency than a half bridge Low noise 	 Specially designed transformer is required. Be difficult to control
Full bridge		> 200 W	 High efficiency Capable of There are many par Be difficult to contro power capacity 	

 Table 1.1
 Typical Topologies and Characteristics of DC-DC Converters

Regarding the basic operation of the DC-DC converter, we are distributing it on our web. Please also refer to the video below.

The Video of the DC-DC converter are shown here \rightarrow

The active clamp forward method described in this document is widely used for power supplies requiring high efficiency because the active clamp operation when resetting the transformer allows products with low tolerant voltage to be used for the MOSFET for the main switch, and the MOSFET for the main switch and active clamp operate at zero volt switching (ZVS) to achieve low switching losses. In order to understand the operation of the active clamp forward method DC-DC converter in a switching method AC-DC power supply, Toshiba provide basic simulation circuits (RD158-SPICE-01) on our website.

This document provides an overview of this basic simulation circuit and explains how to use it. The Cadence's Capture and PSpice [®] A/D tools are required to operate the simulator circuits from OrCAD. Simulation circuits and documentation have been prepared in accordance with OrCAD 17.2.



2. Outline of Active Clamp Forward DC-DC Power Supply

The basic simulation circuit (RD158-SPICE-01) is a 70 W active clamp forward DC-DC power supply.

2.1 Power Supply Specifications

The active clamp forward DC-DC power supply specifications described in this document are as follows:

- Input voltage (V_{in}) : 24 V
- Output voltage (V_{out}) : 3.3 V
- Output current (I_{out}) : 0 to 21 A
- + Secondary MOSFET Operating frequency ($F_c)\,$: 150 kHz
- Winding ratio: $n_1:n_2 = 2:1$
- Allowable ripple current width on the secondary side ($\Delta I_{\text{ripple}})$: 40 %

2.2 Circuit Configuration

Fig. 2.1 shows the simulation circuit for OrCAD[®]. This is the active clamp forward type DC-DC converter power supply, which mainly consists of a power section (active clamp forward) and a PWM controller section. The secondary side of the power section is a synchronous rectification circuit using MOSFETs. The PWM controller section is a general-purpose controller with a built-in MOSFET gate driver, which is provided to realize PWM circuit. The main switching MOSFET is "TPN4R806PL", the active clamping MOSFET is "TPCP8110", the secondary synchronous rectifier MOSFETs are "TPH2R003PL" as example.



Fig. 2.1 Simulation Circuit of 70 W Active Clamp Forward (DC-DC converter) Power Supply

Selection of primary MOSFET

Primary side MOSFET (TPN4R806PL: V_{DSS} =60 V, I_D for the primary main switch = 72 A) is selected from the following viewpoints.

(1) Breakdown-voltage

The voltage applied to the MOSFET at static state is the input voltage (=24 V). Select a MOSFET with a breakdown-voltage of 60 V or higher, considering the surge voltage at the time of switching and other factors.

(2) Current rating

When the input current is maximum, it is at the maximum output power. If the conversion efficiency at the maximum output power (=100W) is 90%, the maximum average input current is 9.3 A. Select a MOSFET with a current rating of 19 A or more.

Here, we selected a 72 A current MOSFET from our product lineup.

Active clamping MOSFET (TPCP8110: VDSS=-60 V, ID =-5 A) of primary side is selected from the following viewpoints.

(1) Breakdown-voltage

The voltage applied to the MOSFET at static state is the input voltage (=-24 V). Select a MOSFET with a breakdown-voltage of -60 V or lower, considering the surge voltage at the time of switching and other factors.

(2) Current rating

Only the exciting current of the transformer flows to the MOSFET for active clamping, and no load current flows.

An excitation current (I_{mag}) of approximately -1.9 A (max.), calculated from the equation below, flows in this MOSFET. In this example, a device with a rated current of -5 A was selected.

$$I_{mag} = \frac{V_{in} \times D_{uty}}{F_c \times L_{mag}} \div 2$$

 $V_{in}:$ 24 V, $D_{uty}:$ 0.5, $F_c:$ 150k Hz, L_{mag} (Excitation inductance) $\,:$ 21u H

Selection of secondary MOSFET

Secondary MOSFET (TPH2R003PL: V_{DSS} =30 V, I_D =100 A) is selected from the following viewpoints. (1) Breakdown-voltage

Since the winding ratio is 10:1, the voltage between the middle point and both ends of the secondary winding at static state is 12 V, which is 1/2 of the input voltage, and 12 V, which is twice the voltage, is applied to each MOSFET on the secondary side.

A surge voltage is generated when the transformer current is switched. Select a MOSFET with a breakdown-voltage of 30 V or more.

(2) Current rating

The maximum output current is at the maximum output power. Since the maximum output current when the maximum output power (=70 W) is 21 A, an element with a current rating of 42 A or more is required. In addition, select an element with as low an on-resistance as possible with emphasis on suppressing conduction loss.

Selection of output inductor

This section explains how to select the output inductor on the secondary side. The inductance value of the output inductor in this simulation circuit can be calculated using the following items, which are power supply specifications.

- Input voltage: $V_{in}(V) = 24$
- Transformer winding ratio: $n_2/n_1 = 1/2$
- Output Voltage: V_{out} (V) = 3.3
- MOSFET switching frequency: F_c (Hz) = 150k
- Max. output current: I_{out_max} (A) = 21
- Allowable ripple current range: $\Delta I_{ripple}(A) = 40$

The inductance value (L_0) of the output inductor is calculated by the following equation:

$$L_{o} = \frac{\left(\frac{n_{2}}{n_{1}} \times V_{in} - V_{out}\right) \times V_{out}}{\frac{n_{2}}{n_{1}} \times V_{in} \times F_{c} \times I_{out_max} \times \Delta I_{ripple} \times 0.01}$$

The inductance value (L_0) of the output inductor is calculated as 1.9 μ H from the above equation, and 2 μ H is selected as the setting value from the power supply specifications of this model. In the actual design, the inductance value of the inductor varies due to the DC superposition characteristic. Select a component that can secure the calculated value in a state where the inductance value is lowered due to the DC superposition characteristic.

3. Simulation Result

The operation simulation waveforms of each part in the simulation circuit are shown by the points in Fig. 3.1 ((1) to (4)).

- (1) Active clamp forward basic operation ("Primary MOSFET Drain-Source Voltage/Current")
- (2) Secondary-side synchronous rectification operation ("Secondary-side MOSFET drain-source voltage/current")
- (3) Output inductor voltage and current at both ends
- (4) "Output voltage and current" as a power supply

When actually using the circuit model, it is possible to display the waveform at any point other than those shown in Fig. 3.1. The waveform display method is described in Chapter 5.



Fig. 3.1 Simulation Waveform Measurement Point List

(1) Active clamp forward basic operation

The basic operation of the active clamp forward method is described in Fig. 3.2, which shows the active clamp forward circuit.



Fig. 3.2 Active Clamp Forward Circuit

In the active clamp forward method, the output voltage is stabilized by controlling the Q_1 by PWM (Pulse Width Modulation).

For the output-voltage V_{out} , it can be calculated by:

$$V_{out} = \frac{n_2}{n_1} \times V_{in} \times \frac{T_{on}}{T}$$

T: Period of the primary side T_{on} : On-time

A. Q_1 is on, Q_2 is off

This is the period during which power is transferred from the primary side to the secondary side. The primary winding voltage at this time is the input voltage (V_{in}). For the secondary winding, the voltages corresponding to the winding ratios are given with the polarity symbol of the n_2 as positive.

$$\frac{n_2}{n_1} \times V_{in}$$

The voltage is applied to the L_0 via the Q_3 ,

$$\Delta i_{Lo(Q1_on)} = \frac{1}{L_o} \times \left(\frac{n_2}{n_1} \times V_{in} - V_{out}\right) \times T_{on}$$

The current determined by is linearly increased to charge the C_{out} and provide the output current (I_{out}). At this time, magnetic energy is stored in the L_0 .

B. Q_1 is off, Q_2 is off

The Q_1 off charges the Q_1 drain-source capacitance $C_{DS(Q1)}$ and increases $V_{DS(Q1)}$. When the $V_{DS(Q1)}$ exceeds the V_{in} , the voltage on the primary side of the transformer (Tx1) is reversed, the Q_3 is turned off, and the energy stored in the L_0 is circulated through the Q_4 . To the L_0 at this time, the current decrease linearly as follows.

$$\Delta i_{Lo(off)} = \frac{-V_{out}}{L_0} \times (T - T_{on})$$

C. Q_1 is off, Q_2 is on

When the $V_{DS(Q1)}$ increases and exceeds the resonant capacitor voltage (V_{Cr}), the body diode $D_{(Q2)}$ of the Q_2 conducts and the exciting current of the Tx1 flows to the C_r . At this time, the $V_{DS(Q2)}$ of the Q_2 is nearly 0 V, so it is turned on with ZVS (zero-volt switching). The Tx1 resonates under the condition determined by the primary inductance and chromium. When the $V_{DS(Q1)}$ reaches the peak, the excitation current flows from the C_r to the V_{in} , and the direction of the Q_2 drain current is negative.

D. Q_1 is off, Q_2 is off

The Tx1's exciting current continues to flow in V_{in} directions, discharging the charge stored in the Q₁'s drain-to-source capacitance ($C_{DS(Q1)}$). After discharging the $C_{DS(Q1)}$, the exciting current flows through the body diode $D_{(Q1)}$ of the Q₁. After this, the Q₁ turns on, but the V_{DS(Q1)} turns on at ZVS since it is almost 0 V.

Fig. 3.3 shows the primary-side MOSFET drain-source voltage and output inductor voltage/current waveforms.



Fig. 3.3 Primary MOSFET Drain-Source Voltage/Current, Output Inductor Voltage/Current

(2) Secondary side synchronous rectification operation

This simulation model uses a synchronous rectifier circuit that uses MOSFET instead of diodes for the secondary rectifier. Generally, the conduction loss due to the on-resistance of the MOSFET is smaller than that of the diode so the synchronous rectifier circuit can reduce the conduction loss. The larger output current, the greater loss reduction effect of the synchronous rectifier circuit, and is often used in applications where high efficiency and large capacity are required.

The operation of the secondary MOSFET in the respective periods are as follows.

a. Q_3 is on, Q_4 is off

Voltage corresponding to the winding ratio with the polarity symbol side of the secondary side winding n_2 as plus voltage,

$$\frac{n_2}{n_1} \times V_{in}$$

is applied, current flows through the Q_3 to the L_0 and charges the C_{out} while supplying the output current (I_{out}).

b. Q_3 is off, Q_4 is off

The energy stored in the $L_{\rm O}$ passes through the Q_4 body diodes, causing an annular current to flow.

c. Q_3 is off, Q_4 is on

The energy stored in the L_0 passes through the MOSFET part of the Q_4 , and an annular current flows.

d. Q₃ is off, Q₄ is off

The energy stored in the L_0 flows through the body diodes of the Q_3 and Q_4 , causing an annular current to flow.

(3) Output inductor voltage and current at both ends

Fig. 3.4 shows the output inductor voltage and current waveforms in conjunction with the secondary-side synchronous rectification operation (secondary-side MOSFET drain-source voltage and current) described in (2).



* : Drain current is positively directed from the source to the drain of the MOSFET.

Fig. 3.4 Secondary-side MOSFET Drains/Source Voltage / Current Output Inductor Voltage / Current Waveforms

(4) "Output voltage and current" as a power supply

Fig. 3.5 shows the output voltage and current waveforms of this power supply circuit. It can be seen that it is stable at the set voltage and current.



Fig. 3.5 Output Voltage and Current Waveforms

4. Product Overview

This section provides an overview of our products that have been tested by incorporating PSpice[®] models into the circuits.

4.1 TPN4R806PL

Features

- V_{DSS}=60 V, I_D=72 A
- High speed switching
- Small gate-input charge: Q_{SW} = 9.5 nC (Typ.)
- Small power charge: Q_{oss} = 24 nC (Typ.)
- Low on-resistance: $R_{DS(ON)}$ = 3.5 m Ω (Typ.) (V_{GS}=10 V)
- Lower leakage current: $I_{DSS} = 10 \ \mu A \ (Max.) \ (V_{DS}=60 \ V)$
- Easy-to-handle enhancement type: $V_{th} = 1.5$ to 2.5 V ($V_{DS}=10$ V, $I_D=0.3$ mA)

Appearance and terminal arrangement



TSON Advance

Width 3.3 \times Length 3.3 \times Height 0.85 (mm)

4.2 TPCP8110

Features

- V_{DSS}=-60 V, I_D=-5 A
- Small gate-input charge: Q_{SW} = 14 nC (Typ.)
- Low on-resistance: $R_{DS(ON)}$ =30.4 m Ω (Typ.) (V_{GS} =-10 V)
- Lower leakage current: $I_{DSS} = -10 \ \mu A \ (Max.) \ (V_{DS} = -60 \ V)$
- Easy-to-handle enhancement type: $V_{th} = -2 \text{ to} 3 \text{ V} (V_{DS} = -10 \text{ V}, \text{ I}_{D} = -1 \text{ mA})$

Appearance and terminal arrangement



Width 2.9 \times Length 2.8 \times Height 0.8 (mm)

4.3 TPH2R003PL

Features

- V_{DSS}=30 V, I_D=100 A
- High speed switching
- Small gate-input charge: Q_{SW} = 22 nC (Typ.)
- Small gate-output charge: Q_{oss} = 41 nC (Typ.)
- Low on-resistance: $R_{DS(ON)}$ = 1.3 m Ω (Typ.) (V_{GS}=10 V)
- Lower leakage current: $I_{DSS} = 10 \ \mu A \ (Max.) \ (V_{DS}=30 \ V)$
- Easy-to-handle enhancement type: $V_{th} = 1.1$ to 2.1 V ($V_{DS}=10$ V, $I_D=0.5$ mA)

Appearance and terminal arrangement



SOP Advance

Width 5.0 \times Length 6.0 \times Height 0.95 (mm)

5. Using the Simulation Circuit

In order to verify the operation according to actual specifications and the changes according to circuit constants, the simulator can freely change various parameters and analyze the operation of the simulator on OrCAD's Capture. This section describes how to set parameters and how to analyze the operation when actually performing a simulation.

Parameter settings

Table 5.1 lists the parameters that can be set by the simulation circuit. Double-clicking a variable in the parameter setting section displays the "Display Properties" window shown in Fig. 5.1. Change the "Value" value in that window.

Variable name	Unit	Description		
Vin	V	Input voltage		
Vout	V	Output voltage		
Fc	Hz	Switching frequencies of the secondary MOSFET		
DCR1	Ω	Primary power plane parasitic resistance		
DCR2	Ω	GND plane parasitic resistance value on the primary side		
Vdrv_H_p	V	Power supply voltage of the primary gate driver		
Rdrv_off_p	Ω	Primary MOSFET Internal resistance of gate driver (off side)		
Rdrv_on_p	Ω	Primary MOSFET Internal resistance of gate driver (on side)		
Vdrv_H_s	V	Power supply voltage of the secondary gate driver		
Rdrv_off_s	Ω	Secondary MOSFET Internal resistance of gate driver (off side)		
Rdrv_on_s	Ω	Secondary MOSFET Internal resistance of gate driver (on side)		
Td	Sec	Dead time of Q1 and Q3		

Table 5.1 List of Variables Settable in Parameter Setting Section

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Display Properties		
Name: Vin Value: 24 Display Format Do Not Display Value Only Name and Value Name Only Both if Value Exists Value if Value Exists	Font Arial 7 Change Use Default Color Default	PARAMETER: vin = 24 Vout = 3.3 Fo = 150k DCR1 = 5m DCR2 = 5m Vdrv_H_p = 12 Rdrv_off_p = 1 Rdrv_on_p = 1 Vdrv_H_s = 5 Rdrv_off_s = 1 Rdrv_on_s = 1 Td = 370n
ОК Са	Text Justification Default ~	

Fig. 5.1 Parameter Setting Screen

How to set analysis

The procedure for executing the simulation of this simulation circuit is described below.

(1) The "New Simulation" window shown in Fig. 5.2 is displayed by clicking "PSpice"-"New Simulation Profile" on OrCAD's Capture menu bar. Specify any profile names and click "Create".

New Simulation	X
Name:	Create
Tran_500ms	
Inherit From:	Cancel
none	 ■
Root Schematic: SCHEMATIC1	

Fig. 5.2 New Simulation window

(2) After the steps in 1., the "Simulation Settings" window shown in Fig. 5.3 is displayed, allowing various analysis settings to be made. First, set the analysis method in Analysis tab. Specify "Time Domain(Transient" for "Analysis Type". Specify the duration of the analysis in "Run To Time" and the largest step length in the analysis in "Maximum Step Size".

	Analysis Type:	Run To Time :	500ms	seconds (TSTOP)
a. Select "Time Domain (Transient)"	Time Domain (Transient)	Start saving data after : 0 seconds Transient options: Maximum Step Size 0.1u seconds Skip initial transient bias point calculation (SKIPBP) C. Enter the m			b. Enter the simulation end tim the maximum tep size
	Save Check Point Restart Simulation	ОК	Cancel	Apply Reset	Help

Fig. 5.3 Simulation Settings"-"Analysis window

(3) Set analysis options in Options tabs It is recommended to activate the auto-convergence function by checking the "Analog Simulation"-"Auto Converge"-"AutoConverge" checkbox as shown in Fig. 5.4.

General Analysis Configura	tion Files	Options Da	a Collection Probe	Window
Analog Simulation General MOSFET Option General General Bias Point Transient Gate Level Simulation	Auto TL1 TL2 TL2 TL4 REL ABS	TOL	Value 000 To check "Aut is recomm	
General Advanced Cutput File General			.001 1.0E-10	.001 1.0E-10

Fig. 5.4 Simulation Settings"-"Options window

- (4) When the above settings are completed, click "OK" and close the "Simulation Settings" window.
- (5) Execute simulations at "PSpice"-"Run" on OrCAD "Capture" menu bar. PSpice A/D starts automatically and the simulations are executed.

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How to check the results

This section describes how to check the results after completion of simulation. There are two methods for displaying the result waveforms on PSpice A/D window. The procedures for each method are described below.

Method 1: Results display with net name specified

- (1) Right-click outside the graph frame in the graph window, and then select "Add Trace". (Fig. 5.5)
- (2) Select the waveforms to be displayed from the "Add Traces" window. Select V (net name) for the voltage waveform and I (element name) for the current waveform. (Fig. 5.6)
- (3) After selecting, click "OK" to display the result waveform. (Fig. 5.7)





Fig. 5.5 Graph Window

Fig. 5.6 "Add Traces" Window



Fig. 5.7 Result Waveform Display (Example: Output Voltage Waveform)

Method 2: Displaying the result using Marker function

- (1) Select Marker type according to the waveform to be displayed from "PSpice"-"Markers" on OrCAD's Capture menu bar. (Fig. 5.8)
- (2) Place Marker at the waveform measuring points on the simulator. (Fig. 5.9)
- (3) The result waveforms are displayed in the graph window of PSpice A/D. (Fig. 5.10)







Fig. 5.9 Placing a marker in the circuit



Fig. 5.10 Simulation waveform view (Example: Output Voltage Waveform)

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