1.2V/100A Output DC-DC Converter Compliant with 48V Bus Voltage

Design Guide

RD040-DGUIDE-03

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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1. Introduction

With the rapid progress of information and communication technologies, the volume of information processed every day has been increasing at an explosive rate in recent years. In response to this trend, many data centers have been constructed and expanded, however, due to increasing the total amount of power by all the data center's activities, we have to reduce those power consumption. Today we consider one of the way to reduce data center's power consumption using 48V bus voltage for server racks to improve its power supply efficiency, which is recommended by the Open Compute Project (OCP). The OCP called "open rack architecture" uses 48V bus lines from the AC voltage to be converted to 48VDC while conventional server uses 12V bus lines from AC voltage to be converted to 12VDC.

The power loss caused by a power line is calculated as I^2R, where R is power line resistance and I is its current so the lower the current, the lower the power loss. Now, let's consider the power consumption when the same amount of power is supplied to server racks through 12V bus lines and 48V ones. The current that passes through a 48V bus line is one-fourth the current that passes through a 12V bus line. If the 48V bus lines and 12V ones have the same resistance of the bus lines, the 48V bus line solution has 1/16th lower power consumption than the 12V one. Although increasing the voltage of a bus line reduces its current and thus power loss, a bus line voltage exceeding 60VDC is considered dangerous by safety standards. Such a high bus line voltage would require safety measures different from those used for 12VDC bus lines that fall under extra-low-voltage (ELV) or safety extra-low voltage (SELV) so the OCP specifies that the input voltage range for the 48V bus line is from 40VDC to 59.5VDC so that the same safety measures as for 12V bus lines can be used.

However, the 48V bus line architecture has its own problems. A rack runs power at 48V all the way to the motherboard and we have to generate around 1V from 48V in order to operate digital electronics such as CPUs, GPUs, and memories. In general, as the input voltage gets higher, step-down DC-DC converters generally become less efficient so converting 48V to 1V causes a potential big power loss. Even if the 48V bus line architecture reduces a loss caused by a power line, its total loss could be equal to or greater than the 12V bus line architecture because of the loss by this DC-DC conversion.

To solve this problem, Toshiba offers a reference design for a DC-DC converter that is high efficiently steps down the 48V bus line voltage to 1.2V to improve total system power consumption. This reference design provides electrical isolation with transformers to achieve high-efficiency conversion with a big input/output voltage difference from 48V to 1.2V.

This design guide describes guidelines for the circuit design and layout of a DC-DC converter. Refer to the reference guide for the specifications, operating method, and electrical performance data of this converter.

Components marked "Not Mounted" in the Bill of Materials (BOM) are not mounted on the PCB even if components are shown in the circuit diagram. The PCB reserves mounting space for them necessary to modify circuit constants when designing a circuit.

1.1. Power MOSFETs Lineup

Toshiba offers the U-MOSVIII and U-MOSIX low-voltage MOSFET series which suits primary (main switch) and secondary (synchronous rectification) sides of DC-DC converters. Toshiba provides MOSFETs with wide range of V_{DSS} from 30V to 250V and various on-resistance types in each V_{DSS} class so you can find proper MOSFETs when designing a DC-DC converter, according to its circuit topology, input and output voltages, output specification, and the locations of MOSFETs on circuit (primary or secondary side). Figure 1.1 shows the lineup of the U-MOSVIII and U-MOSIX MOSFET series.

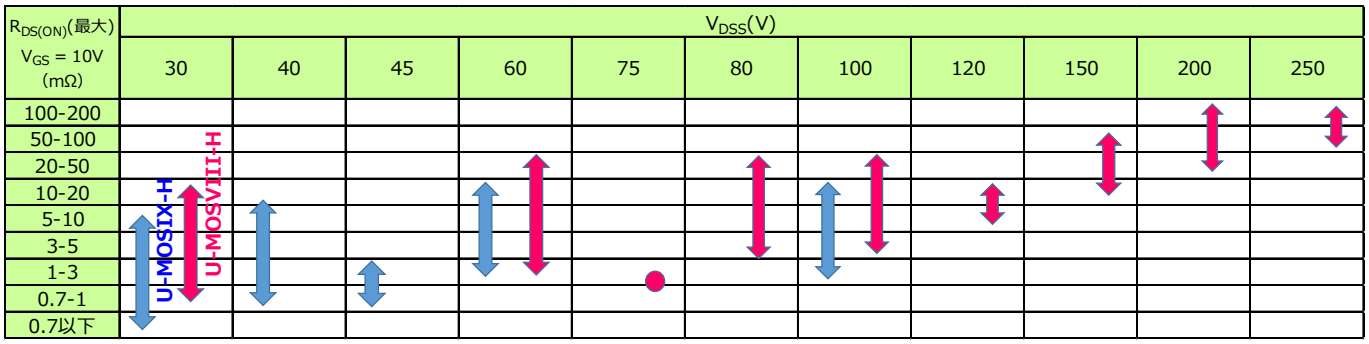


Figure 1.1 Product lineup of the U-MOSVIII and U-MOSIX MOSFET series

The following shows the MOSFETs used in this DC-DC converter. Because this converter has an input voltage range of 40 to 59.5V, an output voltage of 1.2V, and a half-bridge topology, MOSFETs with 100V of V_{DSS} for the primary side and 30V of V_{DSS} for the secondary side are selected. The primary side uses the TPN1200APL with an excellent balanced drive and conduction losses, whereas the secondary side uses the TPHR6503PL with low on-resistance, prioritizing a reduction in conduction loss.

TPN1200APL

For the main switch on the primary side

V_{DSS} = 100V, $R_{DS(ON)}$ = 11.5mΩ (max.) at V_{GS}=10V, TSON Advance package

Balanced conduction and drive loss are achieved by applying the latest U-MOSIX-H process.

TPHR6503PL

For the synchronous rectifier on the secondary side

V_{DSS} = 30V, $R_{DS(ON)}$ = 0.65mΩ (max.) at V_{GS}=10V, SOP Advance package

Low power loss in synchronous rectification is achieved by applying the latest U-MOSIX-H process.

2. Circuit design

This section shows major considerations for the circuit design of this DC-DC converter.

2.1. Half-bridge circuit

This 1.2V/100A DC-DC converter generates a 1.2V output with a half-bridge circuit. A half-bridge circuit is basically configured as a push-pull circuit, which alternately turns on and off with two switching devices to alternately activate two transformers. Although a half-bridge circuit operates in the same way as a push-pull circuit, the half-bridge circuit applies only one-half of Vi across the transformers, making it possible to use low-voltage transistors. Although this increases the efficiency of the transformers, we should take care of heat generated by the switching current that flows through the capacitors on the primary side of the transformers.

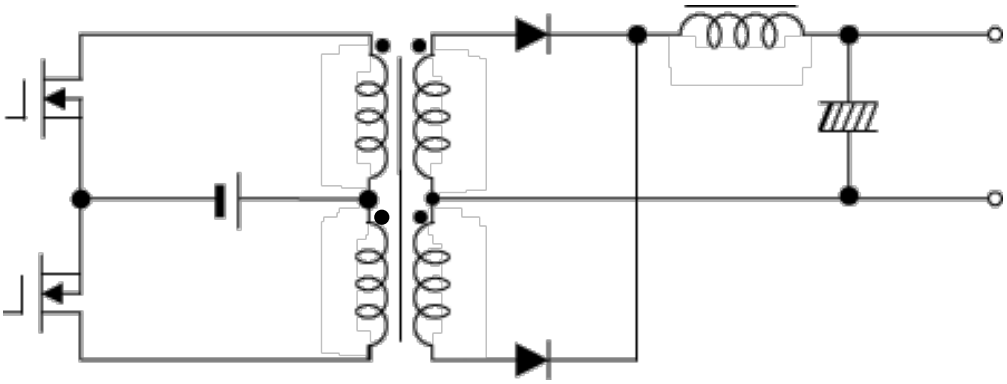


Figure 2.1 Push-pull circuit

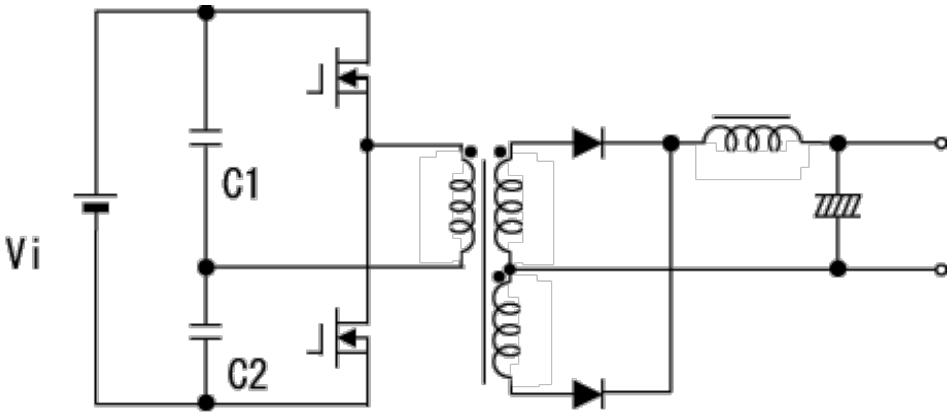


Figure 2.2 Half-bridge circuit

2.2. Designing a half-bridge circuit

The 1.2V/100A DC-DC converter uses the LM5035 half-bridge PWM controller from Texas Instruments to form a half-bridge circuit. This subsection describes the basic design of the half-bridge circuit in the 1.2V/100A DC-DC converter. For the detailed design around the half-bridge PWM controller, see the LM5035 datasheet and other related documents from Texas Instruments. See the Reference Guide (RD040-RGUIDE-02) for the detailed specifications of the 1.2V/100A DC-DC converter, RD040-SCHEMATIC-01 for circuit drawings, and RD040-BOM-01 and Table 2.1 for a bill of materials.

Figure 2.3 shows a block diagram of this circuit, which consists of the following sections.

- A : Around the controller (Figure 2.4)
- B : Around the MOSFETs on the input side (Figure 2.5)
- C : Around the synchronous rectification MOSFETs on the output side (Figure 2.6)
- D : Circuit for setting the output voltage (Figure 2.11)
- E : Output smoothing filter (Figure 2.15)

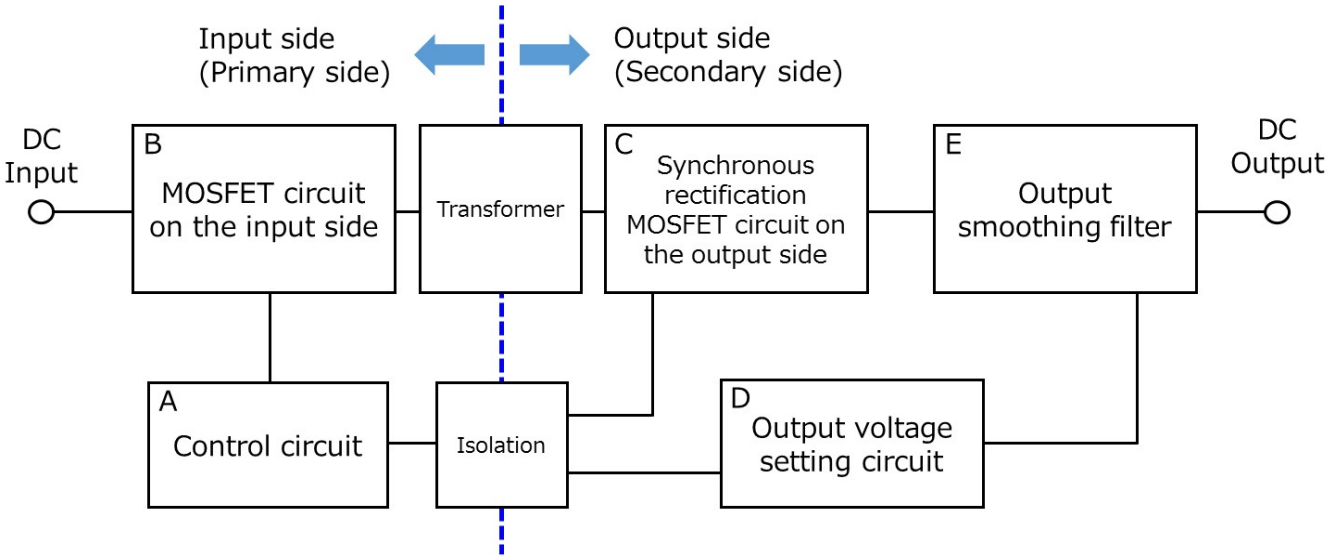


Figure 2.3 Block diagram of a half-bridge circuit

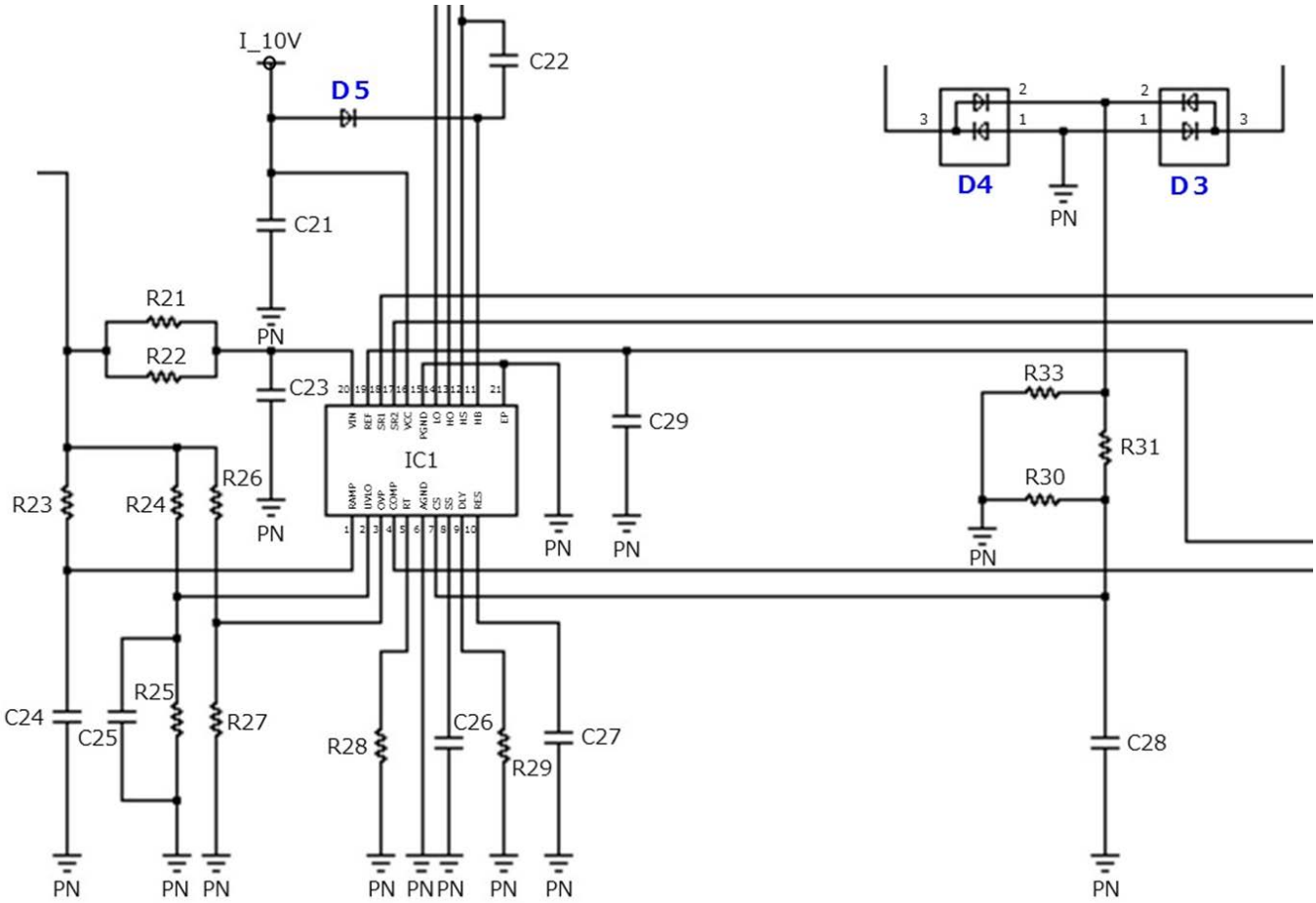


Figure 2.4 Half-bridge circuit 1 (around the controller)

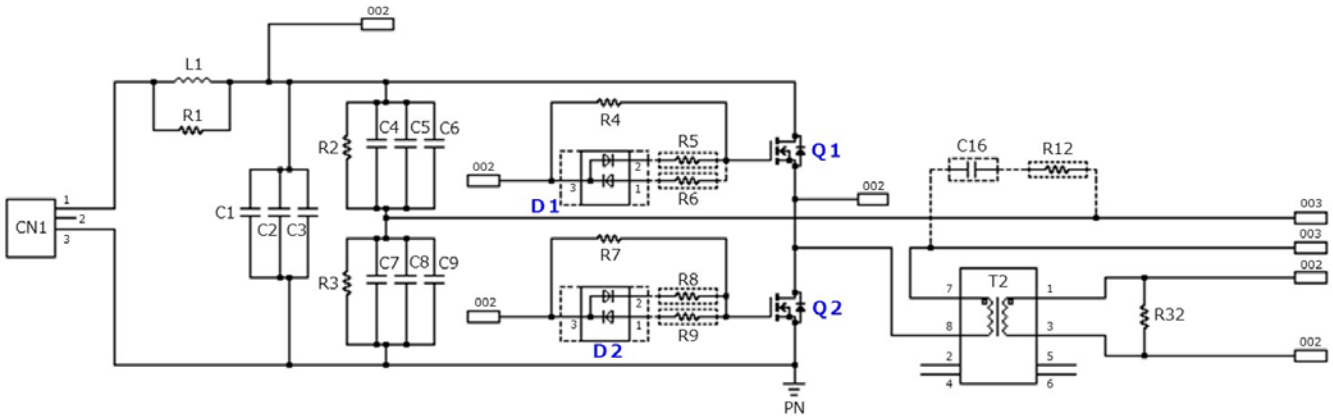


Figure 2.5 Half-bridge circuit 2 (around the MOSFETs on the input side)

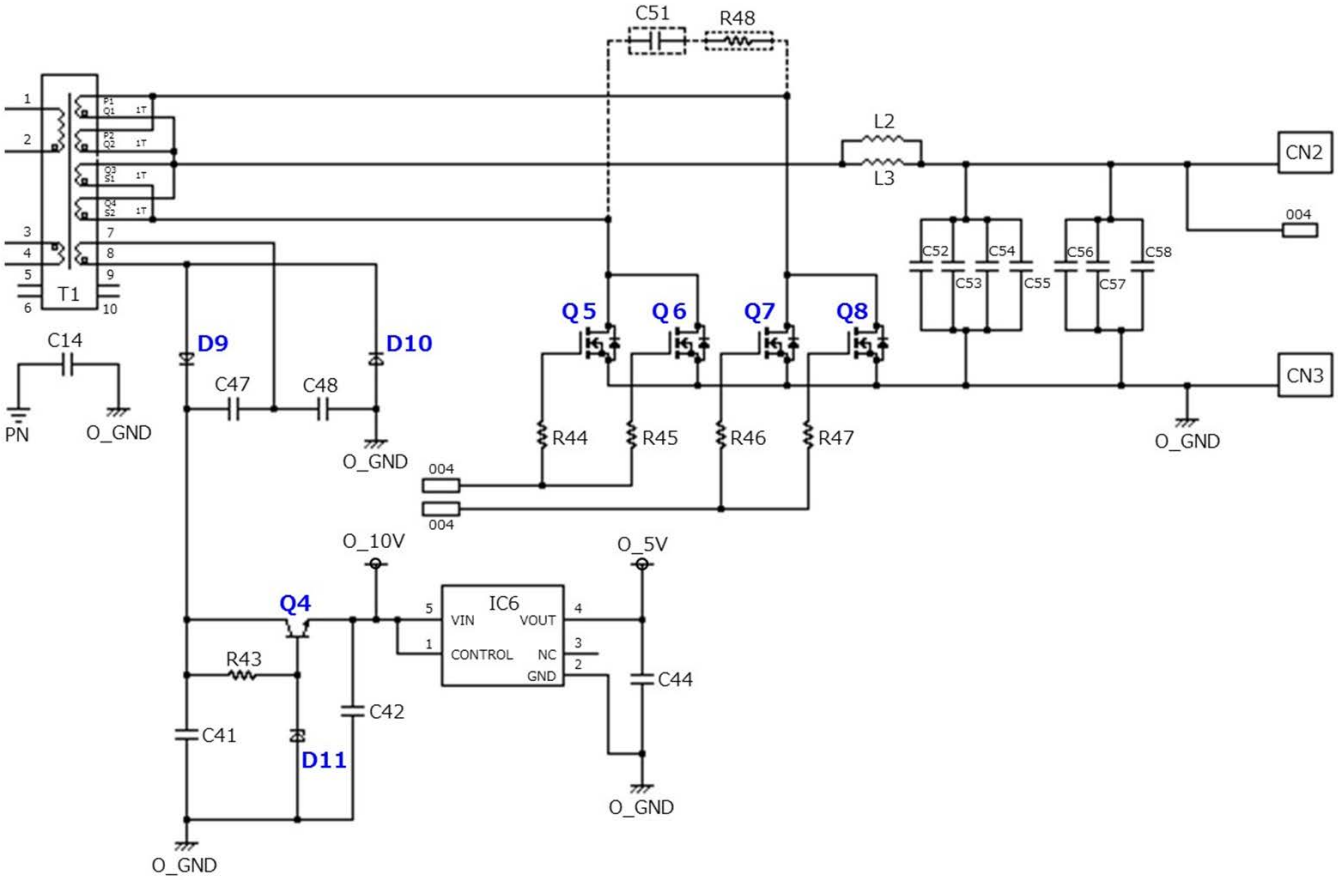


Figure 2.6 Half-bridge circuit 3 (around the synchronous rectification MOSFETs on the output side)

Setting the minimum input operating voltages

The input operating voltage range of this converter can be set with external resistors (R24, and R25) shown in Figure 2.7. The input voltage (V_{in}) is divided by R24, and R25, and the divided voltage is fed to the UVLO pin of the half-bridge PWM controller to set the minimum input operating voltages ($V_{in\_min\_on}$ and $V_{in\_min\_off}$).

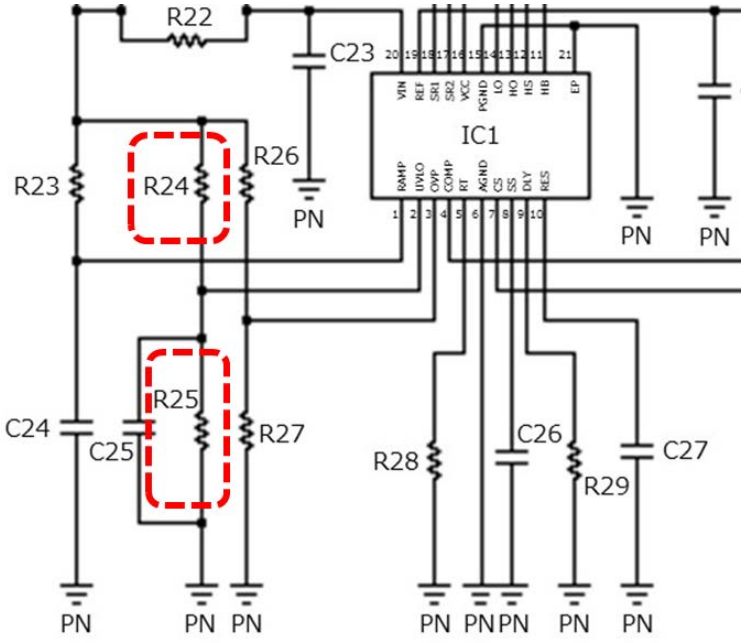


Figure 2.7 Setting the UVLO input voltage range

The UVLO pin voltage is generated by this divided voltage and voltage generated by an internal hysteresis current (23μA). The half-bridge PWM controller enters the active mode when the UVLO pin voltage reaches 1.25V. The internal hysteresis current is disabled once the half-bridge PWM controller enters the active mode. The half-bridge PWM controller shuts down when the UVLO pin voltage drops below the 1.25V threshold. The minimum input operating voltages ($V_{in\_min\_on}$ and $V_{in\_min\_off}$) are calculated by the following equations:

$$\boldsymbol{V_{in\_min\_on}(V) = 1.25(V) \times \frac{(R24 + R25)}{(R25)} + 23(\mu A) \times R24}$$

$$\boldsymbol{V_{in\_min\_off}(V) = 1.25(V) \times \frac{(R24 + R25)}{(R25)}}$$

$V_{in\_min\_on}$ is to be set to 16.05V whereas $V_{in\_min\_off}$ is to be set to 13.75V. In this case, R24 and R25 are calculated to be 100kΩ and 10 kΩ respectively. Figure 2.8 shows the operating modes of the half-bridge PWM controller, depending on the relationship between the input power source voltage (V_{in}) and the UVLO pin voltage.

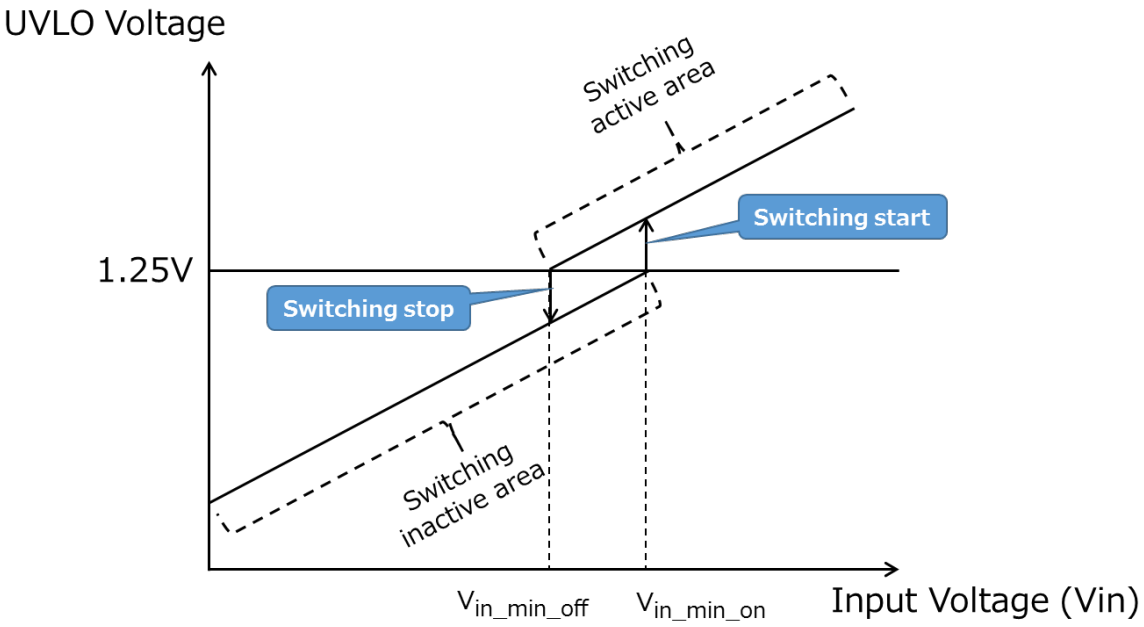


Figure 2.8 Operating modes according to the input power source and UVLO pin voltages

Setting the maximum input operating voltages

The input operating voltage range of this converter can be set with external resistors (R26 and R27) shown in Figure 2.9. The input voltage (V_{in}) is divided by R26, and R27, and the divided voltage is fed to the OVP pin of the half-bridge PWM controller to set the maximum input operating voltages ($V_{in\_max\_on}$ and $V_{in\_max\_off}$).

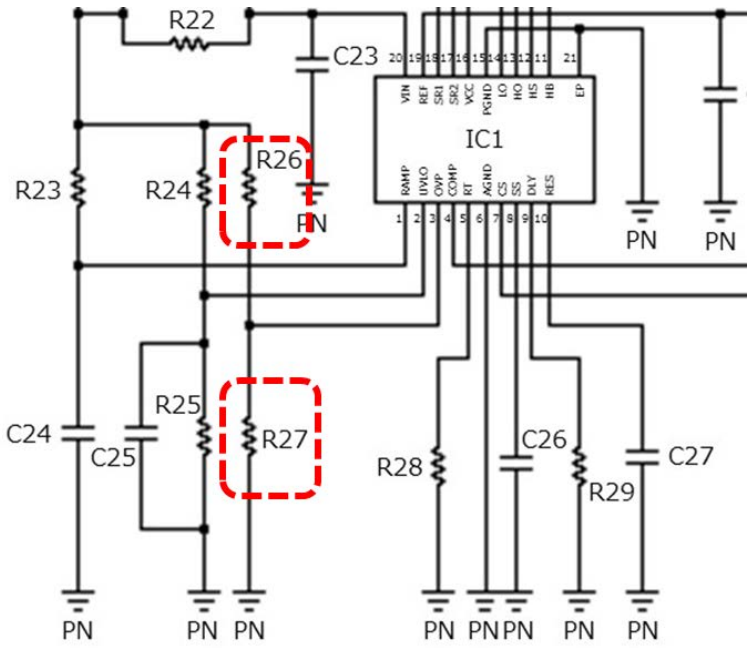


Figure 2.9 Setting the OVP input voltage range

The OVP pin voltage is generated by this divided voltage. The half-bridge PWM controller shuts down when the OVP pin voltage reaches 1.25V. Then, the hysteresis current is enabled, and the half-bridge PWM controller enters active mode when the OVP pin voltage drops below 1.25V. The maximum input operating voltages ($V_{in\_max\_on}$ and $V_{in\_max\_off}$) are calculated by the following equations:

$$\boldsymbol{V_{in\_max\_off}(V) = 1.25(V) \times \frac{(R26 + R27)}{(R27)}}$$

$$\boldsymbol{V_{in\_max\_on}\ (V) = 1.25(V) \times \frac{(R26 + R27)}{(R27)} - 23(\mu A) \times (R26)}$$

$V_{in\_max\_off}$ is to be set to 63.75V whereas $V_{in\_max\_on}$ is to be set to 61.45V. In this case, R26 and R27 are calculated to be 100kΩ and 2.0kΩ, respectively. Figure 2.10 shows the operating modes of the half-bridge PWM controller, depending on the relationship between the input power source voltage (V_{in}) and the OVP pin voltage.

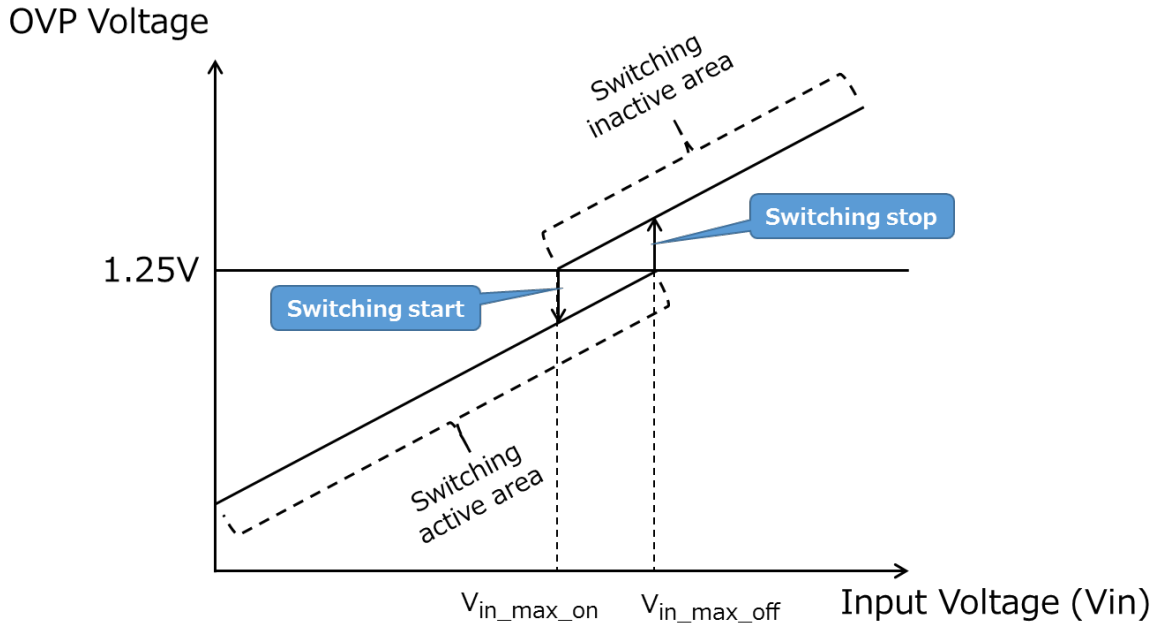


Figure 2.10 Operating modes according to the input power source and OVP pin voltages

Setting the output voltage

The output voltage (V_{out}) of the half-bridge circuit can be set by external resistors (R54, R55, R56, R57, R59, R61, and R65) and a voltage reference (IC8). The LM5035 regulates the photocoupler (IC4) current so that the voltage divided by resistors (R59, R61, and R65) equals the reference voltage (V_{REF}).

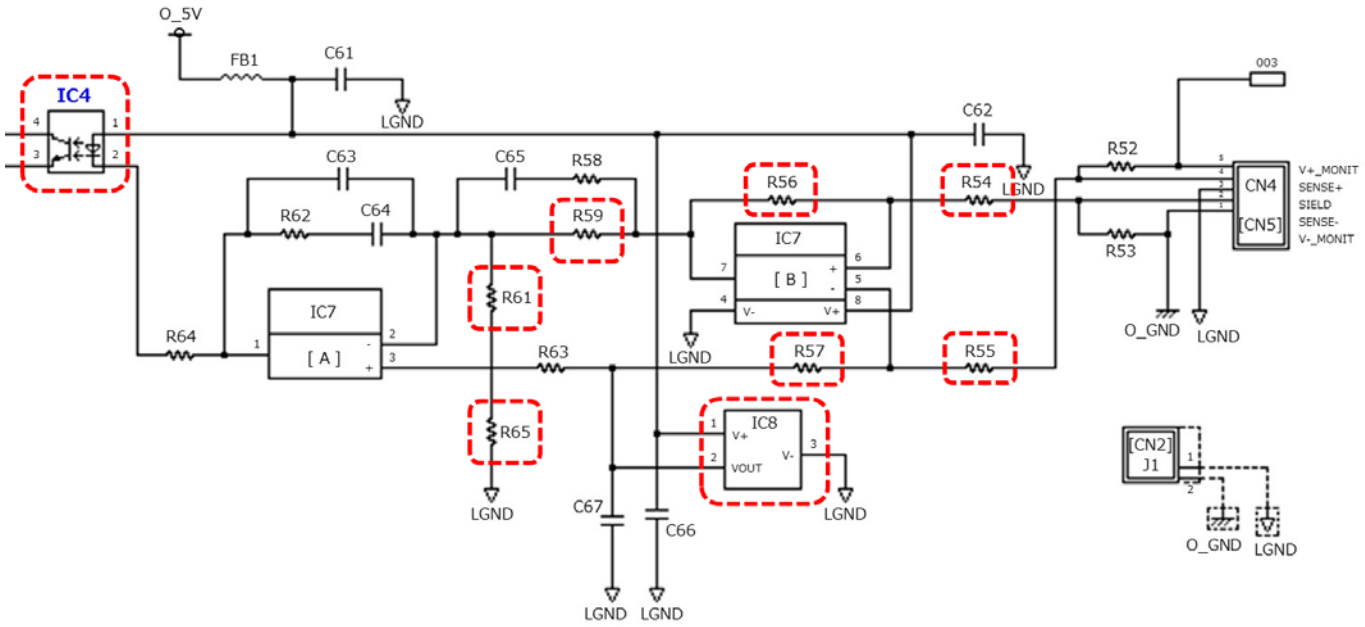


Figure 2.11 Setting the output voltage

The half-bridge PWM controller maintains the output voltage (V_{out}) at a constant level according to the feedback current from the photocoupler (IC4) by controlling the MOSFETs (Q1, Q2, Q5, Q6, Q7, and Q8). If that R54, R55, R56, and R57 are the same resistor with 22kΩ, then the output voltage (V_{out}) is calculated as follows:

$$V_{out}\ (V) = \frac{V_{REF}(V) \times R59}{(R61 + R65)}$$

In this case, the output voltage (V_{out}) is 1.2V, and the reference voltage (V_{REF}) is 1.2V, so R59 is 22kΩ, R61 is 20kΩ, and R65 is 2kΩ resistors.

Setting the switching frequency

The switching frequency (f_{PWM}) of the half-bridge circuit can be set with external resistors (R28).

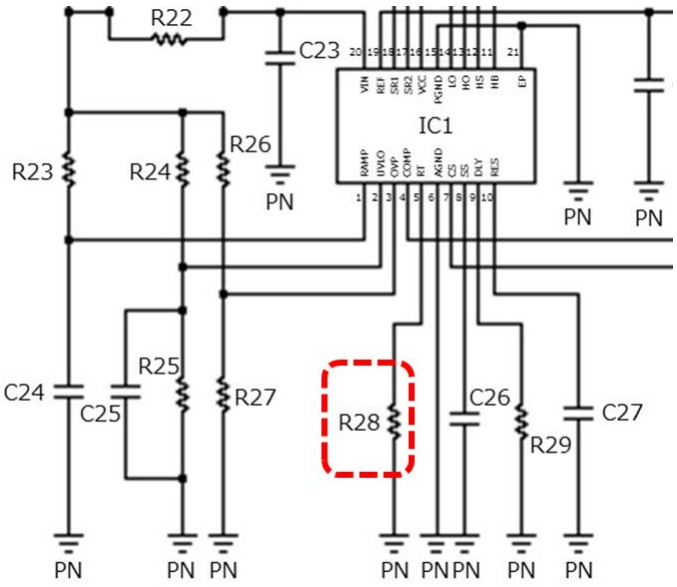


Figure 2.12 Setting the switching frequency

It is calculated by the following equation:

$$f_{PWM}(Hz) = \frac{1}{\left(R28(\Omega)\right) \div (6.25 \times 10^{9}) + 110 \times 10^{-9}}$$

In this case, the switching frequency (f_{PWM}) is to be set to 302kHz, so R28 is calculated to be 20kΩ. The half-bridge PWM controller switches the MOSFETs on the input side (Q1 and Q2) at half the frequency of f_{PWM}. As a result, a ripple voltage at a frequency of f_{PWM} appears at the output.

Current limiter

If the voltage of the CS pin of the half-bridge PWM controller exceeds the current limit threshold of 0.25V, the half-bridge PWM controller controls the MOSFET bridge on the input side to limit the current. Figure 2.5 shows the half-bridge circuit peripheral area of the MOSFET bridge on the input side. The current limiting level (I_limit) is determined by the current limit threshold (0.25V), the value of the current-sensing resistor (R33), the value of the divided resistor (R30 and R31) and the turns ratio of the current transformer (T2).

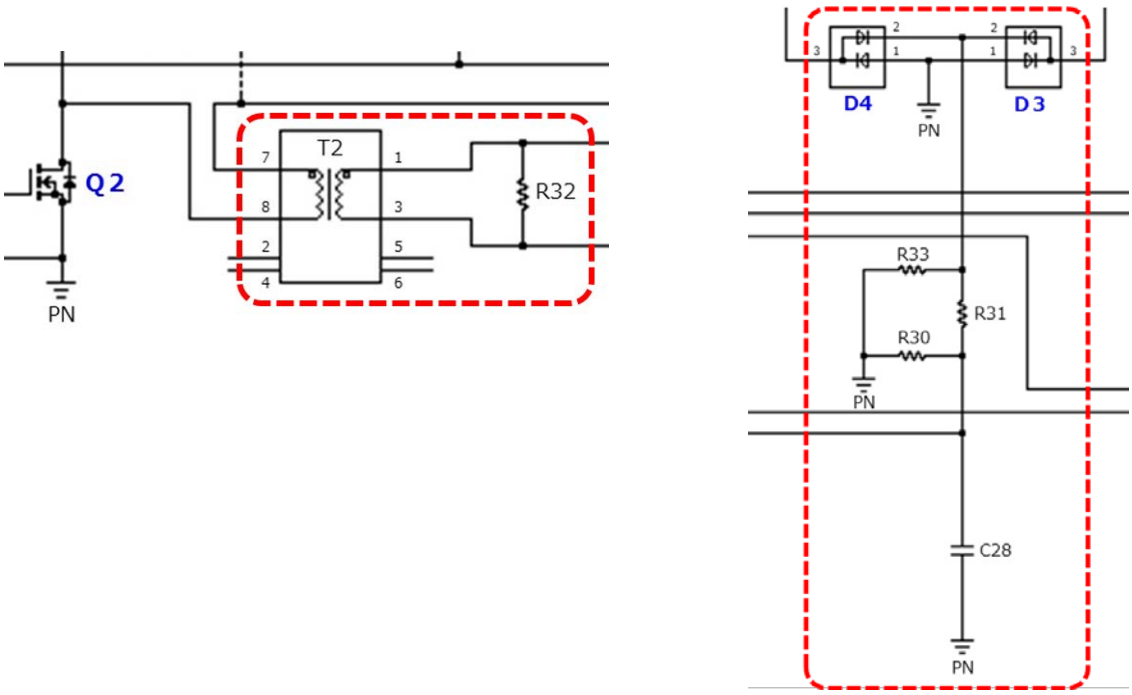


Figure 2.13 Current limiter

The current limiting level is calculated by the following equation:

$$I\_limit = \frac{0.25}{R33 \times (transformer\ turns\ ratio)} \times \frac{R30}{(R30 + R31)}$$

In this case, the current limiting level is 22.7A, so R33 is 2.2Ω, R30 and R31 are 1kΩ, and a current-sense transformer (T2) turn's ratio is 1:100. Actually, it is necessary to adjust the current limiting level using an actual board.

Gate drive circuit

The gate drive circuit affects power efficiency and electromagnetic interference (EMI). In general, there is a trade-off between power efficiency and EMI. Designing a gate drive circuit is a balancing act between power efficiency and EMI. If EMI is considered to be caused by switching noise, determine whether increasing the values of series gate resistors for the Q1 and Q2 MOSFETs (R5, R6, R8, and R9) helps reduce EMI (see Figure 2.14).

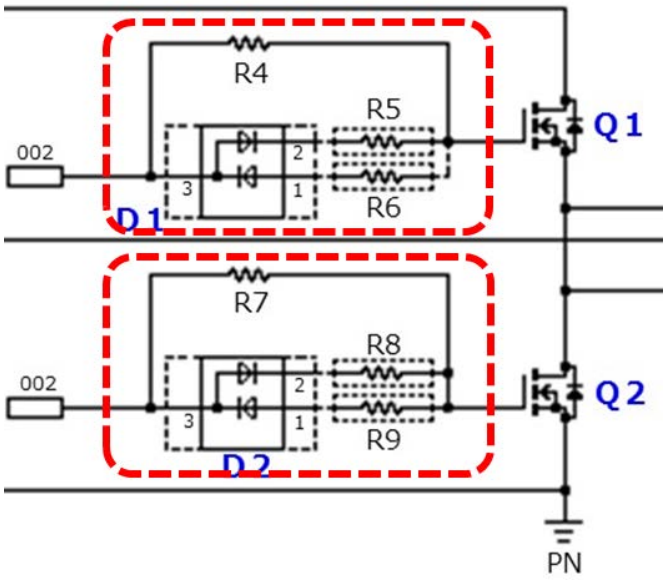


Figure 2.14 Gate drive circuit

The MOSFET turn-on and turn-off times can be adjusted separately. If it is unnecessary to separately adjust the MOSFET turn-on and turn-off times, delete D1, D2, R5, R6, R8, and R9 and use R4 and R7 to adjust the MOSFET switching speeds. The reference design initially sets R4 and R7 to 0Ω and does not have D1, D2, R5, R6, R8, and R9.

Transformer

When the “on” duty cycle on the synchronous rectifier side of a transformer is set to 35% in the static state of the half-bridge circuit, the output voltage is 1.2V and a rectangular wave with an amplitude of 3.4V or so is required on the secondary side. Since one-half of the typical 54.5V input voltage (i.e., 27.25V) is applied across the primary winding, a transformer with a turns ratio of 8:1 should be selected for T1 to generate a 3.4V rectangular wave on the secondary side. To generate supply voltages for the controller on the input side (I_10V), the driver on the output side (O_10V), and the photocoupler (O_5V), a center-tapped transformer having auxiliary windings with a turns ratio of 8:1:1:3:3 should be used for T1. In addition, the isolation voltage between the primary and secondary sides, an increase in the winding temperature, flux saturation, core loss, and other factors should be fully considered. See the bill of materials (RD040-BOM-01) for the specifications of the transformer used in the 1.2V/100A DC-DC converter.

Output smoothing filter

The value of the output capacitor (C_{out}) is selected so that the resulting output voltage ripple (V_{ripple}) meets the required specification. The rectangular waveform that appears at the output side of the transformer (T1) is smoothed by the LC filter comprised of the synchronous rectification coils (L2 and L3) and the output capacitor (C_{out}).

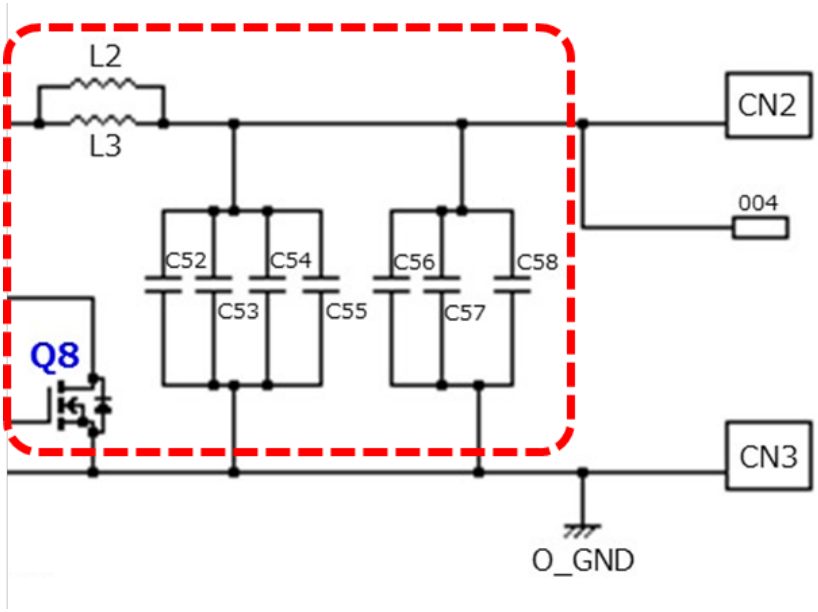


Figure 2.15 Output smoothing filter

The maximum voltage of the rectangular waveform (V_{node}) that appears at the output side of the transformer (T1) is 3.7V when the input voltage is at the maximum value of 59.5V. If the total capacitance of the output capacitor (C_{out}) is 1900μF, then the 302kHz switching frequency is attenuated by roughly -70dB so the output ripple voltage becomes 1.1mV. Actually, the output waveform of the transformer has ripples caused by various factors such as the capacitor's equivalent series resistance (ESR) and equivalent series inductance (ESL). In addition, please be sure to confirm below items:

1. Determine that undershoot and overshoot at the output terminal do not exceed the specified voltage when the load rappidly fluctuates.
2. Determine that the ripple current through the output capacitor does not exceed the permissible limit.
3. Take the tolerance and aging degradation of the output capacitor into consideration.

Reducing the surge voltage on synchronous rectification MOSFETs

If the surge voltage that appears across the output terminals of the transformer (T1) that transfers electrical energy from input to output is excessive, add a snubber circuit as shown in Figure 2.16 to reduce the surge voltage.

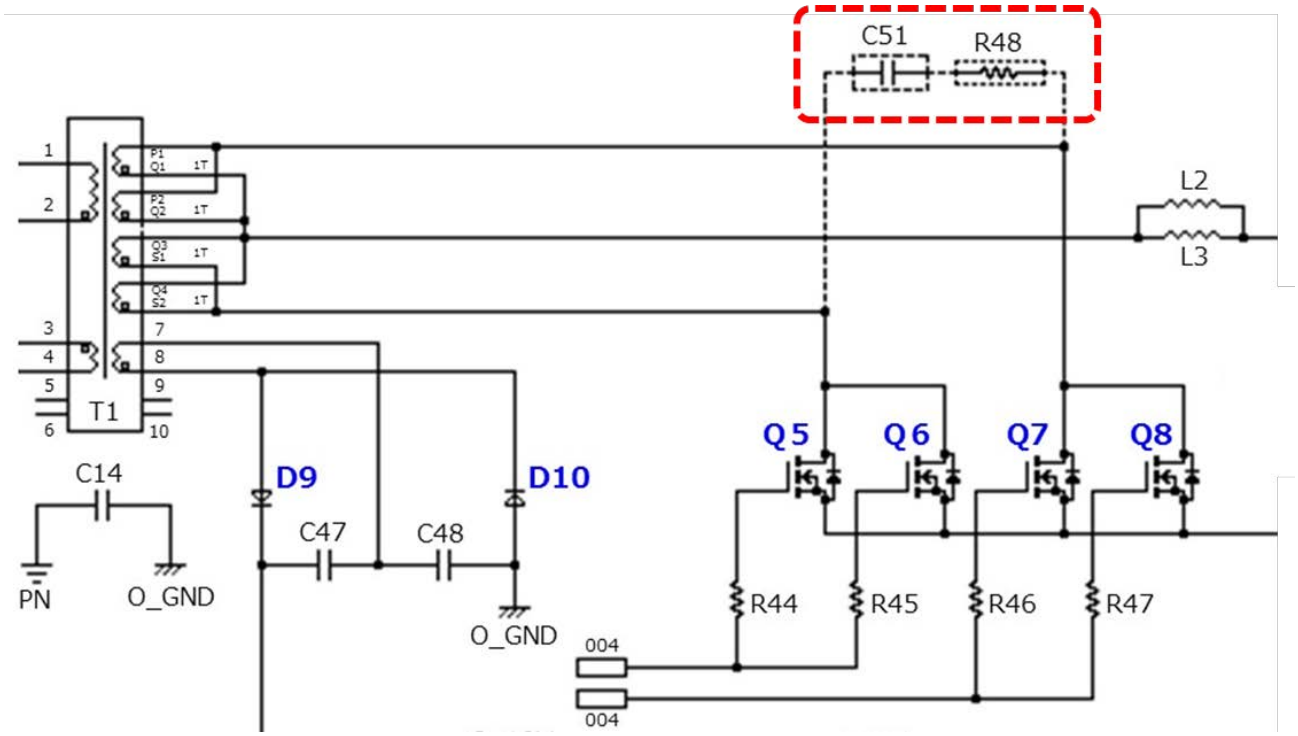


Figure 2.16 Snubber

The snubber circuit is configured of R48 and C51. The RC snubber suppresses the surge voltage (V_{srg}) that occurs across Pin 7 and Pin 10 of T1. At this time, the power loss (P_{d_Rsnb}) by resistor R48 is calculated as:

$$P_{d\_Rsnb} = C51 \times (V_{srg})^2 \times \left(\frac{f_{PWM}}{2}\right)$$

The reference design does not have a snubber circuit as a default. Add a snubber circuit to your application if necessary.

3. PCB design

This section shows considerations for the PCB design for the 1.2V/100A DC-DC converter.

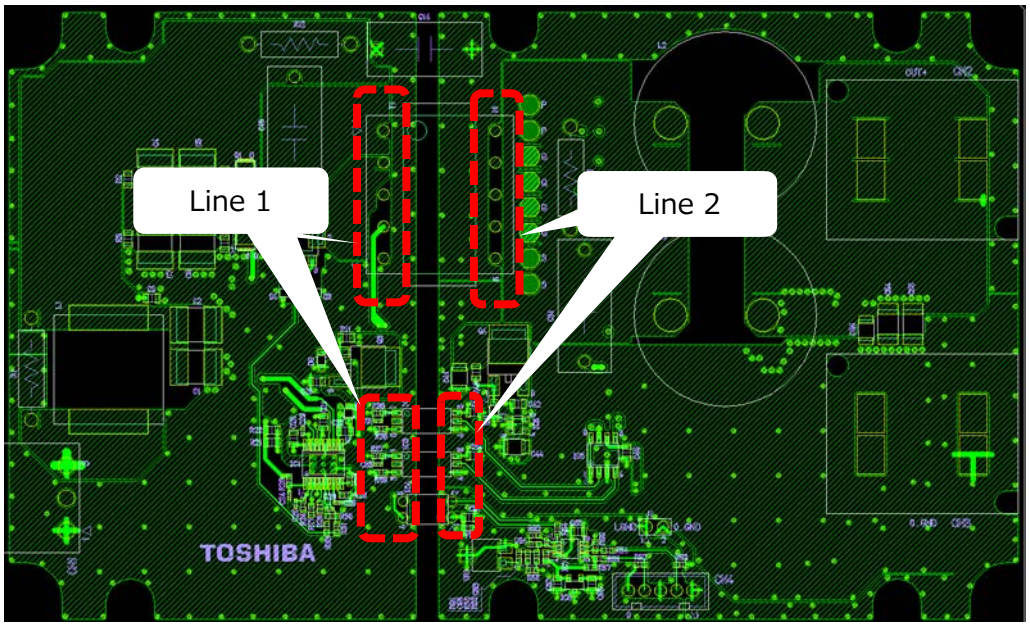
3.1. PCB layout

Creepage distance

Ensure appropriate spatial distance and creepage distances according to the safety standards specified in the required specification. Table 3.1 shows the creepage distances ensured in this converter. The required spatial and creepage distances vary depending on the operating environment, materials, material contamination levels, humidity, altitude (i.e., air pressure), and other factors.

Table 3.1 Minimum creepage distances (design values)

Line 1	Line 2	Creepage distance between Line 1 and Line 2
Input (photocoupler)	Output (photocoupler)	1.4mm
Input (transformer)	Output (transformer)	1.4mm



Current capacity

Each trace on PCB must be wide enough not to cause a temperature rise or IR drop when the maximum current flows through each trace.

3.2. PCB layout for the half-bridge circuit

This subsection shows the considerations for PCB design peripheral area of the half-bridge circuit. Figure 3.1 shows the half-bridge circuit (around the controller). Figure 3.4 and Figure 3.5 show the PCB traces that require special attention in the half-bridge circuit. Refer to the datasheet of the half-bridge PWM controller and the related documents for the guidelines on the layout of peripheral area of the controller.

3.2.1. Considerations for the layout around the controller

1. Place the half-bridge PWM controller (IC1) away from the high-current switching circuit on the secondary side, the transformer, and the reactor.
2. Place the components surrounded by the blue dotted box in Figure 3.1 in the near of the half-bridge PWM controller as shown in Figure 3.2.
3. Provide a single ground plane (PN in Figure 3.1) and connect it to the AGND pin of the half-bridge PWM controller as shown in Figure 3.3.

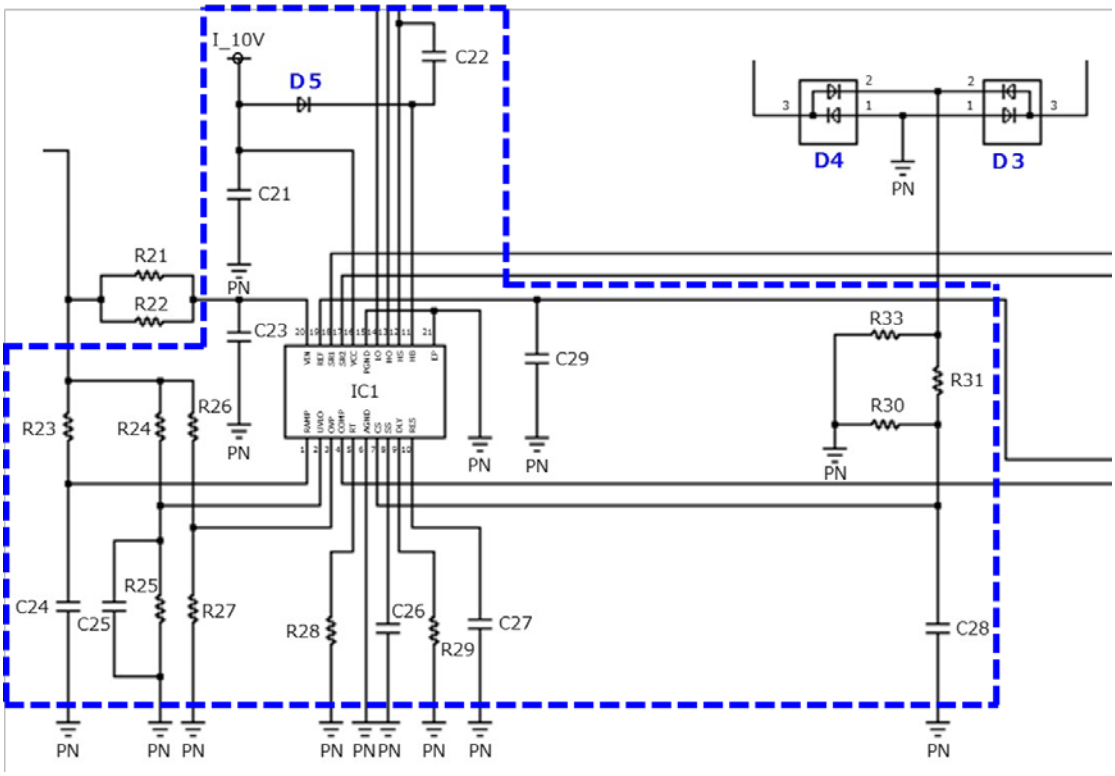


Figure 3.1 Half-bridge circuit (around the controller)

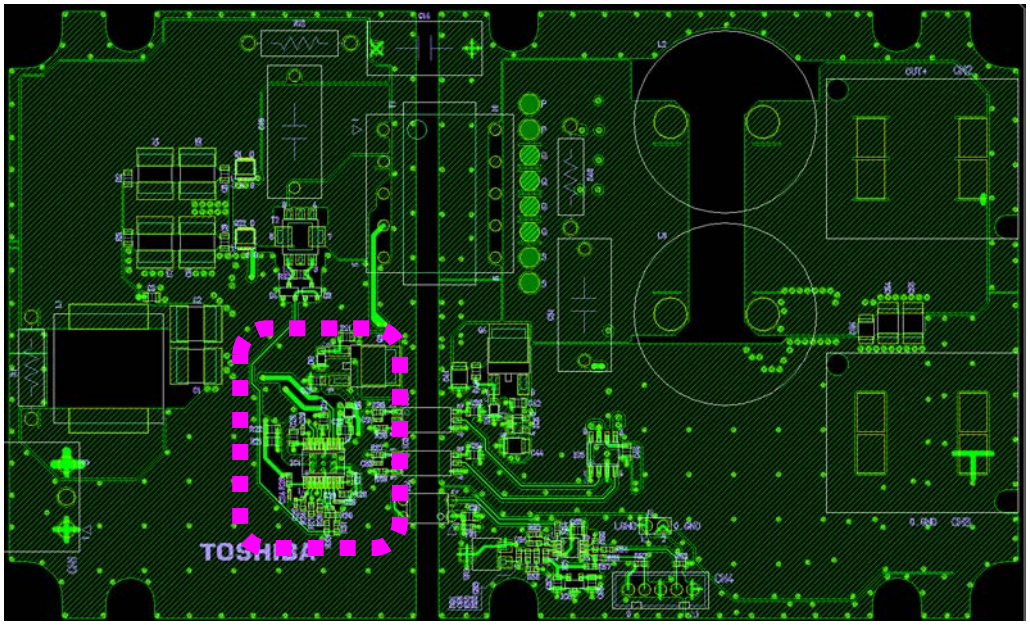


Figure 3.2. Board layout 1

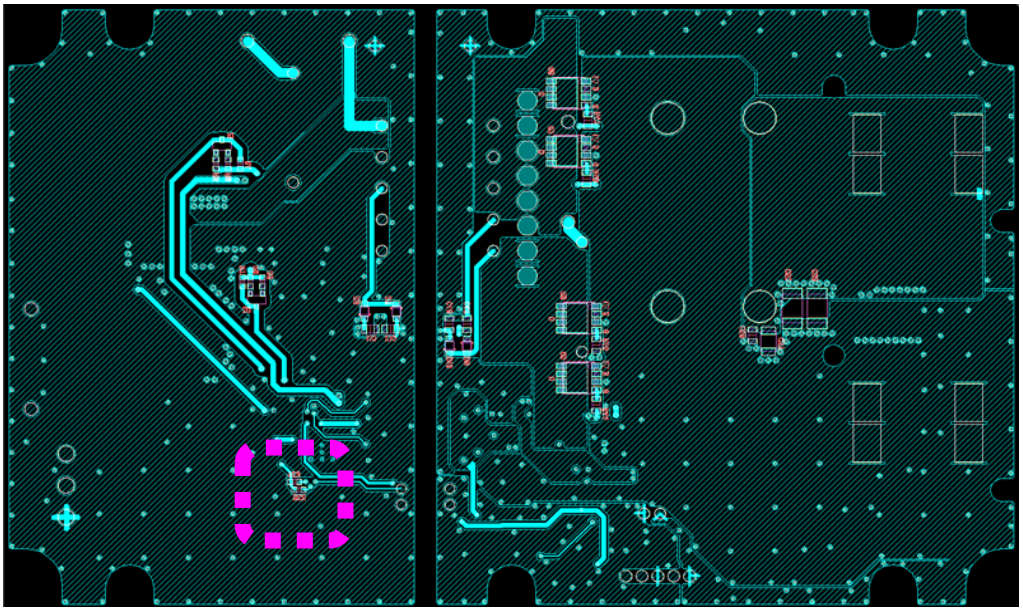


Figure 3.3. Board layout 2

3.2.2. Considerations for the layout around the MOSFETs on the input side

1. Place components in such a manner as to minimize the areas around the switching nodes that are exposed to considerable voltage changes (Line “a” and lines with a voltage change equal to that of Line “a”).
2. Place Q1 and Q2 close to IC1 to minimize the lengths of the driver output lines (“a” and “b” in Figure 3.4) and make them wide enough to be able to conduct the maximum drive current.
3. Decouple the return path of the drive current for Q1 at a position close to its source pin.
4. Decouple the return path of the drive current for Q2 from the GND (PN) plane at a position close to the source pin of Q2, if decoupling is necessary.

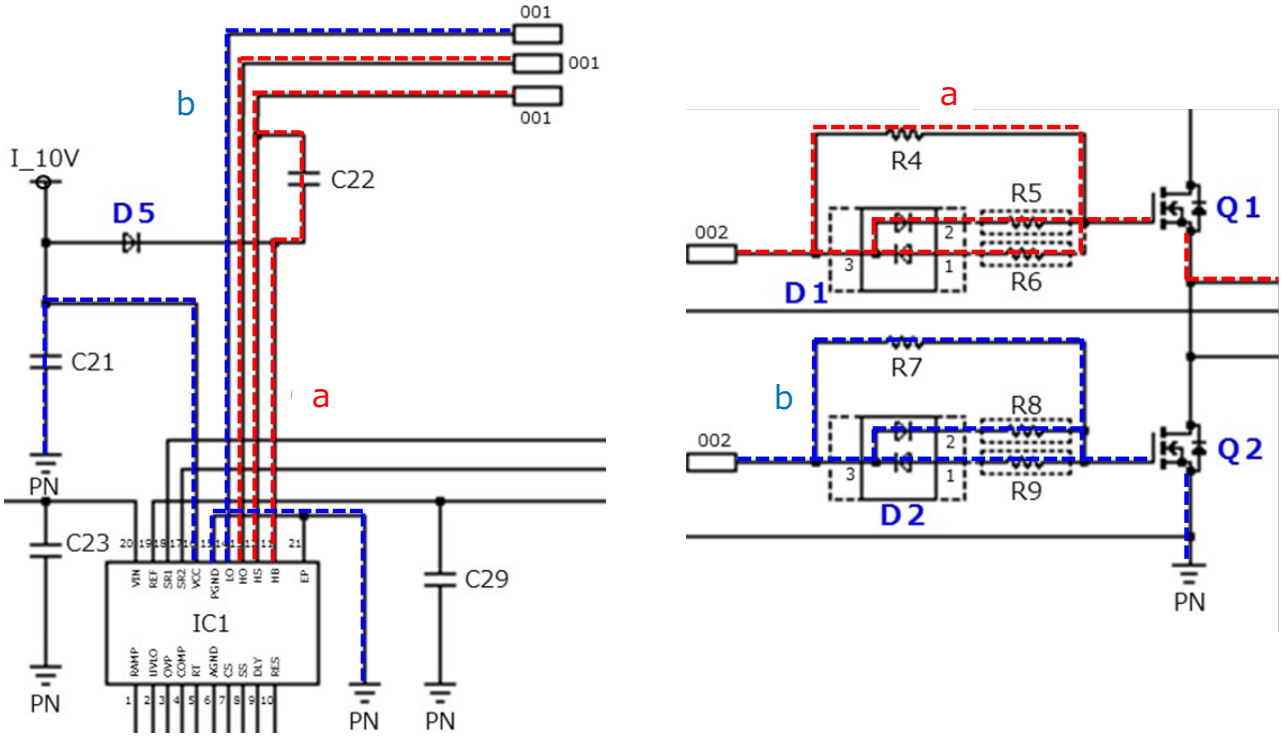


Figure 3.4 PCB layout of the half-bridge circuit requiring special attention

3.2.3. Considerations for the layout around the synchronous rectification MOSFETs on the output side

1. Place Q5, Q6, Q7, and Q8 close to IC5 to minimize the length of the driver output line (“c” in Figure 3.5) and make it wide enough to be able to conduct the maximum drive current.
2. When the GND (O_GND) plane is not used as a return path of the drive current, decouple the drive current at a position close to the source pins of Q5, Q6, Q7, and Q8.
3. Place C51 and R48 that comprise a snubber circuit close to the drain and source pins of Q5, Q6, Q7, and Q8.
4. Place Q5, Q6, Q7, and Q8 close to T1 to minimize the lengths of the loops between the transformer and the synchronous rectification MOSFETs.

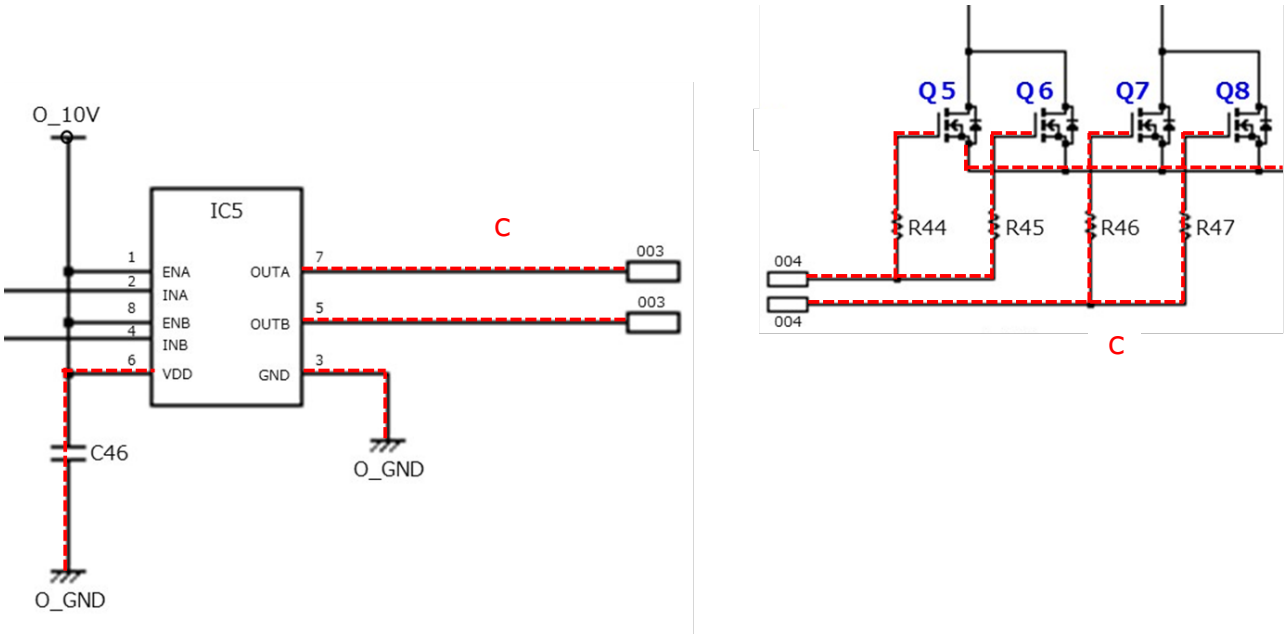


Figure 3.5 PCB layout of the half-bridge circuit requiring special attention

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