Phase-Shift Full Bridge (PSFB) AC-DC Power Supply Basic Simulation Circuit

Reference Guide

RD039-RGUIDE-02

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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1. Introduction

Most of the internal circuits in information and communication equipment, home appliances, and other electrical devices work on DC voltage. Since they cannot work on commercial power (AC voltage) directly, it is necessary to convert AC voltage to DC voltage. An AC-DC power supply is used for this purpose. In some cases, an external AC-DC power supply is installed to an actual applications. In other cases, it is embedded in an actual applications and therefore invisible from outside.

AC-DC power supplies have basically two categories: transformer-based AC-DC power supplies and switched-mode AC-DC power supplies. A transformer-based AC-DC power supply works stepping down the AC voltage through a transformer without changing its frequency, converting the negative portion of each AC cycle to positive voltage through a diode bridge (rectifier bridge), and smoothing out the DC voltage with a capacitor. A very large, heavy transformer that operates at the AC voltage frequency (50 or 60Hz) adds size and weight to the transformer-based AC-DC power supply. A switched-mode AC-DC power supply works rectifying AC voltage to DC voltage, switching the DC voltage at a frequency around 10kHz to 100kHz (much higher than the commercial power frequency), and passing it through a transformer to change the output voltage. The final output DC voltage is controlled by the on/off periods of switching devices. Power transmission at a high frequency allows the use of a small, lightweight transformer, making it possible to reduce the size and weight of an AC-DC power supply. So switched-mode AC-DC power supplies are commonly used nowadays.

Figure 1.1 shows typical block diagram of a switched-mode AC-DC power supply, which consists of four blocks: 1) input filter, 2) rectifier bridge, 3) DC-DC converter, and 4) feedback circuit. The function of each of these blocks is briefly explained below:

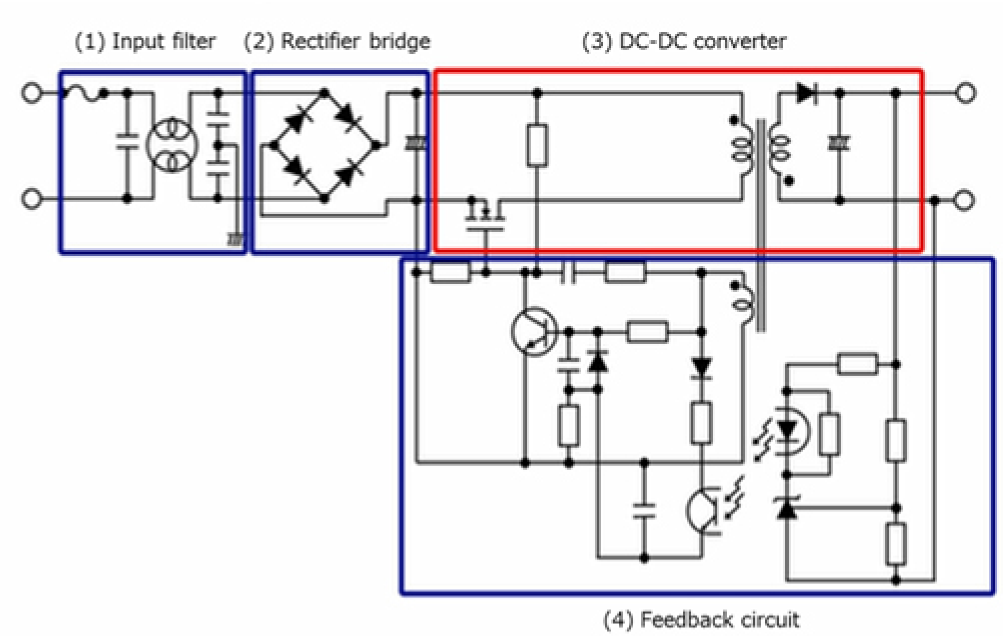


Figure 1.1 Block diagram of a switched-mode AC-DC power supply

(1) Input filter

The input filter prevents noise generated by the switched-mode AC-DC power supply to the commercial power line.

(2) Rectifier bridge

The rectifier bridge rectifies the input AC voltage into a first DC voltage and passes it to the DC-DC converter. The configuration consisting of a rectifier bridge and a capacitor as shown in Figure 1.1 degrades the power factor. In recent years, a power factor correction (PFC) circuit is typically inserted in the rectifier bridge to prevent power factor degradation. Toshiba also offers a basic simulation circuit of a PFC power supply together with a reference design:

For a basic simulation circuit of a PFC power supply → Click Here

(3) DC-DC converter

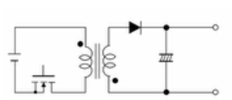
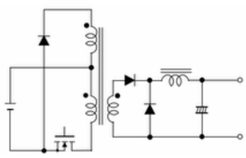
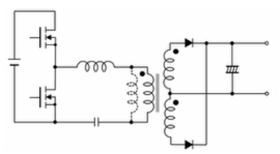
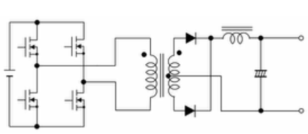
The DC-DC converter converts the rectified voltage to an intermediate DC voltage.

(4) Feedback circuit

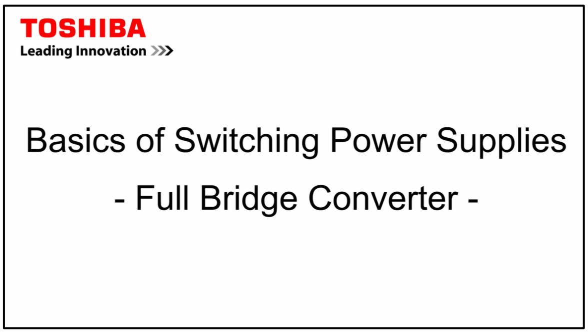
The on/off periods of the switching devices are controlled to generate a desired output voltage.

A switched-mode AC-DC power supply rectifies the AC input voltage into a first DC voltage and converts it to a desired DC voltage through a DC-DC converter. Many topologies exist for the implementation of a DC-DC converter. Table 1.1 shows the most common topologies and their characteristics.

Table 1.1 Commonly used DC-DC converter topologies and their characteristics

Topology		Power Level	Advantage	Disadvantage
Flyback		<120W	• Small part count	• Decrease in efficiency at high power • Large transformer
Forward		100W to 500W	• Higher efficiency than a flyback circuit	• Requires a transformer reset circuit
Resonant half-bridge (LLC resonance)		100W to 1.6kW	• High efficiency • Low noise	• Requires a custom-designed transformer • Difficult to control
Full-bridge		>1kW	• High efficiency • Capable of increasing the power capacity	• Large part count • Difficult to control

A video describing the basic operation of a Full-bridge converter is available for viewing on Toshiba's website.



Full-bridge DC-DC converters require four switching devices on the primary side of it, increasing the number of parts and the complexity of switching control required. However, the full-bridge topology provides higher conversion efficiency than other topologies and makes it possible to create high-capacity DC-DC converters. This reference guide focuses on Phase-Shift Full Bridge (PSFB) DC-DC converters that contain zero-voltage switching (ZVS) circuitry, which turns each switching device on and off when the voltage reaches zero. Because of their low switching loss, PSFB DC-DC converters are widely used for server power supply and other applications requiring high efficiency and power density. A basic simulation circuit of a PSFB DC-DC converter (RD039-SPICE-01) is available for download on Toshiba's website, which will help you understand its operation in switched-mode AC-DC power supplies.

The Reference Guide provides an overview of this simulation circuit and describes its usage. OrCAD® Capture and PSpice® A/D from Cadence are necessary to simulate this circuit. Both the simulation circuit and the Reference Guide are based on OrCAD® Capture 17.2.

2. Overview of the PSFB AC-DC power supply

The basic simulation circuit (RD039-SPICE-01) is a PSFB DC-DC converter for a 1.6kW AC-DC power supply. The assumption is that it receives DC voltage after the input AC voltage is converted to DC voltage by a rectifier bridge and a Power Factor Correction (PFC) circuit.

2.1. Power supply specifications

The specifications of the PSFB AC-DC power supply are as follows:

・Input voltage: 380V
・Output voltage: 12V
・Output current: 0 to 133A
· Secondary-MOSFET operating frequency: 120kHz
· Transformer turns ratio: 20:1:1
· Primary-side resonant inductor: 37μH
· Allowable secondary-side peak-to-peak ripple current: 20% of the input current

2.2. Circuit configuration

Figure 2.1 shows the simulation circuit for OrCAD®. It is a PSFB AC-DC power supply, which mainly consists of a power supply section (PSFB circuit) and a PWM controller. The secondary side of the transformer in the PSFB circuit is synchronous rectifier circuit using MOSFET. The PWM controller is a general-purpose controller with a MOSFET gate driver, which was prepared to create this PSFB AC-DC power supply. The PSFB circuit uses the TK25N60X5 and TPH3R70APL as switching MOSFETs.

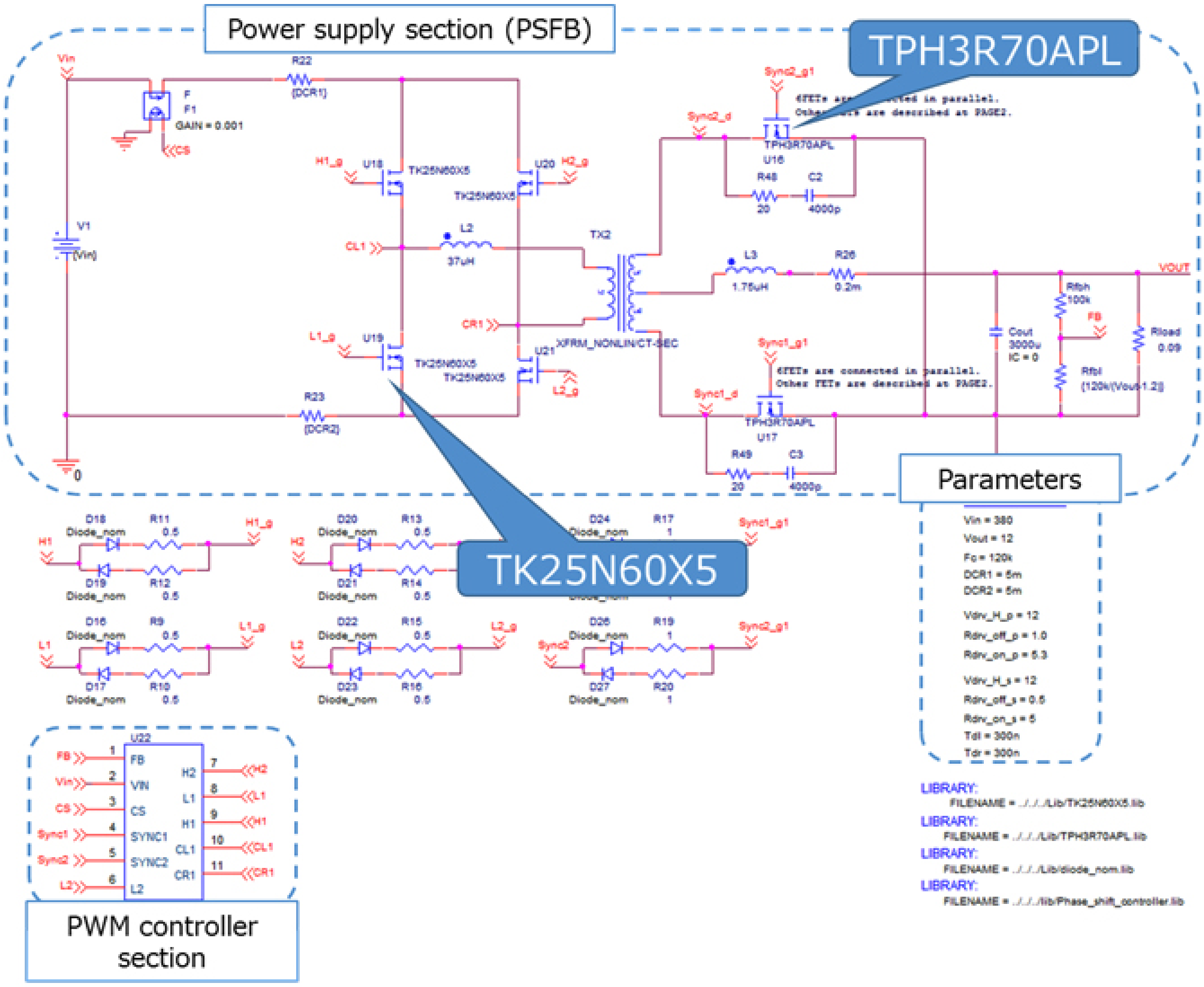


Figure 2.1 Simulation circuit of a 1.6kW PSFB AC-DC power supply

Selection of the primary-side MOSFET

The primary-side MOSFET (TK25N60X5: V_{DSS}=600V, I_D=25A) was selected, taking the following into consideration:

1. Withstand voltage

The static voltage applied to the primary-side MOSFETs is equal to the input voltage of the PSFB AC-DC power supply (380V). Therefore, a MOSFET with a withstand voltage of 600V or higher was selected for the simulation circuit, considering voltage surge that occurs during switching.

(2) Body diode characteristics

A MOSFET with a high-speed body diode was selected because resonant inductor (L) current flows through the body diode of the MOSFET during the freewheeling period.

(3) Current rating

The PSFB AC-DC power supply has the maximum input current when the output power has the maximum value. Suppose that the PSFB AC-DC power supply has a conversion efficiency of 90% at the maximum output power of 1.6kW, then the maximum input current is calculated to be 4.7Arms. Therefore a MOSFET with a current rating of 10A or higher was selected.

Selection of the secondary-side MOSFET

The secondary-side MOSFET (TPH3R70APL with a V_{DSS} of 100V and an I_D of 90A) was selected, taking the following into consideration:

1. Withstand voltage

Since the transformer turns ratio is 20:1, the static voltage across the midpoint of the secondary winding and each end of it is equal to 1/20th of the input voltage, i.e., 19V. A voltage equal to twice this voltage (38V) is applied to each MOSFET on the secondary side. A MOSFET with a withstand voltage of 100V or higher was selected, considering voltage surge that occurs during transformer current switching.

2. Current rating

The PSFB AC-DC power supply has the maximum input current when the output power has the maximum value. At the maximum output power of 1.6kW, the maximum output current (133A) is shared by two phases equally, so 67A is applied per phase. Suppose that six parallel MOSFETs are used per phase to accommodate a large current and conduction loss, then each MOSFET conducts an average of roughly 11A, so a MOSFET with a current rating of 25A or higher is necessary. In addition, it is important to select a MOSFET with as low on-resistance as possible, prioritizing a reduction in conduction loss.

Selection of an output inductor

The following paragraphs describe how to select an inductor on the secondary side. The value of the output inductor to be used in the simulation circuit can be calculated from the following power supply parameters:

- Input voltage: V_{in} (V)
- Transformer turns ratio: n
- Output voltage: V_{out} (V)
- Power conversion efficiency: η (%)
- Switching frequency: F_c (Hz)
- Maximum output current: I_{out_max} (A)
- Allowable peak-to-peak ripple current: ΔI_{ripple} (%)

The value of the output inductor (L_o) can be calculated as follows:

$$I_{out\_max} \times \Delta I_{ripple} \times 0.01 = \frac{\left(\frac{V_{in}}{n} - V_{out}\right) \times V_{out}}{\frac{V_{in}}{n} \times F_c \times L_o \times \eta}$$

where, the input voltage (V_{in}) is 380V, the transformer turns ratio (n) is 20, the output voltage (V_{out}) is 12V, the switching frequency (F_c) is 120kHz, the maximum output current (I_{out_max}) is 133A, and the allowable peak-to-peak ripple current (ΔI_{ripple}) is 20% according to the power supply specifications. Suppose that the conversion efficiency (η) at the maximum output is 90%, then the output inductance (Lo) is calculated to be 1.54μH, so Lo is set to 1.75μH in the simulation circuit.

In practice, the value of the inductor varies because of DC bias characteristics. Select an inductor that exhibits an inductance greater than the result of the above equation even when the inductance decreases because of DC bias characteristics.

3. Simulation results

This section shows the simulation waveforms at the points (1) to (3) shown in Figure 3.1.

(1) Basic operation of the PSFB DC-DC converter (drain-source voltage of the primary-side MOSFETs, and voltage and current of the output inductor)

(2) Synchronous rectification operation on the secondary side (drain-source voltage of the secondary-side MOSFETs, and voltage and current of the output inductor)

(3) Output voltage and current from the AC-DC power supply

The simulation circuit model also allows you to view other waveforms. See Section 5 for how to view waveforms.

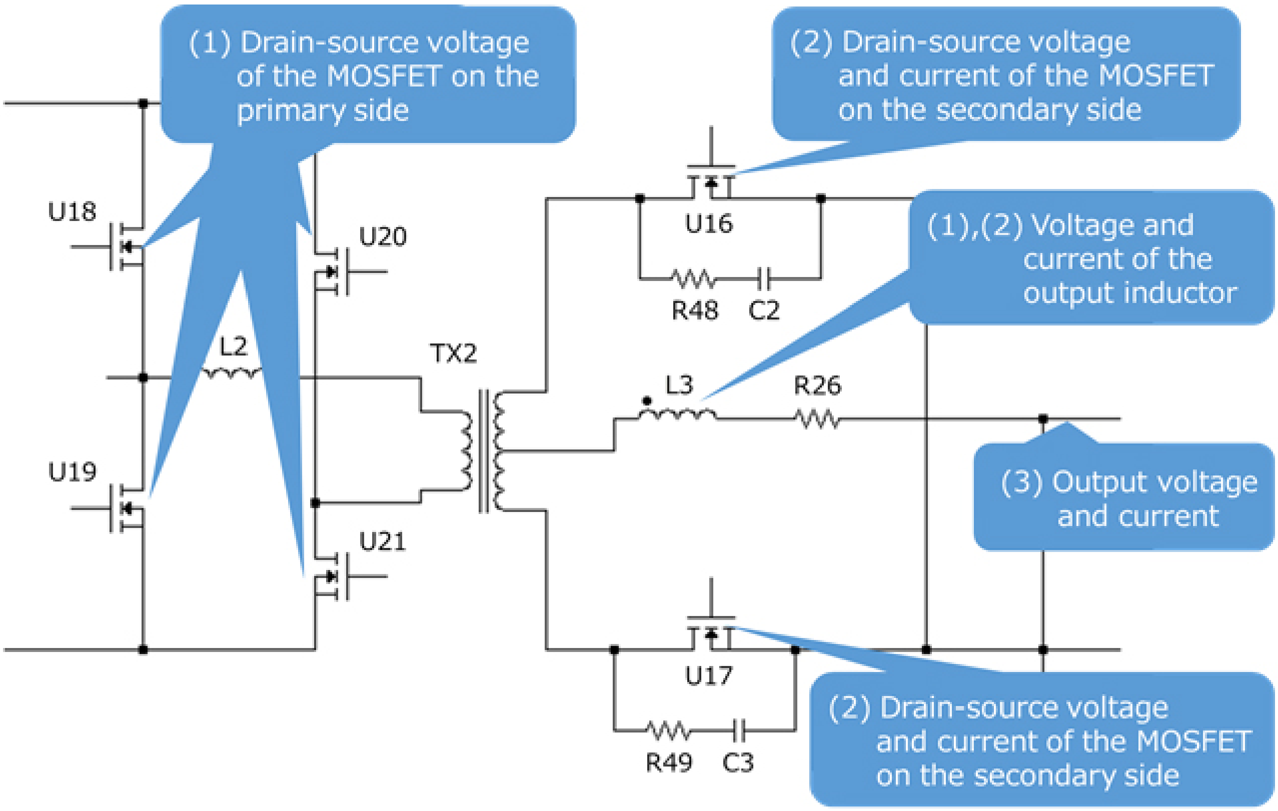


Figure 3.1 Points at which simulation waveforms are measured

(1) Basic operation of the PSFB DC-DC converter

The following describes the basic operation of the PSFB DC-DC converter using the circuit shown in Figure 3.2.

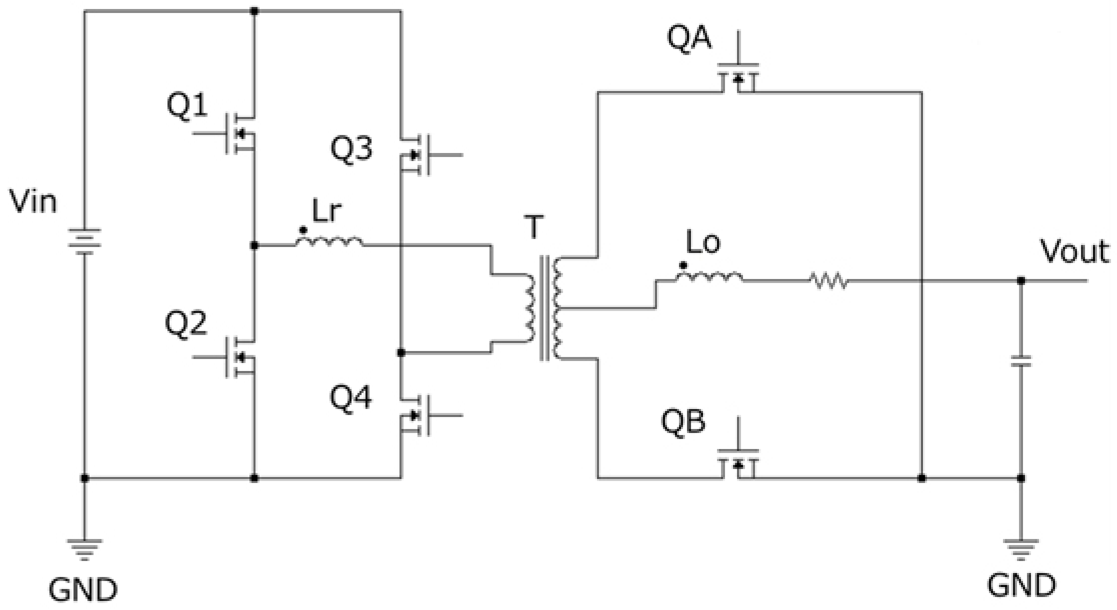


Figure 3.2 PSFB circuit

As shown in Figure 3.2, we put on the label of primary-side MOSFETs as Q1 to Q4, the resonant inductor as Lr, the secondary-side MOSFETs as QA and QB, and the output inductor as Lo. In general, the Q1-Q2 pair is called the leadingt leg whereas the Q3-Q4 pair is called the lagging leg. The PSFB DC-DC converter generates output voltage control by shifting the phase between each leg which upper and lower MOSFET switches on and off state with 50% duty cycle.

Its operation during each on and off period is outlined below.

a. Q1: ON, Q4: ON

During this period, the transformer transfers electric power from the primary side to the secondary side.

At this time, the primary-winding voltage is equal to the input voltage (V_{in}). The side with a polarity dot is positive. Voltage is induced in the secondary winding of the transformer according to its turns ratio:

$$n \times V_{in}$$

This causes current to flow to Lo via QB.

b. Q1: ON (dead-time period of the lagging leg).

At this period, Q4 turns off. Current continues flowing through Lr in the same direction, discharging the output capacitance (C_{oss}) of Q3 and charging C_{oss} of Q4. When the output capacitance of Q3 is fully discharged during this period, its drain-source voltage becomes zero, causing the turn-on of Q3 during next period to be zero-voltage switching (ZVS). When the above discharging and charging are completed, the current flow to Q4 stops, while current flows through the body diode of Q3. On the secondary side, the electric power stored in Lo freewheels through QB.

c. Q1: ON, Q3: ON

At the beginning of this period, Q3 turns on. The electric power stored in Lr and Lo freewheels during this period.

Q3 performs ZVS; i.e., it turns on with its drain-source voltage being zero. The freewheel current on the primary side flows through Q1 and Q3 whereas the freewheel current on the secondary side passes through QB.

d. Q3: ON (dead-time period of the leading leg).

At this period, Q1 turns off. Current continues flowing through Lr in the same direction, charging the output capacitance (Coss) of Q1 and discharging Coss of Q2.

When the output capacitance of Q2 is fully discharged during this period, its drain-source voltage becomes zero, causing the turn-on of Q2 during next period to be ZVS. When the above discharging and charging are completed, the current flow to Q1 stops, while current flows through the body diode of Q2. The freewheel current on the secondary side flows through QB.

e. Q2: ON, Q3: ON

At the beginning of this period, Q2 turns on. The electric power stored in Lr and Lo freewheels during this period.

Q2 performs ZVS; i.e., it turns on with its drain-source voltage being zero. The freewheel current on the primary side flows through Q2 and Q3 whereas the freewheel current on the secondary side passes through QA and QB. When the electric power stored in Lr is fully consumed, the current direction through Lr reverses, causing the operation of the PSFB DC-DC converter to transition to the next period.

f. Q2: ON, Q3: ON

During this period, the transformer transfers electric power from the primary side to the secondary side.

The direction of the current flow on the primary side during this period is opposite to that during period a. The side with the polarity dot is now negative, and a voltage is induced in the secondary winding of the transformer according to its turn ratio:

$$n \times V_{in}$$

This causes current to flow to Lo via QA.

g. Q2: ON (dead-time period of the lagging leg).

At this period, Q3 turns off. Current continues flowing through Lr in the same direction, charging the output capacitance (Coss) of Q3 and discharging Coss of Q4.

When the output capacitance of Q4 is fully discharged during this period, its drain-source voltage becomes zero, causing the turn-on of Q4 during next period to be ZVS. When the above discharging and charging are completed, the current flow to Q3 stops, while current flows through the body diode of Q4. On the secondary side, the electric power stored in Lo freewheels through QA.

h. Q2: ON, Q4: ON

At the beginning of this period, Q4 turns on. The electric power stored in Lr and Lo freewheels during this period.

Q4 performs ZVS; i.e., it turns on with its drain-source voltage being zero. The freewheel current on the primary side flows through Q2 and Q4 whereas the freewheel current on the secondary side passes through QA.

i. Q4: ON (dead-time period of the leading leg).

At this period, Q2 turns off. Current continues flowing through Lr in the same direction, discharging the output capacitance (Coss) of Q1 and charging Coss of Q2.

When the output capacitance of Q1 is fully discharged during this period, its drain-source voltage becomes zero, causing the turn-on of Q1 during next period to be ZVS. When the above discharging and charging are completed, the current flow to Q2 stops, while current flows through the body diode of Q1. The freewheel current on the secondary side flows through QA.

j. Q1 and Q4 are on.

At the beginning of this period, Q1 turns on. The electric power stored in Lr and Lo freewheels during this period.

Q1 performs ZVS; i.e., it turns on with its drain-source voltage being zero. The freewheel current on the primary side flows through Q1 and Q4 whereas the freewheel current on the secondary side passes through QA and QB. When the electric power stored in Lr is fully consumed, the current direction through Lr reverses, causing the operation of the PSFB DC-DC converter to transition to the next period.

Steps a to j are repeated.

The output voltage is controlled by adjusting the periods of a and f during which electric power is transferred from the primary side to the secondary side of a transformer (i.e., the periods during overlapping those phases).

Figure 3.3 shows the waveforms of the drain-source voltage of each MOSFET on the primary side and the voltage and current waveforms of the output inductor. It shows that voltage is applied across the output inductor during periods a and c, causing electric power to be transferred from the primary side to the secondary side.

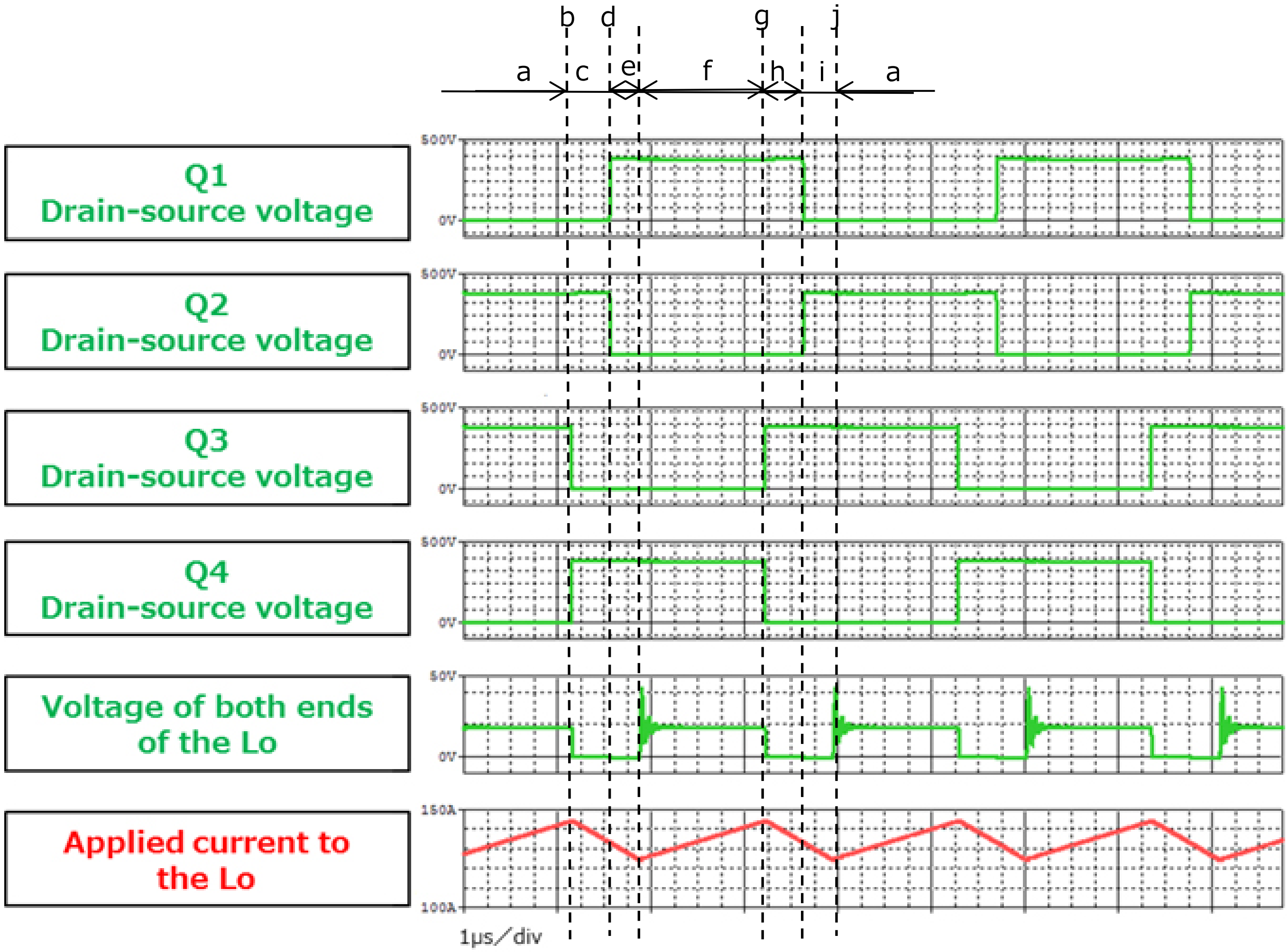


Figure 3.3 Waveforms of the drain-source voltage of the primary-side MOSFETs and the voltage and current waveforms of the output inductor

(2) Synchronous rectification operation on the secondary side

The simulation circuit uses a MOSFET synchronous rectifier circuit on the secondary side instead of a diode rectifier circuit. Generally, the conduction loss caused by the on-resistance of a MOSFET is lower than the conduction loss due to the forward voltage of a diode, so the synchronous rectification circuit helps reduce conduction loss. The larger the output current, the more effective it is in reducing conduction loss. Synchronous rectification circuits are commonly used for applications that require high efficiency and output power.

The operations of the secondary-side MOSFETs during each on-off period are outlined below.

a. QB: ON

The side with the polarity dot is positive. Voltage is induced in the secondary winding of the transformer according to its turn ratio:

$$n \times V_{in}$$

This causes current to flow to Lo via QB.

b–d. QB: ON

The electric power stored in Lo freewheels through QB.

e. QA: ON, QB: ON

The electric power stored in Lo freewheels through QA and QB.

f. QA: ON

The side with the polarity dot is now negative. Voltage is induced in the secondary winding of the transformer according to its turn ratio:

$$n \times V_{in}$$

This causes current to flow to Lo via QA.

g–i. QA is on.

The electric power stored in Lo freewheels through QA.

j. QA and QB are on.

The electric power stored in Lo freewheels through QA and QB.

Figure 3.4 shows the waveforms of the drain-source voltage and drain current of each MOSFET on the secondary side and the voltage and current waveforms of the output inductor. It shows that the secondary-side MOSFETs turn on, causing current to flow.

Period a (period f) begins when the current direction reverses on the primary side of the transformer. At this time, large surge voltage happens across the drain and source terminals. The simulation circuit contains an RC snubber circuit between the drain and source terminals as a surge suppressor. For selecting the type of surge suppressor and the devices used, it is necessary to evaluate operating waveforms using an actual printed circuit board.

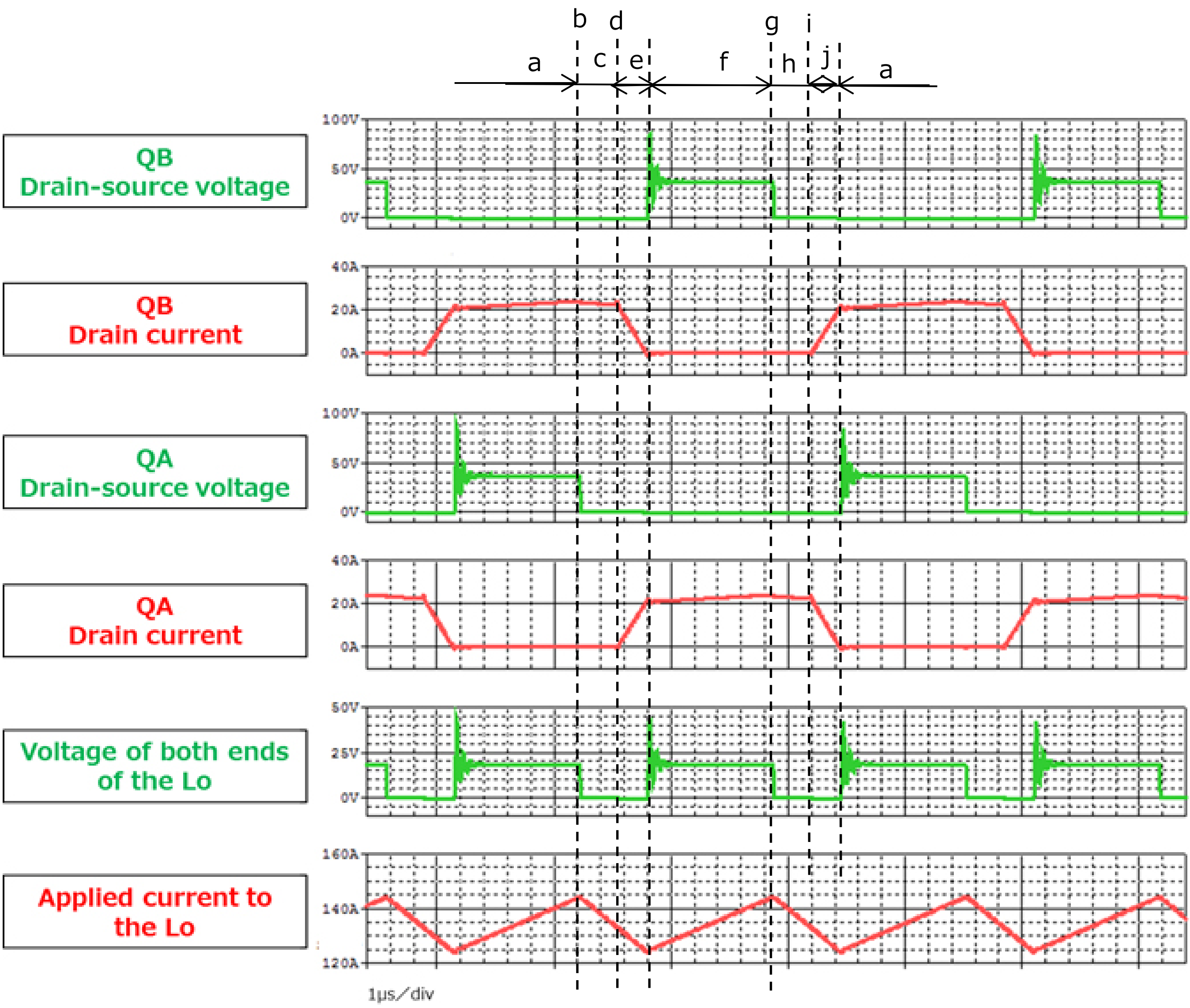


Figure 3.4 Waveforms of the drain-source voltage and drain current of the secondary-side MOSFETs and the voltage and current waveforms of the output inductor

(3) Output voltage and current from the AC-DC power supply

Figure 3.5 shows the waveforms of the output voltage and current from the PSFB AC-DC power supply. It shows that both the output voltage and current are regulated properly.

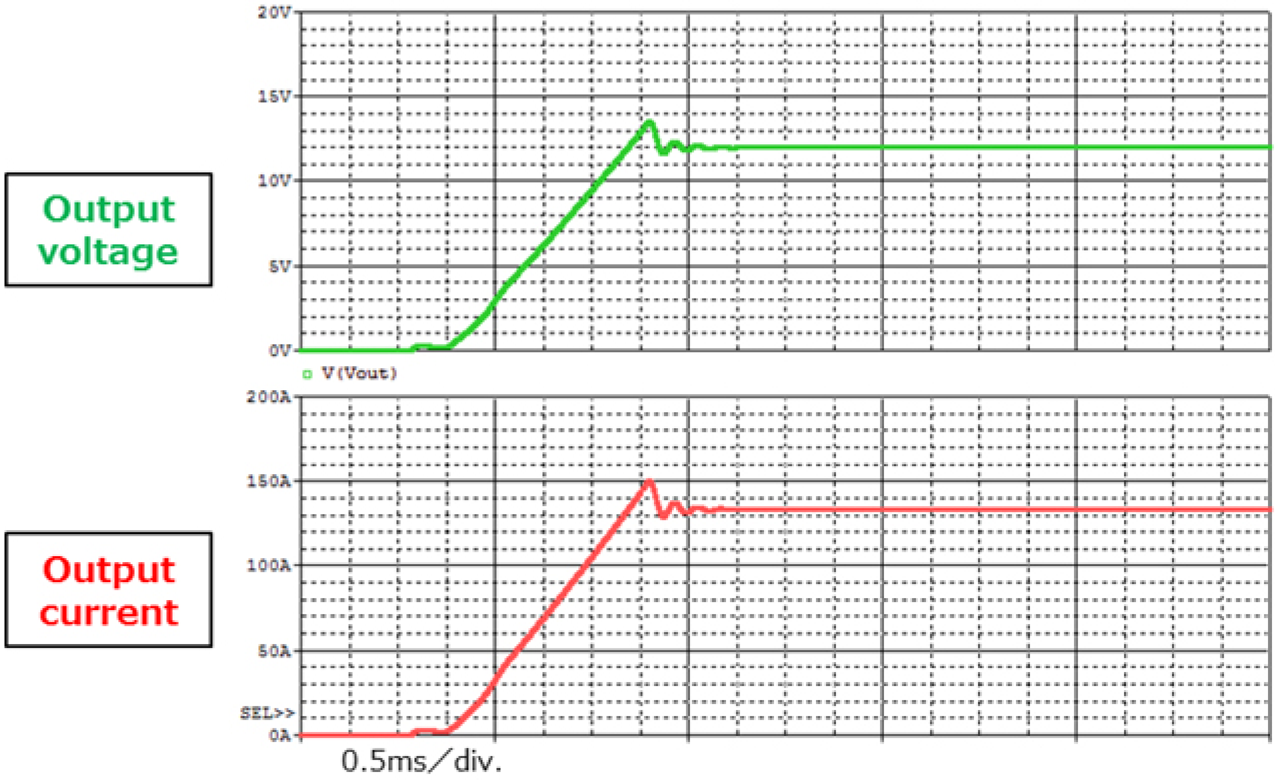


Figure 3.5 Output voltage and current waveforms

4. Product Overview

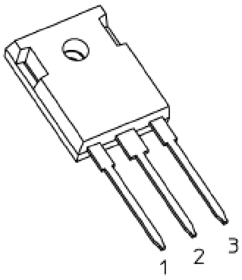
This section provides an overview of Toshiba's devices used as PSpice® models in the simulation circuit.

4.1. TK25N60X5

Characteristics

- V_{DSS}=600V, I_D=25A
- Fast reverse recovery: t_{rr}=120ns (typ.)
- Low on-resistance with a super-junction DTMOS process: $R_{DS(ON)}$=0.12Ω (typ.)
- Optimized gate switching speed
- Easy-to-use enhanced-mode MOSFET: V_{th}=3 to 4.5V（V_{DS}=10V、I_D=1.2mA）

External view and pin assignment



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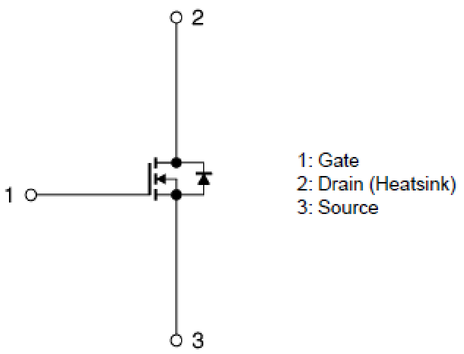
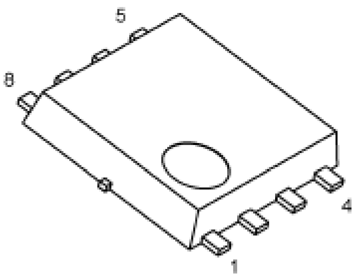


4.2. TPH3R70APL

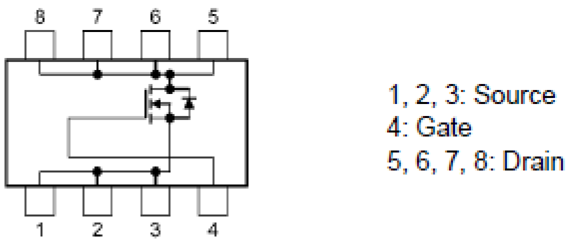
Characteristics

- V_{DSS}=100V, I_D=90A
- Fast switching
- Low input gate charge: Q_{SW}=21nC (typ.)
- Low output charge: Q_{OSS}=74nC (typ.)
- Low on-resistance: $R_{DS(ON)}$=3.1mΩ (typ. at V_{GS}=10V)
- Low leakage current: I_{DSS}=10μA (max. at V_{DS} = 100V)
- Easy-to-use enhanced-mode MOSFET: V_{th}=1.5 to 2.5V（V_{DS}=10V, I_D=1mA）

External view and pin assignment



SOP Advance



5.0mm (W) × 6.0 mm (L) × 0.95mm (H)

5. Using the simulation circuit

You can freely change various parameters with OrCAD® Capture to verify the circuit operation according to the actual power supply specifications and evaluate how these parameters affect the circuit operation. This section shows how to set simulation parameters and verify the circuit operation.

Parameter settings

Table 5.1 shows the parameters you can set for the simulation circuit. Double-click a parameter name in the PARAMETERS section, then the Display Properties dialog box appears as shown in Figure 5.1. Change the value in the Value field.

Table 5.1 Parameters that can be modified in the Parameters section

Parameter name	Unit	Description
Vin	V	Input voltage
Vout	V	Output voltage
DCR1	Ω	Parasitic resistance of the power plane on the primary side
DCR2	Ω	Parasitic resistance of the GND plane on the primary side
Fc	Hz	Switching frequency of the secondary-side MOSFET
Rdrv_on_p	Ω	Internal resistance of the turn-on gate driver for the primary-side MOSFET
Rdrv_off_p	Ω	Internal resistance of the turn-off gate driver for the primary-side MOSFET
Rdrv_on_s	Ω	Internal resistance of the turn-on gate driver for the secondary-side MOSFET
Rdrv_off_s	Ω	Internal resistance of the turn-off gate driver for the secondary-side MOSFET
Vdrv_H_p	V	Supply voltage of the gate driver on the primary side
Vdrv_H_s	V	Supply voltage of the gate driver on the secondary side
Tdl	sec	Dead time of the leading leg
Tdr	sec	Dead time of the lagging leg

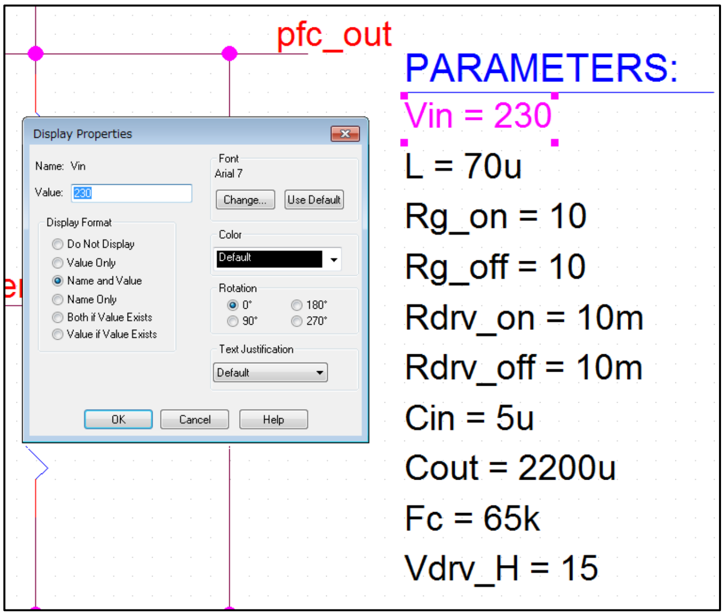


Figure 5.1 Display Properties dialog box

Setting analysis parameters

The following describes how to run a simulation on the simulation circuit.

1. From the menu bar of OrCAD® Capture, select **PSpice** - **New Simulation Profile**. Then, the New Simulation dialog box shown in Figure 5.2 appears. Enter an arbitrary profile name and click **Create**.

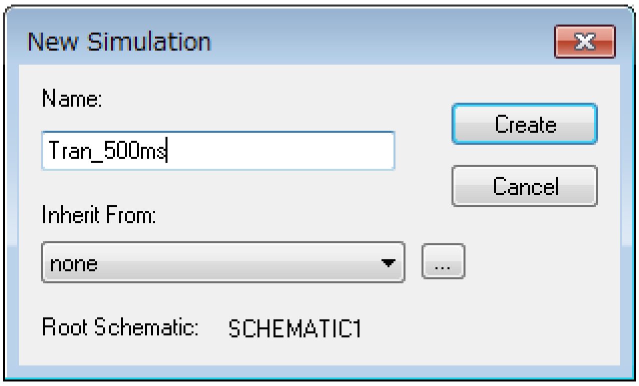


Figure 5.2 New Simulation dialog box

2. Then, the Simulation Settings dialog box shown in Figure 5.3 appears. In this dialog box, you can set parameters for various types of analysis. First, click the **Analysis** tab. Select **Time Domain (Transient)** from the **Analysis Type** drop-down list. Enter the simulation end time in the **Run To Time** field and the maximum step size in the **Maximum Step Size** field.

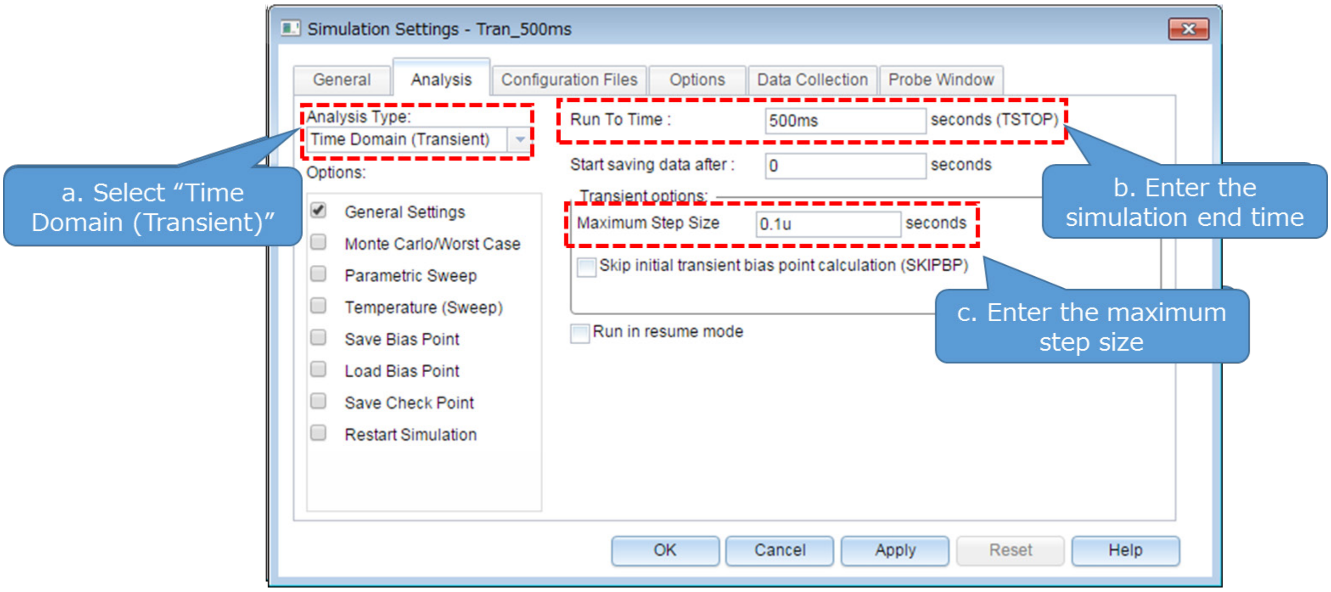
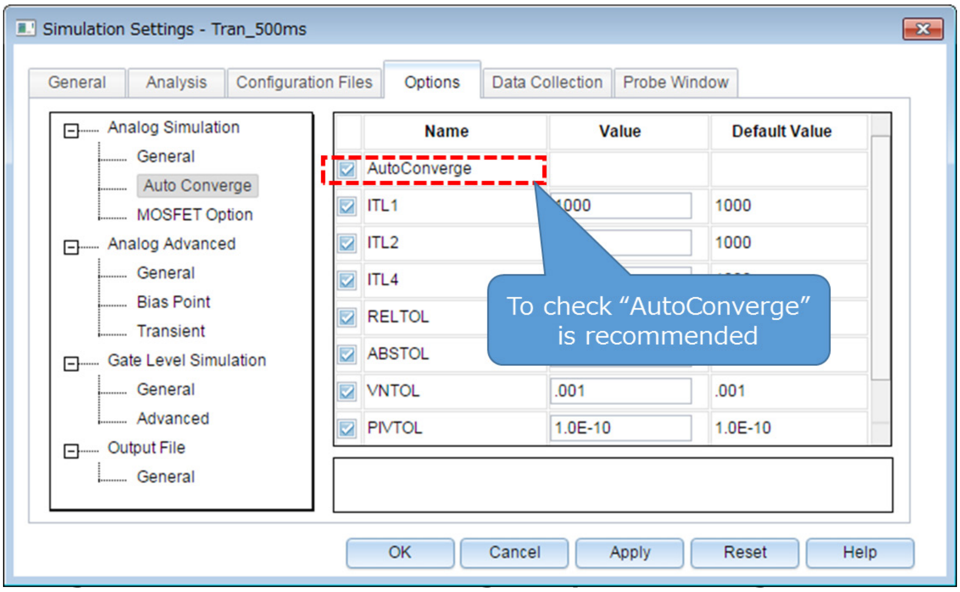


Figure 5.3 Simulation Settings - Analysis dialog box

3. Click the **Options** tab to choose analysis options. For the simulation of our model, it is recommended to check **Analog Simulation** - **Auto Converge** - **AutoConverge** as shown in Figure 5.4 to enable the automatic convergence feature.



4. Click **OK** to close the Simulation Settings dialog box.
5. To run a simulation, select **PSpice** - **Run** from the menu bar of OrCAD® Capture. Then, PSpice A/D starts automatically and runs a simulation.

Viewing simulation results

The following describes how to view the simulation results. You can display the waveforms of the simulation results in two ways.

Method 1: Selecting traces

1. Right-click outside the graph area and select **Add Trace** as shown in Figure 5.5.
2. Then, the Add Traces dialog box shown in Figure 5.6 appears. Select traces to be added to a selected plot. To view a voltage waveform, select V(*trace_name*). To view a current waveform, select I(*device_name*). See Figure 5.6.
3. Click **OK**. Then, the selected waveform appears as shown in Figure 5.7.

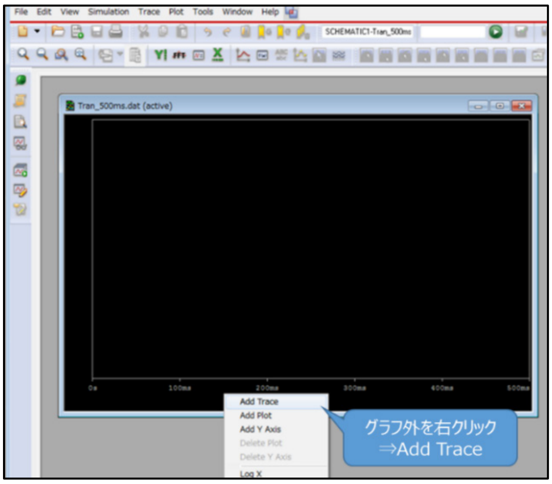
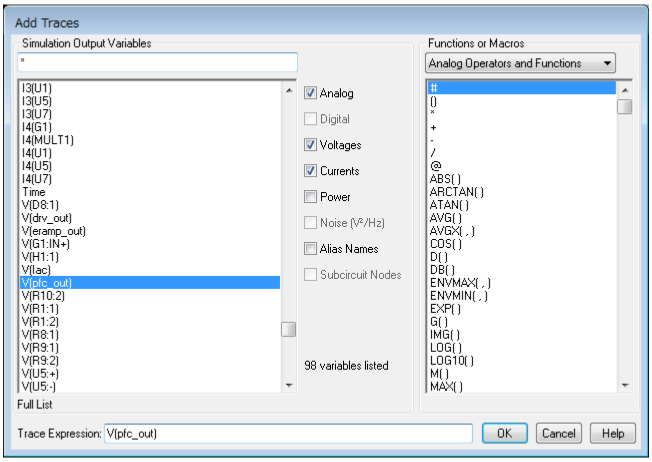


Figure 5.5 Graph window



5.6 Add Traces dialog box

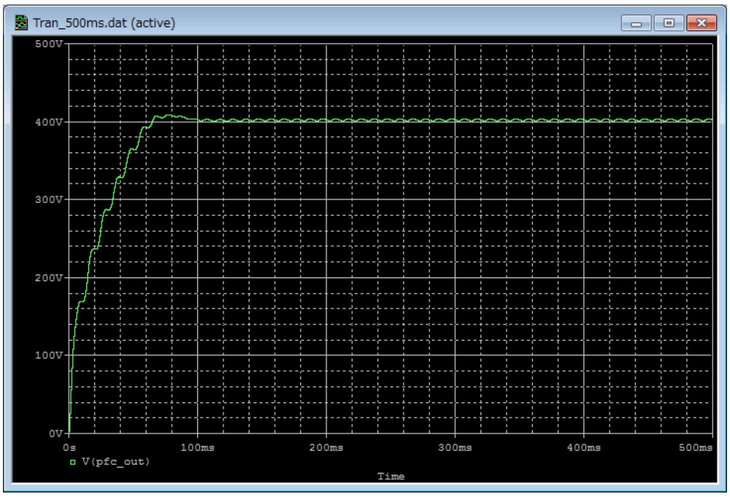


Figure 5.7 Simulation waveform view (Example: PFC output voltage waveform)

Method 2: Adding markers

1. From the menu bar of OrCAD® Capture, select **PSpice** - **Markers** and then a type of marker as shown in Figure 5.8.
2. Place the selected marker on the desired node in the simulation circuit as shown in Figure 5.9.
3. Then, its waveform appears in the graph window of PSpice® A/D as shown in Figure 5.10.

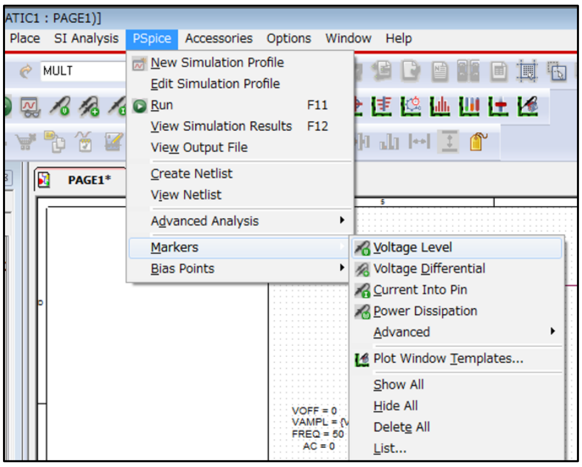


Figure 5.8 Selecting a marker type

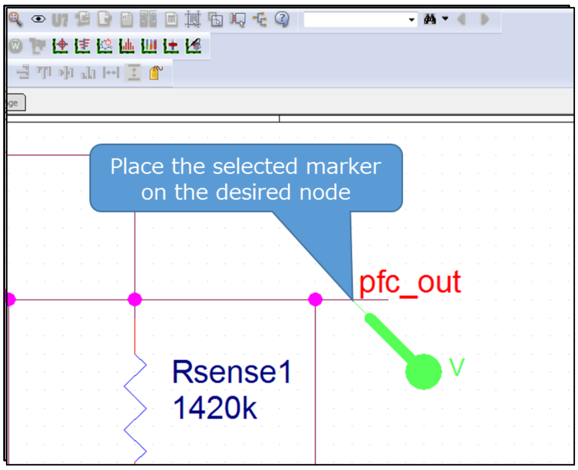


Figure 5.9 Placing a marker in the circuit

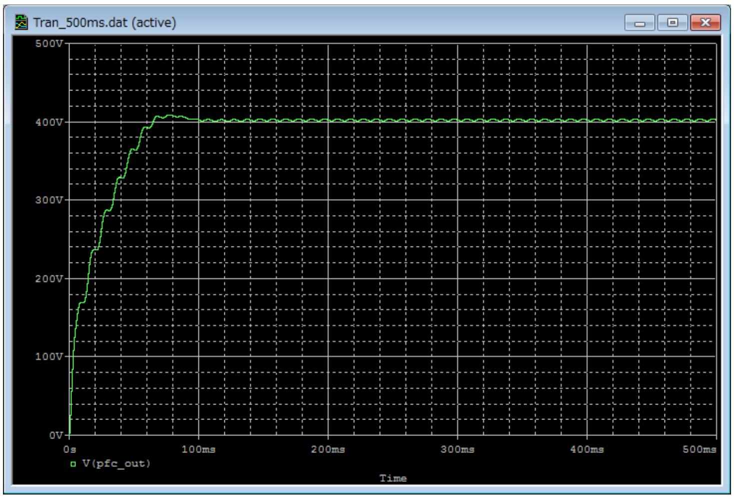


Figure 5.10 Simulation waveform view (Example: Output voltage waveform)

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