# Bridgeless PFC Power Supply
# Basic Simulation Circuit
# Reference Guide

## RD033-RGUIDE-02

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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# 1. Introduction

Ideally, the voltage and current waveforms of alternating power are completely sinusoidal and in phase with each other. However, when an AC power supply is connected to a system, its voltage and current waveforms may go out of phase or become non-sinusoidal. A power factor represents the offset in time between the voltage and the current and is defined by following equations:

Power factor = Active power ÷ Apparent power

Active power is the actual power consumed by the load and can be calculated as an integral of instantaneous power (i.e., instantaneous voltage times instantaneous current) over an AC cycle. Apparent power is the product of the rms values of the input voltage and current.

The power factor takes a value between 0 and 1. A power factor of 1 represents the ideal situation where apparent power is equal to active power. A power factor of 0 indicates that apparent power is equal to reactive power. A load with a low power factor draws more apparent power than a load with a high power factor for the same amount of active power transferred. A load with a low power factor is undesirable because it affects other systems and transmission and distribution equipment. Conventional AC-DC power supplies use a diode bridge and a capacitor. In these power supplies, an AC input is rectified to a varying DC voltage, which in turn is converted to a desired voltage. AC-DC power supplies have a pulsed input current since the capacitor is charged only when the capacitor output voltage falls below the output voltage of the diode bridge. Therefore, AC-DC power supplies have a low power factor. Figure 1.1 shows an example of a diode bridge rectifier with a capacitor filter. Figure 1.2 and Figure 1.3 show its waveforms.

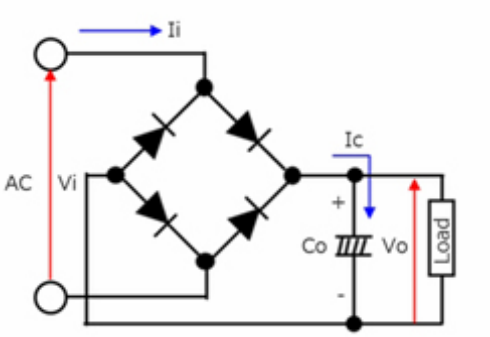



**Figure 1.1 Diode bridge rectifier with a capacitor filter**

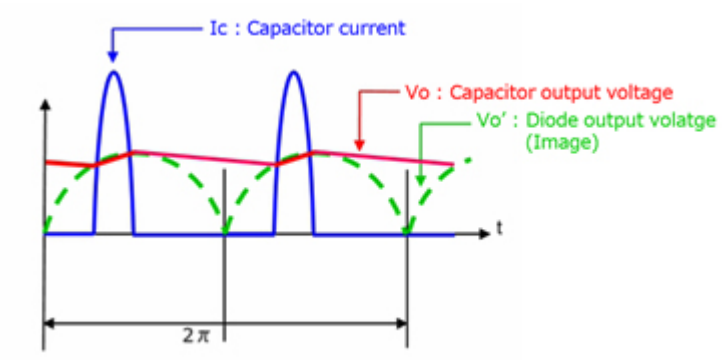



**Figure 1.2 Waveforms at different nodes in the circuit**

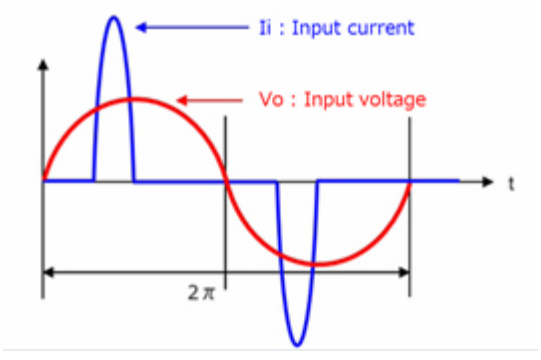
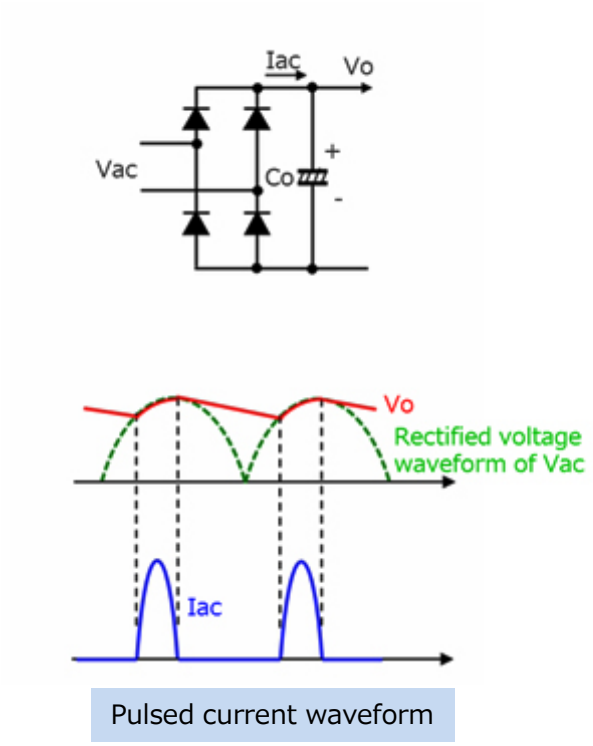


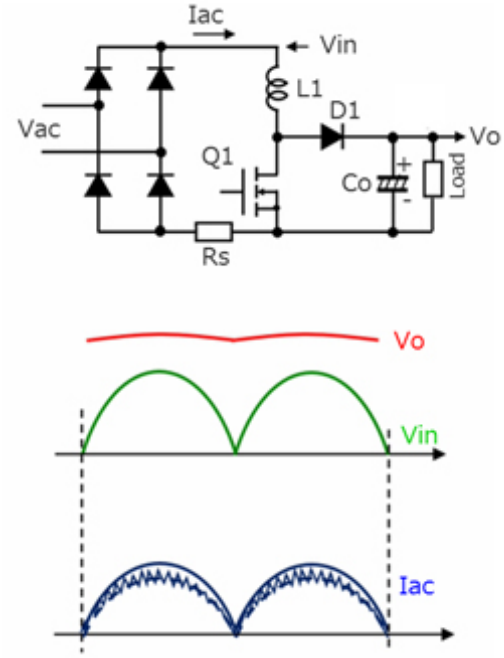

**Figure 1.3 Input current and voltage waveforms**

The aim of a power factor correction (PFC) circuit is to improve the power factor for AC-DC converters. At present, commonly used AC-DC power supplies incorporate a PFC circuit to improve their power factor. Typically, the PFC circuit in an AC-DC power supply is a boost converter in which an AC input is placed after a diode bridge. Figure 1.4 shows a diode bridge rectifier with a capacitor filter whereas Figure 1.5 shows a boost PFC converter.




Pulsed current waveform

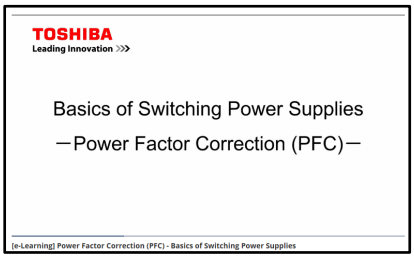
**Figure 1.4 Diode bridge rectifier with a capacitor filter**




The switching of Q1 is controlled to make the current waveform sinusoidal.

**Figure 1.5 Boost PFC converter**

A video describing the power factor of an AC-DC power supply and a PFC circuit is on Toshiba's website.




In typical PFC circuits, a diode bridge is followed by a switching device. Since current flows through the diode bridge, power loss occurs continuously owing to the diode forward voltage. To reduce diode loss, server power supply and other applications that require high efficiency sometimes use a bridgeless PFC power supply that directly switches AC voltage without using a diode bridge. The bridgeless PFC power supply uses different current flow paths in positive and negative AC half cycles instead of rectifying AC power with a diode bridge. Since the current flows through two paths, a bridgeless PFC power supply can use devices with smaller power ratings than a single-phase PFC

power supply with an equal output power. For this reason, bridgeless PFC is commonly used for AC-DC power supplies with relatively high output power that require high efficiency. A basic simulation circuit of a bridgeless PFC power supply (RD033-SPICE-01) is available on Toshiba's website, which will help you understand its operation.

This Reference Guide provides an overview of this simulation circuit and describes its usage. OrCAD® Capture and PSpice® A/D from Cadence are necessary to simulate this circuit. Both the simulation circuit and the Reference Guide are based on OrCAD® 17.2.

# 2. Overview of the PFC power supply

RD033-SPICE-01 is an interleaved PFC power supply with a 1600W output.

## 2.1. Specifications

The specifications of the interleaved PFC power supply are as follows:

- Input voltage: 90 to 264 $V_{rms}$
- Output voltage: 400 V
- Output current: 0 to 4.0 A
- Operating frequency: 65 kHz
- Allowable peak-to-peak ripple current: 40 % of the peak input current
- Inductance setting: 130 µH

## 2.2. Circuit configuration

Figure 2.1 shows the simulation circuit for OrCAD®. It is a continuous-current-mode (CCM) bridgeless PFC power supply, which mainly consists of three sections: a power supply section at the upper portion, a PFC controller at the lower portion, and the PARAMETERS section on the right-hand side. The PFC controller is a general-purpose controller with a MOSFET gate driver, which was prepared to create this PFC power supply. The simulation circuit uses the TK31N60X and TRS8E65F as example of switching MOSFETs and diodes.

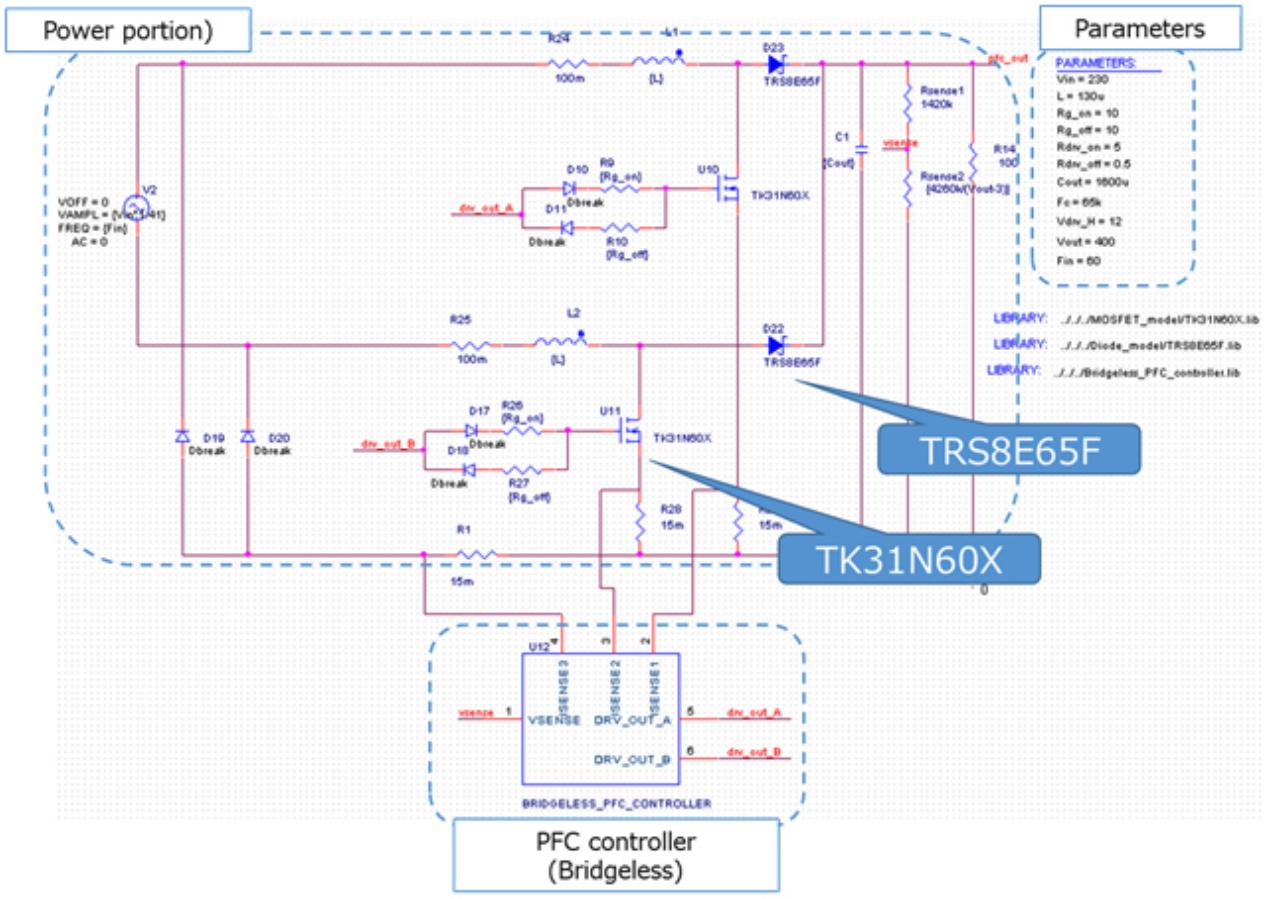



**Figure 2.1 Simulation circuit of a 1200W interleaved PFC power supply**

## Selection of the MOSFET and diode

The MOSFET and diode were selected, taking the following into consideration:

(1) Withstand voltage

In the steady state, the MOSFET and diode conduct the same voltage as the output voltage (400V) of the PFC power supply. Therefore, a MOSFET and diode with a withstand voltage of 600V or higher were selected for the simulation circuit.

(2) Current rating

The PFC power supply has the maximum input current when the output power has the maximum value and the input voltage has the minimum value. Suppose that PFC power supply has a conversion efficiency of 94% and a power factor of 1 at the maximum output power of 1600W. Then, the maximum input current is calculated to be roughly 18.9$A_{rms}$ at the minimum input voltage of 90$V_{rms}$. It is divided into 2 paths.

Assuming a 50% duty cycle, a current of roughly 4.3 $A_{rms}$ is applied to each device. Therefore, a MOSFET and diode with a current rating of 6A or higher were selected for the simulation circuit.

MOSFET: TK31N60X ($V_{DS}$=600V / $I_D$=30.8A / $R_{DS(ON)}$=88mΩ(Max)

Diode: TRS8E65F (650V/8A)

## Selection of the inductor

The following paragraphs describe how to select an inductor. The value of the inductor to be used in the simulation circuit can be calculated from the following power supply parameters:

- Maximum output power: $P_{out}$ (W)
- Minimum AC line input voltage: $V_{in\_min}$ ($V_{rms}$)
- PFC power conversion efficiency: η (%)
- PFC output voltage: $V_{out}$ (V)
- Switching frequency: $F_c$ (Hz)
- Allowable peak-to-peak ripple current: $\Delta I_{ripple}$ (%)

Inductance is calculated by following an equation:

$$\mathrm{L} = \frac{\left(V_{out} - \sqrt{2} \times V_{in\_min}\right) \times \eta \times 0.01 \times {V_{in\_min}}^2}{F_c \times 0.01 \times \Delta I_{ripple} \times P_{out} \times V_{out}}$$

where, the maximum output power ($P_{out}$) is 1600W, the minimum AC line input voltage ($V_{in\_min}$) is 90V, the PFC output voltage is 400V, and the switching frequency ($F_c$) is 65kHz. Suppose that the PFC power conversion efficiency (η) is 94%. Then, inductance (L) is calculated to be 124μH. Therefore, inductance is set to 130μH in the simulation circuit.

In practice, the value of the inductor varies because of DC bias characteristics. Select an inductor that exhibits an inductance greater than the result of the above equation even when the inductance decreases because of DC bias characteristics.

# 3. Simulation results

This section describes the results of the operation of each section of the simulation circuit. The following shows the waveforms of “input voltage and current”, “inductor current”, “output voltage and current”, “MOSFET gate voltage”, and “MOSFET drain-source voltage and current” highlighted in Figure 3.1 The simulation circuit model also allows you to view other waveforms. See Section 5 for how to view waveforms.

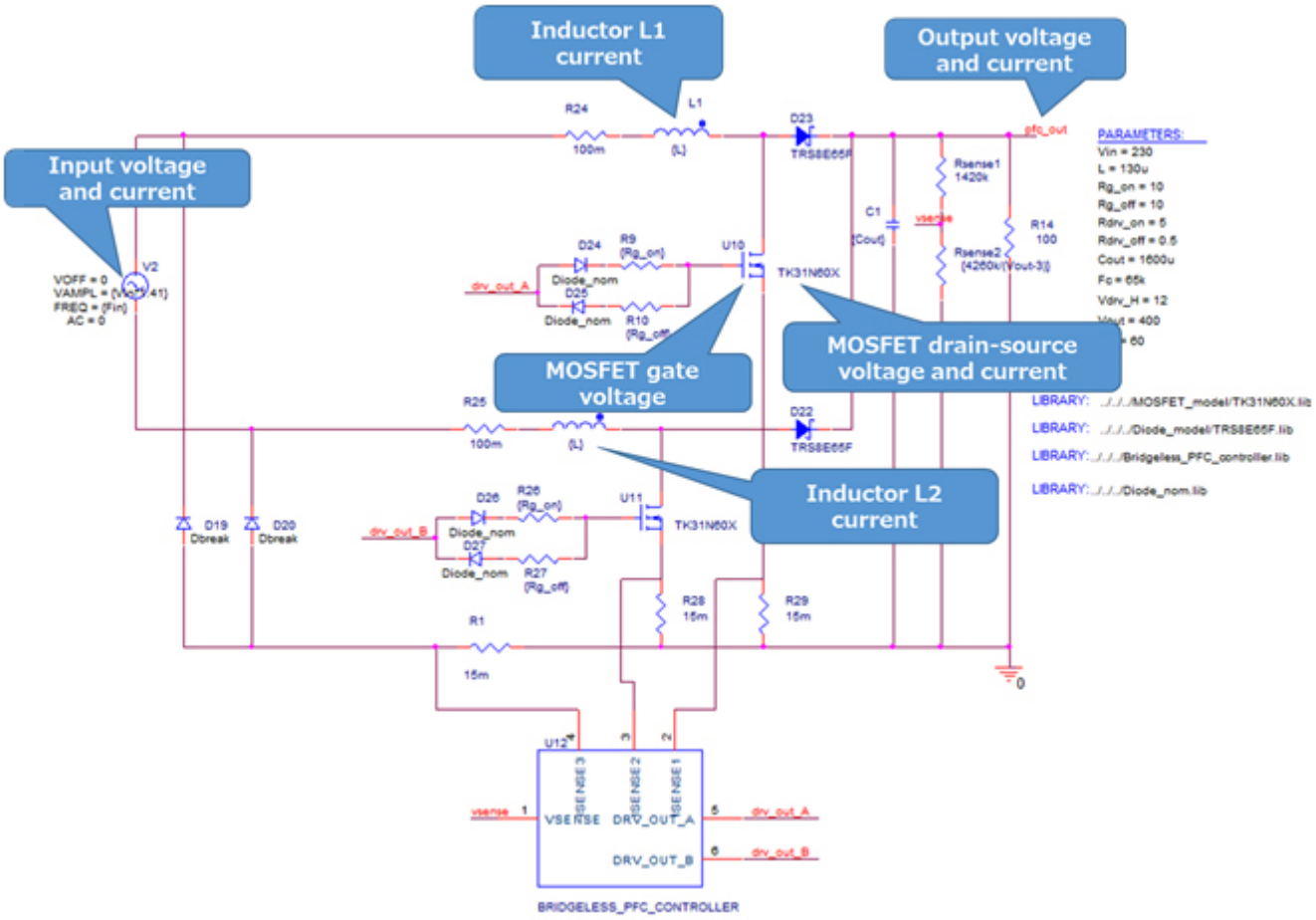



**Figure 3.1 Waveforms observed**

## Input voltage and current, output voltage and current, and inductor current waveforms

Figure 3.2 and Figure 3.3 show the waveforms of the AC input voltage and current, the PFC output voltage and current, and the inductor current. The output voltage waveform (at the top of Figure 3.2 and Figure 3.3) shows that the PFC output is regulated at 400V as required by the power supply specification. The AC input current waveform (at the middle of Figure 3.2 and Figure 3.3) shows it is sinusoidal, increasing the power factor.

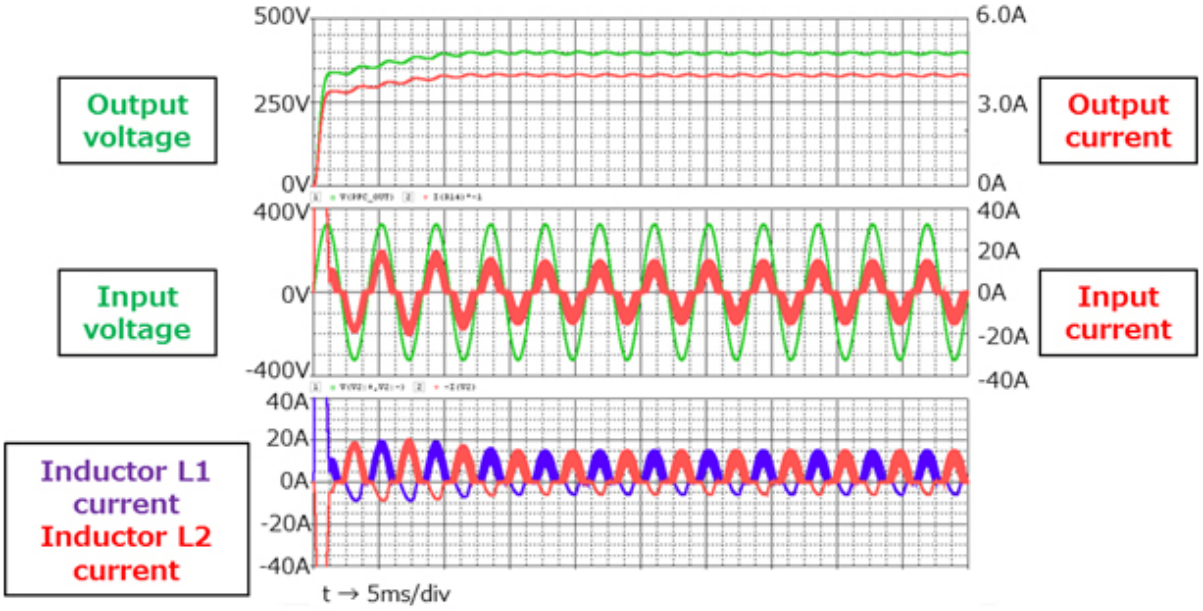



**Figure 3.2 Input voltage and current, output voltage and current, and inductor current waveforms**

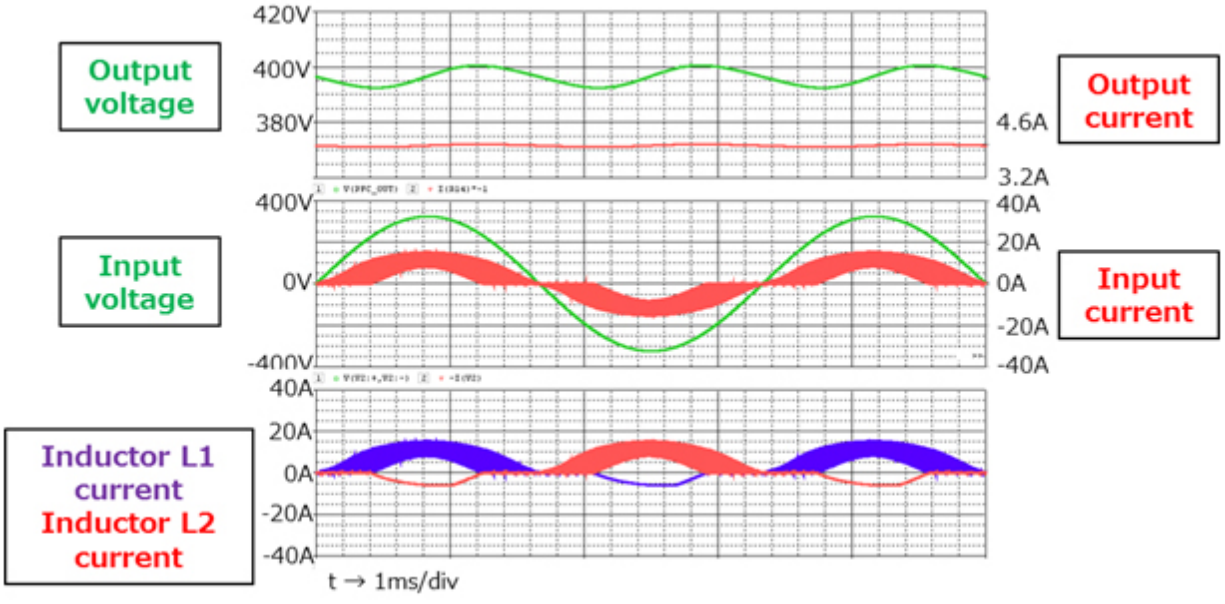



**Figure 3.3 Input voltage and current, output voltage and current, and inductor current waveforms (enlarged view)**

## Input voltage and MOSFET gate voltage waveforms

Figure 3.4 shows the waveforms of the AC input voltage and each MOSFET gate voltage. Figure 3.4 shows that a running MOSFET is switched at half AC cycle to half AC cycle as bridgeless PFC operation. Inductor current waveforms of Figure 3.2 and Figure 3.3 also show that a boost inductor is switched at half AC cycle to half AC cycle.

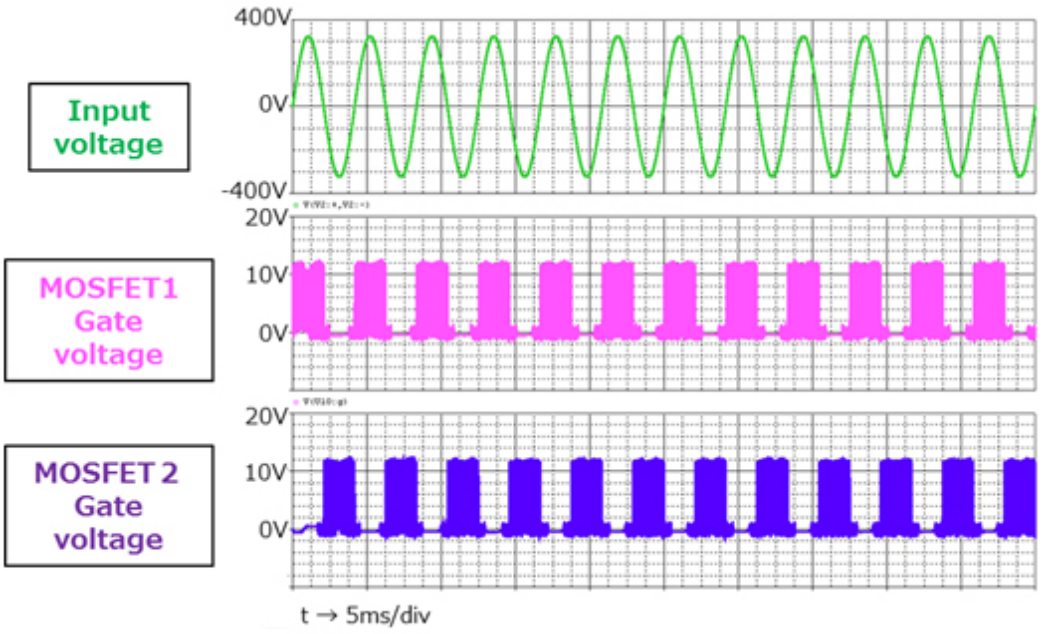
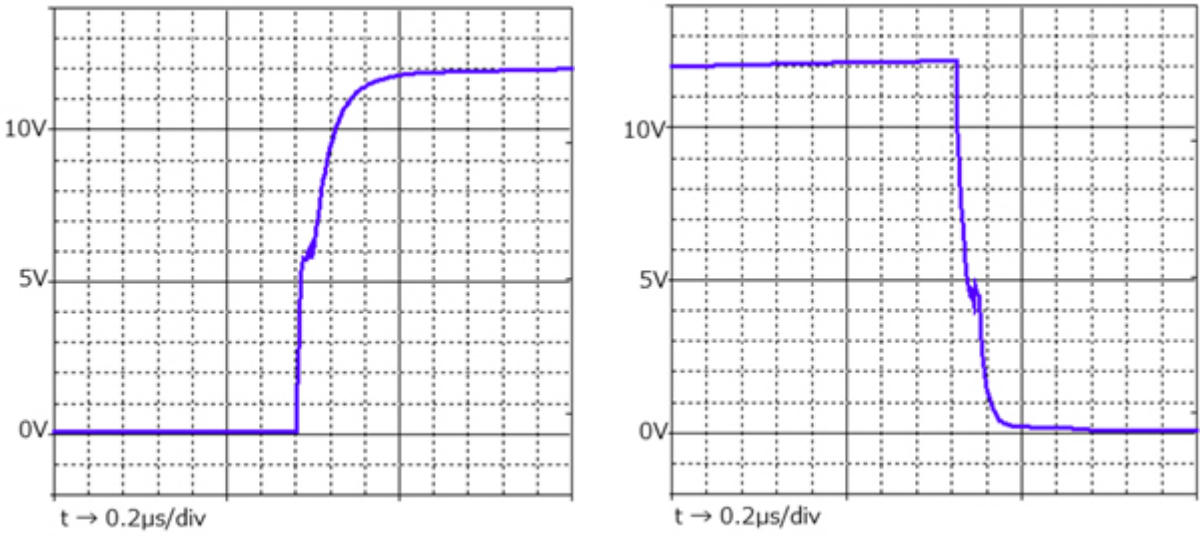



**Figure 3.4 Input voltage and MOSFET gate voltage waveforms**

## MOSFET gate voltage and MOSFET drain-source voltage and current waveforms

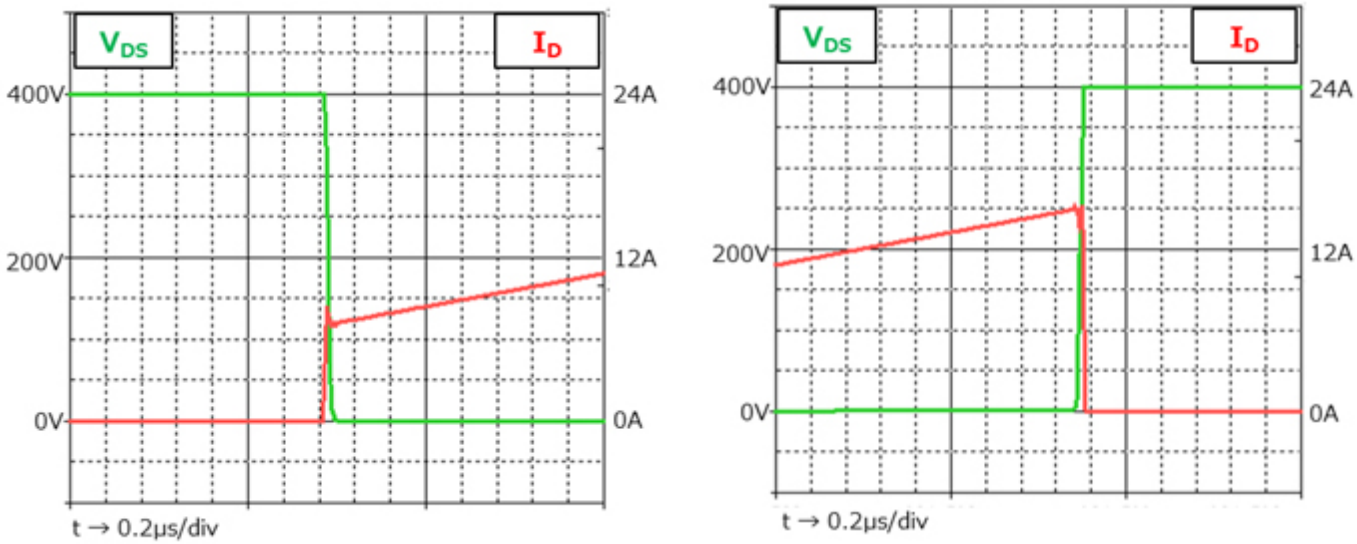
Figure 3.5 shows the waveforms of the gate voltage of the TK31N60X, which is used as a switching MOSFET in the simulation circuit. Figure 3.6 shows the waveforms of the drain-source voltage ($V_{DS}$) and current ($I_D$). The MOSFET is PWM-controlled to generate a half-sinusoidal inductor current. Figure 3.5 and Figure 3.6 show the MOSFET waveforms at the point in time when the inductor current has reached the peak value.

In the simulation circuit, parameters Rg_on and Rg_off are used to specify the parameters of an external resistor connected to the MOSFET gate. You can verify the effect of the gate resistance on the behavior of the MOSFET by changing these parameters.




(a) At turn-on (b) At turn-off

**Figure 3.5 MOSFET gate voltage waveforms**




(a) At turn-on (b) At turn-off

**Figure 3.6 MOSFET drain-source voltage and current waveforms**

# 4. Product overview

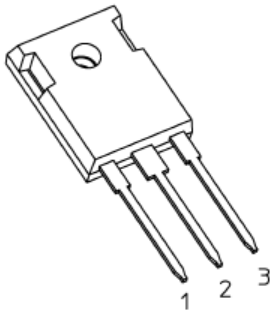
This section provides an overview of Toshiba's devices used as PSpice® models in the simulation circuit.

## 4.1. TK31N60X

**Features**

- Low drain-source on-resistance due to a super-junction DTMOS process: $R_{DS(ON)}$ = 73mΩ (Typ)
- Optimized gate switching speed
- Easy-to-use enhanced-mode MOSFET: $V_{th}$ = 2.7 to 3.7V ($V_{DS}$ = 10V, $I_D$ = 1.5mA)

**Package and Pin assignment**

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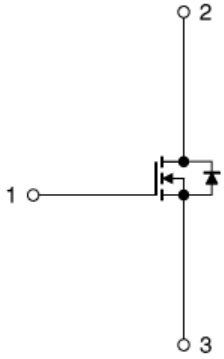


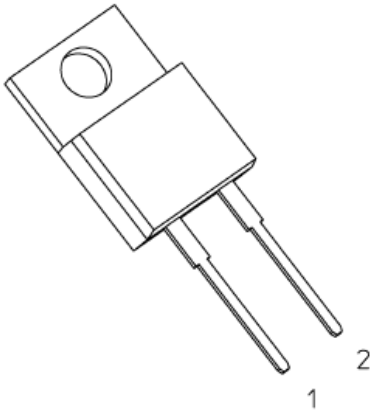

1: Gate
2: Drain (Heatsink)
3: Source

## 4.2. TRS8E65F

**Features**

- High surge current capability: $I_{FSM}$ = 69A (Max)
- Low junction capacitance: $C_j$ = 28pF (Typ.)
- Low leakage current: $I_R$ = 0.4μA (Typ.)

**Package and Pin assignment**

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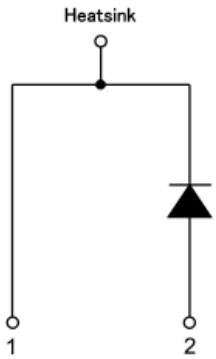



1: Cathode
2: Anode

# 5. Simulation circuit

You can freely change various parameters with OrCAD® Capture to verify the circuit operation according to the actual power supply specifications and evaluate how these parameters affect the circuit operation. This section describes how to set parameters and verify the circuit operation. This simulation circuit appears, when the OPJ file (.opj) inside the folder of RD033-SPICE-01 is opened.

## Parameter Settings

Table 5.1 lists the adjustable parameters which is possible to you can set for the simulation circuit. Double-click a parameter name in the PARAMETERS section. Then, the Display Properties dialog box appears as shown in Figure 5.1. Change the value in the Value field.

**Table 5.1 Adjustable Parameters List on the Parameters section**

| Parameter | Unit | Description |
|---|---|---|
| Vin | $V_{rms}$ | AC input voltage |
| Fin | Hz | AC input frequency |
| Vout | V | PFC output voltage |
| L | H | Boost inductor parameter |
| DCR | Ω | Inductor parasitic resistance |
| Cin | F | Input capacitor parameter |
| Cout | F | Output capacitor parameter |
| Fc | Hz | Switching frequency |
| Rg_on | Ω | External gate resistor value for turn-on |
| Rg_off | Ω | External gate resistor value for turn-off |
| Rdrv_on | Ω | Gate driver internal resistor for turn-on |
| Rdrv_off | Ω | Gate driver internal resistor for turn-off |
| Vdrv_H | V | Supply voltage of the gate driver |

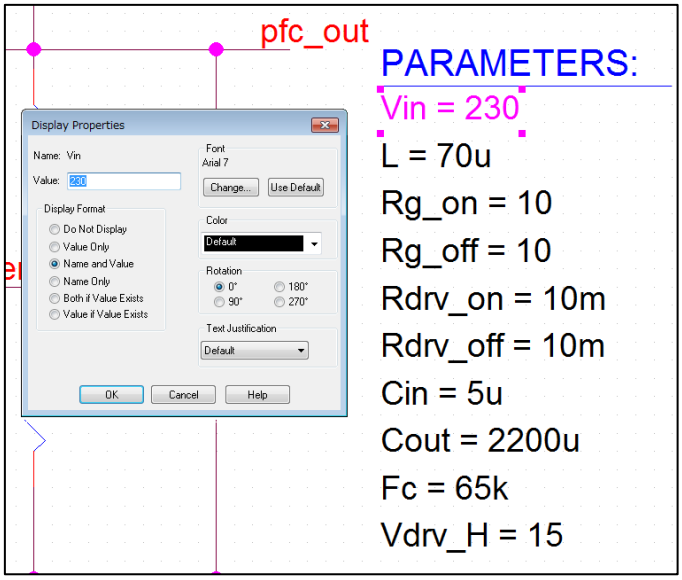



**Figure 5.1 Display Properties dialog box**

## Analysis Setting

The following describes how to run a simulation on the simulation circuit.

1. From the menu bar of OrCAD® Capture, select **PSpice** - **New Simulation Profile**. Then, the New Simulation dialog box shown in Figure 5.2 appears. Enter an arbitrary profile name and click **Create**.

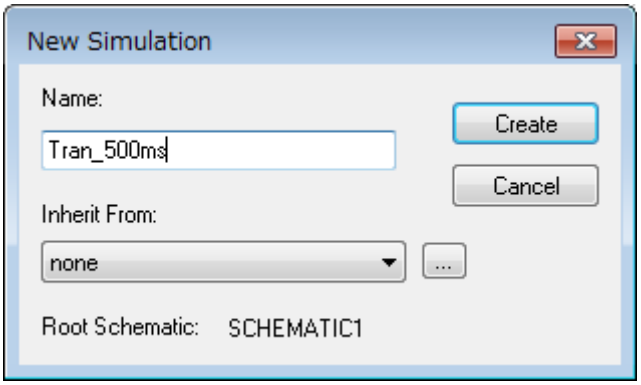



**Figure 5.2 New Simulation dialog box**

2. Then, the Simulation Settings dialog box shown in Figure 5.3 appears. In this dialog box, you can set parameters for various types of analysis. First, click the **Analysis** tab. Select **Time Domain (Transient)** from the **Analysis Type** drop-down list. Enter the simulation end time in the **Run To Time** field and the maximum step size in the **Maximum Step Size** field.

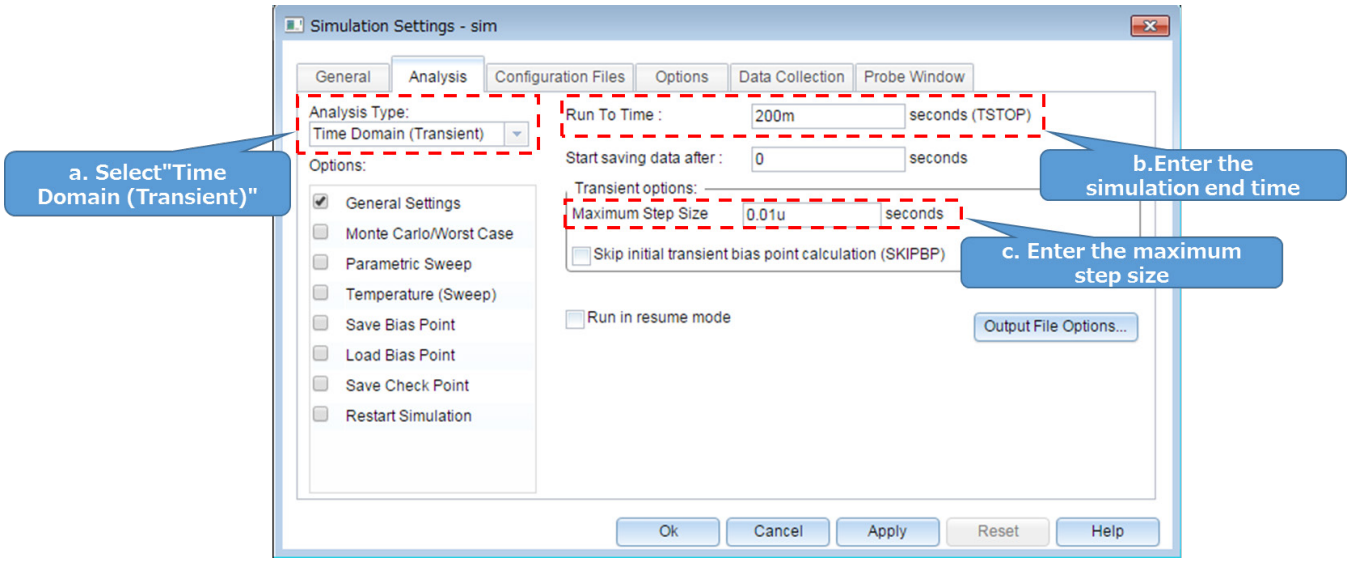



**Figure 5.3 Simulation Settings - Analysis dialog box**

3. Click the **Options** tab to choose analysis options. For the simulation of our model, it is recommended to check **Analog Simulation** - **Auto Converge** - **AutoConverge** as shown in Figure 5.4 to enable the automatic convergence feature.

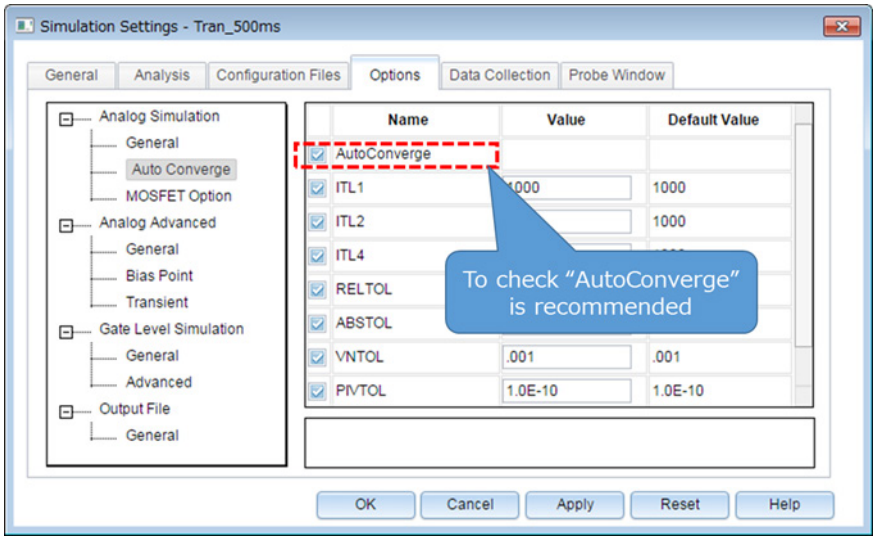



**Figure 5.4 Simulation Settings - Options dialog box**

4. Click **OK** to close the Simulation Settings dialog box.

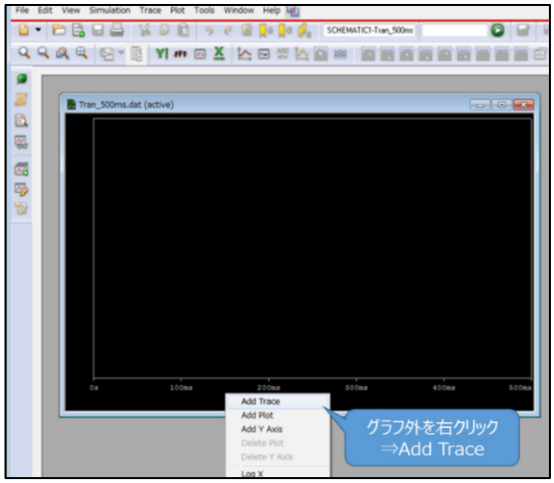
5. To run a simulation, select **PSpice** - **Run** from the menu bar of OrCAD Capture. Then, PSpice A/D starts automatically and runs a simulation.

## Viewing simulation results

The following describes how to view the simulation results. You can display the waveforms of the simulation results in two ways.

## Method 1: Selecting traces

1. Right-click outside the graph area and select **Add Trace** as shown in Figure 5.5.
2. Then, the Add Traces dialog box shown in Figure 5.6 appears. Select traces to be added to a selected plot. To view a voltage waveform, select V(*trace_name*). To view a current waveform, select I(*device_name*).
3. Click **OK**. Then, the selected waveform appears as shown in Figure 5.7.



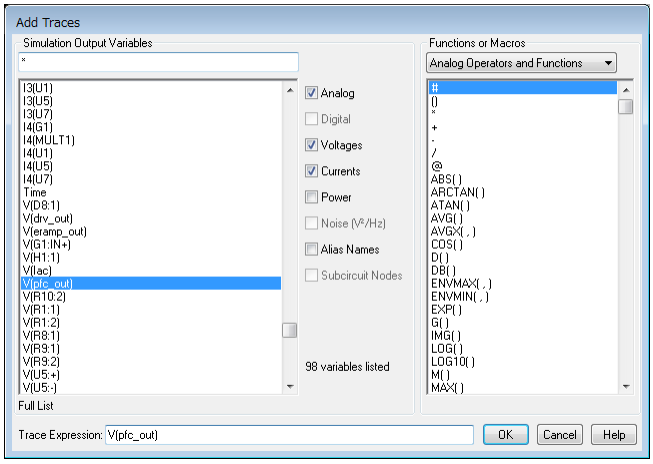




**Figure 5.5 Graph window Figure 5.6 Add Traces dialog box**

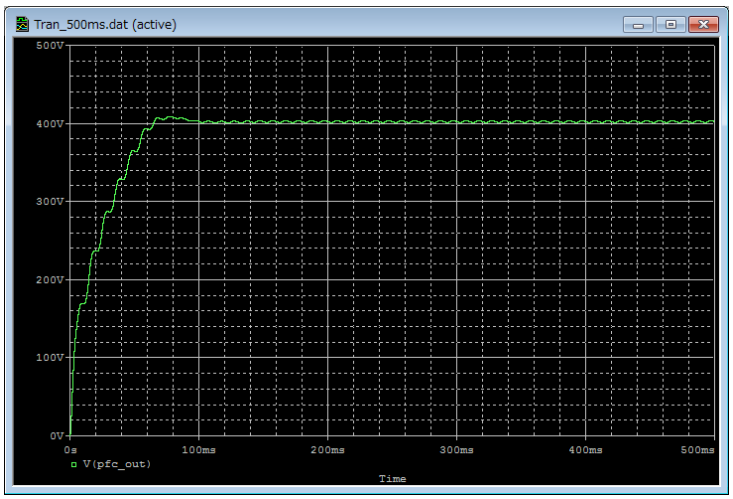



**Figure 5.7 Simulation waveform view (Example: PFC output voltage waveform)**

## Method 2 Adding markers

1. From the menu bar of OrCAD® Capture, select **PSpice** - **Markers** and then a type of marker as shown in Figure 5.8.
2. Place the selected marker on the desired node in the simulation circuit as shown in Figure 5.9.
3. Then, its waveform appears in the graph window of PSpice® A/D as shown in Figure 5.10.

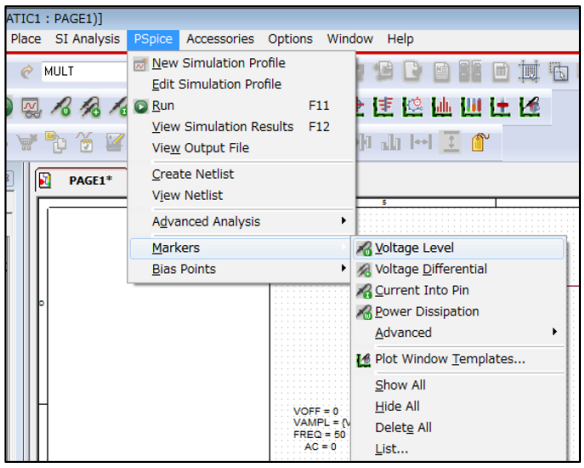



**Figure 5.8 Selecting a marker type**

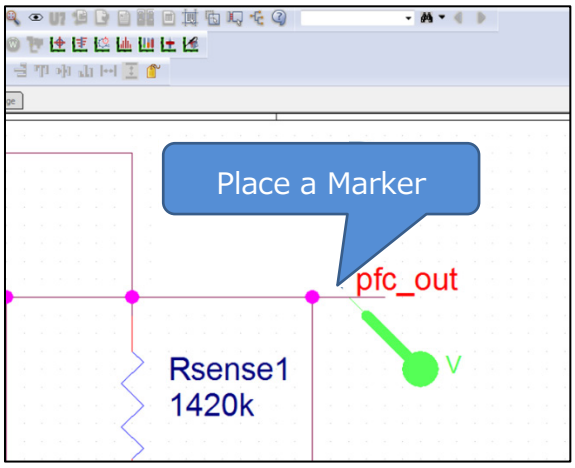



**Figure 5.9 Placing a marker in the circuit**

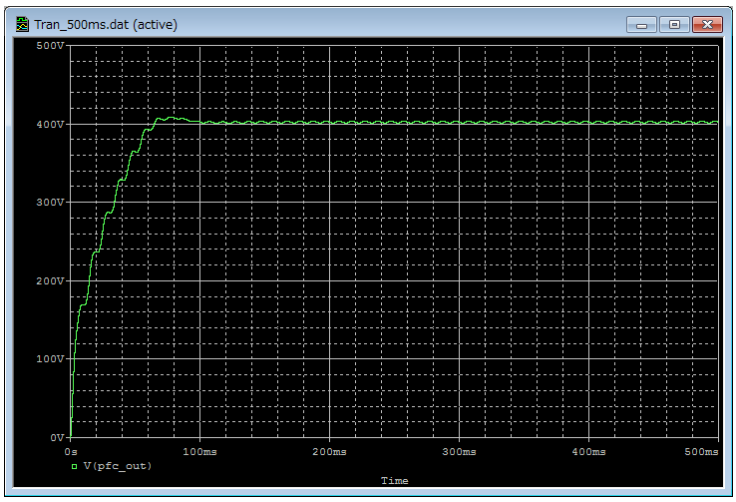



**Figure 5.10 Simulation waveform view (Example: PFC output voltage waveform)**

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