TLP5214A Smart Gate Driver Coupler
Inverter applications

Design Guide

RD021-DGUIDE-04

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

Contents

1. Introduction

Operational stability and reliability are key characteristics of FA devices such as AC servos and general-purpose inverters, as well as inverters used in power conditioners for solar and wind power systems.

Overcurrent and noise in inverter circuits may cause a system malfunction with the potential for equipment damage. The typical ways to protect the IGBT and power MOSFET are: (a) current monitoring with a current transformer (CT); (b) current monitoring with a current sensing resistor; and (c) IGBT saturation voltage monitoring. While each of these has its advantages and disadvantages, approach (c) is the lowest cost solution and has the fastest operating speed and lowest power loss.

The TLP5214A has a built-in IGBT non-saturation ($V_{CE(SAT)}$) detector suitable for IGBT saturation monitoring as per approach (c), active mirror clamping and fault signal feedback. These functions provide superior performance and stability (compared to existing products) particularly with respect to instantaneous pulse noise during switching and non-saturation. The TLP5214A also helps to minimize design effort in peripheral circuit design, reduction outside components, and reduce PCB area. Thus the device suits for a driver coupler for middle power IGBT and power MOSFET direct drive devices. In addition the device guarantees minimum isolation voltage of 5,000Vrms, so it is equally suitable for many types of industrial machinery and equipment.

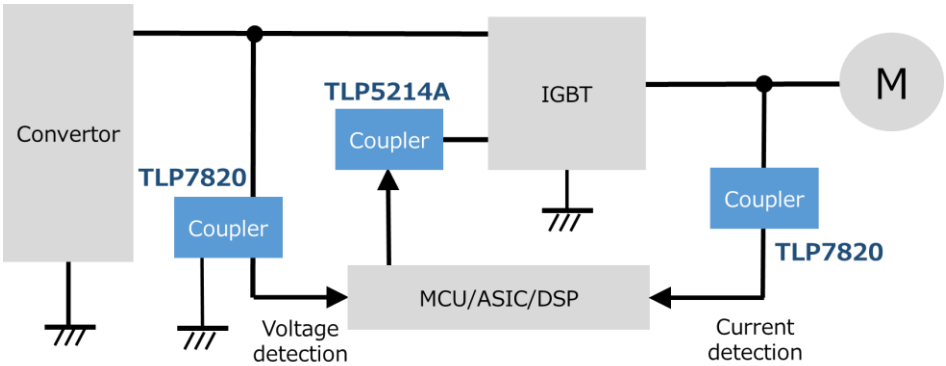
This Design Guide is based on a typical application involving an inverter circuit featuring the TLP5214A. TLP5214A product information including performance characteristics is provided on the datasheet and in the application note.

For detail of the TLP5214A → Click Here

1.1. Target applications

- IGBT/power MOSFET gate drive for FA devices, general-purpose inverters and controllers for AC motors and brushless DC motors

Typical inverter application



Note: Optically coupled isolation amplifier TLP7820 is used for motor phase current detection

For detail of the TLP7820 → Click Here

2. Application circuit examples and bill of materials

2.1. Inverter circuits

Figures 2.1 and 2.2 show examples of inverter circuits for the TLP5214A. The Design Guide (this document) gives two circuit designs, one is with mirror clamping and no negative supply, and the other is with negative supply but no mirror clamping. Table 2.1 shows the two designs.

Table 2.1 Two circuit designs

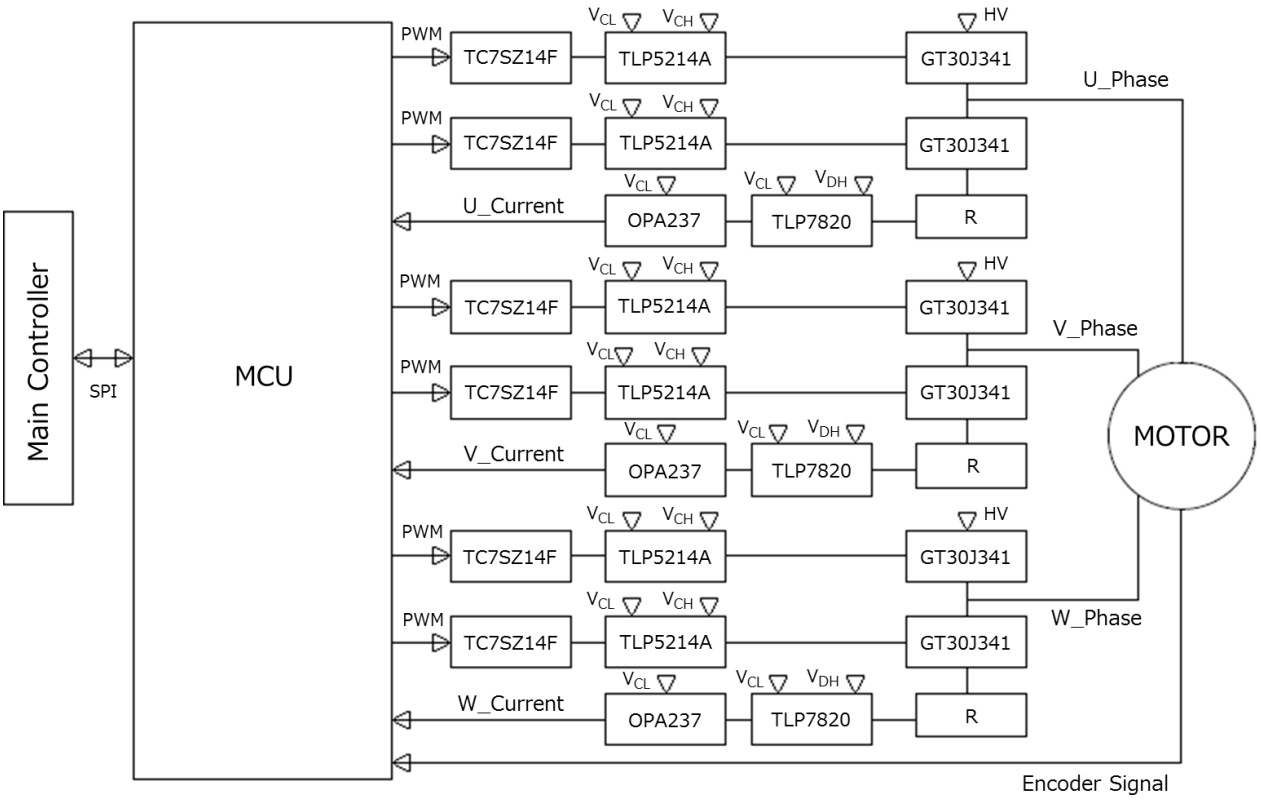
Diagram	Negative power supply	Mirror clamping	V_{CH}	$-V_{EH}$	V_{DH}	V_{CL}
RD021-SCEMATIC1-02	No	Yes	17V	-	5V	5V
RD021-SCEMATIC2-02	Yes	No	17V	10V	5V	5V

Table 2.2 shows the relevant output specifications.

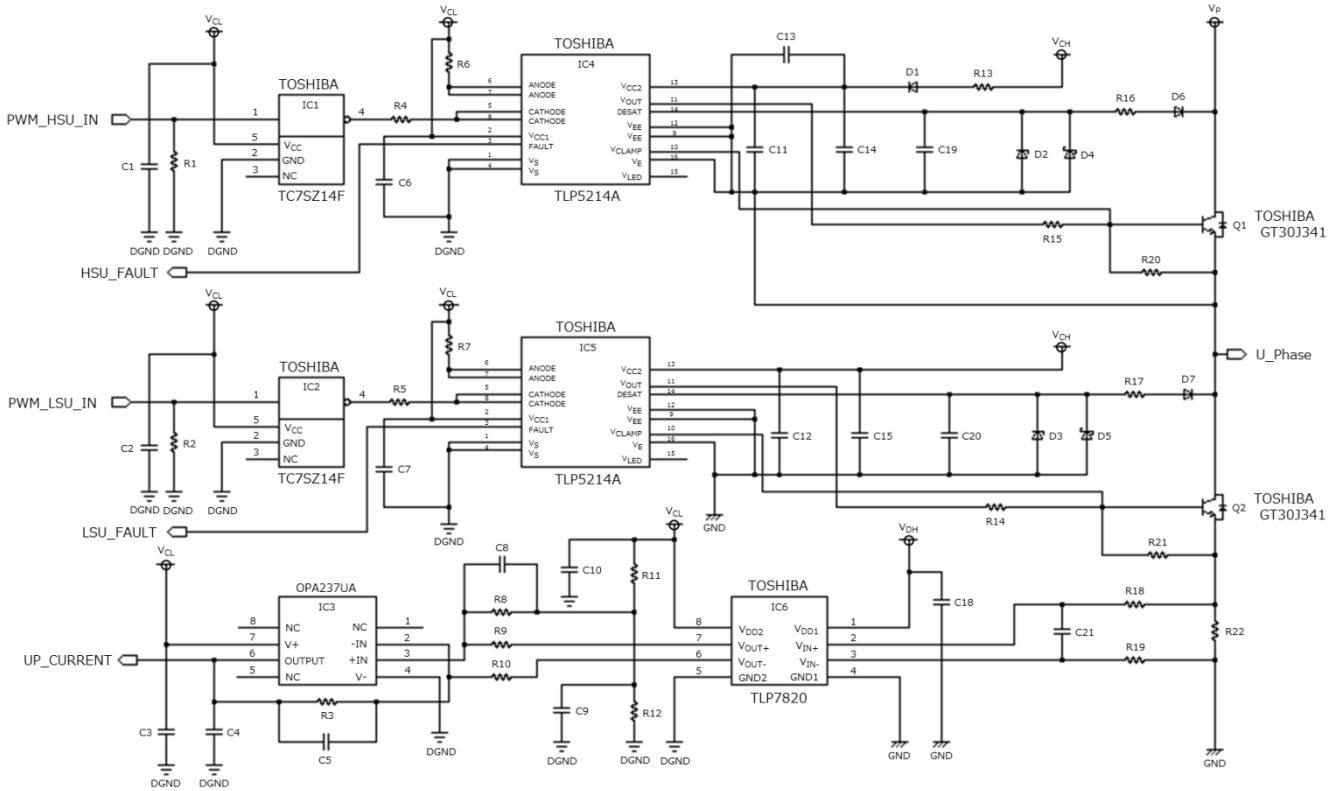
Table 2.2 Output specifications

Supply voltage (V_P)	300	V
Output drive frequency	10	kHz
Output current	±10	A

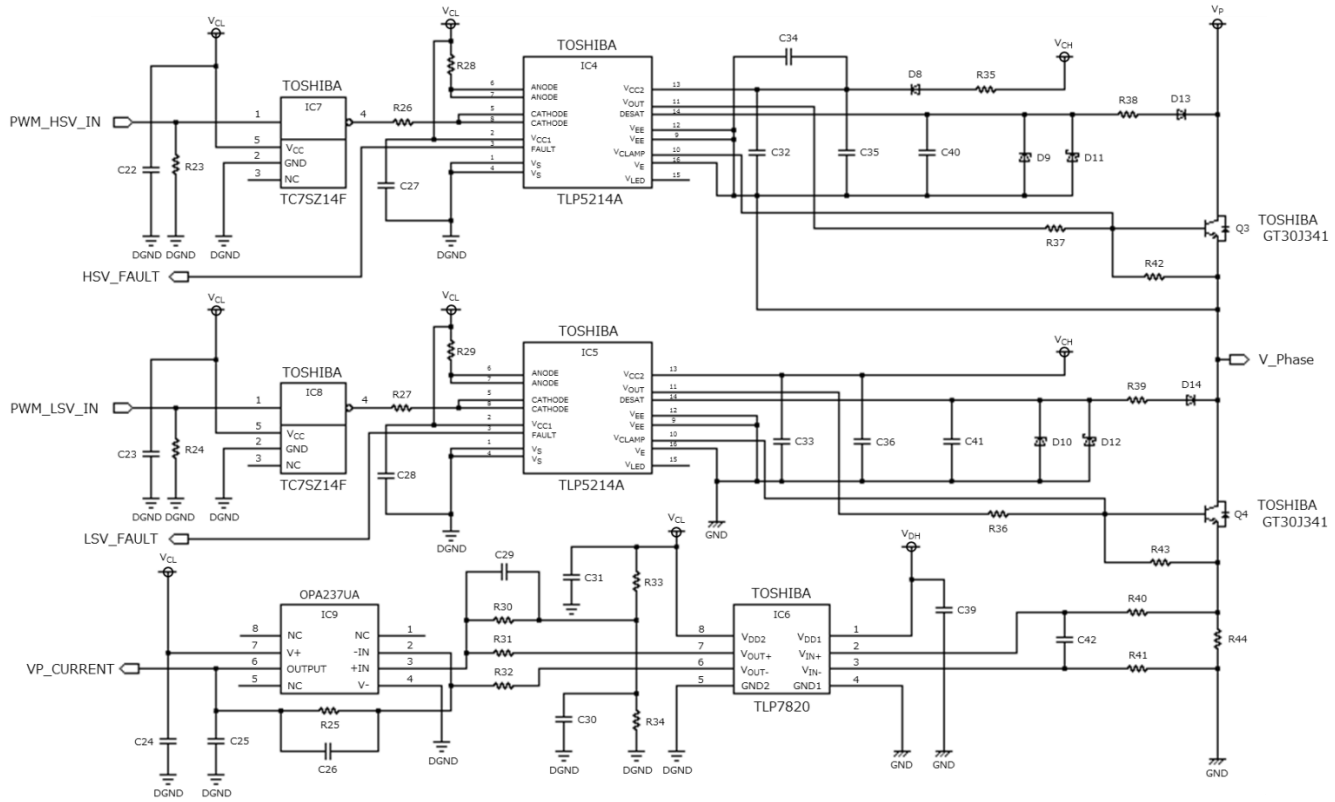
Due to affection between output drive frequency and the length of the cable, adjust and check the frequency with final product.



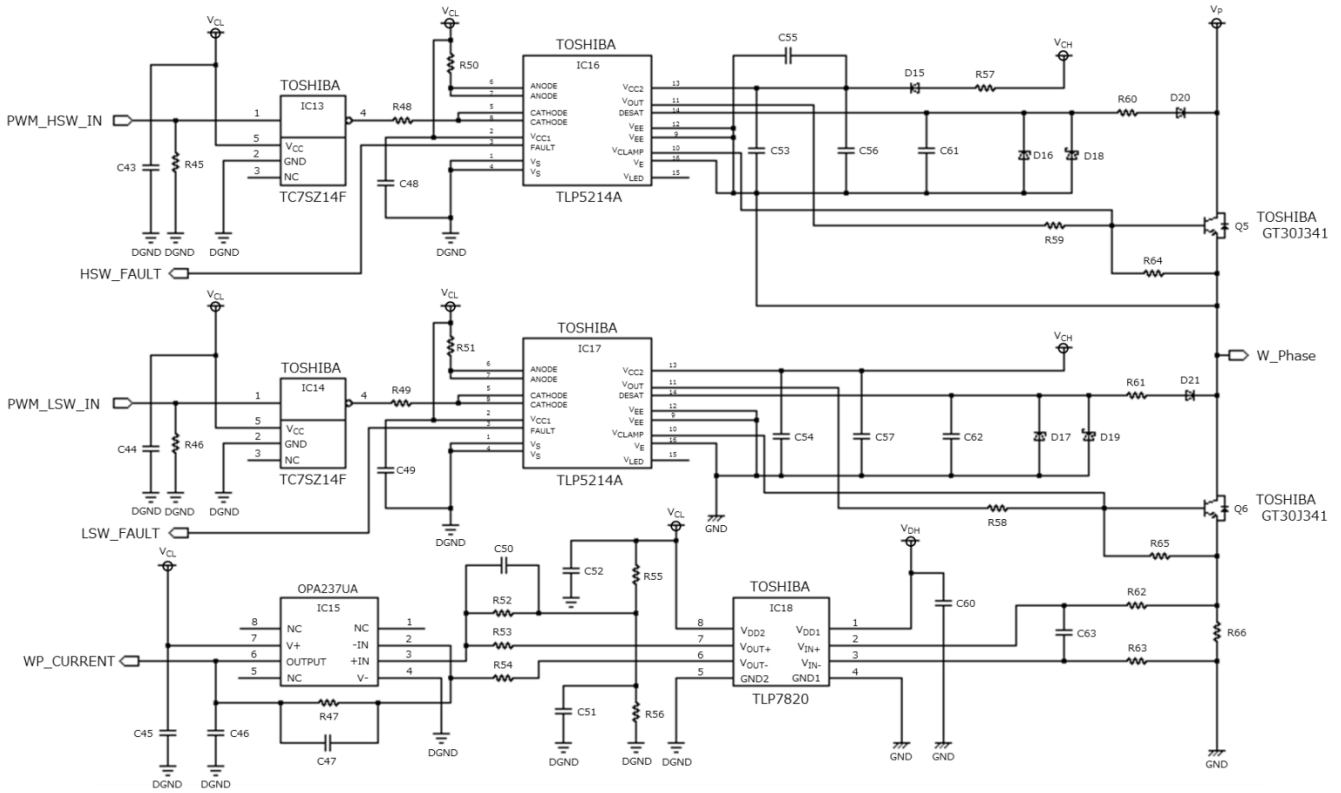
(a) Block diagram for inverter circuit 1



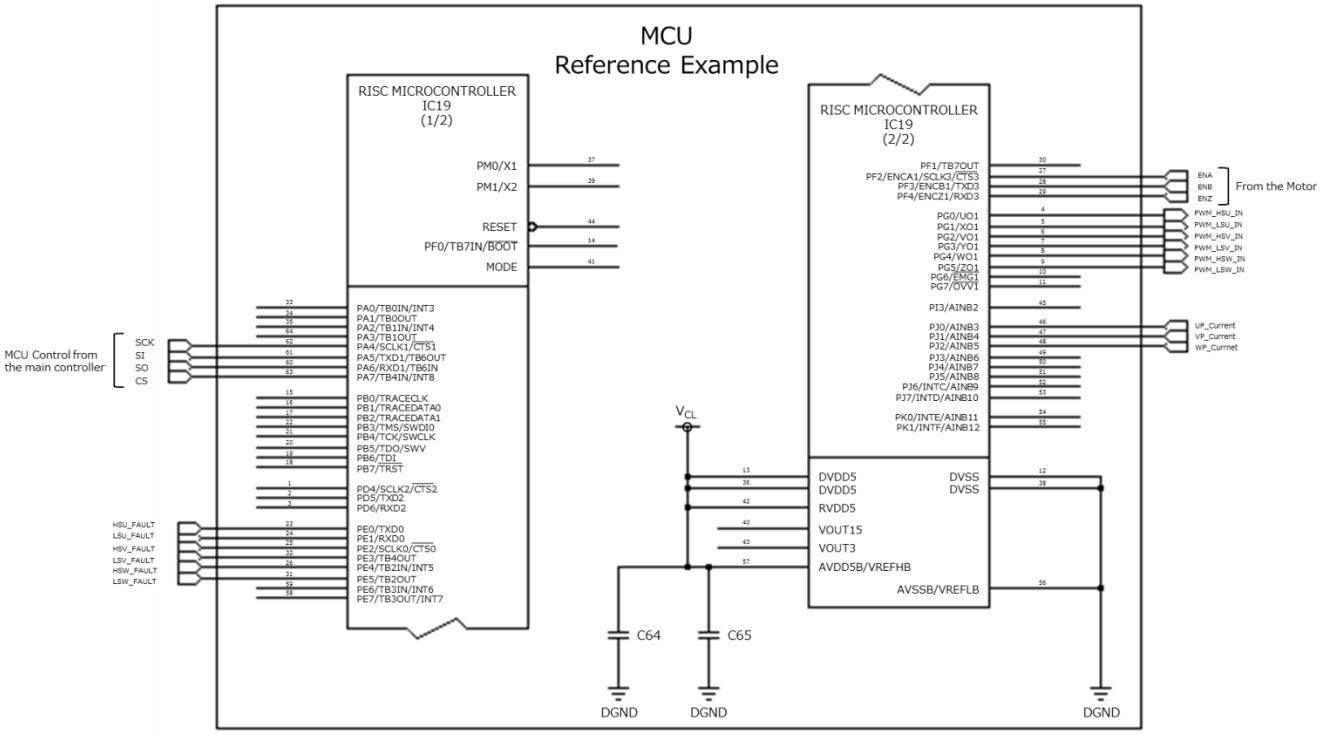
(b) U-Phase diagram for inverter circuit 1



(c) V-phase diagram for inverter circuit 1

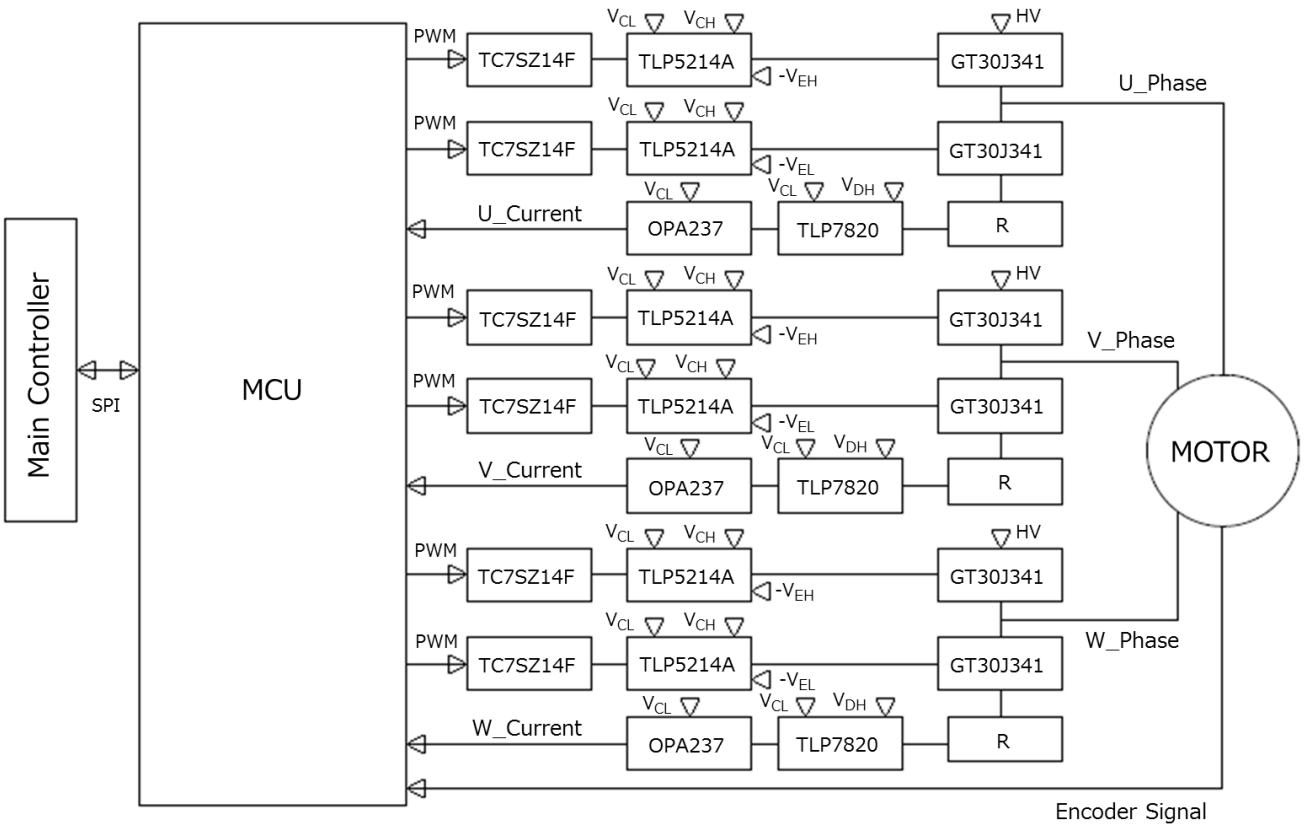


(d) W-phase diagram for inverter circuit 1

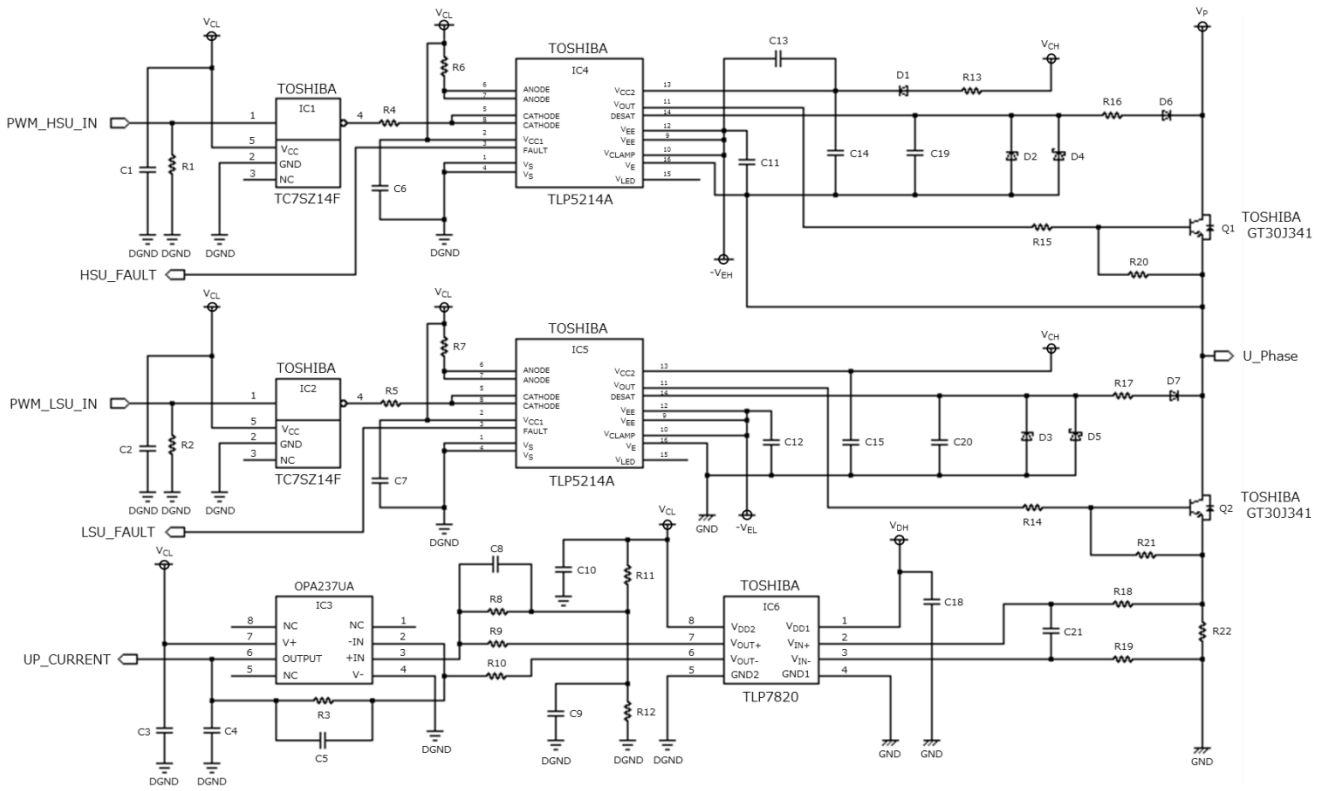


(e) MCU elements in inverter circuit 1

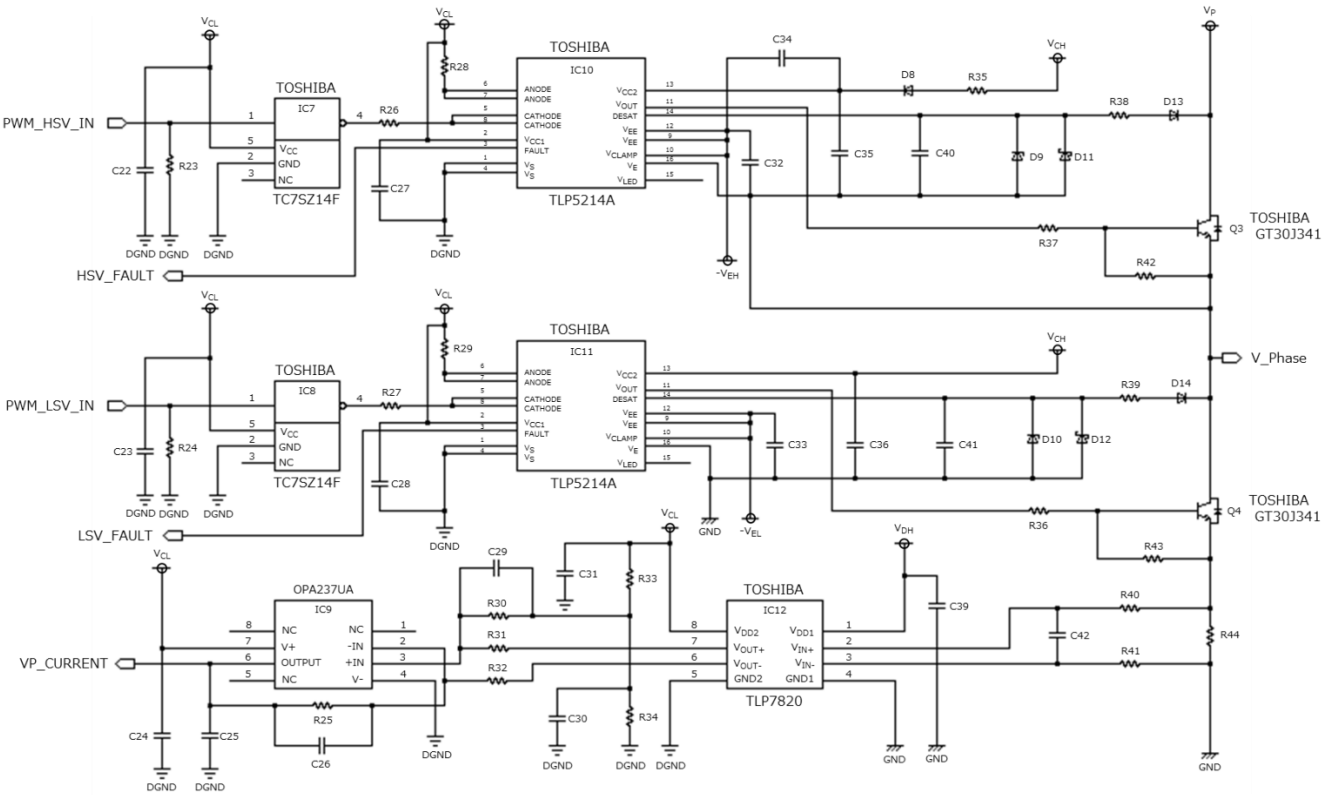
Figure 2.1 Inverter circuit 1 using TLP5214A (RD021-SCEMATIC1-01)



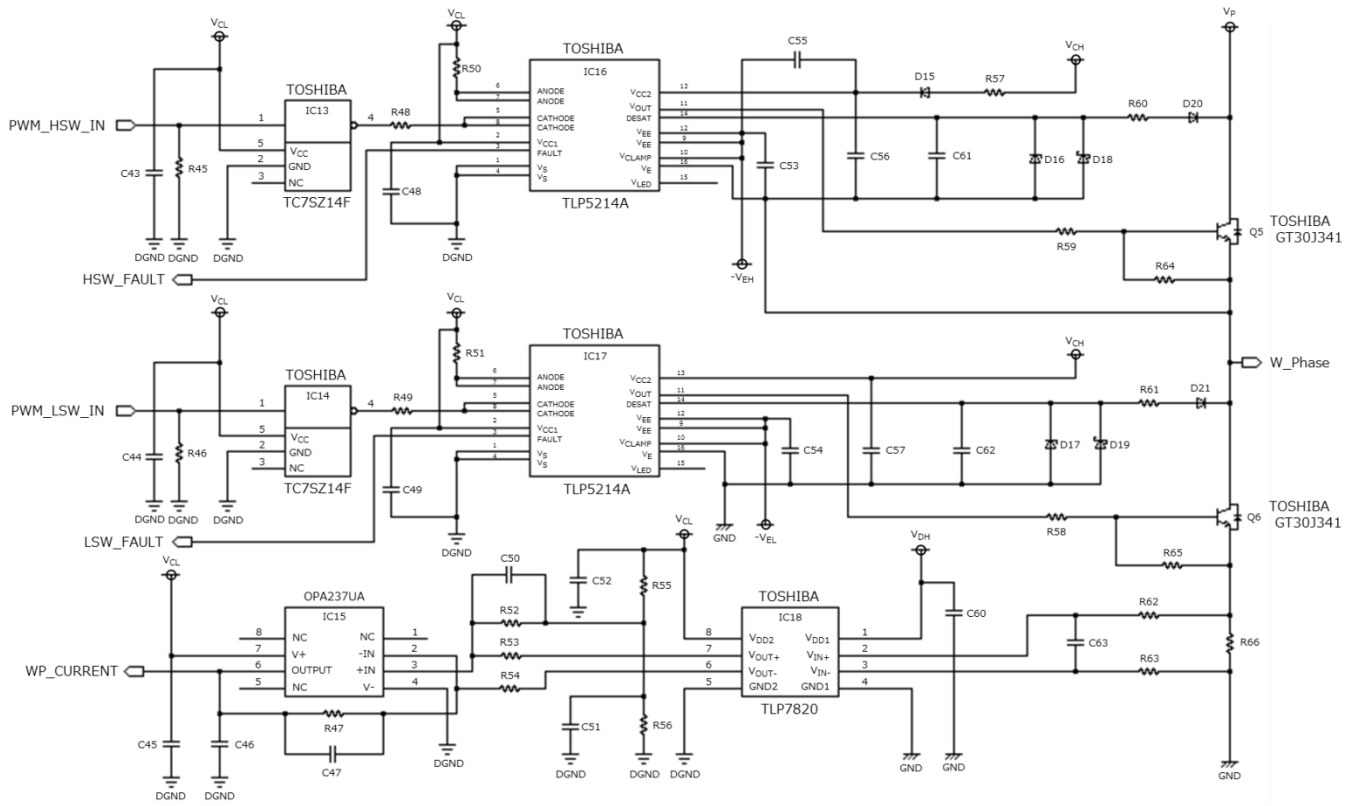
(a) Block diagram for inverter circuit 2



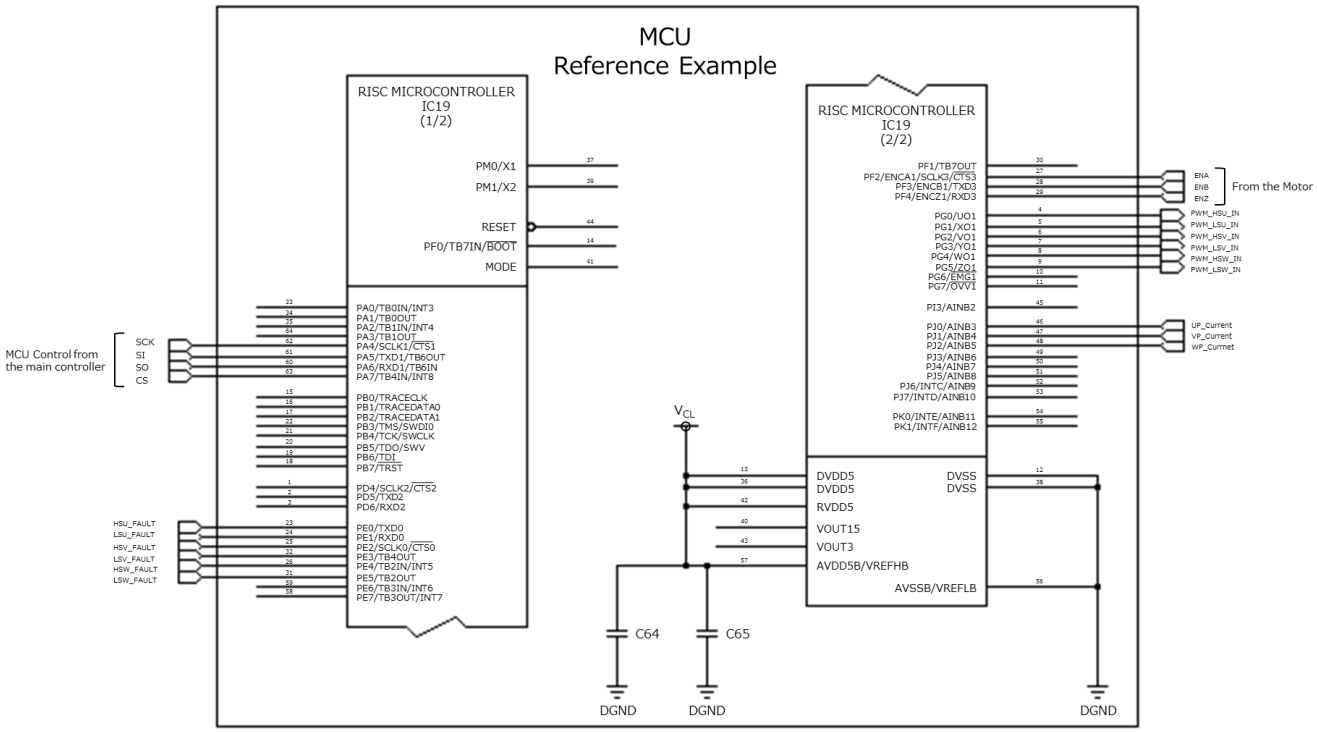
(b) U-phase diagram for inverter circuit 2



(c) V-phase diagram for inverter circuit 2



(d) W-phase diagram for inverter circuit 2



(e) MCU elements in inverter circuit 2

Figure 2.2 Inverter circuit 2 using TLP5214A (RD021-SCEMATIC2-01)

2.2. Bill of materials

Tables 2.3 and 2.4 are the bill of materials of the TLP5214A inverter circuits shown in Figures 2.1 and 2.2.

Table 2.3 Bill of material for TLP5214A inverter circuit 1 (RD021-SCEMATIC1-01)

No.	Label	Qty	Value	Product code	Manufacturer	Description	Package name	Standard dimensions in mm (inches)
1	IC1,IC2,IC7,IC8, IC13,IC14	6	-	TC7SZ14F	TOSHIBA	Buffer	SMV	2.9×2.8
2	IC3,IC9,IC15	3	-	OPA237	Texas Instruments	Op Amp	8SOIC	6x4.9
3	IC4,IC5,IC10, IC11,IC16,IC17	6	-	TLP5214A	TOSHIBA	Photocoupler	SO16L	10.3×10.0
4	IC6.IC12,IC18	3	-	TLP7820	TOSHIBA	Isolation Amplifier	SO8L	11x5.8
5	IC19	1	-	MCU	-	MCU	-	-
6	Q1,Q2,Q3,Q4, Q5,Q6	6	-	GT30J341	TOSHIBA	IGBT	TO-3P(N)	20x15.5
7	D1,D6,D7,D8, D13,D14,D15, D20,D21	9	-	CMF05	TOSHIBA	Diode	M-FLAT	2.4×4.7
8	D2,D3,D9,D10, D16,D17	6	-	CUZ8V2	TOSHIBA	Zener Diode	USC	2.5×1.25
9	D4,D5,D11,D12, D18,D19	6	-	CUS05F30	TOSHIBA	Diode	USC	2.5×1.25
10	R1,R2,R20,R23, R24,R42,R45, R46,R64	9	10kΩ			100 mW ±5%	1608	1.6 x 0.8 (0603)
11	R3,R8,R9,R10, R25,R30,R31, R32,R47,R52, R53,R54	12	10kΩ			100 mW ±0.5%	1608	1.6 x 0.8 (0603)
12	R4,R5,R6,R7, R26,R27,R28, R29,R48,R49, R50,R51	12	160Ω			100 mW ±5%	1608	1.6 x 0.8 (0603)
13	R11,R12,R33, R34,R55,R56	6	1kΩ			100 mW ±5%	1608	1.6 x 0.8 (0603)
14	R13,R16,R17, R35,R38,R39, R57,R60,R61	9	100Ω			250 mW ±5%	2012	2.0 x 1.2 (0805)
15	R14,R15,R36, R37,R58,R59	6	10Ω			100 mW ±5%	1608	1.6 x 0.8 (0603)
16	R18,R19,R40, R41,R62,R63	6	1kΩ			100 mW ±1%	1608	1.6 x 0.8 (0603)
17	R21,R43,R65	3	10kΩ			100 mW ±1%	1608	1.6 x 0.8 (0603)

No.	Label	Qty	Value	Product code	Manufacturer	Description	Package name	Standard dimensions in mm (inches)
18	R22,R44,R66	3	20mΩ	WSHP2818 R0200FEB	Vishay	10 W ±1%	-	7.1 x 4.6
19	C1,C2,C3,C6,C7, C10,C18,C22, C23,C24,C27, C28,C31,C39, C43,C44,C45, C48,C49,C52, C60	21	100nF			Ceramic, 50 V, ±10%	1608	1.6 x 0.8 (0603)
20	C4,C21,C25, C42,C46,C63	6	1nF			Ceramic, 50 V, ±10%	1608	1.6 x 0.8 (0603)
21	C5,C8,C26,C29, C47,C50	6	68pF			Ceramic, 50 V, ±10%	1005	1.0 x 0.5 (0402)
22	C9,C30,C51	3	10μF			Ceramic, 25 V, ±10%	1608	1.6 x 0.8 (0603)
23	C11,C12,C14, C15,C32,C33, C35,C36,C53, C54,C56,C57	12	1μF			Ceramic, 50 V, ±10%	2012	2.0 x 1.2 (0805)
24	C13,C34,C55	3	10μF			Ceramic, 6.3 V, ±10%	2012	2.0 x 1.2 (0805)
25	C19,C20,C40, C41,C61,C62	6	120pF			Ceramic, 50 V, ±10%	1608	1.6 x 0.8 (0603)

Table 2.4 Bill of material for TLP5214A inverter circuit 2 (RD021-SCEMATIC2-01)

No.	Label	Qty	Value	Product code	Manufacturer	Description	Package name	Standard dimensions in mm (inches)
1	IC1,IC2,IC7,IC8, IC13,IC14	6	-	TC7SZ14F	TOSHIBA	Buffer	SMV	2.9×2.8
2	IC3,IC9,IC15	3	-	OPA237	Texas Instruments	Op Amp	8SOIC	6x4.9
3	IC4,IC5,IC10, IC16,IC17	6	-	TLP5214A	TOSHIBA	Photocoupler	SO16L	10.3×10.0
4	IC6,IC12,IC18	3	-	TLP7820	TOSHIBA	Isolation Amplifier	SO8L	11x5.8
5	IC19	1	-	MCU	-	MCU	-	-
6	Q1,Q2,Q3,Q4, Q5,Q6	6	-	GT30J341	TOSHIBA	IGBT	TO-3P(N)	20x15.5
7	D1,D6,D7,D8, D13,D14,D15, D20,D21	9	-	CMF05	TOSHIBA	Diode	M-FLAT	2.4×4.7
8	D2,D3,D9,D10, D16,D17	6	-	CUZ8V2	TOSHIBA	Zener Diode	USC	2.5×1.25

No.	Label	Qty	Value	Product code	Manufacturer	Description	Package name	Standard dimensions in mm (inches)
9	D4,D5,D11, D12,D18,D19	6	-	CUS05F30	TOSHIBA	Diode	USC	2.5×1.25
10	R1,R2,R20,R23, R24,R42,R45, R46,R64	9	10kΩ			100 mW ±5%	1608	1.6 x 0.8 (0603)
11	R3,R8,R9,R10, R25,R30,R31, R32,R47,R52, R53,R54	12	10kΩ			100 mW ±0.5%	1608	1.6 x 0.8 (0603)
12	R4,R5,R6,R7, R26,R27,R28, R29,R48,R49, R50,R51	12	160Ω			100 mW ±5%	1608	1.6 x 0.8 (0603)
13	R11,R12,R33, R34,R55,R56	6	1kΩ			100 mW ±0.5%	1608	1.6 x 0.8 (0603)
14	R13,R16,R17, R35,R38,R39, R57,R60,R61	9	100Ω			250 mW ±5%	2012	2.0 x 1.2 (0805)
15	R14,R15,R36, R37,R58,R59	6	10Ω			100 mW ±5%	1608	1.6 x 0.8 (0603)
16	R18,R19,R40, R41,R62,R63	6	1kΩ			100 mW ±1%	1608	1.6 x 0.8 (0603)
17	R21,R43,R65	3	10kΩ			100 mW ±1%	1608	1.6 x 0.8 (0603)
18	R22,R44,R66	3	20mΩ	WSHP2818 R0200FEB	Vishay	10 W ± 1%	-	7.1 x 4.6
19	C1,C2,C3,C6, C7,C10,C18, C22,C23,C24, C27,C28,C31, C39,C43,C44, C45,C48,C49, C52,C60	21	100nF			Ceramic, 50 V, ±10%	1608	1.6 x 0.8 (0603)
20	C4,C21,C25, C42,C46,C63	6	1nF			Ceramic, 50 V, ±10%	1608	1.6 x 0.8 (0603)
21	C5,C8,C26,C29, C47,C50	6	68pF			Ceramic, 50 V, ±10%	1005	1.0 x 0.5 (0402)
22	C9,C30,C51	3	10μF			Ceramic, 25 V, ±10%	1608	1.6 x 0.8 (0603)
23	C11,C12,C14, C15,C32,C33, C35,C36,C53, C54,C56,C57	12	1μF			Ceramic, 50 V, ±10%	2012	2.0 x 1.2 (0805)
24	C13,C34,C55	3	10μF			Ceramic, 6.3 V, ±10%	2012	2.0 x 1.2 (0805)

No.	Label	Qty	Value	Product code	Manufacturer	Description	Package name	Standard dimensions in mm (inches)
25	C19,C20,C40, C41,C61,C62	6	120pF			Ceramic, 50 V, ±10%	1608	1.6 x 0.8 (0603)

For the detail of the TLP5214A → Click Here

For the detail of the TLP7820 → Click Here

For the detail of the GT30J341 → Click Here

For the detail of the CMF05 → Click Here

For the detail of the CUZ8V2 → Click Here

For the detail of the CUS05F30 → Click Here

For the detail of the TC7SZ14F → Click Here

3. Inverter circuit design guide

This section explains the key design consideration for an inverter circuit using the TLP5214A.

3.1. Blanking time

Blanking time (t_{BLANK}) is the time until overcurrent protection is enabled. The TLP5214A outputs a gate drive current from V_{OUT} in response to input signal, and DESAT is initiated at the same time. For products where the power device takes a long time to turn on, DESAT detects the voltage level and enters shutdown mode while the collector-emitter voltage (V_{CE}) is still decreasing. The t_{BLANK} value can be adjusted the time taken for voltage detection to occur, however it is important not to exceed the IGBT short-circuit withstand capability (IGBT time until failure in the presence of overcurrent).

t_{BLANK} is related to blanking capacitor (C_{BLANK}), DESAT threshold voltage (V_{DESAT}), blanking capacitor charging current (I_{CHG}) and DESAT leading edge blanking time ($t_{DESAT(LEB)}$) by the following equation:

$$t_{BLANK} = \frac{C_{BLANK} \times V_{DESAT}}{I_{CHG}} + t_{DESAT(LEB)}$$

Where V_{DESAT} and I_{CHG} are constants (standard values are 6.5 V and 240 μA respectively), and $t_{DESAT(LEB)}$ is 1.1μs (Typ.). Regarding Figure 3.1, it has GT30J341 (Discrete IGBT) which has 5μs (t_{sc}) value, t_{BLANK} must be set not exceeding this value. If we use C_{BLANK} = 120 pF, then:

$$t_{BLANK} = \frac{120 \times 10^{-12} \ (F) \times 6.5 \ (V)}{240 \times 10^{-6} \ (A)} + 1.1 \times 10^{-6} \ (s) = \mathbf{4.35\ \mu s} < 5\mu s$$

A higher C_{BLANK} value would change the slope of the DESAT terminal voltage, meaning a longer time for overcurrent protection to be enabled shown in Figure 3.2. The C_{BLANK} value should be set to a t_{BLANK} time that is within the short-circuit withstand capability period for the power device without causing overcurrent detection errors. Figure 3.2 shows the relation between t_{BLANK} and C_{BLANK}. Note that in actual circuits, t_{BLANK} is also affected by not only C_{BLANK} but also factors such as the parasitic capacitance of diodes on the DESAT line.

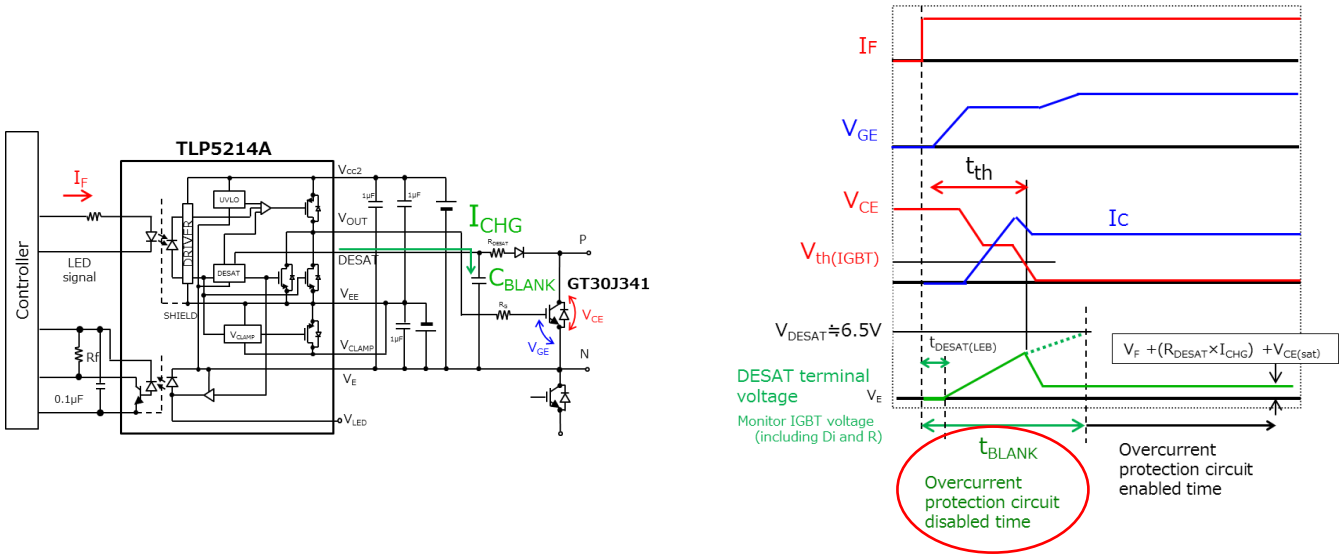


Figure 3.1 Blanking time t_{BLANK}

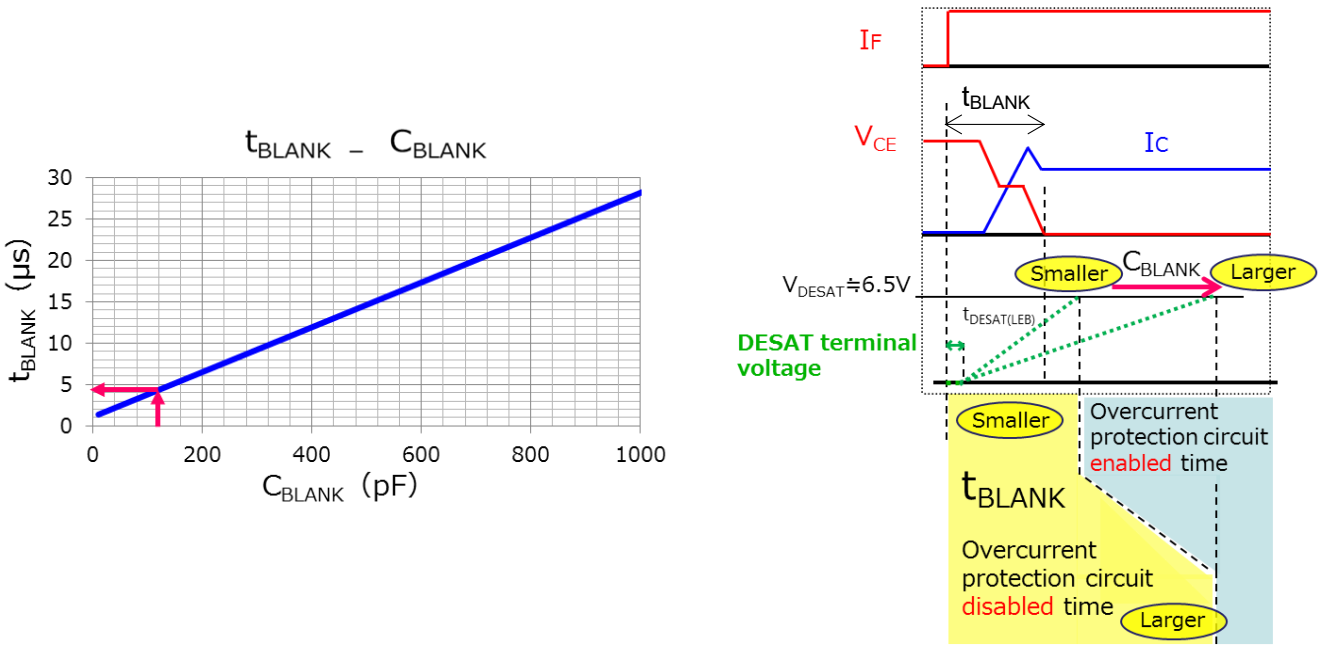


Figure 3.2 Blanking capacity C_{BLANK} vs. blanking time t_{BLANK}

3.2. IGBT short-circuit threshold voltage

The DESAT terminals monitor the collector-emitter voltage V_{CE} of the external IGBT during I_F input. The DESAT protection circuit activates when the terminal voltage V_{DESAT} exceeds 6.5 V (Typ.). The monitored V_{CE} value is different from the actual IGBT V_{CE} one due to monitoring through diode and resister. Figure 3.3 shows how to adjust the short-circuit threshold voltage when diodes are used. If $V_{th(IGBT)}$ is defined the short-circuit threshold voltage based on the IGBT voltage, we can use multiple diodes connection to the DESAT terminals as shown in Figure 3.3, considering the IGBT safe operating range, the voltage drop for V_F during multiple elements will force $V_{th(IGBT)}$ down to a new value (New $V_{th(IGBT)}$) as per the equation below. It is important to choose diodes with high tolerant and fast reverse recovery time.

$$NEW\ V_{th(IGBT)} = V_{DESAT} - (n \times V_F + R_{DESAT} \times I_{CHG})$$

where *n* is the number of diodes

For circuits shown in Fifure2.1 and Figure2.2, GT30J341 IGBT ($V_{GE(OFF)}$ = 5.5 V), a single CMF05 diode (V_F = 2.7 V @ 50 μA) and 100 Ω R_{DESAT} are used. Therefore we have:

$$New\ V_{th(IGBT)} = 6.5 - (1 \times 2.7\ (V) + 100(\Omega) \times 50(\mu A) \fallingdotseq \mathbf{3.8\ V}$$

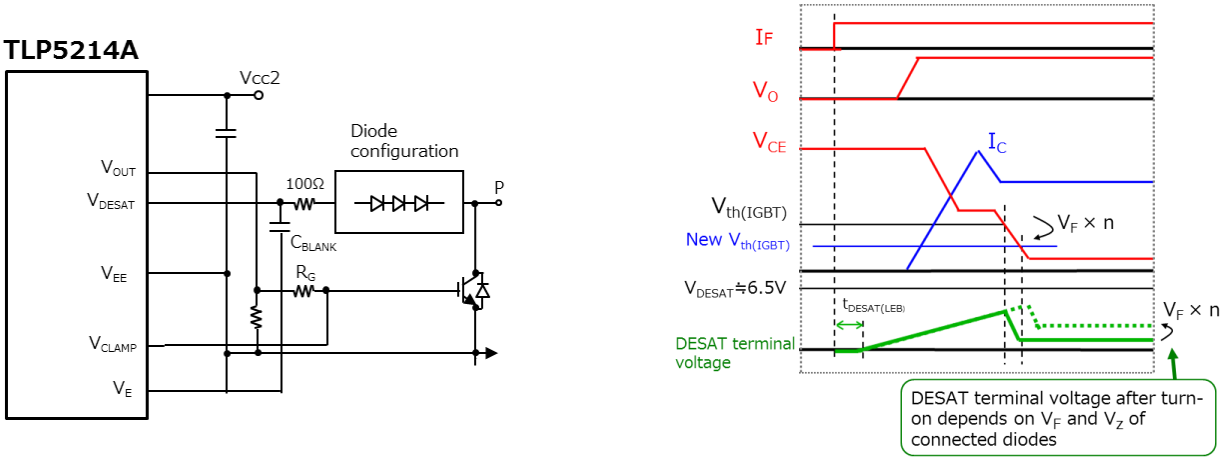


Figure 3.3 Modifying the short-circuit threshold voltage

3.3. Control signal waveform shaping

In case of the control board and motor control board are separated, the longer distance to the TLP5214A may cause generating inductance and other impacts during wiring and the input signal slope is potentially changed.

In Figure 3.4, it has an additional hysteresis buffer circuit before the TLP5214A input terminal to shape the input signal waveform.

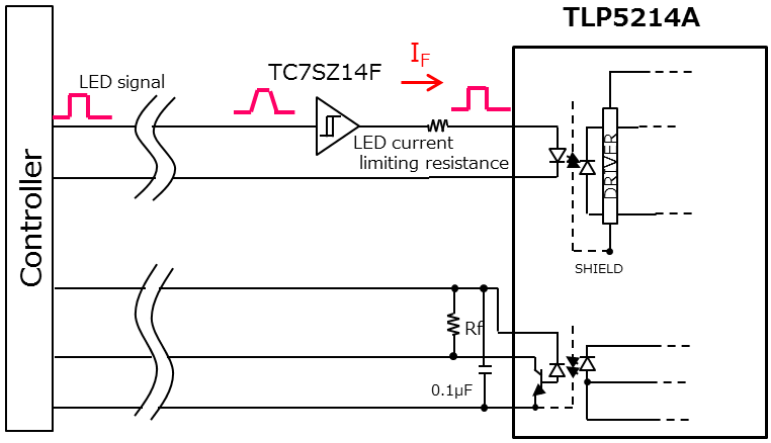


Figure 3.4 Control signal waveform shaping

3.4. Current control shunt resistor

In Figure 2.1 and Figure 2.2, they use the TLP7820 for motor control in a three shunt current detection configuration that measures three-phase current on the controller side. Details of the current detection circuit design are given in the TLP7820 document (RD013-RGUIDE-02).

For detail of reference guide for TLP7820 current detection circuit → Click Here

3.5. Thermal design

In order to supply electric charge to (or withdraw it from) the power device gate over a short period, the gate driver photocoupler has to generate (or absorb) large amounts of output current quickly during switching. With this reason, photocoupler switching loss and heat must also be considered. Switching loss is determined by many factors including the photocoupler drive frequency, drive voltage, gate capacity and gate resistance of power device. The loss of photo detection side accounts for the bulk of the photocoupler losses. Those losses generate heat, so most of the heat is at the photo detection side. Peripheral circuit design must take care of the maximum rated junction temperature for the light receiving chip and LED chip in the photocoupler.

The following definitions are used in this document.

P_{all}: total power loss in photocoupler
$P_{o,all}$: power loss in light receiving chip
P_D: power loss on LED side
I_F: LED forward current
V_F: LED forward voltage
$P_{o,DC}$: current consumption during DC operation
$P_{o(bias:on)}$:DC current consumption with LED on
$P_{o(bias:off)}$: DC current consumption with LED off
$P_{o,sw}$: power consumption during switching
duty: photocoupler duty ratio
E_{sw}: electrostatic energy during switching
I_{CCH}: H level supply current
I_{CCL}: L level supply current
V_{CC}: positive supply voltage on output side
V_{EE}: negative supply voltage on output side (V_{EE} < 0)
f_{sw} : switching frequency
R_g : gate resistance
$R_{on,H}$: photocoupler output resistance (high)
$R_{on,L}$: photocoupler output resistance (low)
C_g: gate capacity (Q_g = C_g x V_{CC} equivalent)
$I_{op,worst}$: maximum value of peak output current
$T_{j,LED}$: LED chip junction temperature*
$T_{j,Photo}$: light receiving chip junction temperature*
$R_{th(j-a),LED}$: thermal resistance of LED chip**
$R_{th(j-a),Photo}$: thermal resistance of light receiving chip**

* TLP5214A maximum rated value = 125 °C
** Thermal resistance of TLP5214A on standard JEDEC substrate:
$R_{th(j-a),LED}$: 0.165 ℃/mW $R_{th(j-a),Photo}$: 0.07 ℃/mW

Figure 3.5 shows the calculation model (which applies equally to TLP5214A).

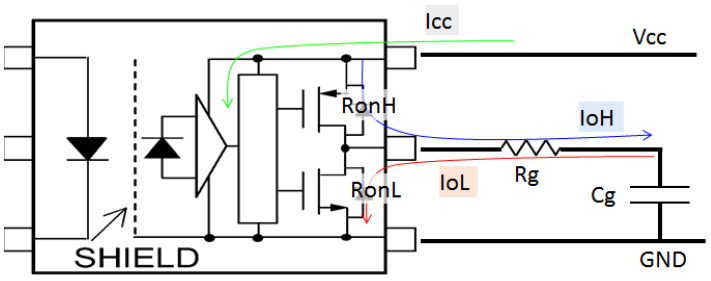


Figure 3.5 Calculating power loss in the light receiving chip

The procedure for determining power loss in the photocoupler light receiving chip is given below. The power loss in the light receiving chip during switching operation is the sum of power consumption during DC operation and switching loss.

(1) Power loss in light receiving chip

$$P_{o,all} = P_{o,DC} + P_{o,sw}$$

(2) Power consumption during DC operation

$$P_{o,DC} = P_{o(bias:on)} + P_{o(bias:off)}$$

$$= duty \times I_{CCH} \times (V_{cc} + |V_{EE}|) + (1 - duty) \times I_{CCL} \times (V_{cc} + |V_{EE}|)$$

(3) Power consumption during switching

The amount of electrostatic energy E_{sw} stored and/or released in a switching operation C_g is defined by:

$$E_{sw} = \frac{C_g \times (V_{cc} + |V_{EE}|)^2}{2}$$

Given that f_{sw} of the C_g electrostatic energy E_{sw} is consumed by R_g, $R_{on,H}$ and $R_{on,L}$ per second, the power consumption during switching $P_{o,sw}$ is calculated as:

$$P_{o,sw} = E_{sw} \times \left[\frac{R_{on,H}}{(R_g + R_{on,H})} + \frac{R_{on,L}}{(R_g + R_{on,L})}\right] \times f_{sw}$$

(4) The following equations can be used to calculate the peak output current and the maximum value of the estimated peak output current of the photocoupler output stage MOSFET on-resistance $I_{op,worst}$ (note that peak output current will generally be lower in practice, since a photocoupler output stage MOSFET on-resistance is also present).

$$I_{op,worst} = \frac{(V_{cc} + |V_{EE}|)}{R_g}$$

This value is used to determine the characteristics curve for the photocoupler output stage on-resistance.

$$R_{on,H} = \frac{[V_{OH} - V_{CC}] \ (@ \ I_{op,worst})}{I_{op,worst}}$$

Note: $[V_{OH} - V_{CC}] \ (@ \ I_{op,worst})$ is taken from the characteristics curve

$$R_{on,L} = \frac{V_{OL} \ (@ \ I_{op,worst})}{I_{op,worst}}$$

Note: $V_{OL} \ (@ \ I_{op,worst})$ is taken from the characteristics curve

We substitute the resistance value into the $P_{o,sw}$ equation to find the switching power consumption.

(5) LED power loss

LED power loss is given by the following equation:

$$P_D = duty \times I_F \times V_F$$

Calculation example

The following circuit conditions are used for calculation example.

V_{CC} = 15 V, V_{EE} = 0 V, I_{CCH} = 3.8 mA, I_{CCL} = 3.8 mA (rated maximum for TLP5214A)

C_g = 25 nF, R_g = 10 Ω, duty = 0.5, f_{sw} = 10 kHz, Ta = 110°C

I_F = 10 mA, V_F = 1.45 V (TLP5214A I_F- V_F curve with Ta = 110°C, I_F = 10 mA)

Light-receiving DC loss

$$P_{o,DC} = P_{o(bias:on)} + P_{o(bias:off)}$$

$$= duty \times I_{CCH} \times (V_{cc} + |V_{EE}|) + (1 - duty) \times I_{CCL} \times (V_{cc} + |V_{EE}|)$$

$$= 0.5 \times 3.8(mA) \times 15(V) + 0.5 \times 3.8(mA) \times 15(V) = \mathbf{57 \ mW}$$

Peak output current

$$I_{op,worst} = \frac{(V_{cc} + |V_{EE}|)}{R_g} = \frac{15(V)}{10(\Omega)} = \mathbf{1.5\ A}$$

Photocoupler output stage on-resistance

If we substitute 1.5 A into the V_O-I_{op} characteristics curve for TLP5214A (Figure 3.6) we get [V_{OH}-V_{CC}](@ $I_{op,worst}$) = -1.2 V and V_{OL}(@ $I_{op,worst}$) = 1.0 V, which gives us on-resistances values as follows:

$$R_{on,H} = \frac{[V_{OH} - V_{CC}]\ (@\ I_{op,worst})}{I_{op,worst}} = \frac{-1.2(V)}{-1.5(A)} = \mathbf{0.8\ \Omega}$$

$$R_{on,L} = \frac{V_{OL}\ (@\ I_{op,worst})}{I_{op,worst}} = \frac{1.0(V)}{1.5(A)} = \mathbf{0.7\ \Omega}$$

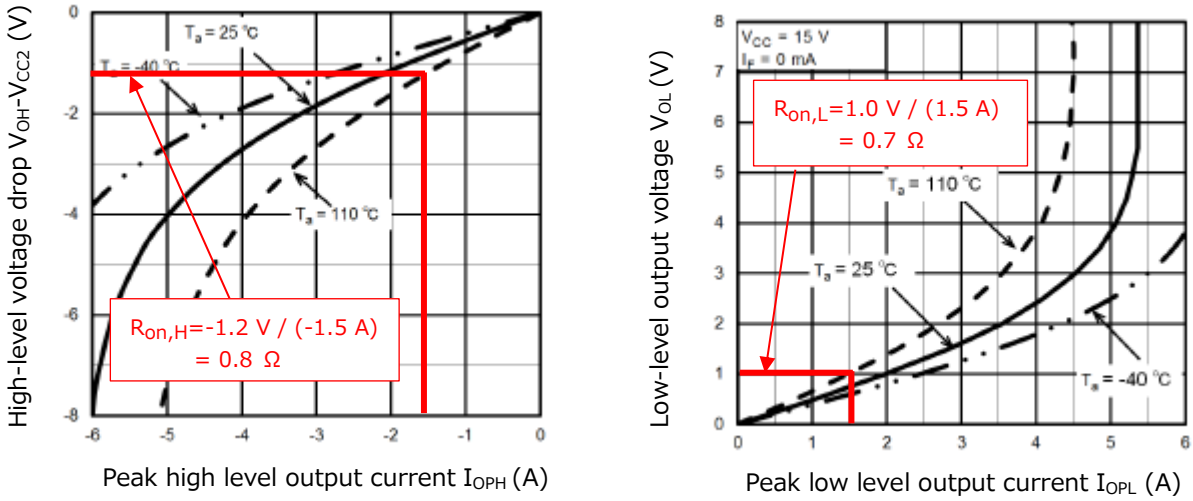


Figure 3.6 Estimating the photocoupler output stage MOSFET on-resistance from the V_O-I_{op} curve

Switching loss

$$P_{o,sw} = E_{sw} \times \left[\frac{R_{on,H}}{(R_g + R_{on,H})} + \frac{R_{on,L}}{(R_g + R_{on,L})}\right] \times f_{sw}$$

$$= \frac{C_g \times (V_{cc} + |V_{EE}|)^2}{2} \times \left[\frac{R_{on,H}}{(R_g + R_{on,H})} + \frac{R_{on,L}}{(R_g + R_{on,L})}\right] \times f_{sw}$$

$$= \frac{25(nF) \times (15(V))^2}{2} \times \left[\frac{0.8(\Omega)}{(10(\Omega) + 0.8(\Omega))} + \frac{0.7(\Omega)}{(10(\Omega) + 0.7(\Omega))}\right] \times 10(kHz)$$

$$= \mathbf{3.9\ mW}$$

Loss in the light receiving chip is given by the following equation:

$$P_{o,all} = P_{o,DC} + P_{o,sw} = 57(mW) + 3.9(mW) = \mathbf{60.9\ mW}$$

LED power loss

LED power loss is given by the following equation:

$$P_D = duty \times I_F \times V_F = 0.5 \times 10(mA) \times 1.45(V) = \mathbf{7.3\ mW}$$

Total photocoupler power consumption

P_{all} is calculated as follows:

$$P_{all} = P_D + P_{o,all} = 7.3\ (mW) + 60.9(mW) = \mathbf{68.2\ mW}$$

A simplified estimate of the junction temperatures in this example ($T_{j,LED}$ and $T_{j,Photo}$), ignoring thermal interference between the LED and light-receiving chip, is shown below.
This gives us an idea of the usable range in terms of thermal considerations.

$$T_{j,LED} = T_a + \Delta T_{j,LED} = 110(℃) + 0.165(℃/mW) \times 7.3(mW) = \mathbf{111.2}\ ℃ < \mathbf{125}\ ℃$$

$$T_{j,Photo} = T_a + \Delta T_{j,Photo} = 110(℃) + 0.07(℃/mW) \times 60.9(mW) = \mathbf{114.3}\ ℃ < \mathbf{125}\ ℃$$

Thermal resistance is different from the material of the substrate, the land pattern and the layer structure. Also, the photocoupler output terminal capacitance includes the parasitic capacitance of the substrate. So the above calculation should be considered no more than a general guide.

Note

When the TLP5214A enters protection mode the FAULT output LED on the feedback side lights and the FAULT terminal output switches from high to low to indicate an IGBT error. If protection mode is continued, the FAULT output LED on the secondary side also lights and a current of approximately 10 mA starts flowing between the V_{CC2} and V_E terminals, increasing the power loss on the secondary side. When protection mode activate, the system must be shut down and reboot immediately (see Figures 3.7 and 3.8).

Ex) V_{CC2} = 30 V, FAULT mode engaged

If feedback LED current = 10 mA and the voltage at the light-receiving chip on the secondary side is 28 V (not including LED voltage drop), then power loss in the light-receiving chip is 28 V x 10 mA = 280 mW. If we take into account thermal resistance on the light-receiving chip side of the TLP5214A, the temperature increase is 0.07 x 280 = 19.6°C. This could be an issue in a hot operating environment.

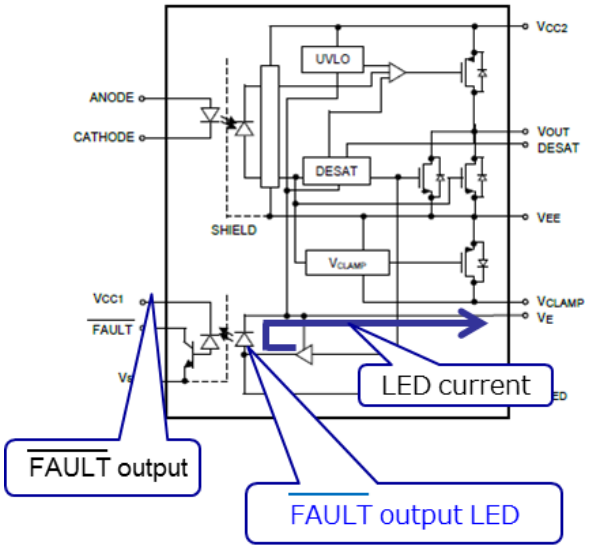


Figure 3.7 Internal circuit diagram (operation path during fault)

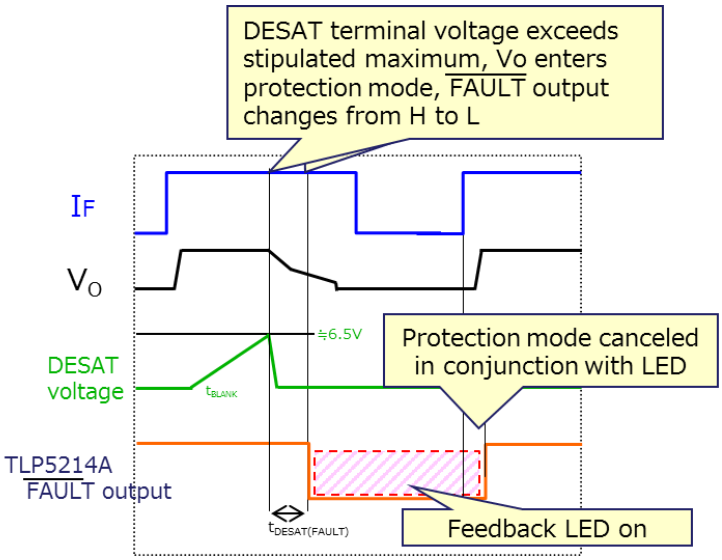


Figure 3.8 TLP5214A timing chart (protection engaged)

4. Product overview

4.1. General

The TLP5214A is an advanced, highly integrated 4.0A output current IGBT gate drive photocoupler housed in a long creepage and clearance SO16L package.

- Peak output current: ±4.0 A (max.)
- Operating temperature range: -40 to +110°C
- Supply current: 3.8 mA (max.)
- Power supply voltage: 15 to 30 V
- Threshold input current: 6 mA (max.)
- Propagation delay (t_{pLH} / t_{pHL}): 150 ns (max.)
- DESAT leading edge blanking time: 1.1 μs (typ.)
- Common mode transient immunity: ±35 kV/μs (min.)
- Isolation voltage: 5,000 Vrms (min.)
- Safety standardsd

  UL approved: UL1577, File No. E67349

  c-UL approved: CSA (Component Acceptance Service) No. 5A, File No. E67349

  Option (D4) VDE: DIN EN60747-5-5, EN60065 or EN60950-1, EN62368-1 *

  CQC: GB4943.1 and GB8898 Japan Factory (Pending)

  * When a EN60747-5-5 approved type is needed, please designate “Option(D4)”

4.2. Appearance and terminal configuration

General appearance and markings

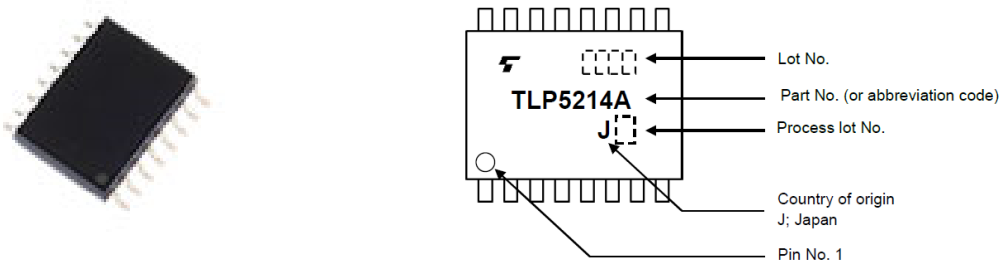
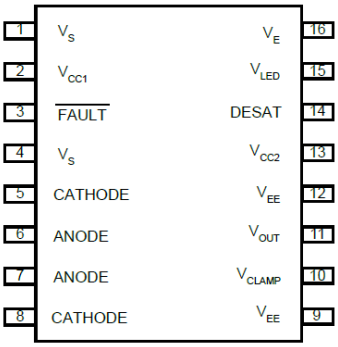


Figure 4.1 TLP5214A appearance and markings

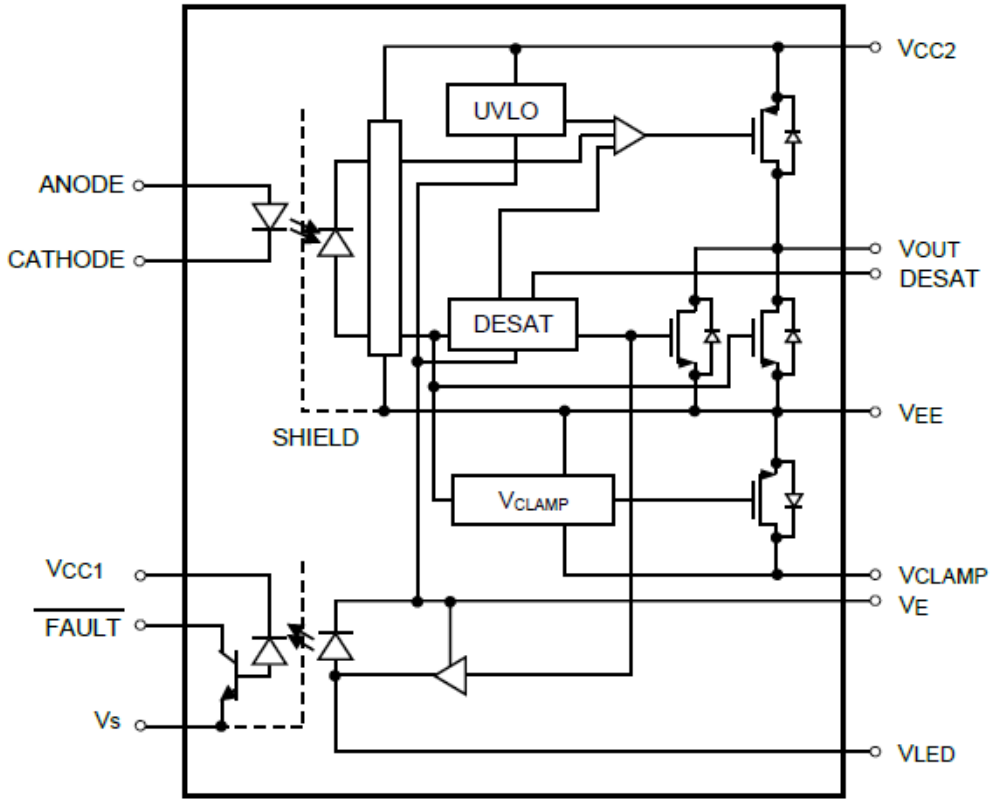


1: V_S
2: V_{CC1}
3: $\overline{FAULT}$
4: V_S
5: CATHODE
6: ANODE
7: ANODE
8: CATHODE
9: V_{EE}
10: V_{CLAMP}
11: V_{OUT}
12: V_{EE}
13: V_{CC2}
14: DESAT
15: V_{LED}
16: V_E

Terminal No.	Name	I/O	Description	Internal circuit configuration
1	V_S	GND	GND on input side	Tr.(Open collector)
2	V_{CC1}	IN	Positive supply on input side	Tr./Photo Di
3	$\overline{FAULT}$	OUT	IGBT short (non-saturation) fault feedback; outputs L when IGBT non-saturation detected	Tr.(Open collector)
4	V_S	GND	GND on input side	Tr.(Open collector)
5	CATHODE	GND	LED cathode on input side	LED
6	ANODE	IN	LED anode on input side	LED
7	ANODE	IN	LED anode on input side	LED
8	CATHODE	GND	LED cathode on input side	LED
9	V_{EE}	IN	Negative supply on output side; connect to V_E if using positive supply (V_{CC2}) only	DMOS/CMOS
10	V_{CLAMP}	IN	Active mirror clamp terminal; connect to IGBT gate (or to V_{EE} if unused)	DMOS
11	V_{OUT}	OUT	Output for IGBT turn-on/turn-off	DMOS
12	V_{EE}	IN	Negative supply on output side; connect to V_E if using positive supply (V_{CC2}) only	DMOS/CMOS
13	V_{CC2}	IN	Positive supply on output side	DMOS/CMOS
14	DESAT	IN	IGBT short (non-saturation) detection terminal; monitors V_{CE} through high-voltage FRD	CMOS
15	V_{LED}	IN	Feedback LED test terminal; leave OPEN for user use	LED/CMOS
16	V_E	GND	Supply common on output side	-

Figure 4.2 TLP5214A terminals

4.3. Internal circuit block diagram



Note: 1 μF bypass capacitor required between pins 9 (V_{EE}) and 13 (V_{CC2}) and between pins 13 and 16 (V_E).

Figure 4.3 TLP5214A internal circuit block diagram

4.4. Truth table

I_F	UVLO (V_{CC2}-V_E)	DESAT (14 pin DESAT terminal input)	FAULT (3 pin FAULT terminal output)	V_O
OFF	Not Active ($>V_{UVLO}^+$)	Not Active	High	Low
ON	Not Active ($>V_{UVLO}^+$)	Low ($<V_{DESATth}$)	High	High
ON	Not Active ($>V_{UVLO}^+$)	High ($>V_{DESATth}$)	Low (FAULT)	Low
ON	Active ($<V_{UVLO}^-$)	Not Active	High	Low
OFF	Active ($<V_{UVLO}^-$)	Not Active	High	Low

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