Single-Output High-Side N-Channel Power MOSFET Gate Driver

Application and Circuit of the TPD7104AF

Reference Guide

RD016-RGUIDE-03

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

Table of Contents

1. Overview

Mechanical relays have traditionally been used as switches to open and close a path between a power supply (e.g., Battery) and a load. However, because mechanical contacts have limited life wearing out with on/off cycles, semiconductor-based solid-state relays are coming into widespread use for applications requiring long-term reliability. Increasing of complex system requirement, solid-state relays must have more capability, especially a load switch with low-on-resistance discrete N-channel power MOSFETs can be used to create a high-current solid-state relay while reducing its power loss and heat generation.

The TPD7104AF is a single-output N-channel power MOSFET gate driver with a charge pump for high-side switch applications and it can realize a high current load switch with external discrete N-channel MOSFETs. The TPD7104AF also has a comparator for Load Short-circuit (Overcurrent) Detection and a Power Supply Reverse Connection Protection circuit in order to protect and ensure safe operation of high-current applications that have unexpected such kind of accidents.

This reference guide focuses on the operations and applications of load short-circuit detection and Power Supply Reverse Connection Protection available with the TPD7104AF that are crucial for the safe function of systems with high-current load switches.
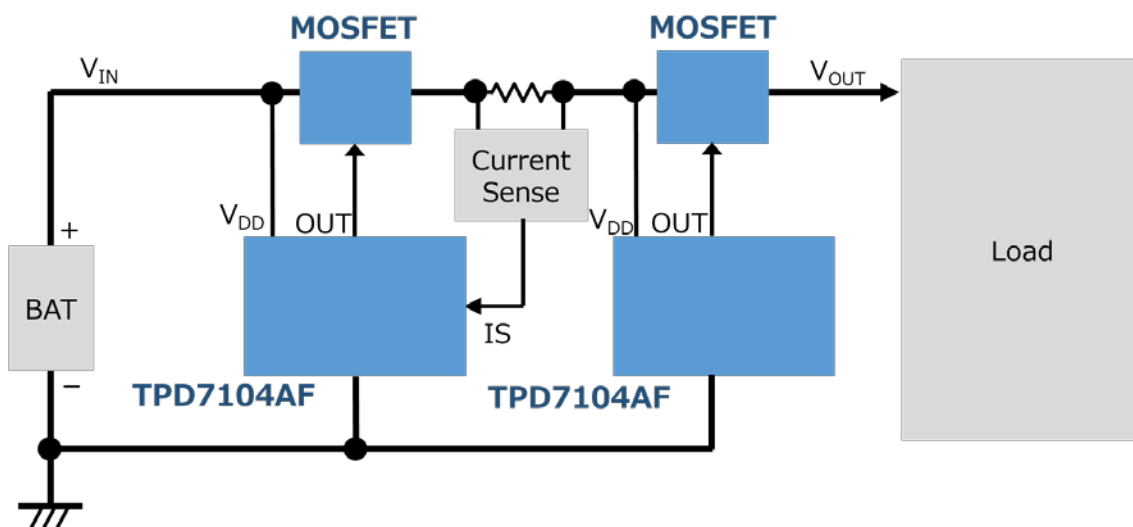
For details of other features and functions of the TPD7104AF, see its datasheet.

To download the datasheet for the TPD7104AF → [Click Here]

1.1. Target applications

- Solid-state relays
- Battery management systems (BMS)

Circuit example

* Toshiba offers a portfolio of MOSFETs suitable for these applications.

For details of MOSFETs → [Click Here]

2. Load Short-circuit (Overcurrent) Detection circuit
2.1. Circuit example

Figure 2.1.1 shows an example of a circuit for Load Short-circuit (Overcurrent) Detection. In this circuit, two MOSFETs are connected in series and the TPD7104AF that drives MOSFET1 is used for Load Short-circuit (Overcurrent) Detection.
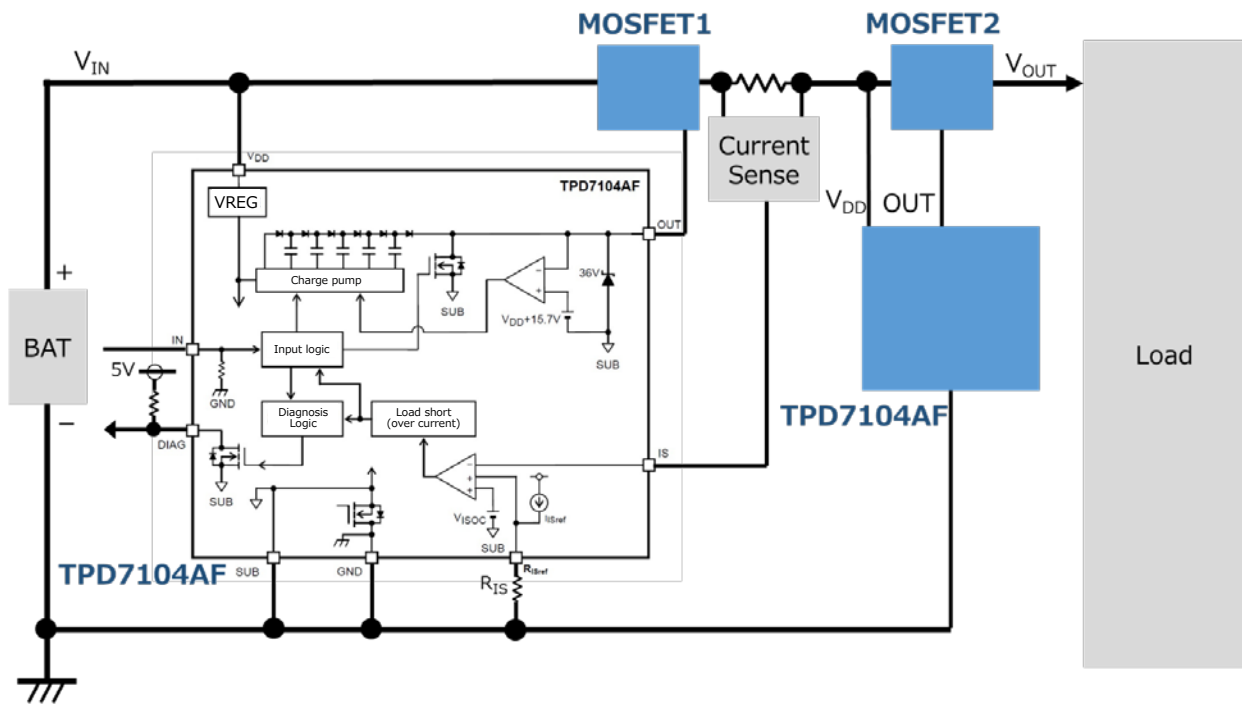

Figure 2.1.1 Example of a Load Short-circuit (Overcurrent) Detection circuit and the TPD7104AF internal block diagram

When a load current increases, the TPD7104AF detects a Load Short-circuit (Overcurrent) condition since the IS pin voltage (V_{IS}) reaches the threshold voltage (V_{det}). At this time, the TPD7104AF acts:

- Disables the OUT output to shut down the load current.
- Turn the DIAG output High to indicate a load short-circuit condition.

The threshold voltage (V_{det}) for overcurrent detection is programmable via the R_{ISref} pin. When the R_{ISref} pin is left open, V_{det} is equal to the default V_{ISOC} value (1.02V typical). To set V_{det} to a voltage lower than the default, connect a resistor (R_{IS}) between the R_{ISref} and GND pins. In this case, V_{det} is equal to the voltage (V_{RISref}) derived from R_{IS} and the internal constant-current source (I_{ISREF}=38 µA typical) associated with the R_{ISref} pin. However, V_{det} becomes equal to V_{ISOC} when V_{RISref} exceeds V_{ISOC}.

2019-05-10
Rev.3

Figure 2.1.2 shows the relationship between R_{IS} and V_{det}.

How to set V_{det} with R_{IS}:
1. When the R_{ISref} pin is open:

   $V_{det} = V_{ISOC}$ (1.02V typical)
2. When a resistor (R_{IS}) is connected to the R_{ISref} pin and $V_{RISref} \leq V_{ISOC}$:

   $V_{det} = V_{RISref} = I_{ISREF} \times R_{IS} = 38\mu A$ (typical) $\times R_{IS}$
3. When a resistor (R_{IS}) is connected to the R_{ISref} pin and $V_{RISref} > V_{ISOC}$:

   $V_{det} = V_{ISOC}$ (1.02V typical)
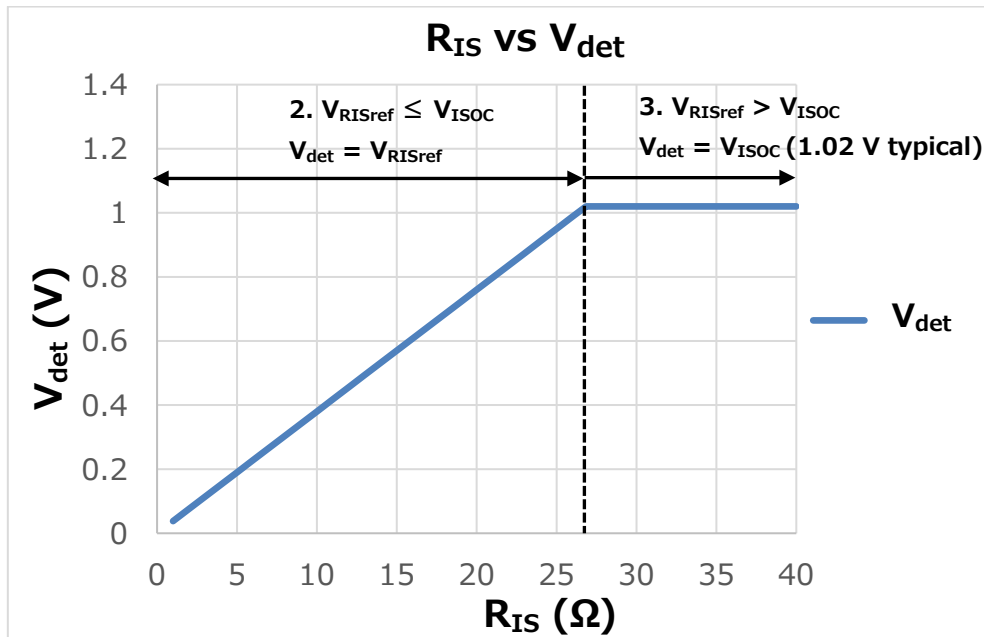
Figure 2.1.2 Relationship between R_{IS} and V_{det}

2.2. Timing chart

Figure 2.2.1 shows a timing chart for Load Short-circuit (Overcurrent) Detection.

Figure 2.2.1 Load Short-circuit (Overcurrent) Detection timing

Note: Upon detection of a load short-circuit (overcurrent) condition, the output shuts down and remains latched to protect (turn off) the driven power MOSFET. At this time, the diagnostic output, DIAG, is driven High. Setting V_{IN} to a Low level de-latches the output.

3. Power Supply Reverse Connection Protection circuit
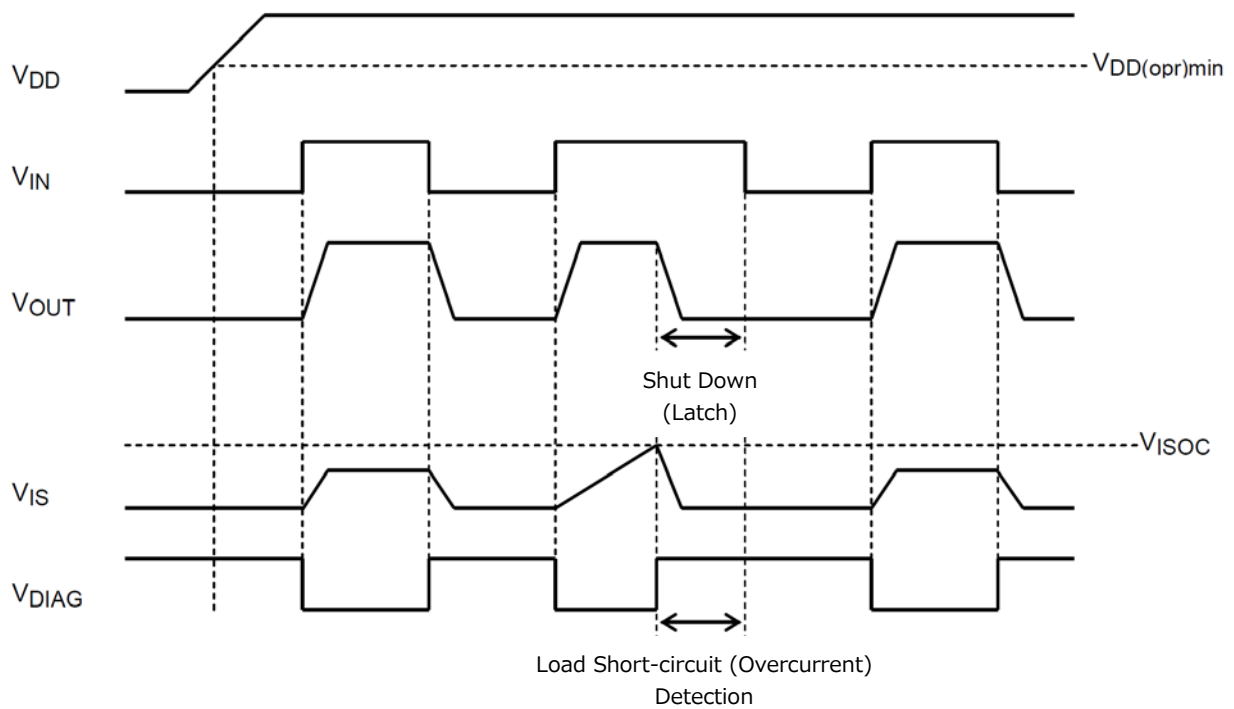
3.1. Circuit example

Figure 3.1.1 shows an example of a circuit for Power Supply Reverse Connection Protection. In this circuit, two MOSFETs are connected in series and the TPD7104AF that drives MOSFET2 is used for Power Supply Reverse Connection Protection. Power Supply Reverse Connection Protection is enabled when the SUB pin is left open. Even if a power supply is connected in the reverse direction, MOSFET2 does not turn on because the TPD7104AF does not have power supply and no internal current flow so total system is protected from critical damage. It should be noted, however, that devices closer to the power supply (V_{IN}) than MOSFET2 (e.g., the Current Sense block in Figure 3.1.1) are not protected so some separate protection circuits are necessary if a system design has any current paths from ground to the power supply.
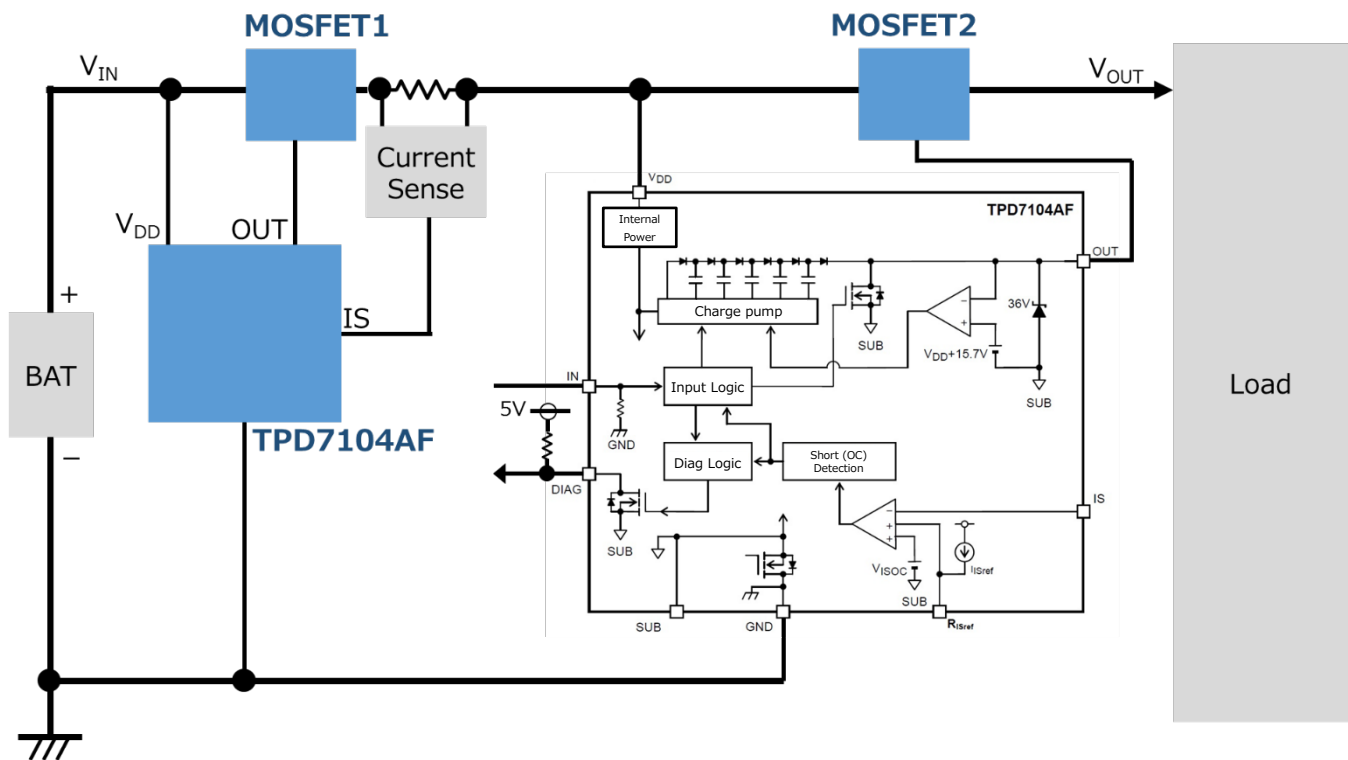

Figure 3.1.1 Example of a Power Supply Reverse Connection Protection circuit and the TPD7104AF internal block diagram

4. Application circuit example and bill of materials

4.1. Application circuit example

Figure 4.1.1 shows an example of an application circuit for a solid-state relay using two TKR74F04PB N-channel power MOSFET and two TPD7104AF. The use of the low-on-resistance TKR74F04PB (with a V_{DS} of 40V and a maximum $R_{DS(ON)}$ of 0.74mΩ) makes it possible to flow a current up to 40A. Two TPD7104AF, IC1 and IC2, drive separate MOSFETs. IC1 provides Load Short-circuit (Overcurrent) Detection whereas IC2 provides Power Supply Reverse Connection Protection.
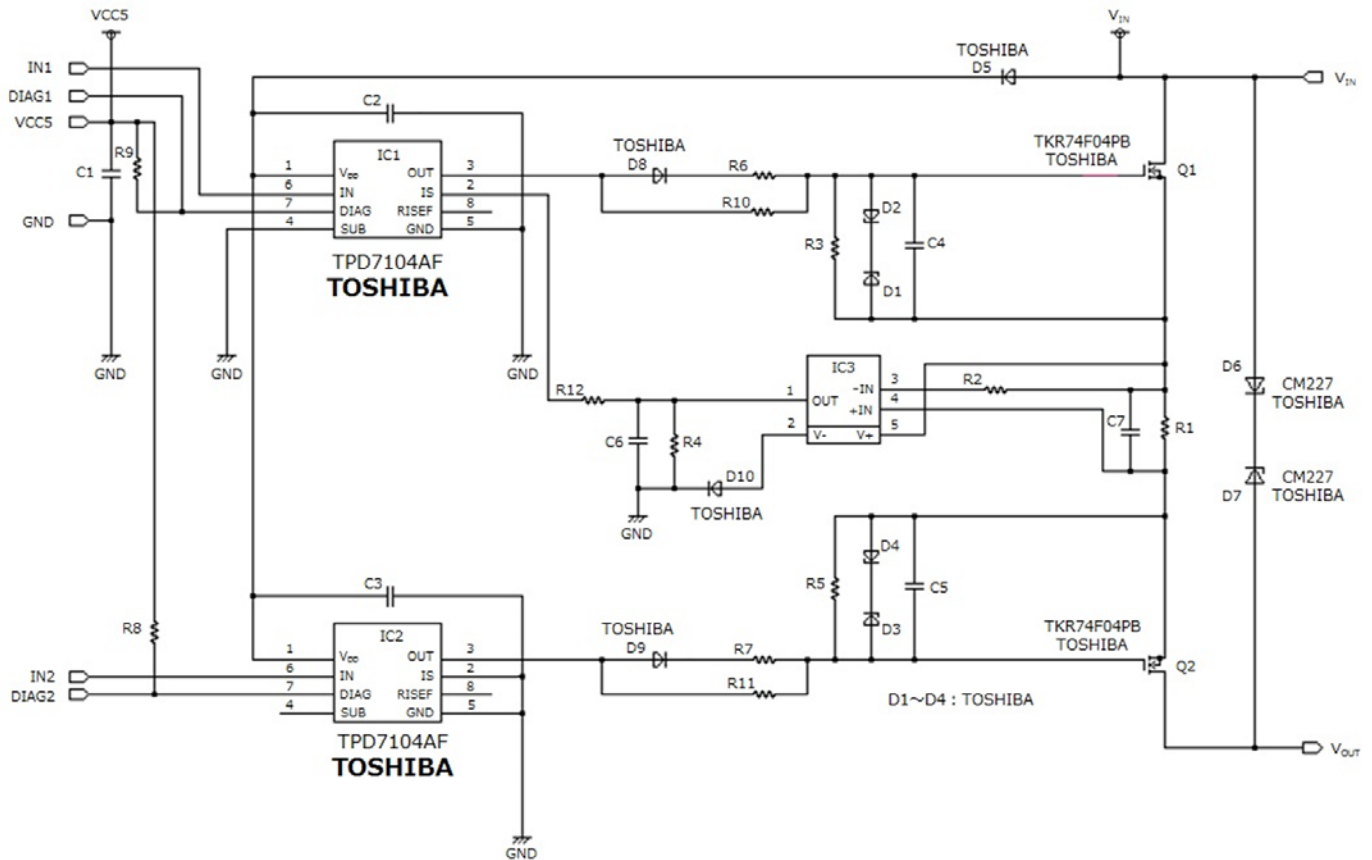

Figure 4.1.1 Application circuit example for the TPD7104AF

4.2. Bill of materials

Table 4.2.1 shows the bill of materials for the application circuit.

Table 4.2.1 Bill of materials for the TPD7104AF application circuit

No.	Ref.	Qty	Value	Part Number	Manufacturer	Description	Packaging	Typical Dimensions mm (inches)
1	IC1, IC2	2	—	TPD7104AF	TOSHIBA	MOSFET gate driver	PS8	2.9 x 2.8
2	IC3	1	—	LTC6101BCS5	Analog Devices	Current sense amplifier	TSOT-23	2.9 x 2.8
3	Q1, Q2	2	—	TKR74F04PB	TOSHIBA	Power MOSFET	TO220-SM(W)	10 x 13
4	D1, D2, D3, D4	4	—	CRZ16	TOSHIBA	Zener diode	S-FLAT	3.5 x 1.6
5	D5	1	—	CMG07	TOSHIBA	Diode	M-FLAT	4.7 x 2.4
6	D6, D7	2	—	CMZ27	TOSHIBA	Zener diode	M-FLAT	4.7 x 2.4
7	D8, D9, D10	3	—	1SS352	TOSHIBA	Diode	USC	2.5 x 1.25
8	R1	1	0.5MΩ	PSJ2NTEBL500F BVS-M-R0005-1.0	KOA Isabellenhutte	10W, ±1% 9W, ±1%	—	10 x 5.2
9	R2	1	300Ω			63mW, ±1%	—	1.6 x 0.8 (0603)
10	R3, R5	2	100kΩ			63mW, ±5%	—	1.6 x 0.8 (0603)
11	R4	1	10kΩ			63mW, ±1%	—	1.6 x 0.8 (0603)
12	R6, R7, R8, R9	4	10kΩ			63mW, ±5%	—	1.6 x 0.8 (0603)
13	R10, R11	2	20kΩ			63mW, ±5%	—	1.6 x 0.8 (0603)
14	R12	1	1kΩ			63mW, ±5%	—	1.6 x 0.8 (0603)
15	C1, C2, C3	3	1µF			Ceramic, 25V, ±10%	—	1.6 x 0.8 (0603)
16	C4, C5	2	10nF			Ceramic, 50V, ±10%	—	1.6 x 0.8 (0603)
17	C6	1	100nF			Ceramic, 50V, ±10%	—	1.6 x 0.8 (0603)
18	C7	1	15pF			Ceramic, 50V, ±5%	—	1.6 x 0.8 (0603)

5. Guidelines for application circuit design

This section provides design guidelines for Load Short-circuit (Overcurrent) Detection and Power Supply Reverse Connection Protection using the 40-A solid-state relay shown in Figure 4.1.1.

5.1. Designing Load Short-circuit (Overcurrent) Detection circuit

In Figure 4.1.1, IC1 (TPD7104AF IPD driver) and IC3 (LTC6101BCS5 current-sense amplifier) provide overcurrent detection. The load current (I_{det}) is calculated as follow:

$$I_{det} = V_{det} \times \frac{R2}{R1 \times R4} \cdots (1)$$

Whereas:

I_{det}(A) : Load Current

R1(Ω) : Current Sense Resistor

R2(Ω) : Current Sense Amplifier Input Resistor

R4(Ω) : Current Sense Amplifier Output Resistor

The values of V_{det}, R2, R1, and R4 can be determined as follows.

1. Determine the maximum system load current: Imax

The maximum current to be supplied to a system from its specification. For example, the solid-state relay shown in Figure 4.1.1 is designed to switch 40A, the Imax is 40A.

2. Determine the value of the R1

To reduce power consumption, select a small-value resistor for R1, considering the performance of the current-sense amplifier. For example, if the power system design requires 1W loss, R1 should be less than 0.625mΩ so it should be 0.5mΩ in the case. The voltage between the terminals of R1 is 20mV at Imax. To ensure current-sensing accuracy, this voltage must be sufficiently lower than the input offset voltage of the current-sense amplifier. The temperature drift of the current-sense amplifier should also be considered as necessary. The LTC6101BCS5 has ±0.81mV input offset voltage and ±3μV/°C temperature drift. If the LTC6101BCS5 is exposed to a temperature change of 100°C during operation, then the LTC6101BCS5 has 1.11mV total offset voltage, which translates to a current-sensing error of 2.22A.

3. Determine the value of R2 and R4

A Load Short-circuit (Overcurrent) condition must not be detected at Imax or lower. Therefore, the gain of the current-sense amplifier must satisfy the following equation:

$$\text{Gain} < \frac{V_{det}(min)}{I_{max} \times R1} \cdots (2)$$

$$\text{Gain} = \frac{R4}{R2} \cdots (3)$$

Since $V_{det}(min) = (V_{ISOC}(min)) = 0.8V$, the gain must be less than 40 per (2). Taking variations in parts characteristics into consideration, it should be used 300Ω±1% resistor as R2 and 10kΩ±1% resistor as R4 to generate a gain of 33 per (3) in the case.

4. Confirm variations

Using the above parameters to calculate I_{det} variations in order to ensure that the selected parts meet the design requirements.

Imax must be greater than $I_{det}(min)$. Per (1) and each values, $I_{det}(min)$ is:

$$I_{det}(min) = 0.80 \times 300*0.99 / (0.5m \times 1.01 \times 10k \times 1.01) - 2.22$$
$$= 44.4A$$

Therefore, $I_{det}(min)$ has around 10% margin against I_{max} (=40A). $I_{det}(min)$ is acceptable even when slight TCR variations of resistors are taken into account.

The maximum ratings of the parts must not be exceeded at $I_{det}(max)$. Per (1) and each values, $I_{det}(max)$ is:

$$I_{det}(max) = 1.2 \times 300*1.01 / (0.5m \times 0.99 \times 10k \times 0.99) + 2.22$$
$$= 76.4A$$

At this time, the current-sense resistor (R1) has a power loss of 2.9W. Therefore, R1 has enough margin relative to its rated power of 5W (at a pin temperature of 100°C).

Calculate $I_{det}(typical)$, Per (1) and each values, $I_{det}(typical)$ is:

$$I_{det}(typical) = 1.02 \times 300 / (10k \times 0.5m)$$
$$= 61.2A$$

5.2. Designing Power Supply Reverse Connection Protection circuit

In Figure 4.1.1, IC2 (TPD7104AF) provides Power Supply Reverse Connection Protection. Its Power Supply Reverse Connection Protection function is enabled when the SUB pin is left open. For more detail, see 3.1 description.

6. Simulation

6.1. Function of Load Short-circuit (Overcurrent) Detection

This section shows the simulation result of the Load Short-circuit (Overcurrent) Detection function available with the TPD7104AF. Figure 6.1.1Figure 6.1.1 shows the circuit simulated using OrCAD. It is similar to the circuit of Figure 4.1.1, but uses the ideal op amp available with OrCAD for current sensing. The circuit shown in Figure 6.1.1 is available for download at RD016-SPICE-02.

We performed a simulation as follows:

■ **Conditions**
- VIN: 12V
- VCC5: 5V
- IN1, IN2: 0V
- Load switch (U14): Off (The load current, Iout, is off.)

■ **Procedure**
- Simulation starts (at t =0).
- At t = 0.5ms, IN1 is set to the High level. (Q1 turns on.)
- At t = 0.6ms, IN2 is set to the High level. (Q2 turns on.)
- At t = 2ms, the load switch (U14) is turned on. (The short-circuit current turns on.)
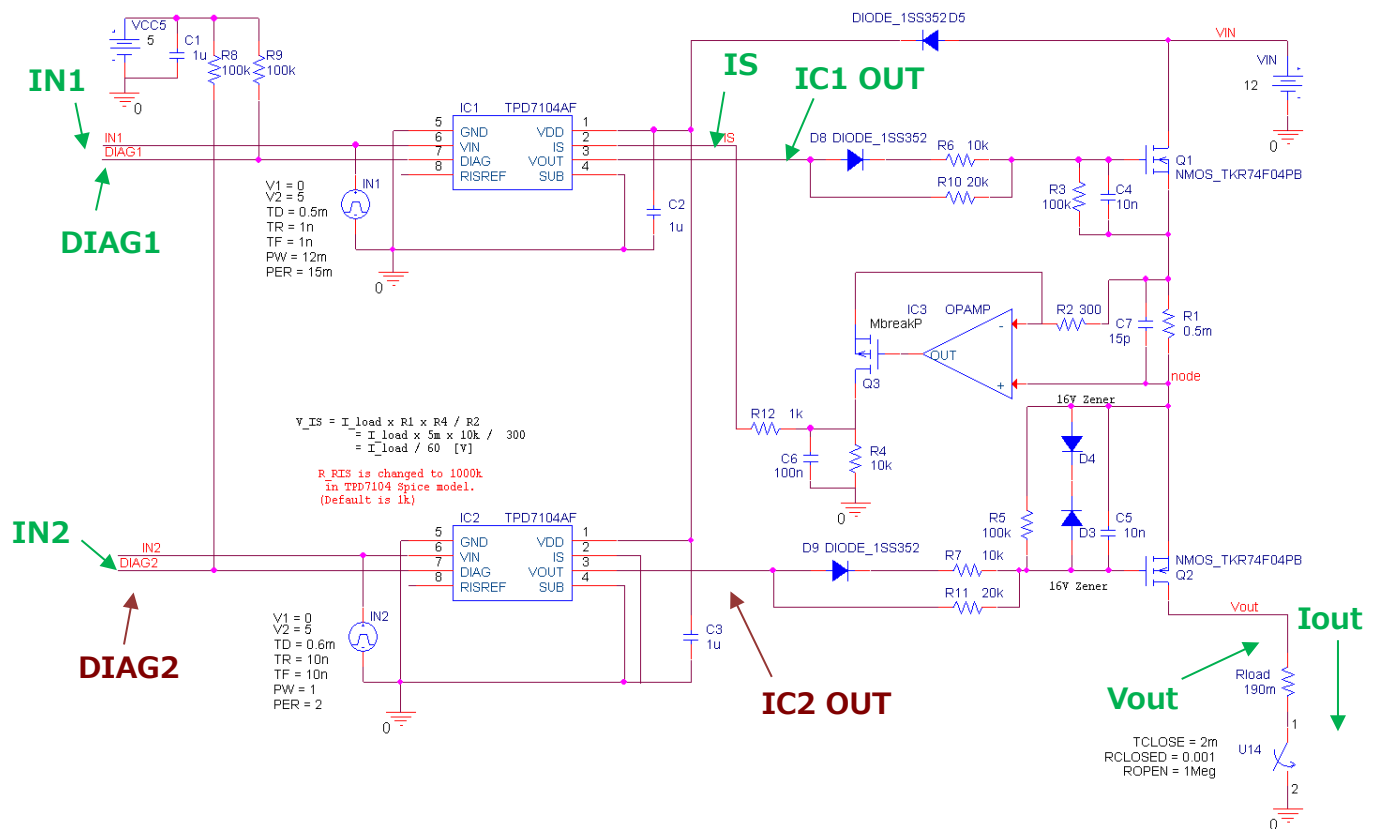

Figure 6.1.1 Simulation Circuit for Load Short-circuit (Overcurrent) Detection

Figure 6.1.2 shows the simulation results. When the load switch turns on, a short-circuit current flows. Upon detection of an overcurrent, the TPD7104AF:

- Turns off Q1 to cut off the load current;
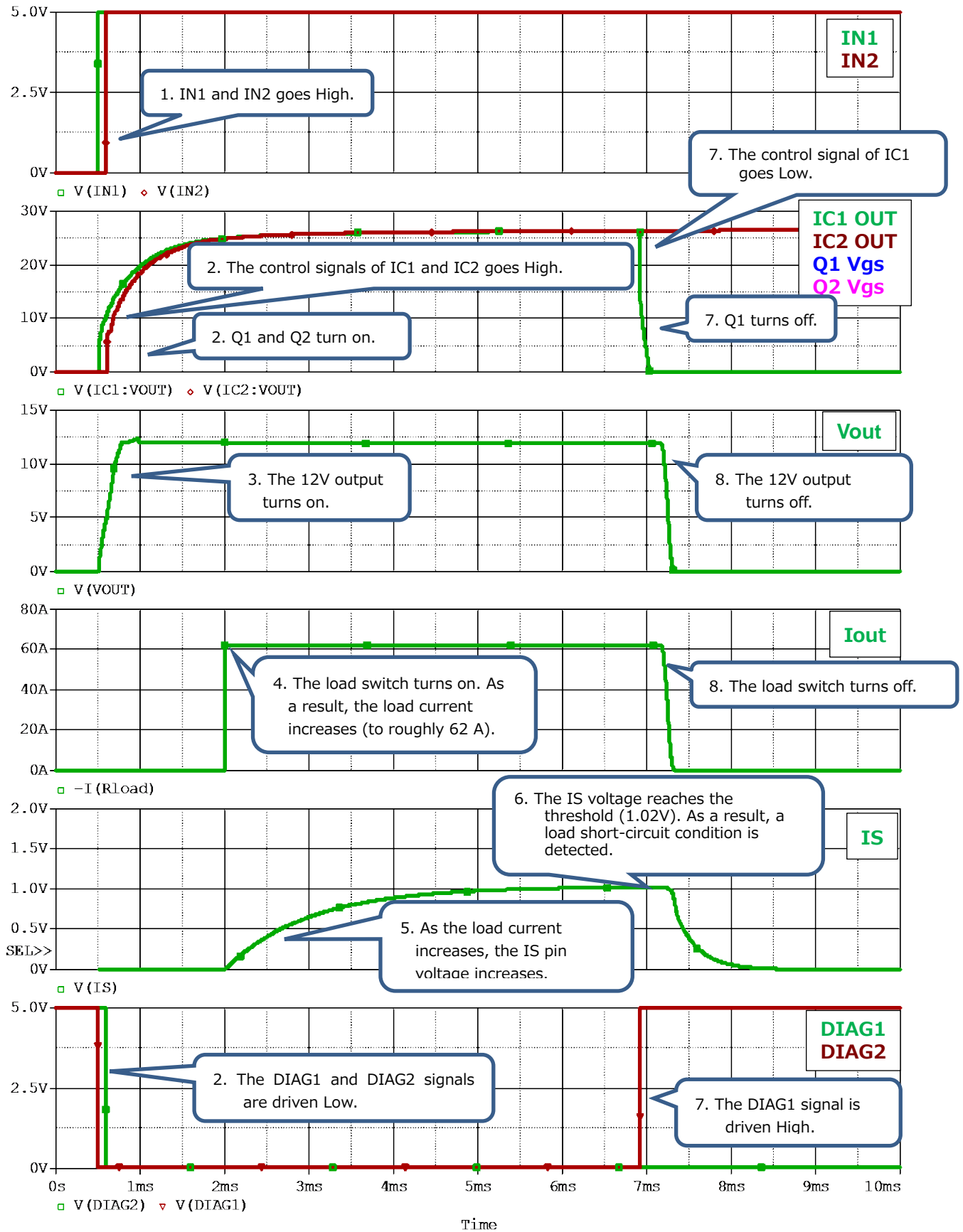- Drives the DIAG1 signal High to indicate an overcurrent condition.

Figure 6.1.2 Simulation result for Load Short-circuit (Overcurrent) Detection

6.2. Function of Power Supply Reverse Connection Protection

This section shows the simulation result of Power Supply Reverse Connection Protection function with the TPD7104AF. Figure 6.2.1 shows the circuit simulated using OrCAD.

In case a power supply is connected to VIN in the reverse direction, IC2 and Q2 provide Power Supply Reverse Connection Protection. The circuit shown in Figure 6.2.1 is available for download at RD016-SPICE-02.

- ■ **Conditions**
  - VIN: -12V (reverse direction)
  - VCC5, IN1, IN2: 0V
  - The SUS pin is left open to enable Power Supply Reverse Connection Protection.
- ■ **Procedure**
  - Simulation is started, with Power Supply Reverse Connection Protection enabled.
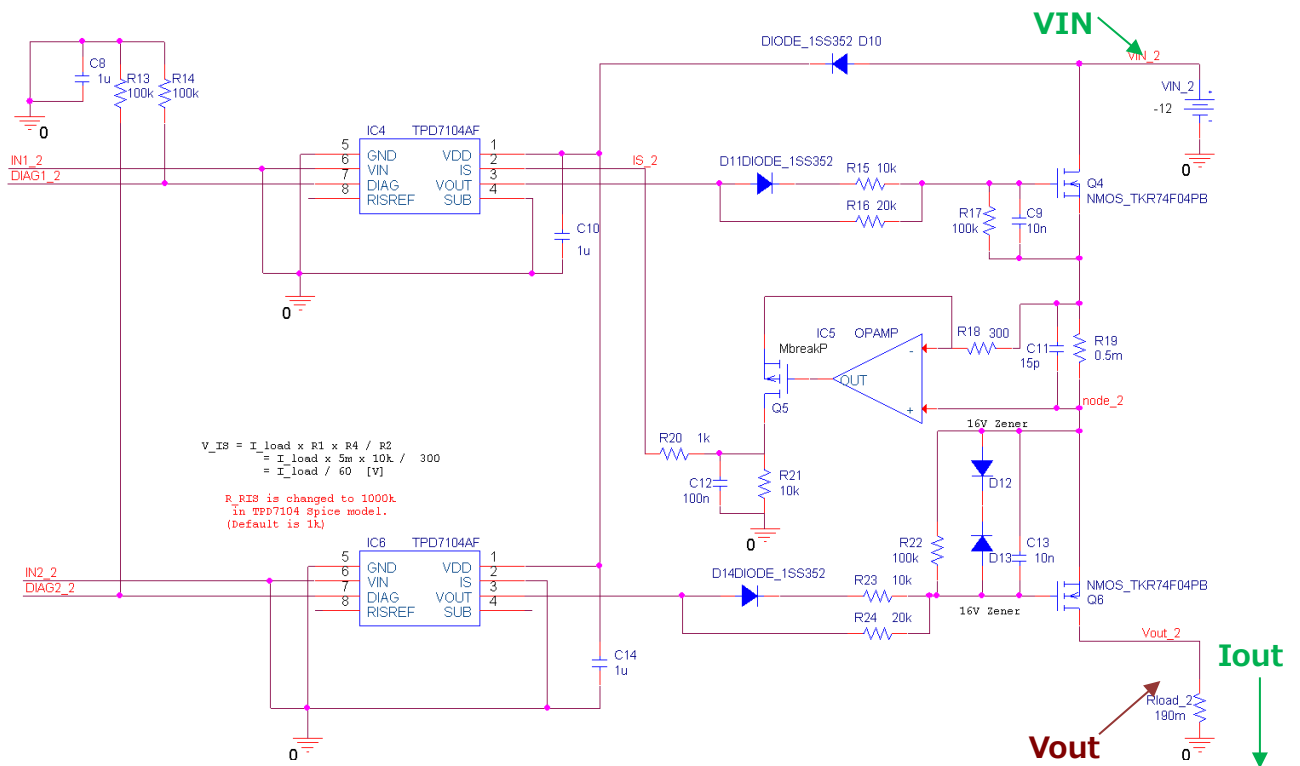

Figure 6.2.1 Simulation Circuit for Power Supply Reverse Connection Protection

Figure 6.2.2 shows the simulation results. VIN-GND is in reverse polarity (= -12V). Since Power Supply Reverse Connection Protection is enabled, no load current flows for a period of 5ms after the simulation starts.
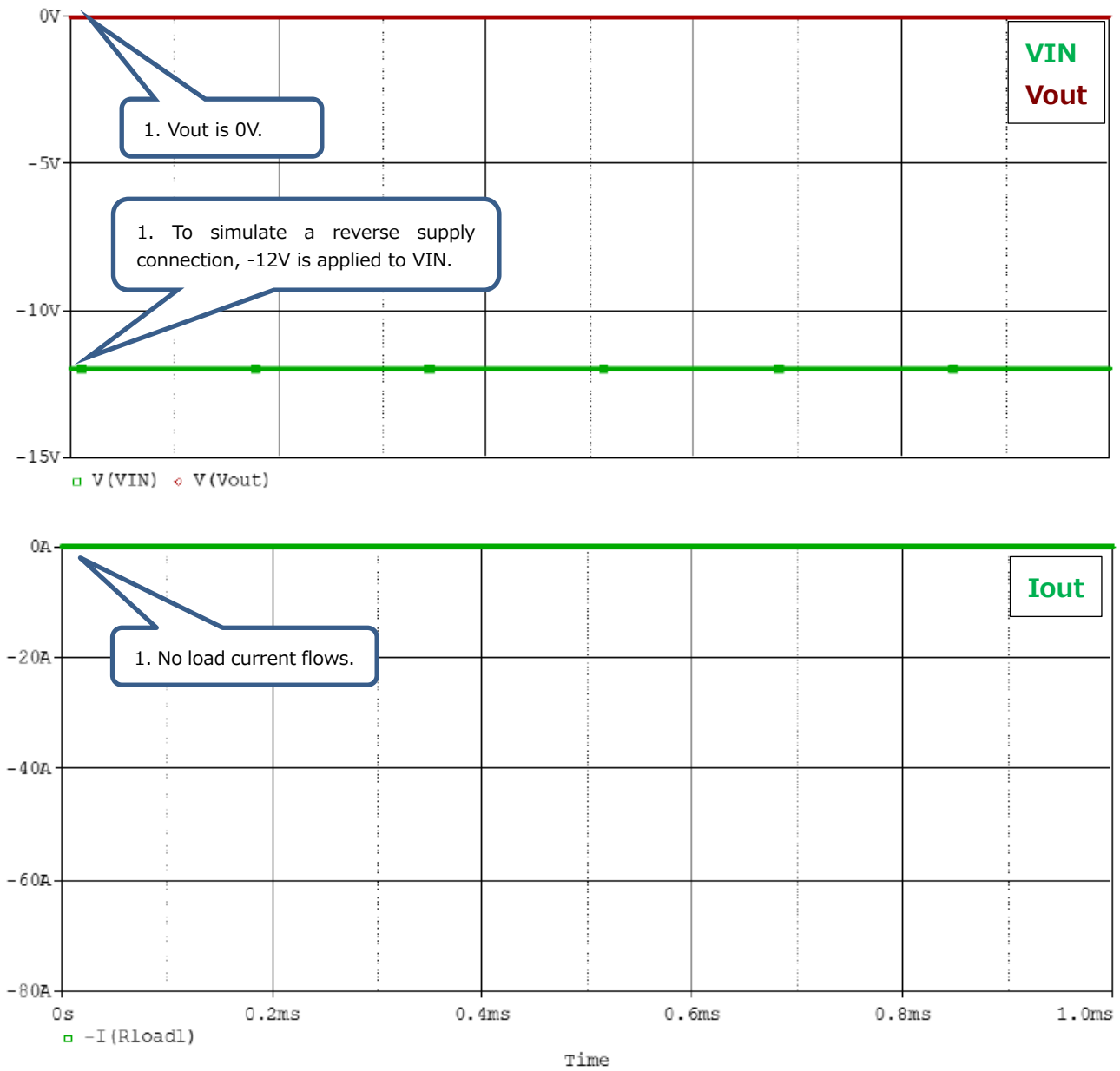
Figure 6.2.2 Simulation result for Power Supply Reverse Connection Protection

7. Product overview

7.1. TPD7104AF

7.1.1. Overview

The TPD7104AF is a single-output N-channel power MOSFET gate driver for high-side switch applications. With a charge pump circuit, the TPD7104AF simplifies a load switch design for high-current applications.

- Integrated a charge pump circuit
- Provides Load Short-circuit (Overcurrent) Detection and Power Supply Reverse Connection Protection
- Small package (PS-8)

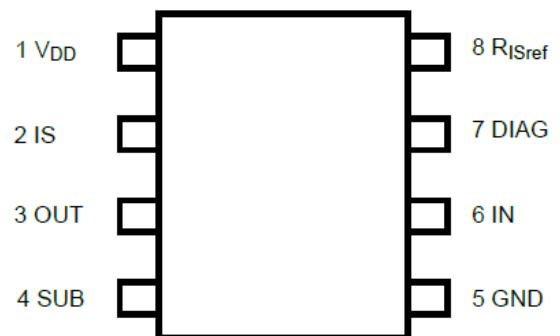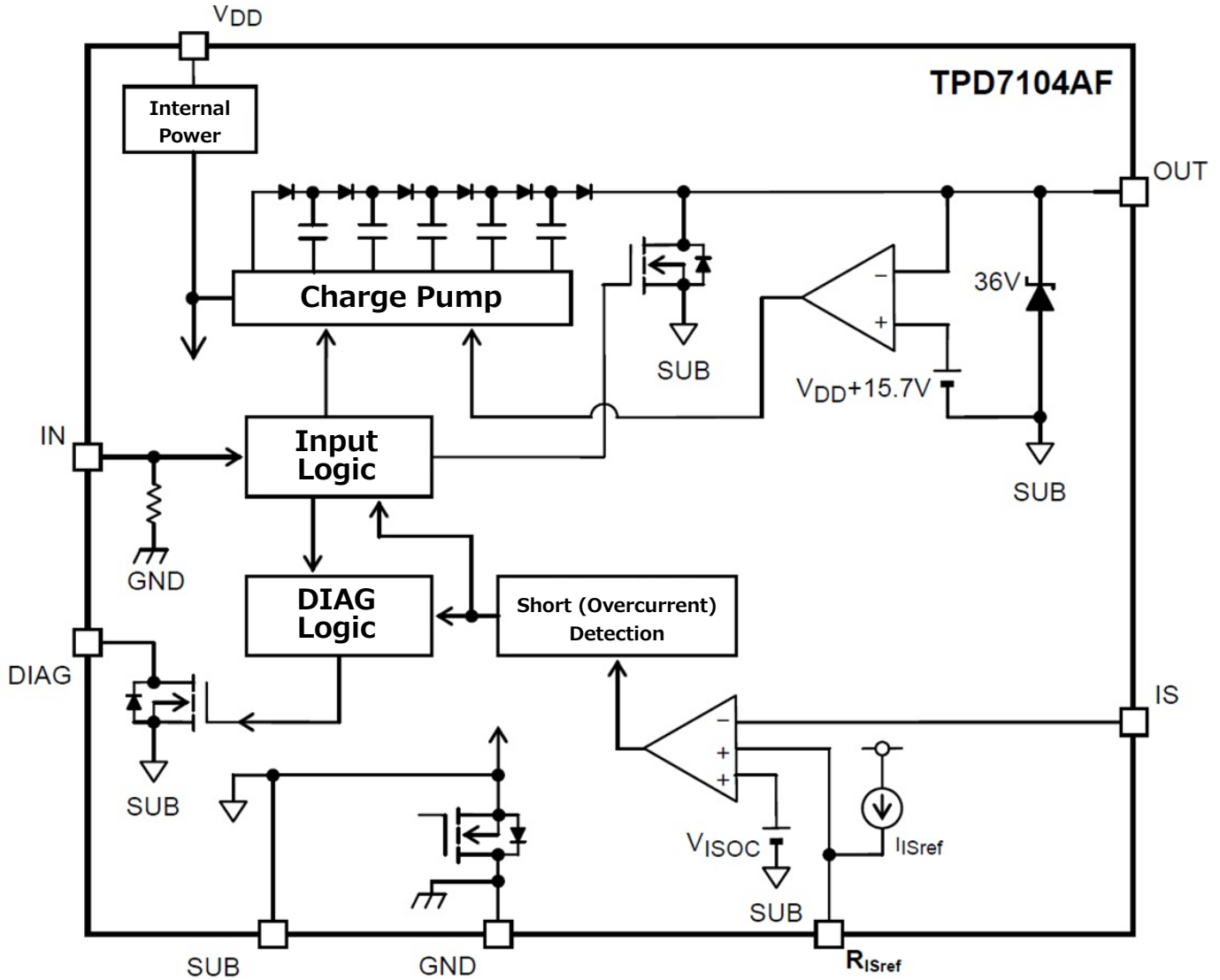### 7.1.2. External view and pin assignment
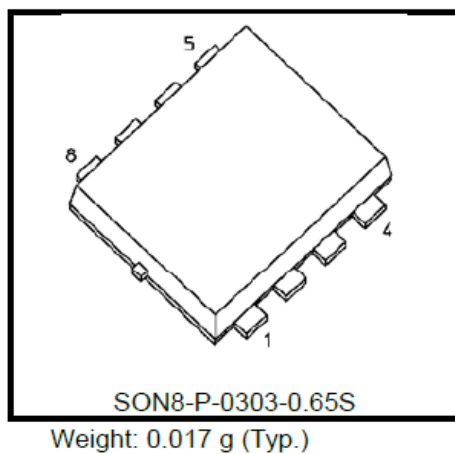
Figure 7.1.2.1 External view and pin assignment

7.1.3. Internal block diagram

7.1.4. Pin description

Table 7.1.4.1 Pin description

Pin No.	Symbol	Function
1	V_{DD}	Power supply pin.
2	IS	Detection pin for short circuit. If short circuit detection is not used, IS pin connect to GND.
3	OUT	Output pin for an external MOSFET drive. State is off if detect short circuit.
4	SUB	Please use open if use protection for reverse connection of power supply. If protection for reverse connection of power supply is not used, SUB pin connect to GND.
5	GND	Ground pin.
6	IN	Input pin. IN has a pull-down resistor.
7	DIAG	Diagnosis detection pin. It is open drain composition. Output is inverted if detect short circuit.
8	R_{ISref}	Adjust pin for sense level for short circuit detection. If R_{ISref} is not used, R_{ISref} pin is open.

7.2. TKR74F04PB
7.2.1. Overview

The TKR74F04PB is Toshiba's low-on-resistance, high-current MOSFET fabricated using the latest low-voltage U-MOSIX-H process.

- Low drain-source on-resistance: $R_{DS(ON)}$= 0.6mΩ typical (@V_{GS}=10V)
- Maximum drain current: I_D = 250A (DC)
- Maximum drain-source voltage: V_{DSS} = 40V

7.2.2. External view and pin assignment

TO-220SM(W)

1: Gate
2: Drain (Heatsink)
3: Source

End of Document

2019-05-10
Rev.3
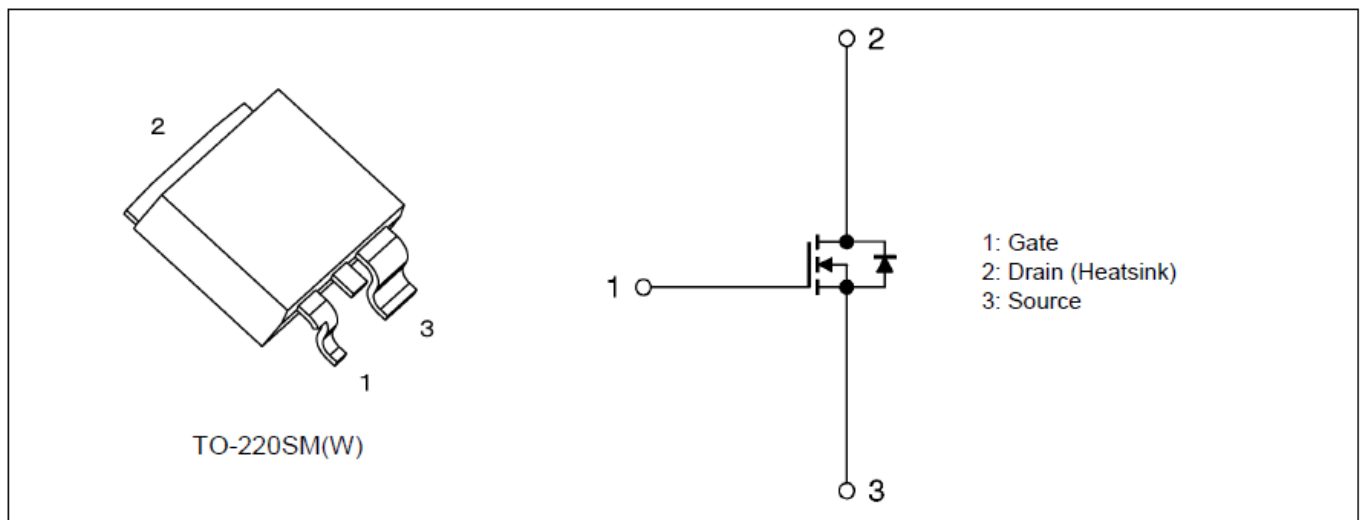
Terms of Use

This terms of use is made between Toshiba Electronic Devices and Storage Corporation ("We") and customers who use documents and data that are consulted to design electronics applications on which our semiconductor devices are mounted ("this Reference Design"). Customers shall comply with this terms of use. Please note that it is assumed that customers agree to any and all this terms of use if customers download this Reference Design. We may, at its sole and exclusive discretion, change, alter, modify, add, and/or remove any part of this terms of use at any time without any prior notice. We may terminate this terms of use at any time and for any reason. Upon termination of this terms of use, customers shall destroy this Reference Design. In the event of any breach thereof by customers, customers shall destroy this Reference Design, and furnish us a written confirmation to prove such destruction.

1. Restrictions on usage
   1. This Reference Design is provided solely as reference data for designing electronics applications. Customers shall not use this Reference Design for any other purpose, including without limitation, verification of reliability.
   2. This Reference Design is for customer's own use and not for sale, lease or other transfer.
   3. Customers shall not use this Reference Design for evaluation in high or low temperature, high humidity, or high electromagnetic environments.
   4. This Reference Design shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.

2. Limitations
   1. We reserve the right to make changes to this Reference Design without notice.
   2. This Reference Design should be treated as a reference only. We are not responsible for any incorrect or incomplete data and information.
   3. Semiconductor devices can malfunction or fail. When designing electronics applications by referring to this Reference Design, customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of semiconductor devices could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Customers must also refer to and comply with the latest versions of all relevant our information, including without limitation, specifications, data sheets and application notes for semiconductor devices, as well as the precautions and conditions set forth in the "Semiconductor Reliability Handbook".
   4. When designing electronics applications by referring to this Reference Design, customers must evaluate the whole system adequately. Customers are solely responsible for all aspects of their own product design or applications. WE ASSUME NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.
   5. No responsibility is assumed by us for any infringement of patents or any other intellectual property rights of third parties that may result from the use of this Reference Design. No license to any intellectual property right is granted by this terms of use, whether express or implied, by estoppel or otherwise.
   6. THIS REFERENCE DESIGN IS PROVIDED "AS IS". WE (a) ASSUME NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (b) DISCLAIM ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO THIS REFERENCE DESIGN, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.

3. Export Control
   Customers shall not use or otherwise make available this Reference Design for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). This Reference Design may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of this Reference Design are strictly prohibited except in compliance with all applicable export laws and regulations.

4. Governing Laws
   This terms of use shall be governed and construed by laws of Japan.