LDO Regulator
Application and Operation of the TCR15AGADJ

Reference Guide

RD007-RGUIDE-02

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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1. Overview

For the purpose of requiring low power consumption application, it is general that average power consumption goes down balancing total system utilization and supplying power. Especially smartphone and tablet, there is a trade-off between the size and weight of the device and their battery capacity while a high level of power management is necessary, but in the application there are various electronic circuits including wireless communication, camera, display, audio, and storage circuits, so it is necessary to control their power supplies surely.

Power management ICs (PMICs) are used in smartphones, tablets, and other small battery-operated devices to achieve accurate power management. A PMIC consists of a few to a few dozen power supply channels of DC-DC converters and low-dropout (LDO) regulators, and a controller to control the on/off of each power supply and output according to commands from a main system-on-a-chip (SoC). PMICs specifically designed for smartphone and tablet applications, are constrained by size limits. Therefore, the power supply ICs integrated in some of these PMICs do not compare favorably with discrete power supply ICs in terms of performance. The power supplies from a PMIC might not satisfy system requirements, depending on the loads (ICs and modules) that they serve. In addition, mobile devices with wireless communication capabilities might generate electromagnetic interference (EMI) that affects bad impact to not only the communication quality but also internal power supply circuits. PMICs are generally designed for applications that are not subject to frequent remodeling. However, smartphones are upgraded frequently to add new features and improve performance, and each upgrade entails changes to the specifications of internal circuits. It is therefore impractical to rely on a single PMIC for the power management of all the internal circuits from the viewpoints of both system design and PMIC design.

In addition, with the global uptake of the LTE wireless standard, many smartphone users now share photographs and movies on SNS. This is driving substantial improvement in the performance of smartphone cameras, which have a CMOS image sensor with low power consumption and high read speed. Generally, it is necessary to supply different voltages to the sensor, core (control) and I/O sections of a CMOS image sensor. The digital core of a CMOS image sensor that processes data at high speed tends to consume a lot of power. Nowadays, the digital core is designed to operate at a very low voltage (around 1 V) to reduce power consumption. In order to accommodate the decreasing voltage and increasing current consumption, the power supply for the digital core needs to have excellent AC characteristics, including a high power supply rejection ratio (PSRR) and a fast load transient response, while providing a high current drive capability. Ultra-small packaging is also an important factor for space-critical designs like smartphones.

In addition to the V_{IN} input, Toshiba's LDO regulators of the TCR15AG series have a separate power supply for the output circuit in order to achieve low dropout voltage and thus stable voltage regulation even at low input voltage. The TCR15AG series provides outstanding PSRR and load transient response required for CMOS image sensors for smartphone applications. In addition, the TCR15AG series has a circuit that allows the output voltage to be adjusted over a wide range. While providing accurate voltage regulation, all the LDO regulators of the TCR15AG series are available in

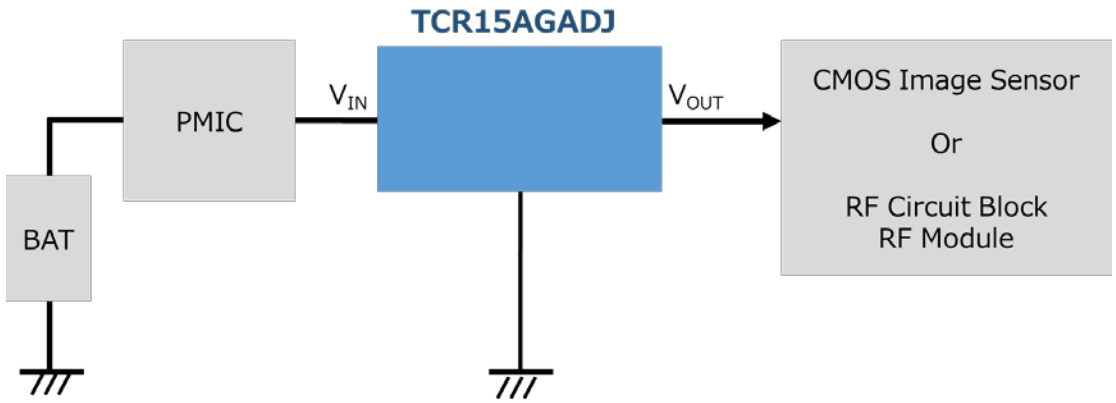
an ultra-small, thin-profile WCSP package. Furthermore, the TCR15AG series has a drive capability of up to 1.5 A and thus meets the current requirement of CMOS image sensors, and provides overcurrent protection, thermal shutdown, inrush current limiting, undervoltage lockout, and auto output discharge.

This reference guide uses the TCR15AGADJ adjustable-output LDO regulator as an example to describe the major features and characteristics of the TCR15AG series. For details of other features and functions of the TCR15AGADJ, see datasheet.

To download the datasheet for the TCR15AGADJ→ Click Here

1.1. Target applications

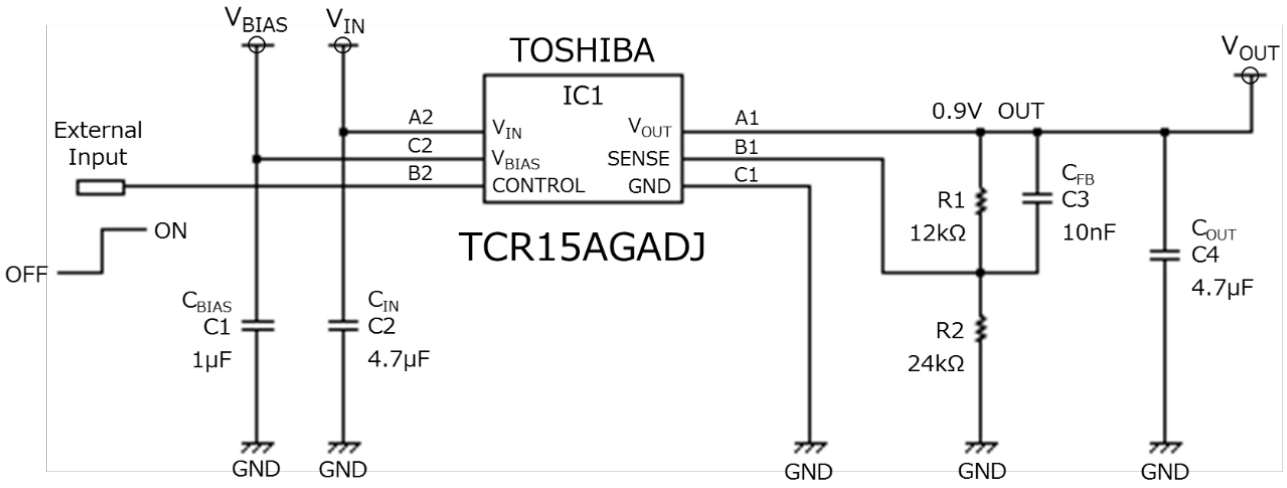
- Power supply circuits for CMOS image sensors and RF blocks/modules for smartphone applications



2. Application circuit example and bill of materials

2.1. Application circuit example

Figure 2.1.1 shows an example of a circuit using the TCR15AGADJ LDO regulator.



V_{BIAS} voltage conditions:

When $V_{OUT} \leq 1.1V$: 2.5 to 5.5V

When $V_{OUT} > 1.1V$: V_{OUT} + 1.4 to 5.5V

V_{IN} and V_{BAIS} can be connected together if they meet the above

Figure 2.1.1 Example of a circuit using the TCR15AGADJ LDO regulator

2.2. Bill of materials

Table 2.2.1 Bill of materials

No.	Ref.	Qty	Value	Part Number	Manufacturer	Description	Packaging	Typical Dimensions mm (inches)
1	IC1	1	—	TCR15AGADJ	TOSHIBA		WCSP6F	1.2 x 0.8
2	C1	1	1.0 µF			Ceramic, 10 V, ±10%	—	1.0 x 0.5 (0402)
3	C2	1	4.7 µF			Ceramic, 10 V, ±10%	—	1.6 x 0.8 (0603)
4	C3	1	10 nF			Ceramic, 50 V, ±10%	—	1.0 x 0.5 (0402)
5	C4	1	4.7 µF			Ceramic, 10 V, ±10%	—	1.6 x 0.8 (0603)
6	R1	1	Selectable			Ceramic, 50 V, ±1%	—	1.0 x 0.5 (0402)
7	R2	1	Selectable			Ceramic, 50 V, ±1%	—	1.0 x 0.5 (0402)

3. Major features of the TCR15AG series

Fabricated using a CMOS process, the LDO regulators of the TCR15AG series feature low current consumption and small size. With small process geometries, the output device of the TCR15AG series has low on-resistance and thus a low input-output voltage differential (i.e., dropout voltage). LDO regulators with a low dropout voltage help reduce the thermal loss and increase the running time of battery-operated devices.

The TCR15AGADJ has a bias voltage input (V_{BIAS}) separate from the V_{IN} input, making it possible to reduce dropout voltage to a level lower than that achievable with the conventional CMOS process. Due to this circuit configuration, the TCR15AGADJ provides much lower dropout voltage than typical CMOS LDO regulators and thus helps reduce thermal loss. As a result, despite the ultra-small WCSP package, the TCR15AGADJ has a current drive capability of 1.5A. Being independent of the V_{IN} input of the LDO regulator, the V_{BIAS} pin helps the TCR15AGADJ achieve stable voltage regulation, even in the low input voltage region, without being affected by V_{IN}. The output voltage is therefore adjustable to as low as 0.65V. The following subsections show the unique characteristics of the TCR15AGADJ derived from the V_{BIAS} pin.

3.1. V_{BIAS} pin

Figure 3.1.1 shows a conventional LDO regulator. Operating with a power supply from V_{IN}, this LDO regulator drives the gate of an internal P-channel MOSFET with V_{IN} to provide an output voltage. Consequently, when V_{IN} is low, the MOSFET gate voltage decreases to a level that makes it impossible for the LDO regulator to maintain a regulated output voltage. Even when a low output voltage is necessary, a conventional LDO regulator is restricted by the lower limit of input operating voltage range specified in the datasheet. Therefore, despite the superior low-dropout advantage, conventional LDO regulators are not well suited for applications requiring a regulated low-voltage supply.

By way of comparison, Figure 3.1.2 shows the internal configuration of the TCR15AGADJ, which drives the gate of an internal MOSFET with a power supply from the V_{BIAS} pin. Being independent of the V_{IN} input, the V_{BIAS} pin provides several benefits. First, this configuration allows the use of an N-channel MOSFET. Since it is easier to reduce the on-resistance of the N-channel MOSFET than that of the P-channel MOSFET, the use of an N-channel MOSFET makes it possible to reduce dropout voltage. This, in turn, helps reduce power loss and therefore achieve a high-current drive capability. Second, the LDO regulator can operate at a low input voltage irrespective of V_{IN} and provides a regulated low output voltage with minimum power loss. Next, let's look at the changes in characteristics over a range of voltage applied to the V_{BIAS} pin.

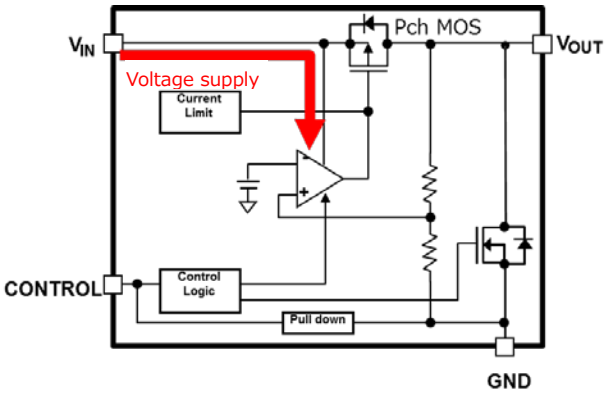


Figure 3.1.1 Gate voltage supply of the internal MOSFET of an LDO regulator without the V_{BIAS} pin

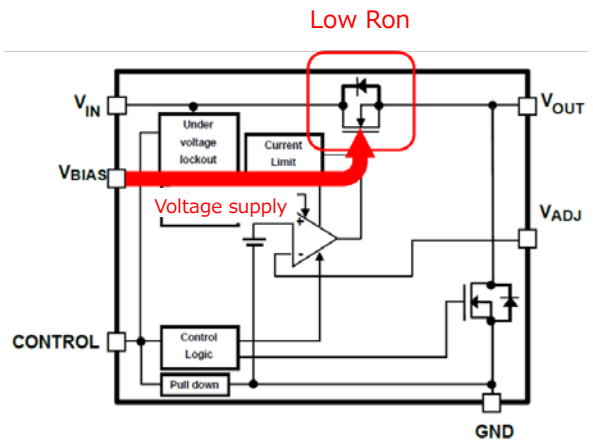


Figure 3.1.2 Gate voltage supply of the internal MOSFET of an LDO regulator with the V_{BIAS} pin

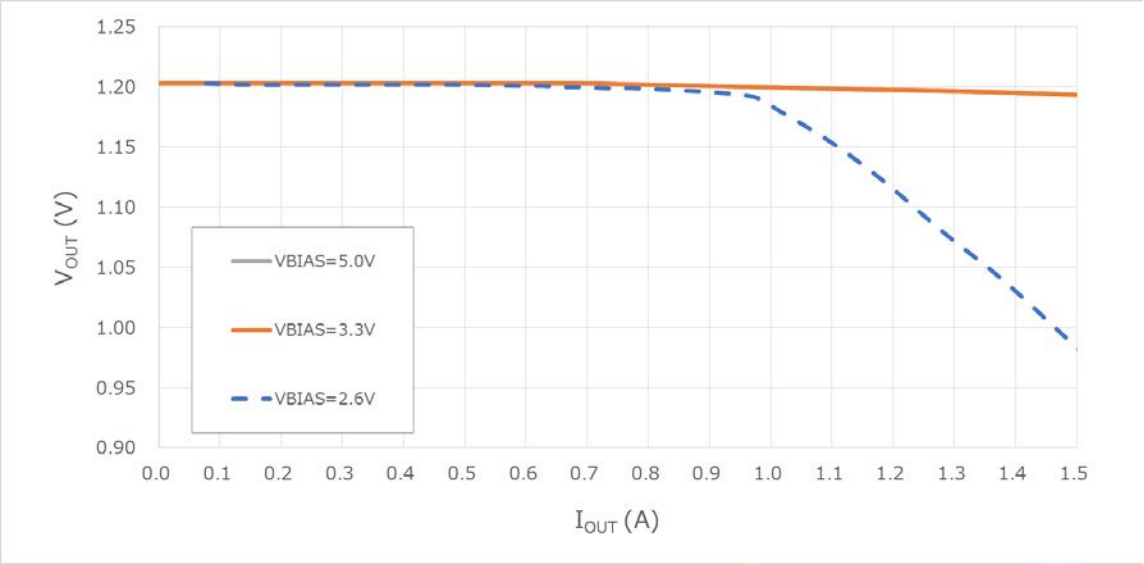


Figure 3.1.3 V_{OUT}-I_{OUT} curve with different V_{BIAS} voltages

Figure 3.1.3 shows the V_{OUT}-I_{OUT} curves of the TCR15AGADJ at different V_{BIAS} voltages. As shown in Figure 3.1.3, when the V_{BIAS} pin is 3V or higher, the TCR15AGADJ maintains low-dropout performance over the entire output current range of up to 1.5A. The minimum V_{BIAS} voltage shown in the datasheet is a voltage at which the functional operation of the TCR15AGADJ is guaranteed under the specified test conditions. Care should be taken as to variations in performance depending on the V_{BIAS} voltage. The minimum V_{BIAS} voltage specified in the datasheet is 2.6V when V_{OUT} = 1.2V. The dashed curve shows the V_{OUT}-I_{OUT} characteristics when V_{BIAS} = 2.6V. In contrast, the solid line shows the V_{OUT}-I_{OUT} performance when V_{BIAS} = 3V. Compared to the solid line, the V_{OUT}-I_{OUT} curve at V_{BIAS} = 2.6V begins to decline at an I_{OUT} around 0.5A. Therefore, for systems requiring a current of 0.5A or more, a 3V or higher power supply should be applied to the V_{BIAS} pin. However, this causes some design concerns. For example, depending on the system configuration, a long power supply line might need to run around a board, making it susceptible to noise. Another concern is that a system might be unable to supply enough power to the V_{BIAS} pin. Generally, the impact of a long and complex power supply line can be fixed by adding a 1-µF capacitor to the V_{BIAS} pin as shown in Figure 2.1.1 or selecting an optimal capacitor while checking the output waveform from an actual system board. In order to ensure output voltage regulation, a 1µF or larger capacitor should be placed even if V_{BIAS} is free from noise. Since the sink current (I_{BIAS}) running into the V_{BIAS} pin is roughly 20µA at the maximum as shown in Figure 3.1.4, it is usually unnecessary to be concerned about a voltage drop caused by an insufficient power supply to the V_{BIAS} pin.

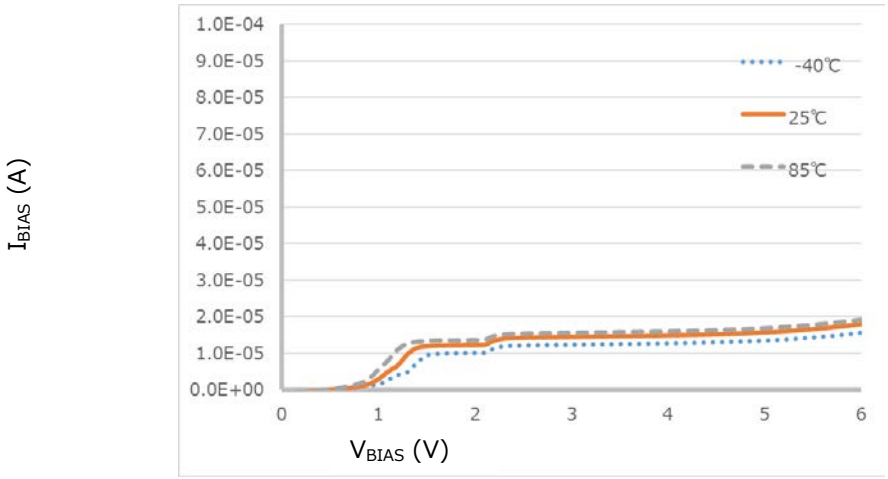
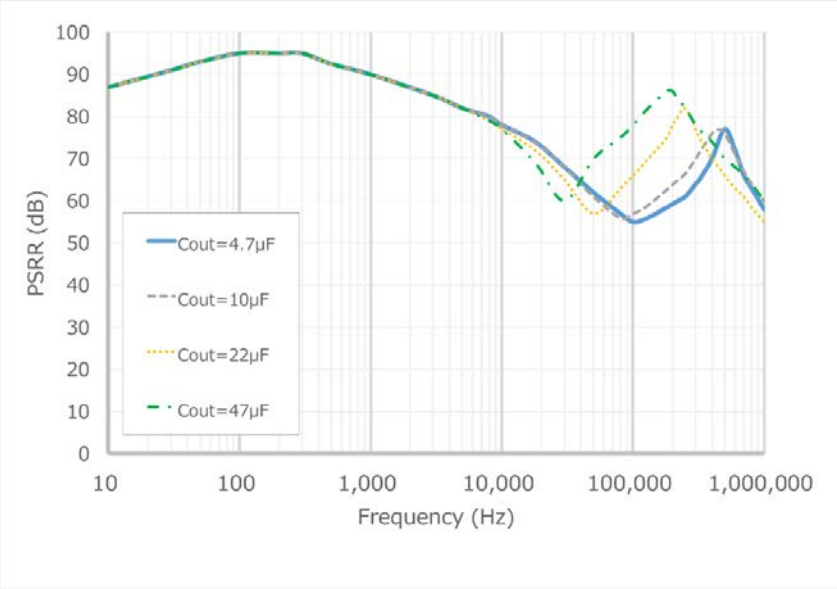


Figure 3.1.4 I_{BIAS}-V_{BIAS} curves

If the power supply to the V_{BIAS} pin is connected to other loads in parallel, a sudden change in any of their load currents could cause sudden drop the V_{BIAS} voltage. In order to maintain the V_{BIAS} pin at a proper voltage even in this situation, a 1-μF or greater capacitor should be placed to the V_{BIAS} pin as shown in Figure 2.1.1.

3.2. Achieving a high PSRR and the influence of an output capacitor on the PSRR

In order to achieve a low dropout voltage and a high current-drive capability of 1.5 A, the TCR15AGADJ drives an internal MOSFET with a supply voltage from the V_{BIAS} pin separate from V_{IN}. With a low dropout voltage performance, the TCR15AGADJ can regulate a low output voltage at a low input voltage, so it suits high-current applications such as CMOS image sensors and RF circuit blocks/modules. Important parameters for these applications include the PSRR that affects the amount of noise on a power supply to the load circuit and the load transient response, i.e., the response to sudden changes in the load current that occurs in high-speed digital signal processing circuits. Figure 3.2.1 shows the PSRR-frequency characteristics of the TCR15AGADJ.



V_{OUT}= 1.2 V
V_{Ripple} = 200 mVp-p
I_{OUT} = 10 mA
V_{BAT} = 5.5 V

Figure 3.2.1 PSRR-frequency characteristics

The PSRR, also known as a ripple rejection ratio, indicates the capability of an LDO regulator to suppress variations noise in the input power supply. Expressed in decibels (dB), the greater the PSRR, the better performance. The PSRR varies with the frequency of noise added on the input power supply. At frequencies of noise below 1kHz, the TCR15AGADJ regulates the output voltage through an internal feedback loop and thus reach a very high PSRR performance about 90dB. The TCR15AGADJ also provides a high PSRR from 75 to 80dB at 10kHz. As the frequency increases, the PSRR decreases. The amount of decrease in the PSRR is determined by the frequency characteristics of an error amplifier used in the internal feedback loop of an LDO regulator. The TCR15AGADJ has a PSRR about 55dB even at 100kHz with the recommended output capacitor (C_{OUT}) value of 4.7μF. This shows that the high-performance error amplifier used in the TCR15AGADJ is effective in increasing the PSRR. Figure 3.2.1 shows PSRR-vs-frequency characteristics for different C_{OUT} values. As C_{OUT} increases, the PSRR begins to decline at lower frequencies. On the other hand, a larger C_{OUT} provides a higher PSRR in the high-frequency region due to the positive effect of larger capacitance. For example, at 100 kHz, the TCR15AGADJ has a PSRR of about 55 dB when C_{OUT}=4.7μF whereas it provides a PSRR of about 65dB, 10dB higher, when C_{OUT}=22μF.

This improvement of the PSRR is the effect of a larger output capacitance rather than the ripple rejection performance of the LDO regulator. In a higher-frequency region, the PSRR declines again. The points of inflection on the PSRR curve depend on the value of the output capacitor (C_{OUT}), the frequency characteristics of the capacitance, resistance, and inductance of the output capacitor, and distributed parameters of a board. For noise-sensitive applications that operate at a frequency of 10 kHz or higher, it is recommended to test with different types and values of capacitors and select the good one.

3.3. Achieving a fast load transient response

In order to achieve a low dropout voltage and a high current-drive capability of 1.5A, the TCR15AGADJ drives an internal MOSFET with a supply voltage from the V_{BIAS} pin separate from V_{IN}. With a low dropout voltage performance, the TCR15AGADJ can regulate a low output voltage. LDO regulators with a low output voltage are commonly used for SoCs, memories, and other high-speed digital signal processing applications, which is typically up and down rapid change in power consumption. Obviously, in the face of sudden changes in the load current, LDO regulators must supply a precisely regulated output voltage to the load. Therefore, a load transient response, which is defined as a change in the regulated output voltage that occurs as a result of a change in the load current, is important.

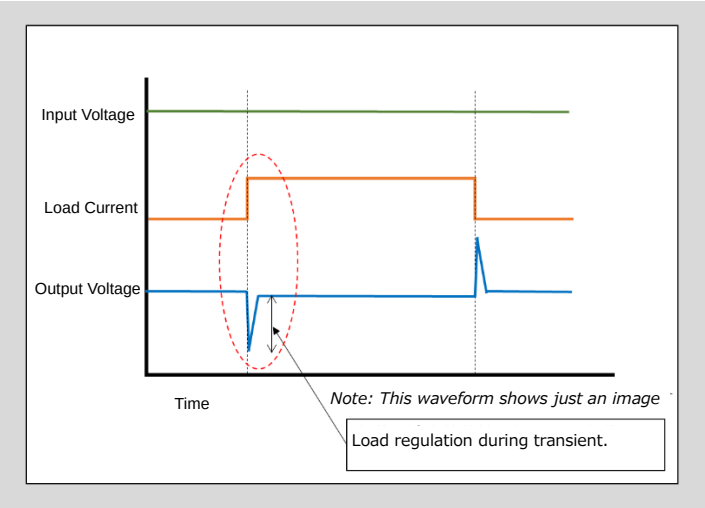
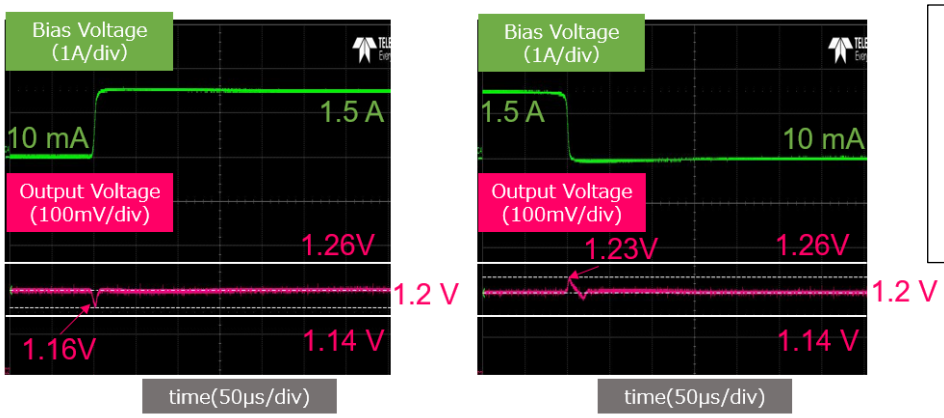


Figure 3.3.1 Image of a typical load transient response

Figure 3.3.1 shows an image of a typical load transient response. Generally, as the load current increases, the output capacitor (C_{OUT}) begins to discharge. Then, the LDO regulator starts voltage control via an internal feedback loop to maintain a regulated output voltage. However, in the event of a sudden change in the load current, C_{OUT} is discharged a moment, causing the output voltage to decrease. If the voltage control feedback loop is slow to respond, the output voltage continues decreasing until the feedback loop starts to act its effect to bring the output voltage back to the regulated level. The load transient response is important since a problem occurs if the output voltage drops below the minimum operating voltage required by the load. In the event of an excessive voltage drop, the load suffers a loss in performance or possibly a shutdown. Such an event may lead adversely lacking the operation or performance of the entire system. The fast load transient response and the ability to provide a low output voltage make the TCR15AGADJ suits a power supply for high-speed digital signal processing applications, including SoCs and the digital core (control) of CMOS image sensors. Figure 3.3.2 shows examples of load transient response waveforms of the TCR15AGADJ.



C_{IN} = 4.7μF
C_{OUT}= 4.7μF
C_{BIAS} = 1μF
V_{IN} = 3.3V
V_{CT} = 1.5V
V_{BIAS} = 3.3V
I_{OUT}= 10mA → 1.5A → 10mA

Figure 3.3.2 Example of load transient response waveforms

The left-side image shows the output voltage waveform in response to a change in the load current from 10mA to 1.5A. The right-side image shows the waveform in response to a load current change from 1.5 A to 10 mA. Here, the typical output voltage is set to 1.2V. For example, the load current changes rapidly in case of the digital core of a CMOS image sensor transitions from an idle state to an active mode or in case of a memory device performs a burst transfer at high speed. The load transient responses of the TCR15AGADJ shown in Figure 3.3.2 are the results of measurement under more severe conditions than these cases. As described in the previous section, a high-performance error amplifier integrated in the TCR15AGADJ makes it possible to maintain a regulated output voltage even in the event of sudden change in the load current. In fact, LDO regulators are seldom exposed to load current changes as rapid as those shown in Figure 3.3.2. Therefore, the TCR15AGADJ provides a sufficient design margin even for systems sensitive to power supply swing.

4. Adjusting the output voltage

The output voltage of the TCR15AGADJ is adjustable between 0.55V and 3.6V via two external resistors (R1 and R2). The output voltage is calculated as follows:

$$V_{OUT} = V_{ADJ} \times \left(1 + \frac{R1}{R2}\right)$$

V_{ADJ} = 0.588V (min) to 0.612V (max)
0.6V (typ.)

By way of reference, Table 4.1 shows the output voltages obtained with different values of R1 and R2.

Table 4.1 Reference of output voltage adjustment resistors

Output Voltage (Typical)	R1	R2
0.6 V	0 Ω	Open
0.65 V	2 kΩ	24 kΩ
0.7 V	4 kΩ	24 kΩ
0.8 V	8 kΩ	24 kΩ
0.9 V	12 kΩ	24 kΩ
1.0 V	16 kΩ	24 kΩ
1.1 V	20 kΩ	24 kΩ
1.2 V	24 kΩ	24 kΩ
1.3 V	28 kΩ	24 kΩ
1.8 V	48 kΩ	24 kΩ
2.5 V	76 kΩ	24 kΩ
3.0 V	96 kΩ	24 kΩ
3.3 V	108 kΩ	24 kΩ
3.6 V	120 kΩ	24 kΩ

In actual design work, the upper and lower limits for the V_{ADJ} pin voltage, the accuracy of the R1 and R2 resistors, and other factors should be taken into consideration. The load transient response should also be evaluated using an actual PCB.

Fixed-voltage LDO regulators have an output voltage error relative to the expected typical output voltage shown in the datasheet. The output voltage and accuracy shown in the datasheet are typical values under the test conditions given in the datasheet. At a higher output current, the output has a greater dropout voltage.

In the case of an adjustable-output LDO regulator, output voltage can be divided with external resistors to obtain desired voltages. For example, for high-current applications, a typical output voltage of an LDO regulator can be set, considering a dropout voltage that will occur under specific current conditions. In such cases, the output voltage becomes higher in the low-current region than the typical setpoint voltage. However, the V_{BIAS} pin of the TCR15AGADJ helps minimize the dropout voltage and thus a change in output voltage over the entire current range. See Figure 3.1.3 for the V_{OUT}-I_{OUT} curves. In addition, the voltage supplied to a load can be changed valuable by dynamically changing the external resistors. For example, in addition to controlling the on/off of a power supply, reducing the supply voltage helps reduce the current consumption of an RF circuit for wireless communication. One way to achieve this is to use a register bank in a PMIC to dynamically select from a set of external resistors. As described above, adjustable-output LDO regulators have many benefits. This means there are many factors and situations to be considered for system design.

5. Design considerations

- External capacitors

  A ceramic capacitor can be used as an output capacitor for the TCR15AGADJ. However, the characteristics of some ceramic capacitors have very large temperature dependence. An output capacitor should be carefully selected, taking the environmental conditions into account. It is also recommended to use a ceramic capacitor with an equivalent series resistance (ESR) of 1.0Ω or less. To ensure stable operation, use an input capacitor of 4.7μF or greater, a bias capacitor of 1.0μF or greater, and an output capacitor of 4.7μF or greater.

- Board assembly

  Provide as large a GND plane as possible to reduce wire impedance. Voltage overshoot and undershoot may happen depending on transient responses of the input and output voltage and current, a PCB layout, and internal parasitic of an IC.

- Power dissipation

  Designing PCB, the IC temperature remains well below the maximum rated temperature during operation even at the maximum power dissipation point. For PCB design, ambient temperature, input voltage, and output current, and other environmental conditions should also be considered.

- Overcurrent protection and thermal shutdown

  The TCR15AGADJ has feedback loops for overcurrent protection and thermal shutdown. It should be noted that these features are not intended to guarantee that the device is kept below the absolute maximum ratings. Exposure to conditions exceeding the absolute maximum ratings might adversely affect the functionality and reliability of the device. The device might be permanently damaged if the output and GND pins of the TCR15AGADJ become partially short-circuited.

  Apply the above design considerations and derate the absolute maximum rated values as described in the Toshiba Semiconductor Reliability Handbook to ensure that none of the absolute maximum ratings will be exceeded under any circumstances. It is recommended to add fail-safe and other safety features to an application system.

- Adjustable-output LDO regulator

  The TCR15AGADJ is an adjustable-output LDO regulator. V_{ADJ} is an output voltage control pin. See the recommended application circuit and the output voltage adjustment resistor table. Select resistors (R1 and R2), taking resistance variations into consideration according to system requirements. Place R1 and R2 in such a manner as to minimize common-impedance paths. R1 and R2 should be placed as close as possible to the V_{ADJ} pin to avoid the influence of noise.

6. Product overview

6.1. TCR15AGADJ

6.1.1. Overview

The TCR15AGADJ is an ultra-low-dropout, single-output CMOS LDO regulator with a control input pin featuring a fast load transient response and an inrush current limiting circuit.

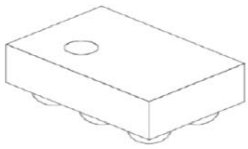
The TCR15AGADJ allows the output voltage to be adjusted between 0.60V and 3.6V and is capable of supplying an output current of up to 1.5A. The TCR15AGADJ provides overcurrent protection, thermal shutdown, inrush current limiting, undervoltage lockout, and auto output discharge functions.

The TCR15AGADJ is housed in the ultra-small WCSP6F package (0.8 mm x 1.2 mm typical; t: 0.33 mm maximum). Since small ceramic capacitors can be used as input and output capacitors, the TCR15AGADJ is ideal for applications that require high-density board assembly such as mobile devices.

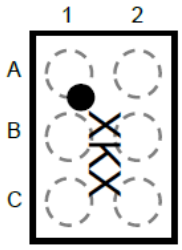
- Ultra-small package: WCSP6F (0.8mm x 1.2mm typical; t: 0.33mm maximum)
- Wide range of output voltage (V_{OUT}): Adjustable between 0.6V and 3.6V
- Fast load transient response: -100 / +115mV (typical) at 0.01A ⇔ 1.5A, C_{OUT} = 4.7μF
- High Power Supply Rejection Ratio : PSRR = 95dB (typical) at 1kHz
- Overcurrent protection
- Thermal shutdown
- Auto output discharge function
- Inrush current limiting
- Output-voltage soft-start
- Undervoltage lockout threshold: 0.5 V (typical)

6.1.2. External view and pin assignment

External view and marking



Bottom view



Pin assignment

	1	2
A	V_{OUT}	V_{IN}
B	V_{ADJ}	CONTROL
C	GND	V_{BIAS}

Figure 6.1.1 External view, marking, and pin assignment

6.1.3. Internal block diagram

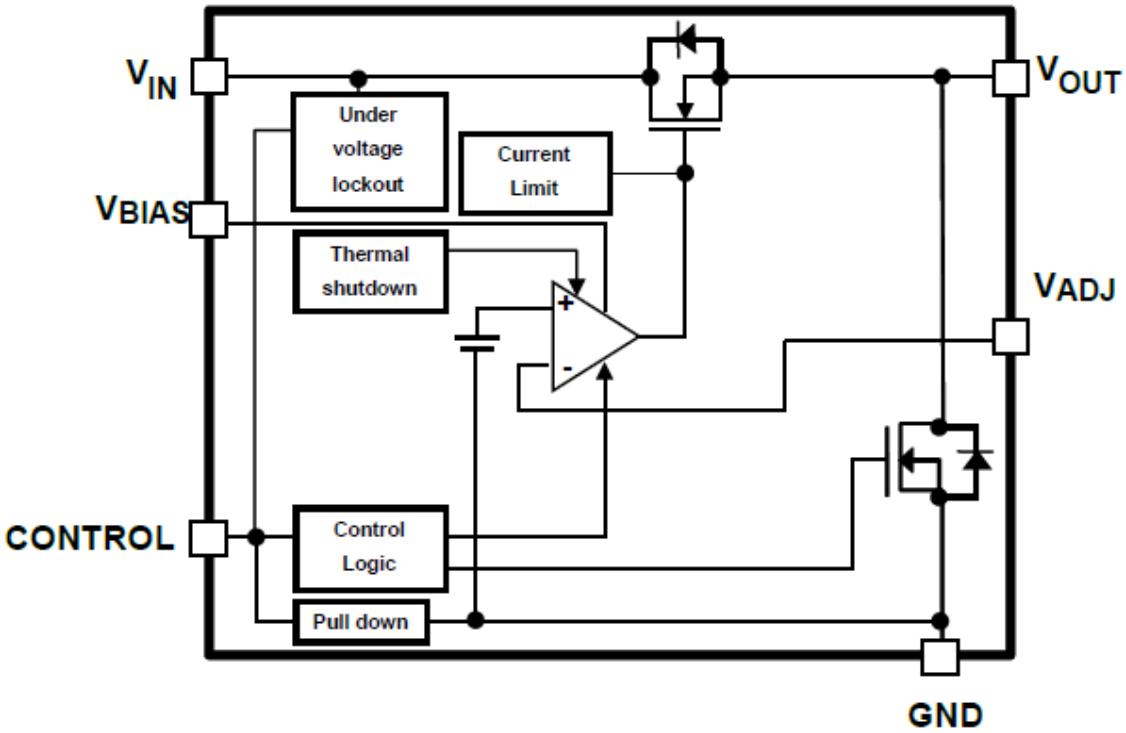


Figure 6.1.2 Internal block diagram

6.1.4. Pin description

Table 6.1 Pins of the TCR15AGADJ

Pin	Name	Description
A1	V_{OUT}	Output. For stable operation, add an output capacitor of 4.7μF or greater.
B1	V_{ADJ}	Output voltage control pin. R1 and R2 should be placed as close as possible to the V_{ADJ} pin to avoid the influence of noise.
A2	V_{IN}	Power supply input. The maximum V_{IN} voltage is 5.5V. For stable operation, add an input capacitor of 4.7μF or greater
B2	CONTROL	Output on/off control pin. A High on this input turns on the output. A Low on this input turns off the output. The CONTROL pin is internally connected to GND via a pulldown resistor.
C1	GND	Ground
C2	V_{BIAS}	Bias power supply pin. For stable operation, add a bias capacitor of 1.0μF or greater (with an ESR of 1.0Ω or less).

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