TOSHIBA BiCD Integrated Circuit Silicon Monolithic

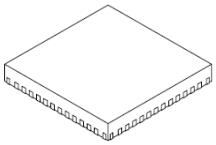
TB67S103AFTG, TB67S103AFNG

Serial-in controlled Bipolar Stepping Motor Driver

1. Description

The TB67S103A is a two-phase bipolar stepping motor driver using a PWM chopper. The data bank setting function by serial control I/F is built in.Fabricated with the BiCD process, rating is 50 V/4.0 A .

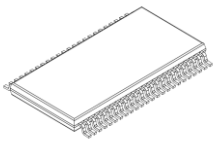
FTG



P-WQFN48-0707-0.50-003

weight 0.10 g（Typ.）

FNG



HTSSOP48-P-300-0.50

weight 0.21 g（Typ.）

2. Features

- BiCD process integrated monolithic IC.
- Capable of controlling 1 bipolar stepping motor.
- PWM controlled constant-current drive.
- Allows full, half, quarter, 1/8, 1/16, 1/32 step operation.
- ID (2 bits) setup is possible.
- Low on-resistance (High + Low side=0.49 Ω(Typ.)) MOSFET output stage.
- High efficiency motor current control mechanism (Advanced Dynamic Mixed Decay)
- High voltage and current (For specification, please refer to absolute maximum ratings and operation ranges)
- Error detection (TSD/ISD) signal output function
- Built-in error detection circuits (Thermal shutdown (TSD)、over-current shutdown (ISD), and power-on reset (POR))
- Built-in VCC regulator for internal circuit use.
- Chopping frequency of a motor can be customized by external resistance and condenser.
- Multi package lineup
  TB67S103AFTG: P-WQFN48-0707-0.50-003
  TB67S103AFNG: HTSSOP48-P-300-0.50

Note: Please be careful about thermal conditions during use.

3. Block Diagram

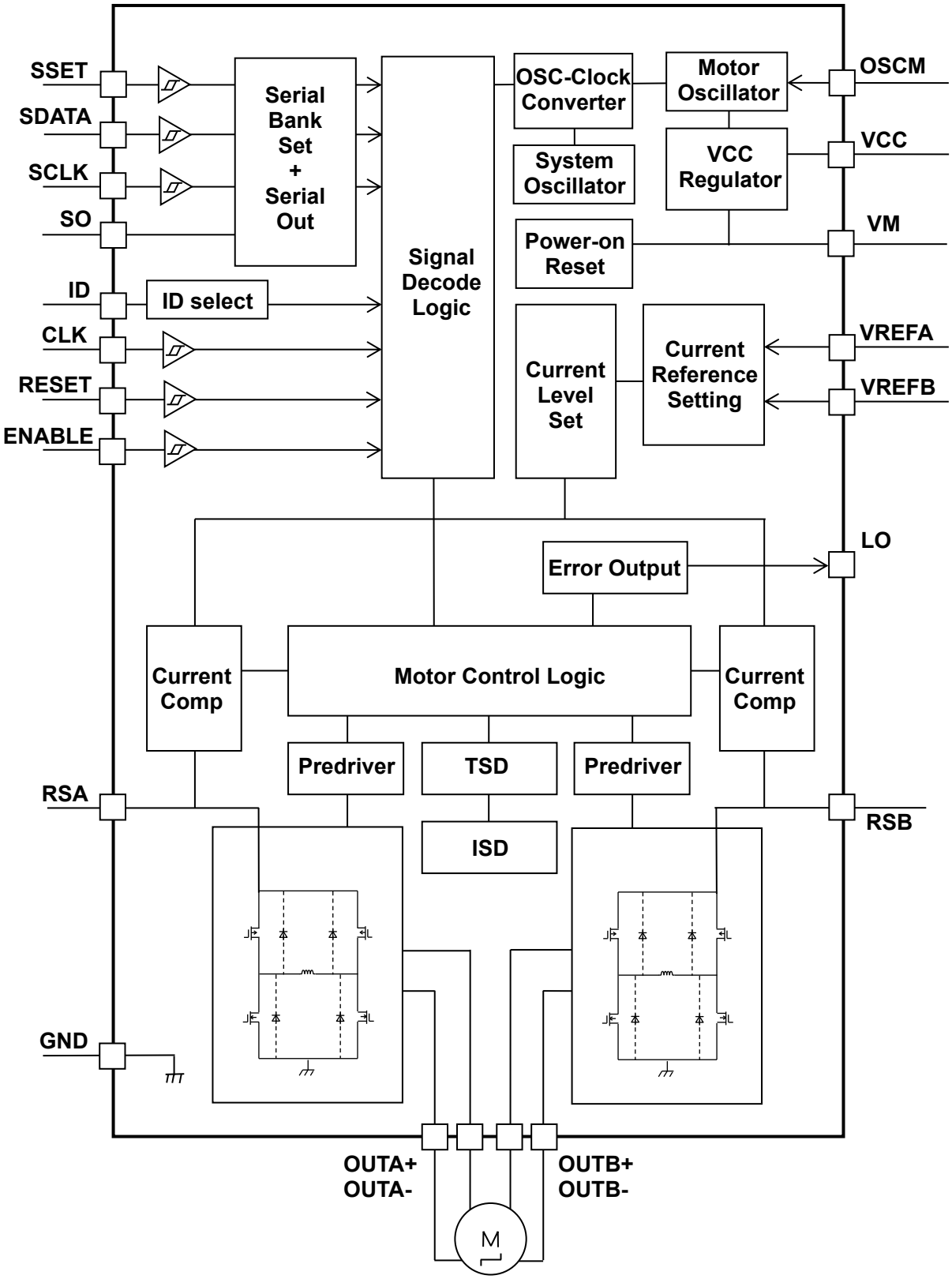


Figure 3.1 Block Diagram

Note: Functional blocks/circuits/constants in the block chart etc. may be omitted or simplified for explanatory purposes.

Note: All the grounding wires of the TB67S103A must run on the solder mask on the PCB and be externally terminated at only one point. Also, a grounding method should be considered for efficient heat dissipation.
Careful attention should be paid to the layout of the output, VDD(VM) and GND traces, to avoid short circuits across output pins or to the power supply or ground. If such a short circuit occurs, the device may be permanently damaged.
Also, the utmost care should be taken for pattern designing and implementation of the device since it has power supply pins (VM, RS, OUT, GND) through which a particularly large current may run. If these pins are wired incorrectly, an operation error may occur or the device may be destroyed.
The logic input pins must also be wired correctly. Otherwise, the device may be damaged owing to a current running through the IC that is larger than the specified current.

4. Pin Assignments

4.1. Pin assignment (FTG)

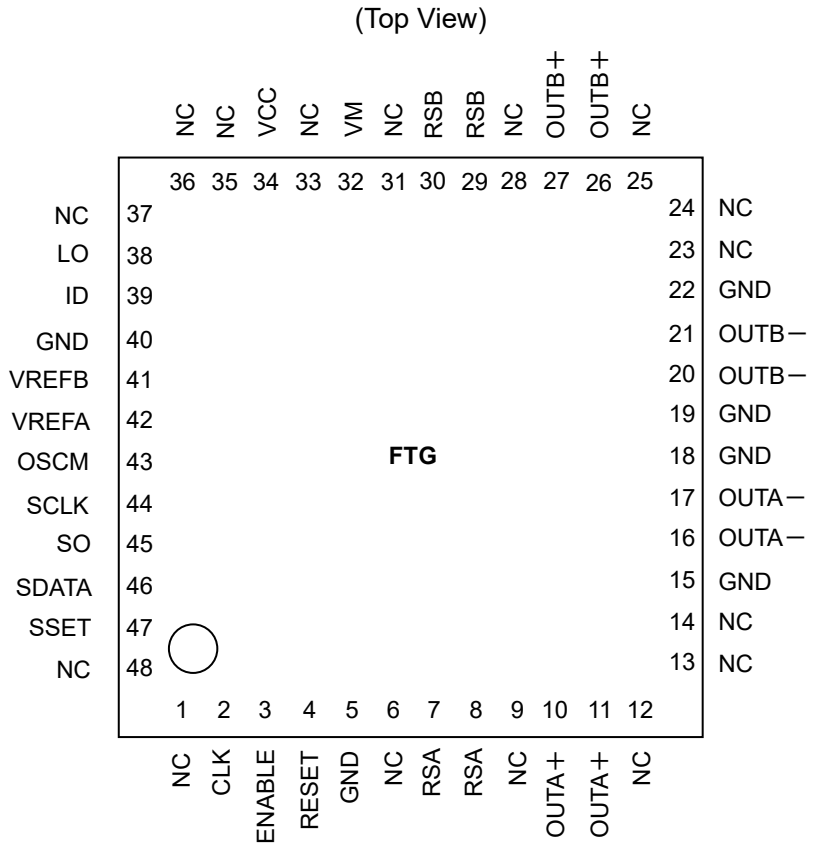


Figure 4.1 Pin Assignments (FTG)

Note: Please mount the four corner pins of the QFN package and the exposed pad to the GND area of the PCB.

4.2. Pin assignment (FNG)

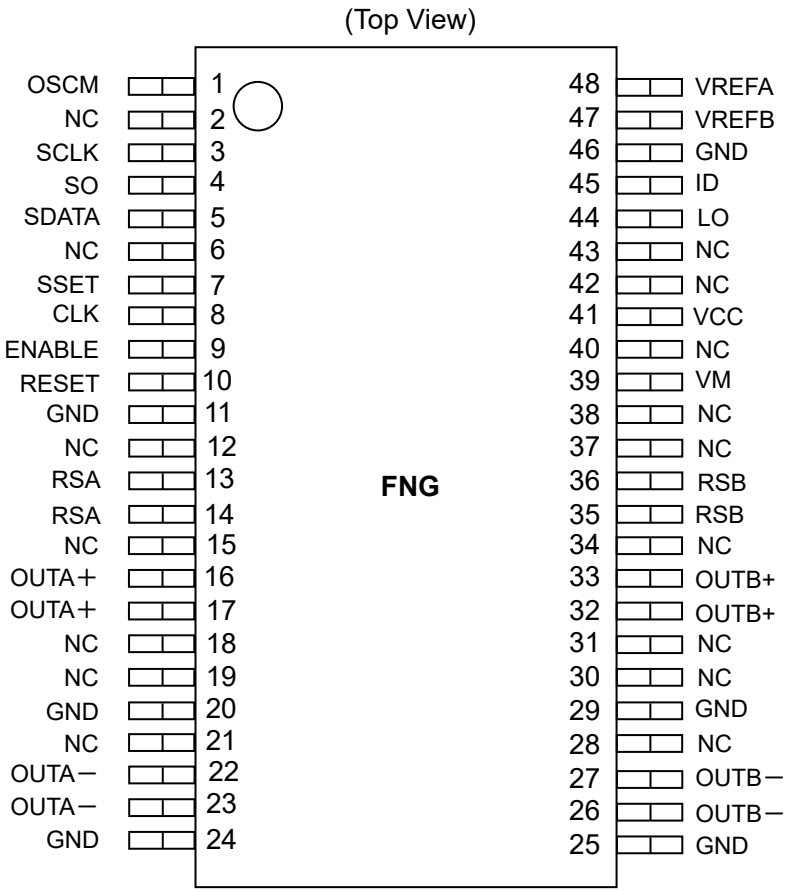


Figure 4.2 Pin Assignments (FNG)

Note: Please mount the exposed pad of the HTSSOP package to the GND area of the PCB.

5. Pin Description

5.1. TB67S103AFTG (QFN48)

Table 5.1 Pin Description(1 to 28)

Pin No.	Pin Name	Function
1	NC	Non-connection pin
2	CLK	CLK signal input pin
3	ENABLE	Ach/Bch output stage ON/OFF control pin
4	RESET	Electric angle reset pin
5	GND	Ground pin
6	NC	Non-connection pin
7	RSA (Note)	Motor Ach current sense pin
8	RSA (Note)	Motor Ach current sense pin
9	NC	Non-connection pin
10	OUTA+ (Note)	Motor Ach (+) output pin
11	OUTA+ (Note)	Motor Ach (+) output pin
12	NC	Non-connection pin
13	NC	Non-connection pin
14	NC	Non-connection pin
15	GND	Ground pin
16	OUTA- (Note)	Motor Ach (-) output pin
17	OUTA- (Note)	Motor Ach (-) output pin
18	GND	Ground pin
19	GND	Ground pin
20	OUTB- (Note)	Motor Bch (-) output pin
21	OUTB- (Note)	Motor Bch (-) output pin
22	GND	Ground pin
23	NC	Non-connection pin
24	NC	Non-connection pin
25	NC	Non-connection pin
26	OUTB+ (Note)	Motor Bch (+) output pin
27	OUTB+ (Note)	Motor Bch (+) output pin
28	NC	Non-connection pin

Note: Please connect the pins with the same names, at the nearest point of the device.
Please do not run patterns under NC pins.

Table 5.2 Pin Description(29 to 48)

Pin No.	Pin Name	Function
29	RSB (Note)	Motor Bch current sense pin
30	RSB (Note)	Motor Bch current sense pin
31	NC	Non-connection pin
32	VM	Motor power supply pin
33	NC	Non-connection pin
34	VCC	Internal VCC regulator monitor pin
35	NC	Non-connection pin
36	NC	Non-connection pin
37	NC	Non-connection pin
38	LO	Error detect signal output pin
39	ID	ID set pin
40	GND	Ground pin
41	VREFB	Motor Bch output set pin
42	VREFA	Motor Ach output set pin
43	OSCM	Oscillating circuit frequency for chopping set pin
44	SCLK	Serial clock input pin
45	SO	Serial data output pin
46	SDATA	Serial data input pin
47	SSET	Set signal input pin
48	NC	Non-connection pin

Note: Please connect the pins with the same names, at the nearest point of the device.
Please do not run patterns under NC pins.

5.2. TB67S103AFNG (HTSSOP48)

Table 5.3 Pin Description(1 to 28)

Pin No.	Pin Name	Function
1	OSCM	Oscillating circuit frequency for chopping set pin
2	NC	Non-connection pin
3	SCLK	Serial clock input pin
4	SO	Serial data output pin
5	SDATA	Serial data input pin
6	NC	Non-connection pin
7	SSET	Set signal input pin
8	CLK	CLK signal input pin
9	ENABLE	Ach/Bch output stage ON/OFF control pin
10	RESET	Electric angle reset pin
11	GND	Ground pin
12	NC	Non-connection pin
13	RSA (Note)	Motor Ach current sense pin
14	RSA (Note)	Motor Ach current sense pin
15	NC	Non-connection pin
16	OUTA+ (Note)	Motor Ach (+) output pin
17	OUTA+ (Note)	Motor Ach (+) output pin
18	NC	Non-connection pin
19	NC	Non-connection pin
20	GND	Ground pin
21	NC	Non-connection pin
22	OUTA- (Note)	Motor Ach (-) output pin
23	OUTA- (Note)	Motor Ach (-) output pin
24	GND	Ground pin
25	GND	Ground pin
26	OUTB- (Note)	Motor Bch (-) output pin
27	OUTB- (Note)	Motor Bch (-) output pin
28	NC	Non-connection pin

Note: Please connect the pins with the same names, at the nearest point of the device.
Please do not run patterns under NC pins.

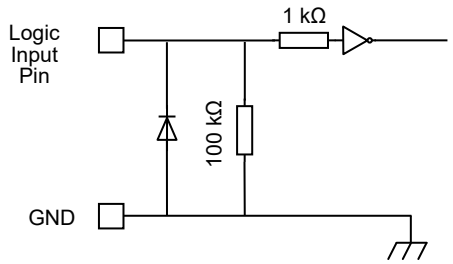
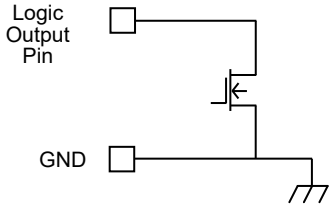
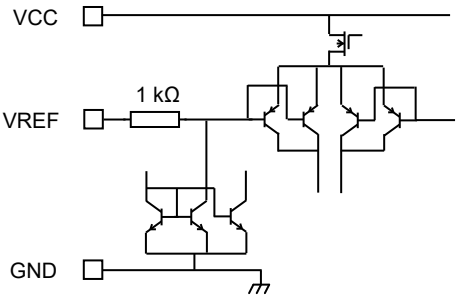
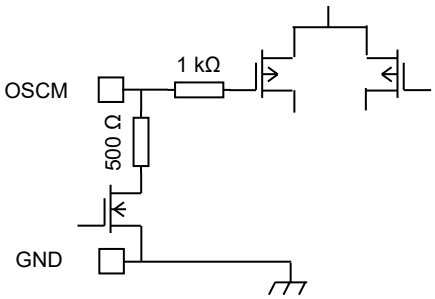
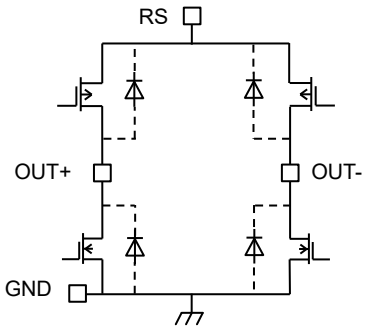
Table 5.4 Pin Description(29 to 48)

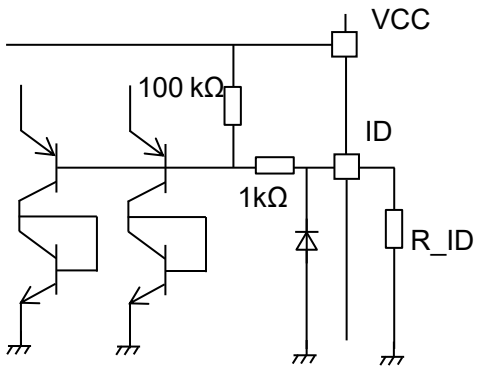
Pin No.	Pin Name	Function
29	GND	Ground pin
30	NC	Non-connection pin
31	NC	Non-connection pin
32	OUTB+ (Note)	Motor Bch (+) output pin
33	OUTB+ (Note)	Motor Bch (+) output pin
34	NC	Non-connection pin
35	RSB (Note)	Motor Bch current sense pin
36	RSB (Note)	Motor Bch current sense pin
37	NC	Non-connection pin
38	NC	Non-connection pin
39	VM	Motor power supply pin
40	NC	Non-connection pin
41	VCC	Internal VCC regulator monitor pin
42	NC	Non-connection pin
43	NC	Non-connection pin
44	LO	Error detect signal output pin
45	ID	ID set pin
46	GND	Ground pin
47	VREFB	Motor Bch output set pin
48	VREFA	Motor Ach output set pin

Note: Please connect the pins with the same names, at the nearest point of the device.
Please do not run patterns under NC pins.

5.3. INPUT/OUTPUT equivalent circuit (TB67S103A)

Table 5.5 equivalent circuit (TB67S103A)

Pin name	IN/OUT signal	Equivalent circuit
SCLK SDATA SSET CLK ENABLE RESET	Digital Input (VIH/VIL) VIH: 2.0 V(Min)~5.5 V(Max) VIL : 0 V(Min)~0.8 V(Max)	
SO LO	Digital Output (VOH/VOL) (Pullup resistance :10 k～100 kΩ)	
VCC VREFA VREFB	VCC voltage range 4.75 V(Min)~5.0 V(Typ.)~5.25 V(Max) VREF voltage range 0 V~3.6 V	
OSCM	OSCM frequency setting range 0.64 MHz(Min)~1.12 MHz(Typ.)~2.4 MHz(Max)	
OUTA+ OUTA- OUTB+ OUTB- RSA RSB	VM power supply voltage range 10 V(Min)~47 V(Max) OUT pin voltage 10 V(Min)~47 V(Max)	

Pin name	IN/OUT signal	Equivalent circuit
ID	<ID1:ID0> <1:1> R_ID=Open (5 V set) <1:0> R_ID=100 kΩ (2.5 V set) <0:1> R_ID=33 kΩ (1.25 V set) <0:0> R_ID=GND (0 V set) It is possible to change ID setup of a device by attaching resistance (or GND short-circuit / Open) to ID terminal. When <ID1:ID0> set up with ID terminal and <ID1:ID0> of a serial input are in agreement, the serial data inputted to the device are made to reflect. *The variation in resistance is ±30 %.	

Note: The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

6. Functional Description (Stepping motor)

6.1. CLK Function

Each up-edge of the CLK signal will shift the motor's electrical angle per step.

Table 6.1 CLK Function

CLK Input	Function
Up-edge	Shifts the electrical angle per step.
Down-edge	(State of the electrical angle does not change.)

6.2. ENABLE function

The ENABLE pin controls the ON and OFF of the corresponding output stage. This pin serves to select if the motor is stopped in Off (High impedance) mode or activated. Please set the ENABLE pin to 'L' during VM power-on and power-off sequence.

Table 6.2 ENABLE Function

ENABLE Input	Function
H	Output stage='ON' (Normal operation mode)
L	Output stage='OFF) (High impedance mode)

6.3. RESET function

Table 6.3 RESET Function

RESET Input	Function
H	Sets the electrical angle to the initial condition.
L	Normal operation mode

The current for each channel (while RESET is applied) is shown in the table below. MO will show 'L' at this time.

Table 6.4 current for each channel while RESET

Step resolution setting	Ach current setting	Bch current setting	Default electrical angle
Full step	100 %	100 %	45 °
Half step (Type (A))	100 %	100 %	45 °
Half step (Type (B))	71 %	71 %	45 °
Quarter step	71 %	71 %	45 °
1/8 step	71 %	71 %	45 °
1/16 step	71 %	71 %	45 °
1/32 step	71 %	71 %	45 °

6.4. Step resolution setting and initial angle

6.4.1. Full step resolution

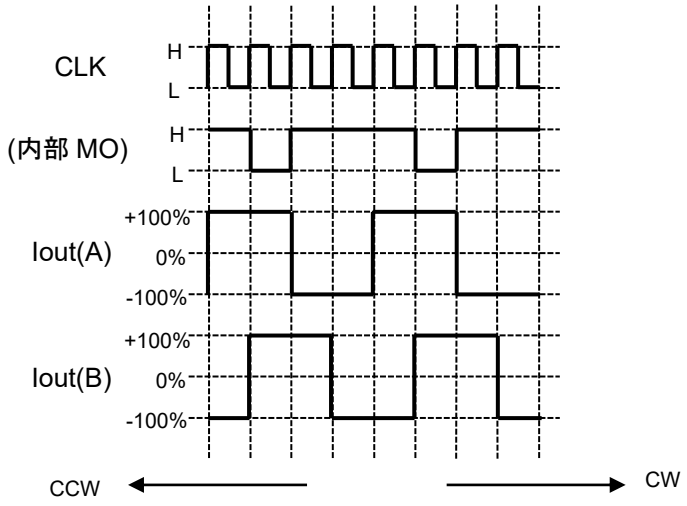


Figure 6.1 Full step resolution

6.4.2. Half step resolution (Type A)

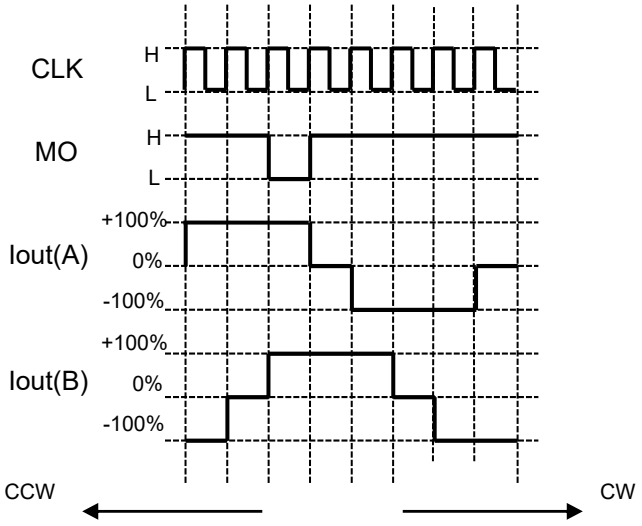


Figure 6.2 Half step resolution (Type A)

MO output shown in the timing chart is when the MO pin is pulled up.

Note: Timing charts may be simplified for explanatory purpose.

6.4.3. Half step resolution (Type B)

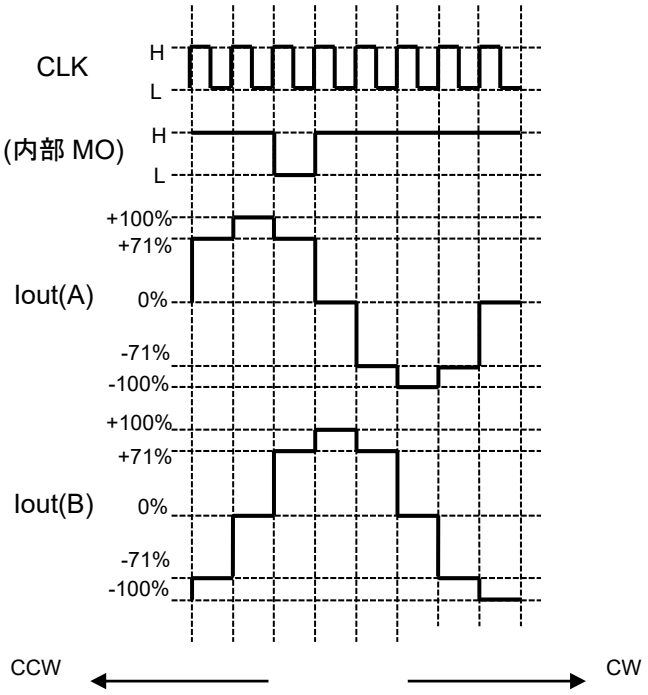


Figure 6.3 Half step resolution (Type B)

6.4.4. Quarter step resolution

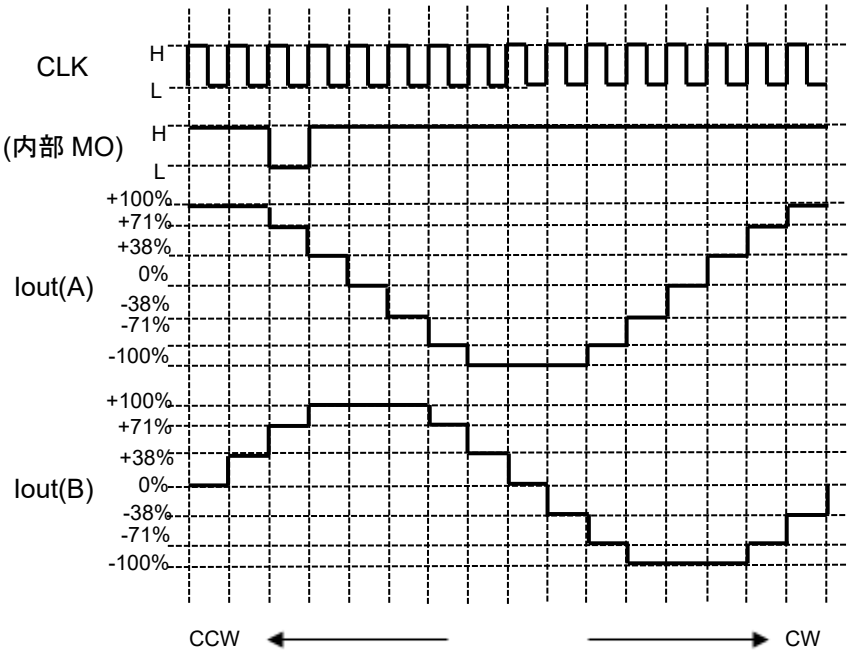


Figure 6.4 Quarter step resolution

MO output shown in the timing chart is when the MO pin is pulled up.

Note: Timing charts may be simplified for explanatory purpose.

6.4.5. 1/8 step resolution

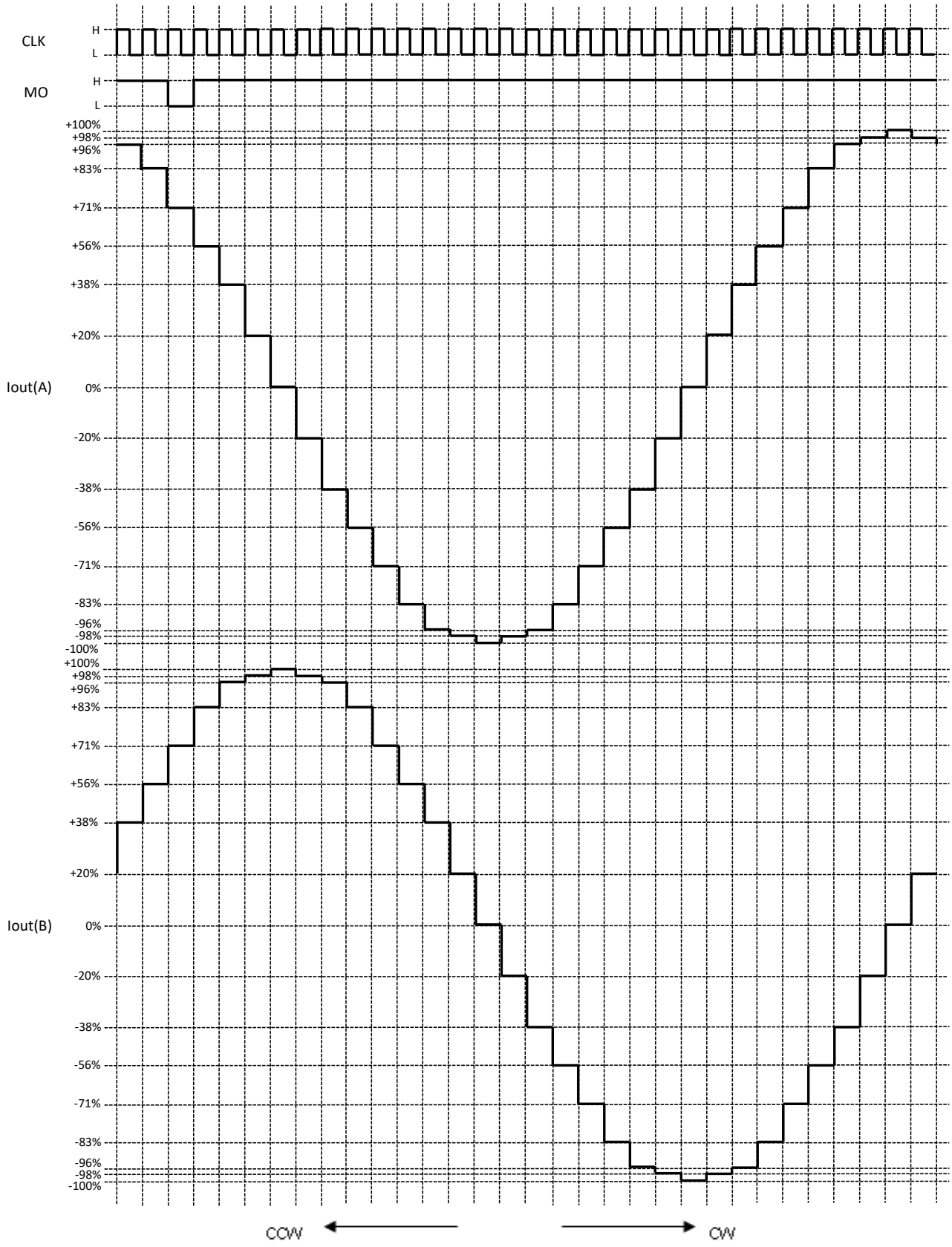


Figure 6.5 1/8 step resolution

MO output shown in the timing chart is when the MO pin is pulled up.

Note: Timing charts may be simplified for explanatory purpose.

6.4.6. 1/16 step resolution

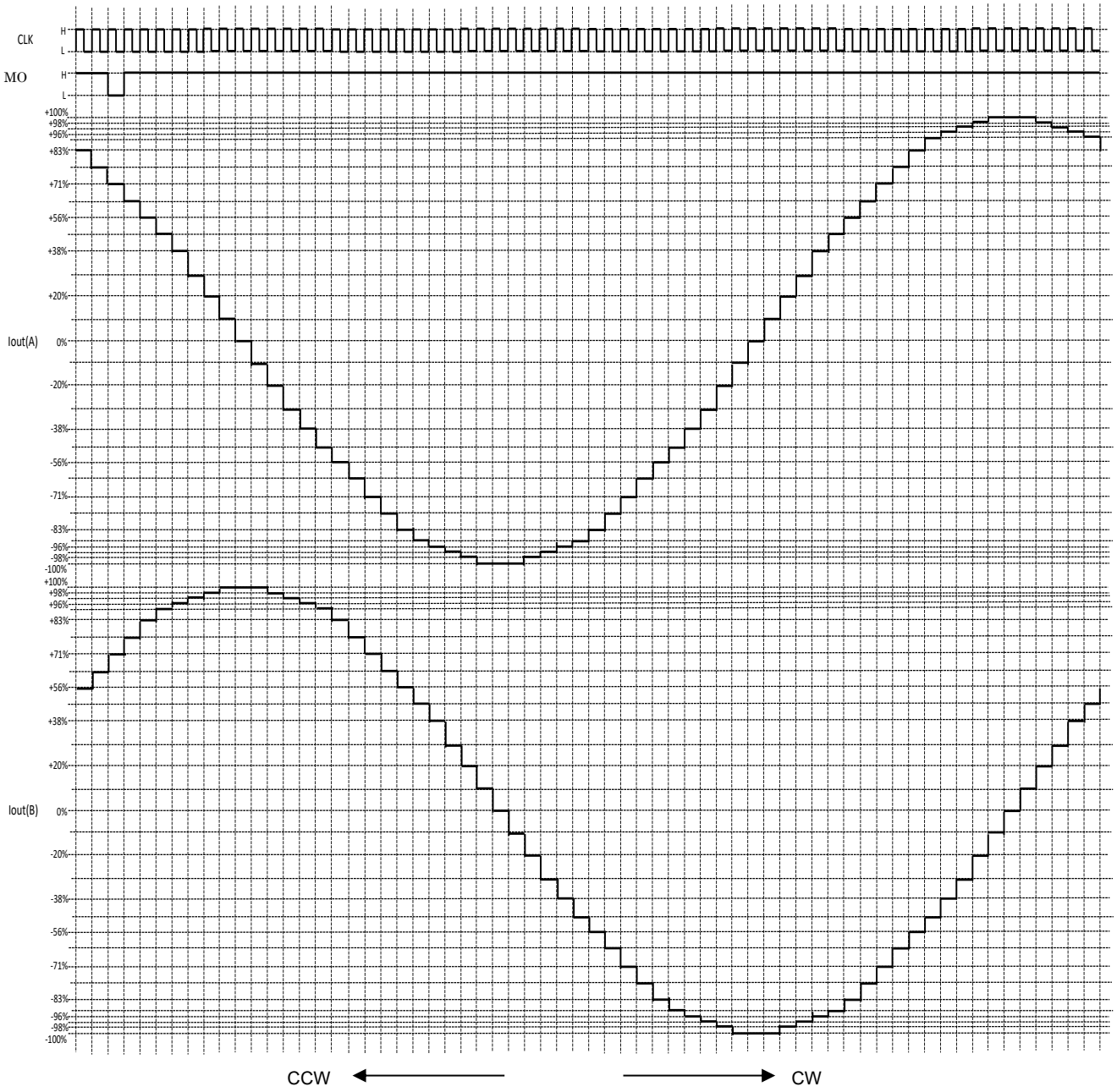


Figure 6.6 1/16 step resolution

MO output shown in the timing chart is when the MO pin is pulled up.

Note: Timing charts may be simplified for explanatory purpose.

[1/32 step resolution]

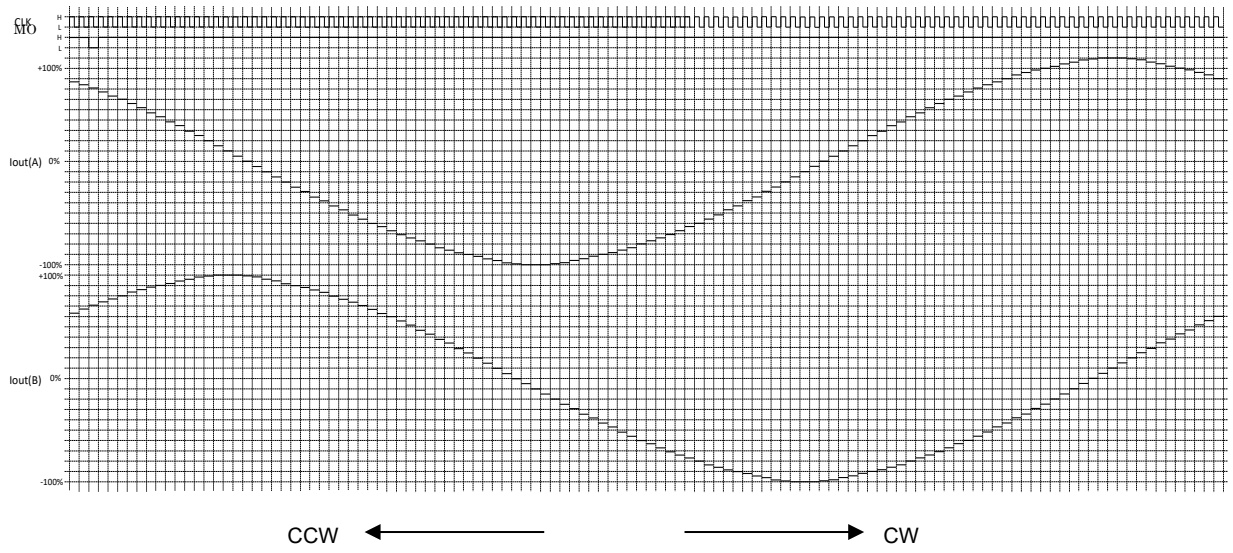


Figure 6.7 1/32 step resolution

MO output shown in the timing chart is when the MO pin is pulled up.

Note: Timing charts may be simplified for explanatory purpose.

6.5. Device distinction circuit (ID_SELECT)

Table 6.5 ID setting

ID	<ID1:ID0>			
	<0:0>	<0:1>	<1:0>	<1:1>
R_ID=GND	○	-	-	-
R_ID=33 kΩ(1.25 V set)	-	○	-	-
R_ID=100 kΩ(2.5 V set)	-	-	○	-
R_ID=Open	-	-	-	○

It is possible to change ID setup of a device by attaching resistance (or GND short-circuit / Open) to ID terminal.
When <ID1:ID0> set up with ID terminal and <ID1:ID0> of a serial input are in agreement, the serial data inputted to the device are made to reflect.

6.6. About serial input data (TB67S103A)

A serial input is effective only when a SSET pin is "H". A setup of operation is possible by 3 line serial input of "SCLK", "SDATA", and "SSET."

■Specification of Setup Mode (timing chart)

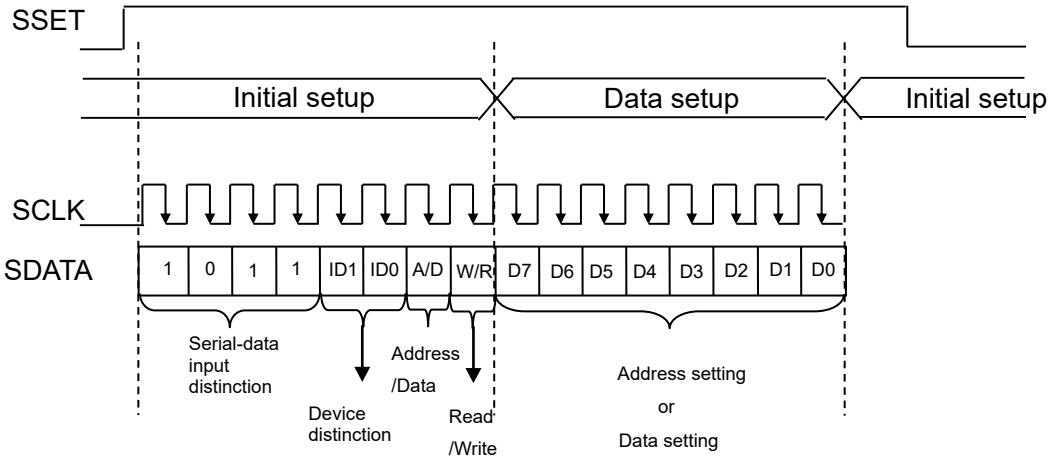


Figure 6.8 Setup Mode timing chart

Note: Timing charts may be simplified for explanatory purpose.

Input data is 16-bit composition (it decodes every 8 bits).
Please input serial data in order of the following.
(SSET input is switched to H from L)→ (Initial setup input) → (Data setup input)

In order that TB67S103A may prevent the incorrect input of serial data, it is checked whether serial data have been normally inputted in Initial setup.

(Example) The case of IC of ID setup ='00'
Data setup is received when Initial setup='1011 0000' is inputted.
Data setup is not received when Initial setup='1011 0100' is inputted.
Data setup is not received when Initial setup='1010 0000' is inputted.
Please input “1011(S103 characteristic value)” into 4 bits of heads.

In 1 to 4 bits=”1011” and 5 to 6 bits=”ID setup”, serial data are received.
7 bits is an A/D setup. (0: Address Setup and 1: Data Setup)
8 bits is a W/R setup. (0: Write mode and 1: Read mode)
In Write mode, an address or data is set up by [Data setup].
In Read mode, it is possible to output the value (an address or data) of a register from SO pin.

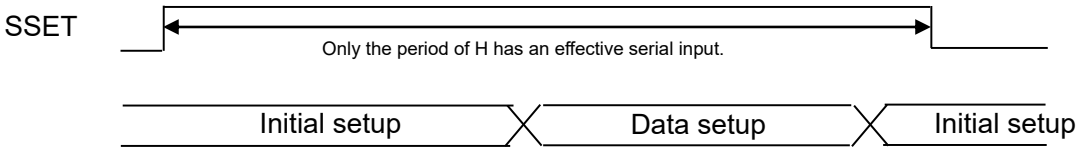


Figure 6.9 SSET timing chart

The input of serial data becomes effective only in SSET=H. The serial data inputted between SSET=L are not received.

■About a serial input (Initial setup→Data setup Flow chart)

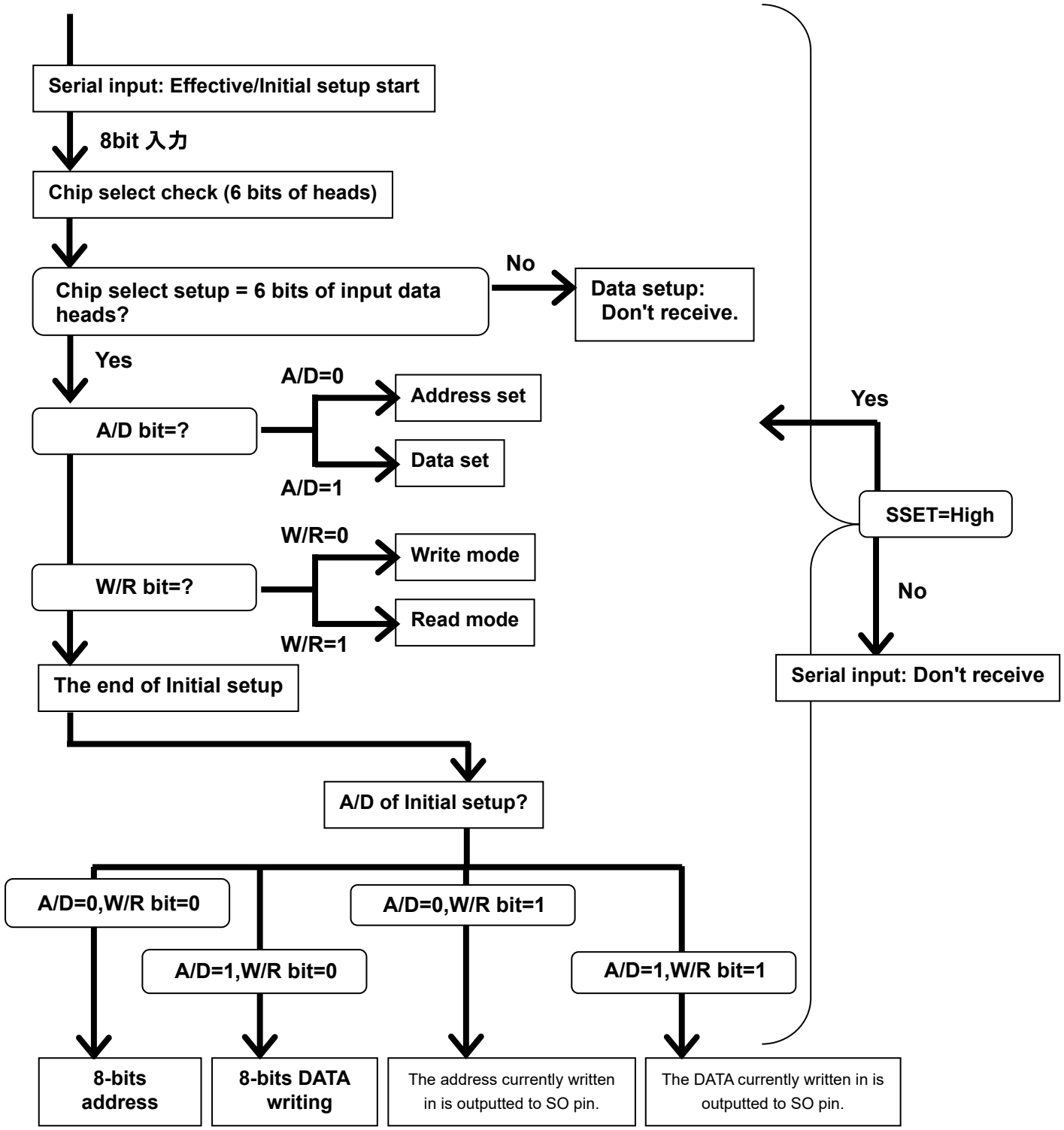


Figure 6.10 Input flow

◆The change of a Serial bank

Table 6.6. The change of a Serial bank

DATA Bit			Function
[A2]	[A1]	[A0]	
0	0	0	It is a serial-data input to BANK0.
0	0	1	It is a serial-data input to BANK1.
0	1	0	It is a serial-data input to BANK2.
0	1	1	It is a serial-data input to BANK3.
1	0	0	It is a serial-data input to BANK4.
1	0	1	It is a serial-data input to BANK5.
1	1	0	It is a serial-data input to BANK6.
1	1	1	It is a serial-data input to BANK7.

6.7. BANK Setup

6.7.1. BANK0: Motor drive: Setup 1 (basic setup)

Table6.7.1.1 <D7:D6>

DATA Bit		Function
[D7]	[D6]	
0	0	- Don't care
0	1	- Don't care
1	0	- Don't care
1	1	- Don't care

fOSCM=1.6MHz(Typ.)

Table6.7.1.2 <D5:D4> Motor drive：torque setting

DATA Bit		Function
[D5]	[D4]	
0	0	Iout×40 % **(Initial)**
0	1	Iout×60 %
1	0	Iout×80 %
1	1	Iout×100 %

Table6.7.1.3 < D3> Motor drive：CW/CCW setting

DATA Bit	Function
[D3]	
0	CCW (At the time of charge OUT+pin：L, OUT-pin：H) (**Initial)**
1	CW (At the time of charge OUT+pin：H, OUT-pin：L)

Table6.7.1.4 <D2:D0> Motor drive：Step resolution setting

DATA Bit			Function
[D2]	[D1]	[D0]	
0	0	0	Standby mode (Power-saving mode) **(Initial)** (Note)
0	0	1	**Full step resolution**
0	1	0	**Half step resolution(Type (A))**
0	1	1	**Quarter step resolution**
1	0	0	**Half step resolution(Type (B))**
1	0	1	**1/8 step resolution**
1	1	0	**1/16 step resolution**
1	1	1	**1/32 step resolution**

Note: Standby mode : the OSCM is disabled and the output stage is set to 'OFF' status.

6.7.2. BANK1: Motor drive: Setup 2 (basic setup)

Table6.7.2.1 < D7:D6> Motor drive：Decay mode setting

DATA Bit		Function
[D7]	[D6]	
0	0	Mixed Decay mode **(Initial)**
0	1	Slow Decay only
1	0	Fast Decay only
1	1	Auto Decay mode

Note: About a Decay mode setting：Please carry out change to Auto Decay mode(<D7:D6>=[1,1]) after stopping a motor.
（Please carry out the change of <D7:D6>=[0,0]/[0,1]/[1,0]⇔[1,1] after stopping a motor.）

Table6.7.2.2<D5:D4> Motor drive：fchop setting

DATA Bit		Function
[D5]	[D4]	
0	0	fchop=100 kHz **(Initial)**
0	1	fchop=50 kHz
1	0	fchop=66.6 kHz
1	1	Test mode (Don’t use)

Note: At the time of fOSCM=1.6MHz(Typ) setting, fchop=100kHz

Table6.7.2.3< D3:D2> Motor drive：Mixed decay timing(MDT) setting

DATA Bit		Function
[D3]	[D2]	
0	0	MDT=37.5 % **(Initial)**
0	1	MDT=50 %
1	0	MDT=25 %
1	1	MDT=12.5 %

Note: About MDTsetting：Only in Mixed Decay mode(<D7:D6>=[0,0]), this setup is effective.

Table6.7.2.4<D1:D0> Motor drive：revolving speed setting

DATA Bit		Function
[D1]	[D0]	
0	0	fCLK×100 % **(Initial)**
0	1	fCLK×50 %
1	0	fCLK×25 %
1	1	fCLK×12.5 %

Note: When a setup of BANK is changed during operation, it is reflected in the timing of the next fchop start.

6.7.3. BANK2　Others: Option setup (Reference value)

Table6.7.3.1 < D7:D6> Error detection function：ISD Masking time setting

DATA Bit		Function
[D7]	[D6]	
0	0	8×1/foscs (1.25 μs) **(Initial)**
0	1	4×1/foscs (0.625 μs)
1	0	16×1/foscs (2.5 μs)
1	1	32×1/foscs (5.0 μs)

Table6.7.3.2 Error detection function：TSD Masking time setting

DATA Bit		Function
[D5]	[D4]	
0	0	16×1/foscs (2.5 μs) **(Initial)**
0	1	4×1/foscs (0.625 μs)
1	0	8×1/foscs (1.25 μs)
1	1	32×1/foscs (5.0 μs)

Table6.7.3.3 < D3:D2> Error detection function：VRS Masking time setting

DATA Bit		Function
[D3]	[D2]	
0	0	8×1/foscs (1.25 μs) **(Initial)**
0	1	4×1/foscs (0.625 μs)
1	0	16×1/foscs (2.5 μs)
1	1	32×1/foscs (5.0 μs)

foscs=6.4MHz(Typ.) internal clock
SERIAL DATA: BANK2 <D7:D6>(ISD Masking time)/<D3:D2>(VRS Masking time)
In the case of ”0,0”: About 1/foscs×7~8clk(1.09μs~1.25μs)
In the case of ”0,1”: About 1/foscs×3~4clk(0.47μs~0.63μs)
In the case of ”1,0”: About 1/(foscs/2) ×7~8clk=1/foscs×14~16clk(2.5 μs~2.8 μs)
In the case of ”1,1”: About 1/(foscs/4) ×7~8clk=1/foscs×32~36clk(5.0 μs~5.6 μs)

foscs=6.4MHz(Typ.) internal clock
SERIAL DATA: BANK2 <D:5/D4>(TSD Masking time)
In the case of ”0,0”: About 1/(foscs/2) ×7~8clk=1/foscs×14~16clk(2.5 μs~2.8 μs)
In the case of ”0,1”: About 1/foscs×3~4clk(0.47 μs~0.63 μs)
In the case of ”1,0”: About 1/foscs×7~8clk(1.09 μs~1.25 μs)
In the case of ”1,1”: About 1/(foscs/4) ×7~8clk=1/foscs×32~36clk(5.0 μs~5.6 μs)

Table6.7.3.4 < D1:D0> Motor drive：Digital tblank setting

DATA Bit		Function
[D1]	[D0]	
0	0	2×1/fOSCM **(Initial)**
0	1	3×1/fOSCM
1	0	4×1/fOSCM
1	1	6×1/fOSCM

fOSCM=1.6 MHz(Typ.)

Note: When a setup of BANK is changed during operation, it is reflected in the timing of the next fchop start.

6.8. LO(Error detect signal) output function

When Thermal shutdown(TSD) or Over-current shutdown(ISD) is applied, the LO voltage will be switched to Low(GND) level.

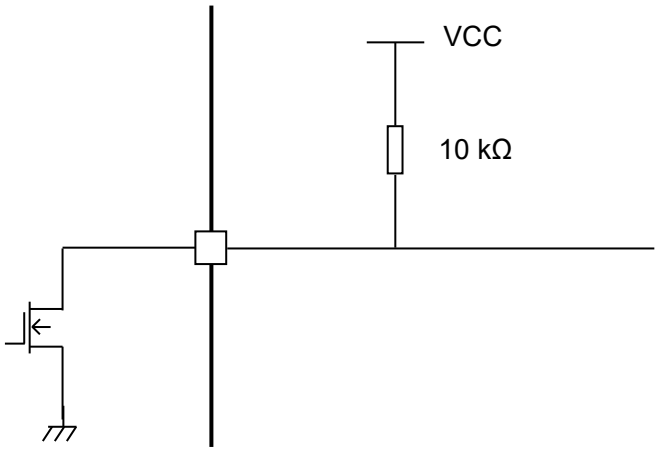


Figure 6.11 LO pin

The LO is an open-drain output pin. LO pin needs to be pulled up to 3.3 V/5.0 V level for proper function. During regular operation, the LO pin level will stay High(VCC level). When error detection (TSD, ISD) is applied, the LO pin will show Low (GND) level.

6.9. Decay function

6.9.1. ADMD(Advanced Dynamic Mixed Decay) constant current control

The Advanced Dynamic Mixed Decay threshold, which determines the current ripple level during current feedback control, is a unique value.

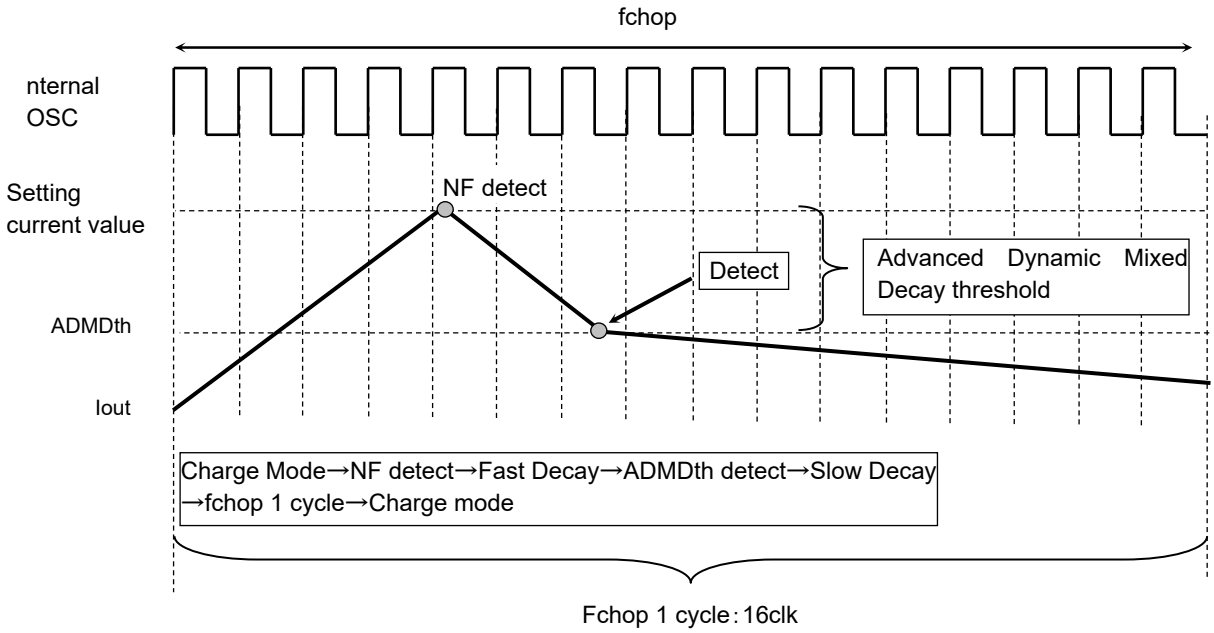


Figure 6.12 ADMD(Advanced Dynamic Mixed Decay) constant current control

6.9.1.1. Auto Decay Mode current waveform

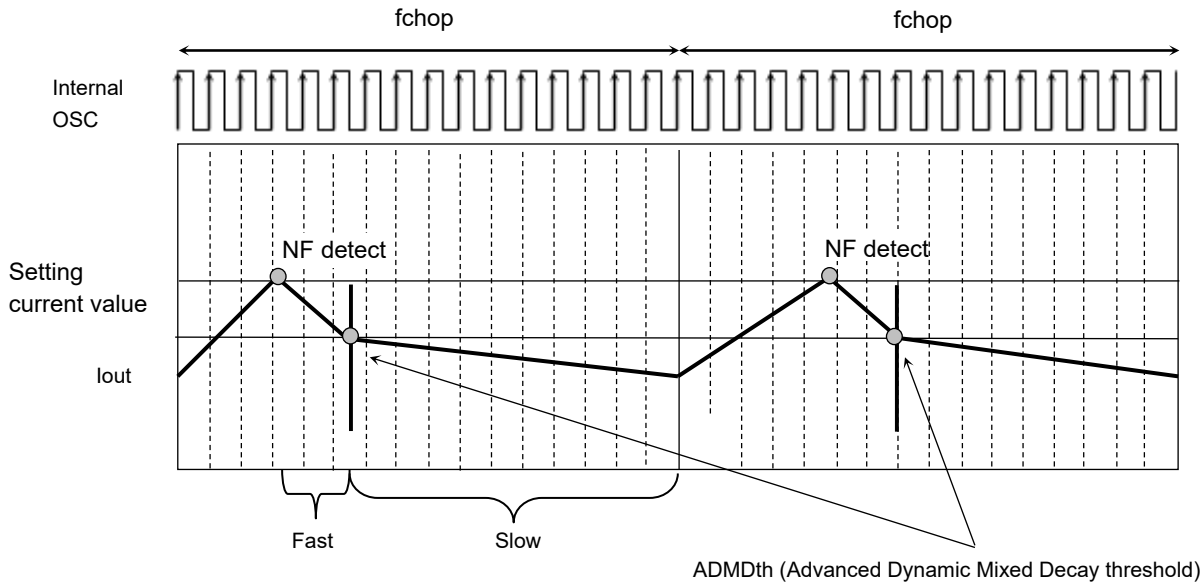


Figure 6.13 Auto Decay Mode current waveform

Note : Timing charts may be simplified for explanatory purpose.

6.9.2. ADMD current waveform

6.9.2.1. When the next current step is higher :

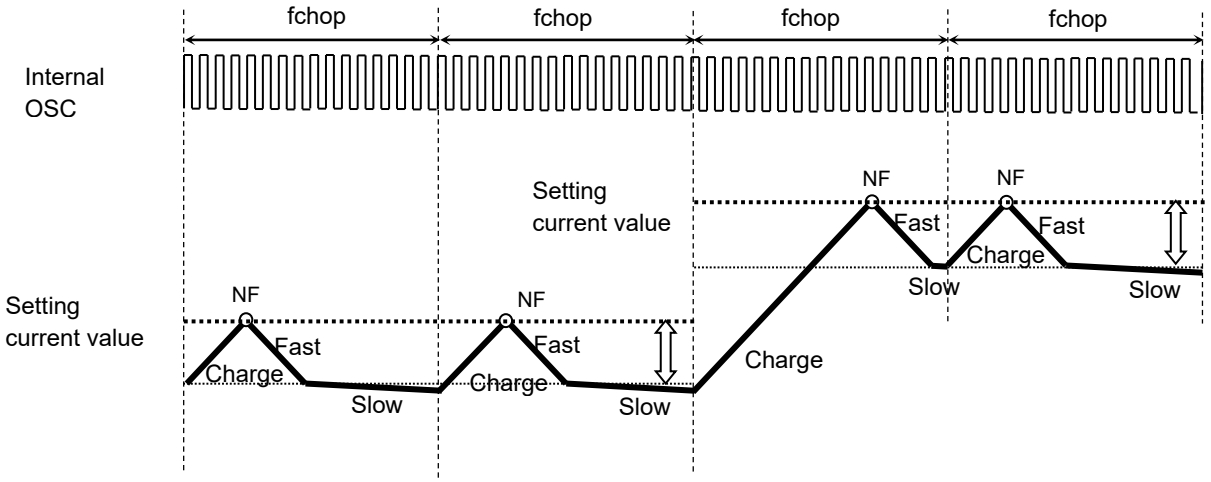


Figure 6.14 When the next current step is higher

6.9.2.2. When Charge period is more than 1 fchop cycle :

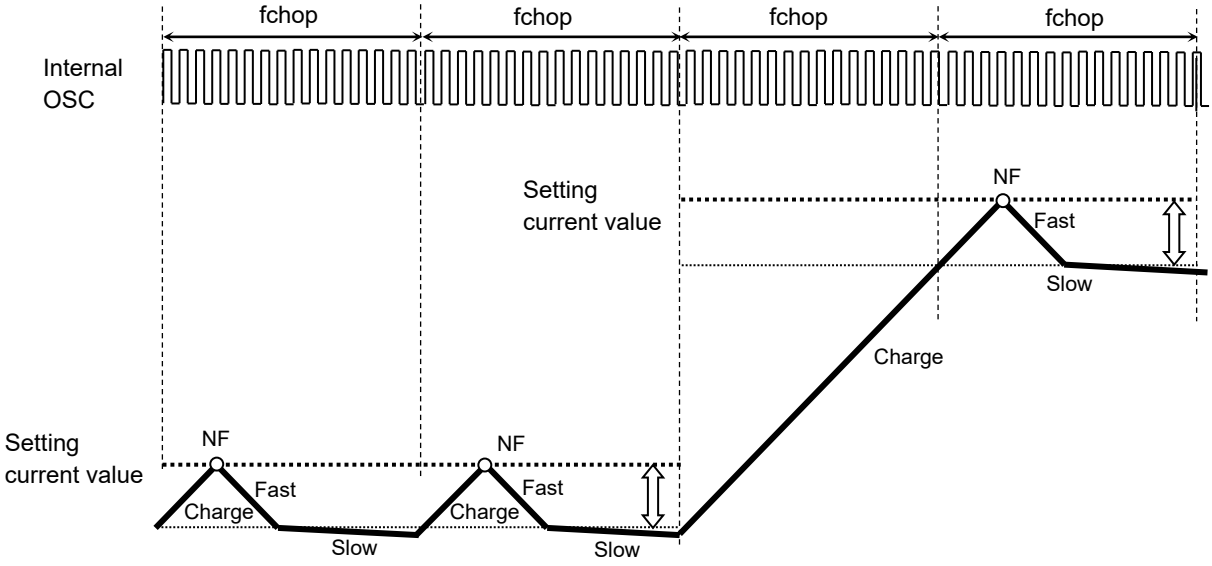


Figure 6.15 When Charge period is more than 1 fchop cycle

When the Charge period is longer than fchop cycle, the Charge period will be extended until the motor current reaches the
NF threshold. Once the current reaches the next current step, then the sequence will go on to decay mode.

Note : Timing charts may be simplified for explanatory purpose.

6.9.2.3. When the next current step is lower :

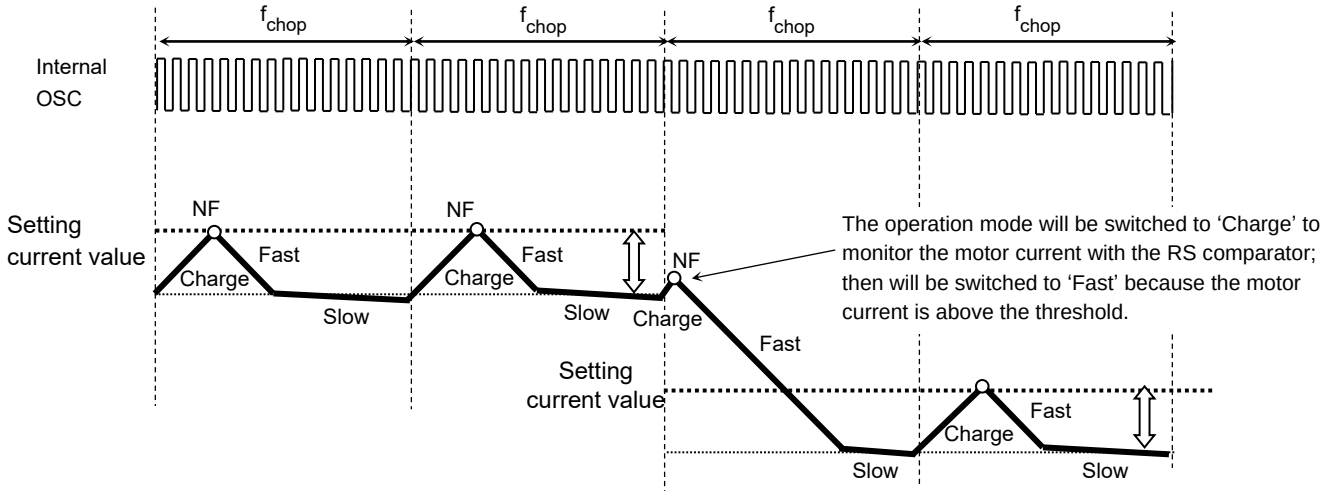


Figure 6.16 When the next current step is lower

6.9.2.4. When the Fast continues past 1 fchop cycle (the motor current not reaching the ADMD threshold during 1 fchop cycle)

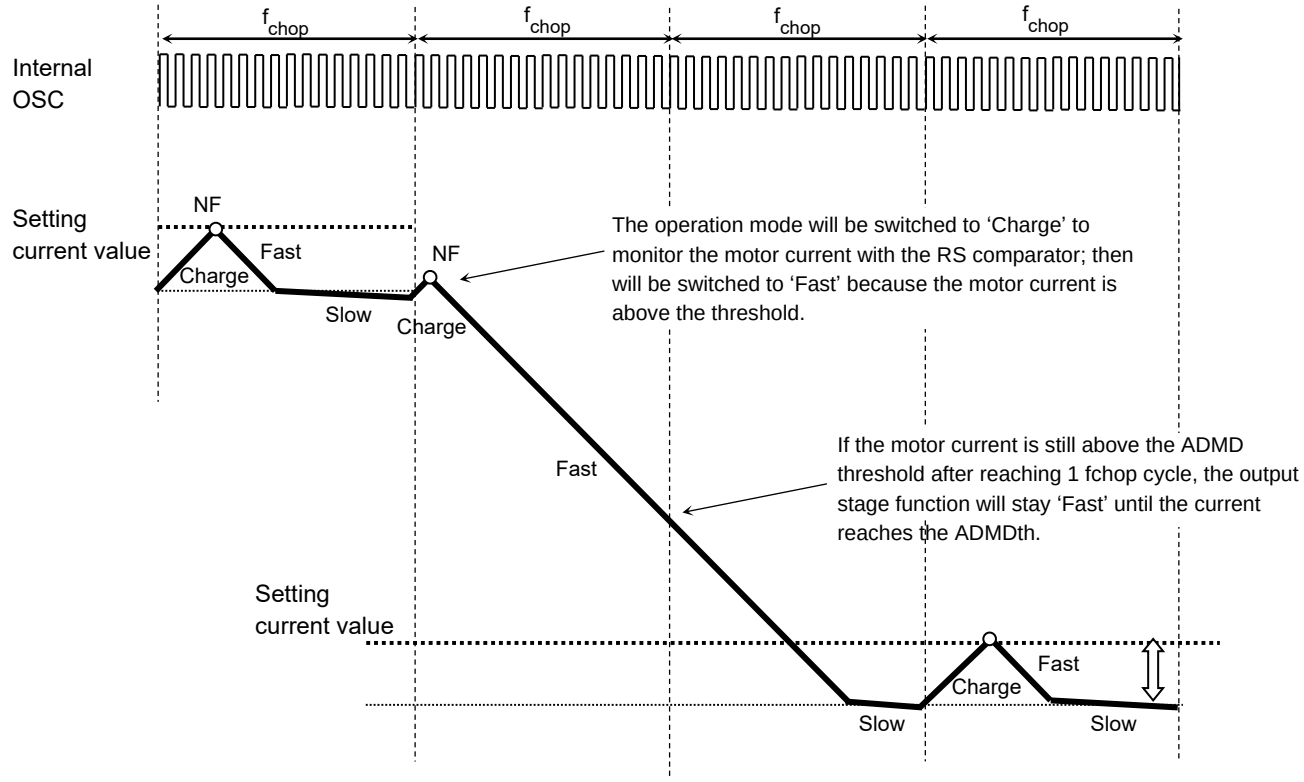


Figure 6.17 When the Fast continues past 1 fchop cycle

Note : Timing charts may be simplified for explanatory purpose.

6.9.3. Mixed Decay Mode current waveform

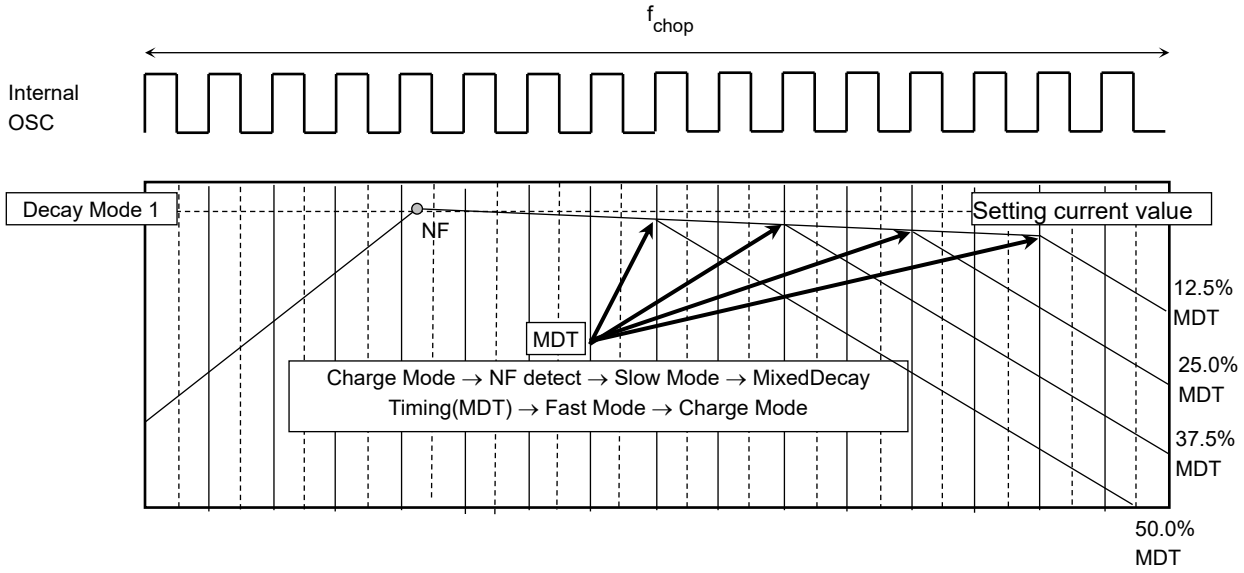


Figure 6.18 Mixed Decay Mode current waveform

6.9.4. Fast Decay (only) Mode current waveform

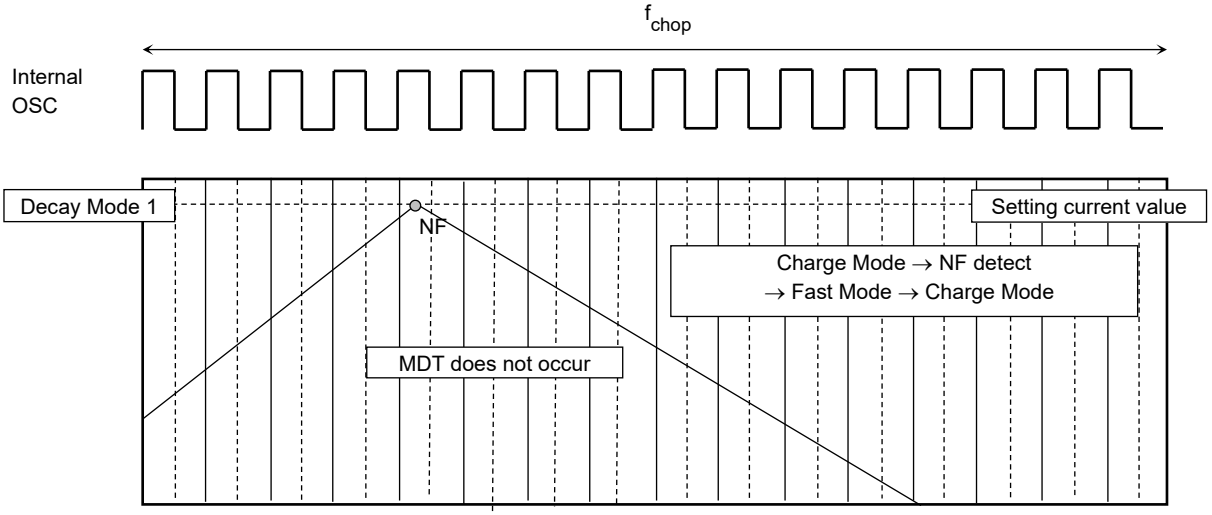


Figure 6.19 Fast Decay (only) Mode current waveform

Note : Timing charts may be simplified for explanatory purpose.

6.9.5. Slow Decay (only) Mode current waveform

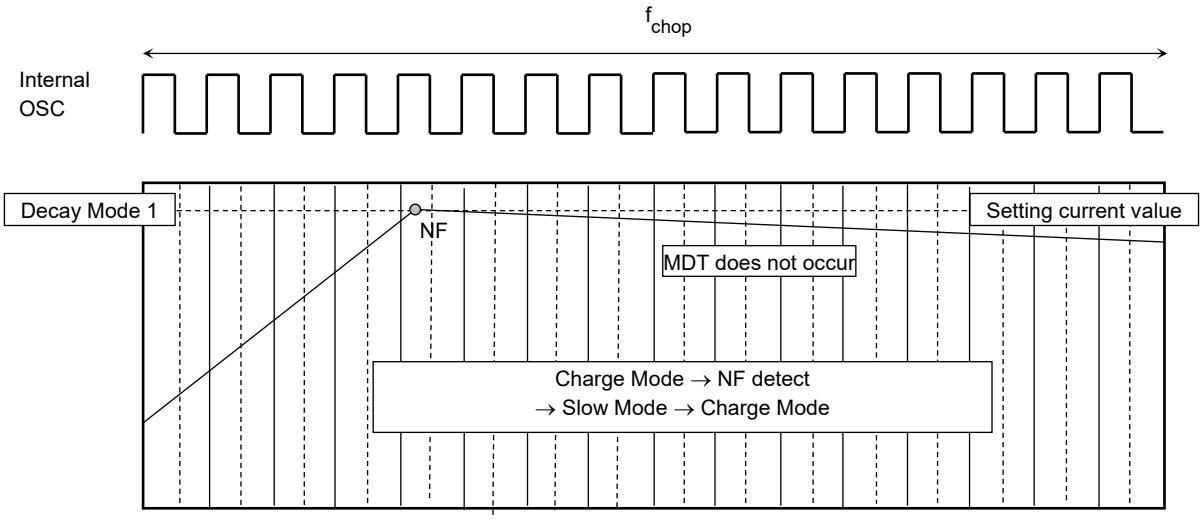


Figure 6.20 Slow Decay (only) Mode current waveform

Note: Timing charts may be simplified for explanatory purpose.

6.10. Output transistor function mode

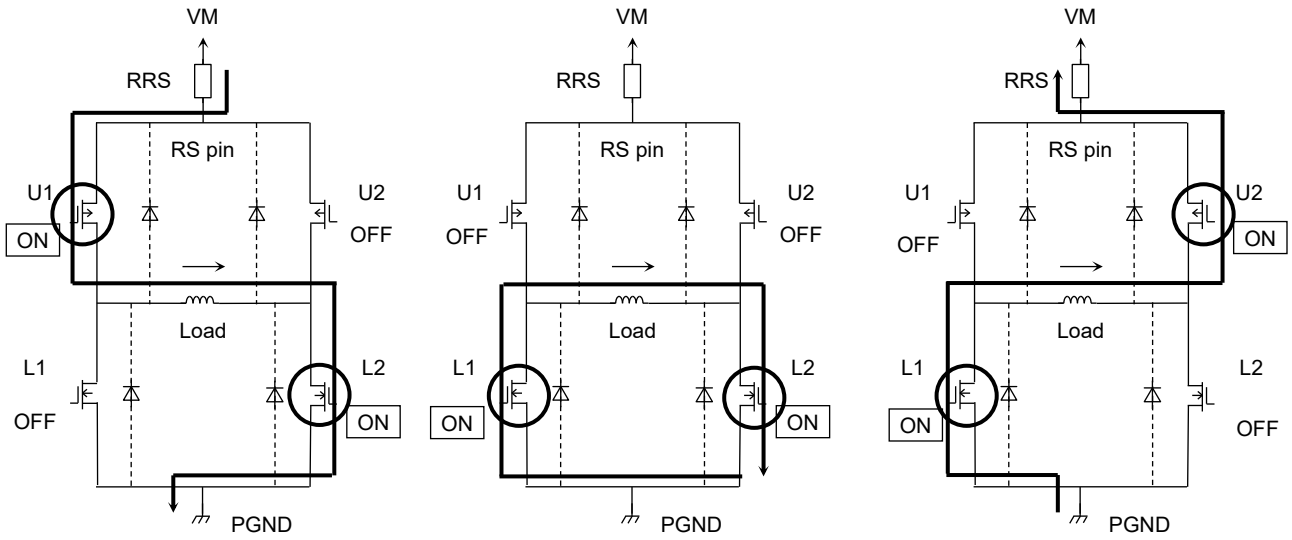


Figure 6.21 Output transistor function mode

6.10.1. Output transistor function

Table 6.7 The change of a Serial bank

MODE	U1	U2	L1	L2
CHARGE	ON	OFF	OFF	ON
SLOW	OFF	OFF	ON	ON
FAST	OFF	ON	ON	OFF

Note: This table shows an example of when the current flows as indicated by the arrows in the figures shown above.
If the current flows in the opposite direction, refer to the following table.

MODE	U1	U2	L1	L2
CHARGE	OFF	ON	ON	OFF
SLOW	OFF	OFF	ON	ON
FAST	ON	OFF	OFF	ON

This IC controls the motor current to be constant by 3 modes listed above.

Note: The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

6.11. Calculation of the Predefined Output Current

For PWM constant-current control, this IC uses a clock generated by the OSCM oscillator.
The peak output current (Setting current value) can be set via the current-sensing resistor (RS) and the reference voltage (Vref), as follows:

$$Iout(Max) = Vref(gain) \times \frac{Vref(V)}{R_{RS}(\Omega)}$$

Vref(gain) : the Vref decay rate is 1/ 5.0 (Typ.)

For example : In the case of a 100 % setup
when Vref = 3.0 V, Torque=100 %,RS=0.51 Ω, the motor constant current (Setting current value) will be calculated as:

Iout = 3.0 V / 5.0 / 0.51 Ω= 1.18 A

6.12. Calculation of the OSCM oscillation frequency (chopper reference frequency)

An approximation of the OSCM oscillation frequency (fOSCM) and chopper frequency (fchop) can be calculated by the following expressions.

fOSCM=1/[0.56x{Cx(R1+500)}]
C,R1: External components for OSCM (C=270 pF , R1=5.1 kΩ => About fOSCM= 1.12 MHz(Typ.))

fchop = fOSCM / 16
fOSCM=1.12 MHz => fchop =About 70 kHz

If chopping frequency is raised, Rippl of current will become small and wave-like reproducibility will improve. However, the gate loss inside IC goes up and generation of heat becomes large.

By lowering chopping frequency, reduction in generation of heat is expectable. However, Rippl of current may become large. It is a standard about about 70 kHz. A setup in the range of 50 to 100 kHz is recommended.

7. Absolute Maximum Ratings

Table 7.1 Absolute Maximum Ratings (Ta = 25 °C)

Characteristics			Symbol	Rating	Unit	Remarks
Motor power supply			VM	50	V	-
Motor output voltage			Vout	50	V	-
Motor output current			Iout	4.0	A	(Note 1)
Internal Logic power supply			VCC	6.0	V	When externally applied.
Logic input voltage			VIN(H)	6.0	V	-
			VIN(L)	-0.4	V	-
SO output voltage			VSO	6.0	V	-
LO output voltage			VLO	6.0	V	-
SO Inflow current			ISO	30	mA	-
LO Inflow current			ILO	30	mA	-
Power dissipation	WQFN48	Device alone	PD	1.3	W	(Note2)
		When mounted on a PCB		4.1	W	(Note3)
	HTSSOP48	Device alone	PD	1.3	W	(Note3)
		When mounted on a PCB		4.1	W	(Note3)
Operating temperature			TOPR	-20 to 85	°C	-
Storage temperature			TSTR	-55 to 150	°C	-
Junction temperature			Tj(Max)	150	°C	-

Note 1: Usually, the maximum current value at the time should use 70 %(Iout≦2.8 A) or less of the absolute maximum ratings for a standard on thermal rating. The maximum output current may be further limited in view of thermal considerations, depending on ambient temperature and board conditions.

Note 2: Device alone. (Ta =25 °C)
If the ambient temperature is above 25 °C, the power dissipation must be de-rated by 10.4 mW/°C.

Note 3: When mounted on a specially designed PCB (4-layer, Board thermal resistance at mounting=25 °C/W, Ta =25 °C)
If the ambient temperature is above 25 °C, the power dissipation must be de-rated by 32.8 mW/°C.

.

Ta: Ambient temperature
Topr: Ambient temperature while the IC is active
Tj: Junction temperature while the IC is active. The maximum junction temperature is limited by the thermal shutdown (TSD) circuitry. It is advisable to keep the maximum current below a certain level so that the maximum junction temperature, Tj (MAX), will not exceed 120 °C.

Caution: Absolute maximum ratings

The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating (s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion.
The value of even one parameter of the absolute maximum ratings should not be exceeded under any circumstances. This product does not have overvoltage detection circuit. Therefore, the device is damaged if a voltage exceeding its rated maximum is applied.
All voltage ratings, including supply voltages, must always be followed. The other notes and considerations described later should also be referred to.

(For reference) PD-Ta graph

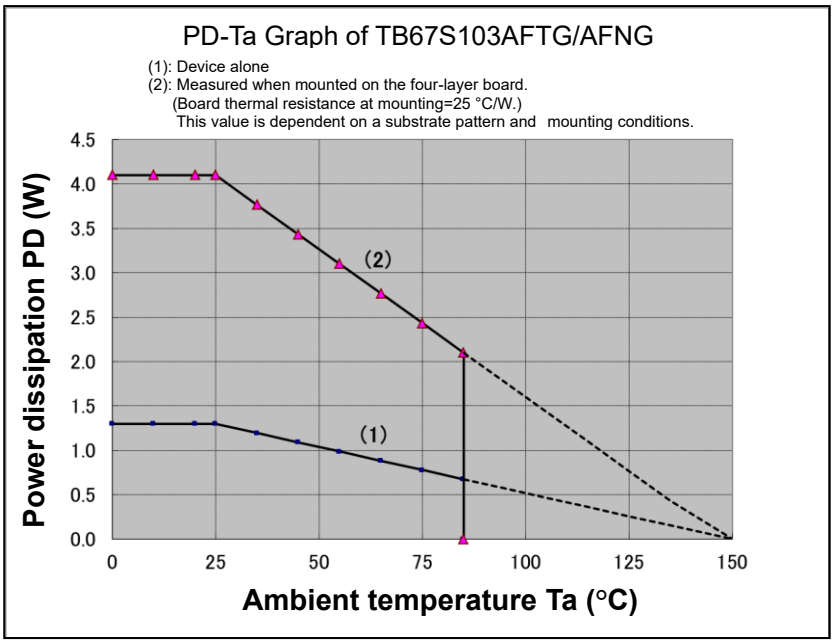


Figure7 (For reference) PD-Ta graph

8. Operating Ranges

Table 8.1 Operating Ranges (Ta=-20 to 85 °C)

Characteristics	Symbol	Min	Typ.	Max	Unit	Remarks
Motor power supply	VM	10	24	47	V	-
Motor output current	Iout	-	1.5	3.0	A	(Note 1)
Logic input voltage	VIN(H)	2.0	-	5.5	V	Logic input High Level
	VIN(L)	0	-	0.8	V	Logic input Low Level
SO output pin voltage	VSO	-	3.3	5.0	V	-
LO output pin voltage	VLO	-	3.3	5.0	V	-
Clock input frequency	fCLK	-	-	100	kHz	-
Chopper frequency	fchop(range)	40	70	150	kHz	-
Vref input voltage	Vref	GND	2.0	3.6	V	-

Note 1: Maximum current for actual usage may be limited by the operating circumstances such as operating conditions (exciting mode, operating time, and so on), ambient temperature, and heat conditions (board condition and so on).

9. Electrical Characteristics

9.1. Electrical Specifications 1 (Ta = 25 °C, VM = 24 V, unless specified otherwise)

Table.9.1 Electrical Characteristics 1

Characteristics		Symbol	Test condition	Min	Typ.	Max	Unit
Logic input voltage	HIGH	VIN(H)	Logic input (Note)	2.0	-	5.5	V
	LOW	VIN(L)	Logic input (Note)	0	-	0.8	V
Logic input hysteresis voltage		VIN(HYS)	Logic input (Note)	100	-	300	mV
Logic input current	HIGH	IIN(H)	Logic input of measurement=3.3 V	-	33	-	µA
	LOW	IIN(L)	Logic input of measurement=0V	-	-	1	µA
SO output pin voltage	LOW	VOL(SO)	IOL=24 mA output=Low	-	0.2	0.5	V
LO output pin voltage	LOW	VOL(LO)	IOL=24 mA output=Low	-	0.2	0.5	V
Power consumption		IM1	Output pins=open Standby mode	-	2	3.5	mA
		IM2	Output pins=open Standby release ENABLE=Low	-	3.5	5.5	mA
		IM3	Output pins=open Full step resolution	-	5.5	7	mA
Output leakage current	High-side	IOH	VRS=VM=50 V,Vout=0V	-	-	1	µA
	Low-side	IOL	VRS=VM=Vout=50 V	1	-	-	µA
Motor current channel differential		ΔIout1	Current differential between Ch	-5	0	5	%
Motor current setting accuracy		ΔIout2	Iout=1.5 A	-5	0	5	%
RS pin current		IRS	VRS=VM=24 V	0	-	10	µA
Motor output ON-resistance (High-side+Low-side)		Ron(H+L)	Tj=25 °C, Forward direction (High-side+Low-side)	—	0.49	0.6	Ω

Note: VIN (H) is defined as the VIN voltage that causes the outputs (OUTA+/-,OUTB+/-) to change when a pin under test is gradually raised from 0 V. V IN (L) is defined as the V IN voltage that causes the outputs (OUTA+/-, OUTB+/-) to change when the pin is then gradually lowered. The difference between V IN (H) and V IN (L) is defined as the V IN (HYS).

Note: When the logic signal is applied to the device whilst the VM power supply is not asserted; the device is designed not to function, but for safe usage, please apply the logic signal after the VM power supply is asserted and the VM voltage reaches the proper operating range.

9.2. Electrical Specifications 2 (Ta =25 °C, VM = 24 V, unless specified otherwise)

Table.9.2 Electrical Characteristics 2

Characteristics	Symbol	Test condition	Min	Typ.	Max	Unit
Vref input current	Iref	Vref=2.0 V	-	0	1	μA
VCC voltage	VCC	ICC=5.0 mA	4.75	5.0	5.25	V
VCC current	ICC	VCC=5.0 V	-	2.5	5	mA
Vref gain rate	Vref(gain)	Vref=2.0 V	1/5.2	1/5.0	1/4.8	—
Thermal shutdown(TSD) threshold (Note1)	T_jTSD	—	145	160	175	°C
VM recovery voltage	VMR	—	7.0	8.0	9.0	V
Over-current detection (ISD) threshold (Note2)	ISD	—	4.1	4.9	5.7	A

Note1: About TSD
When the junction temperature of the device reached the TSD threshold, the TSD circuit is triggered; the internal reset circuit then turns off the output transistors. Noise rejection blanking time is built-in to avoid misdetection. Once the TSD circuit is triggered, the device will be set to standby mode, and can be cleared by reasserting the VM power source, or reinput of serial data after a STANDBY (BANK0 <D2:D0>= [0, 0, 0]) setup. The TSD circuit is a backup function to detect a thermal error, therefore is not recommended to be used aggressively.

Note2: About ISD
When the output current reaches the threshold, the ISD circuit is triggered; the internal reset circuit then turns off the output transistors. Once the ISD circuit is triggered, the device keeps the output off until power-on reset (POR), is reasserted or reinput of serial data after a STANDBY (BANK0 <D2:D0>= [0, 0, 0]) setup. For fail-safe, please insert a fuse to avoid secondary trouble.

Back-EMF

While a motor is rotating, there is a timing at which power is fed back to the power supply. At that timing, the motor current recirculates back to the power supply due to the effect of the motor back-EMF.
If the power supply does not have enough sink capability, the power supply and output pins of the device might rise above the rated voltages. The magnitude of the motor back-EMF varies with usage conditions and motor characteristics. It must be fully verified that there is no risk that the IC or other components will be damaged or fail due to the motor back-EMF.

Cautions on Overcurrent Shutdown (ISD) and Thermal Shutdown (TSD)

The ISD and TSD circuits are only intended to provide temporary protection against irregular conditions such as an output short-circuit; they do not necessarily guarantee the complete IC safety.
If the device is used beyond the specified operating ranges, these circuits may not operate properly: then the device may be damaged due to an output short-circuit.
The ISD circuit is only intended to provide a temporary protection against an output short-circuit. If such a condition persists for a long time, the device may be damaged due to overstress. Overcurrent conditions must be removed immediately by external hardware.

IC Mounting

Do not insert devices incorrectly or in the wrong orientation. Otherwise, it may cause breakdown, damage and/or deterioration of the device.

9.3. AC Electrical Specification (Ta = 25°C, VM = 24 V, 6.8 mH/5.7 Ω)

Table.9.3 AC Electrical Characteristics

Characteristics	Symbol	Test condition	Min	Typ.	Max	Unit
Inside filter of CLK input minimum High width	tCLK(H)	The CLK(H) minimum pulse width	300	-	-	ns
Inside filter of CLK input minimum Low width	tCLK(L)	The CLK(L) minimum pulse width	250	-	-	ns
Output transistor switching specific	tr	-	30	80	130	ns
	tf	-	40	90	140	ns
	tpLH(CLK)	CLK-Output	-	1000	-	ns
	tpHL(CLK)	CLK-Output	-	1500	-	ns
Analog noise blanking time	AtBLK	VM=24V,Iout=1.5A Analog tblank	250	400	550	ns
Oscillator frequency accuracy	ΔfOSCM	COSC=270 pF, ROSC=5.1 kΩ	-15	-	+15	%
Oscillator reference frequency	fOSCM	COSC= 270 pF, ROSC =5.1 kΩ	952	1120	1288	kHz
Chopping frequency	fchop	Output:Active(Iout =1.5 A), fOSC = 1120 kHz	-	70	-	kHz

AC Electrical Specification Timing chart

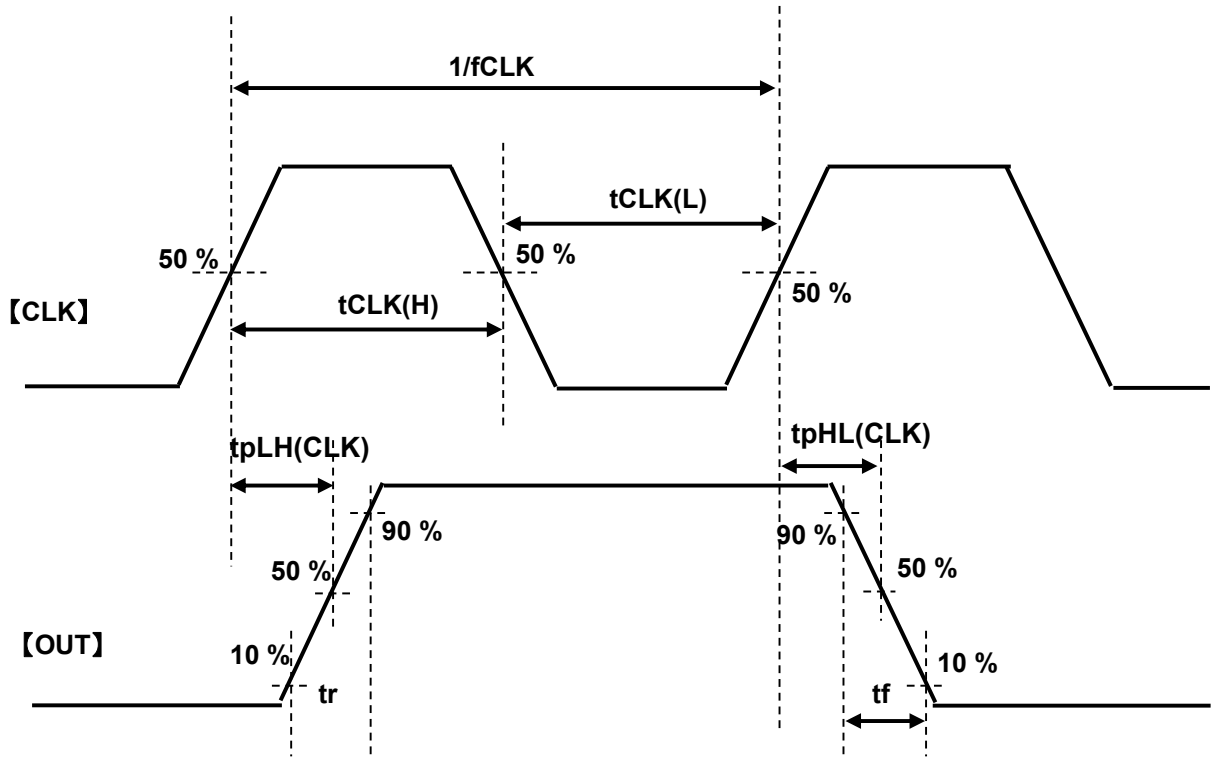


Figure 9.1 AC Electrical Specification Timing chart

Note: Timing charts may be simplified for explanatory purpose.

Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass-production design stage.
Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.

5. Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

10. IC Usage Considerations

10.1. Notes on handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.Exceeding the rating(s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in the case of overcurrent and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead to smoke or ignition. To minimize the effects of the flow of a large current in the case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

(3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition. Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

(4) Do not insert devices in the wrong orientation or incorrectly. Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion.
In addition, do not use any device inserted in the wrong orientation or incorrectly to which current is applied even just once.

(5) Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator.
If there is a large amount of leakage current such as from input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure may cause smoke or ignition. (The overcurrent may cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection-type IC that inputs output DC voltage to a speaker directly.

10.2. Points to remember on handling of ICs

Overcurrent detection Circuit

Overcurrent detection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the overcurrent detection circuits operate against the overcurrent, clear the overcurrent status immediately.

Depending on the method of use and usage conditions, exceeding absolute maximum ratings may cause the overcurrent detection circuit to operate improperly or IC breakdown may occur before operation. In addition, depending on the method of use and usage conditions, if overcurrent continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

Thermal Shutdown Circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over-temperature, clear the heat generation status immediately.

Depending on the method of use and usage conditions, exceeding absolute maximum ratings may cause the thermal shutdown circuit to operate improperly or IC breakdown to occur before operation.

Heat Radiation Design

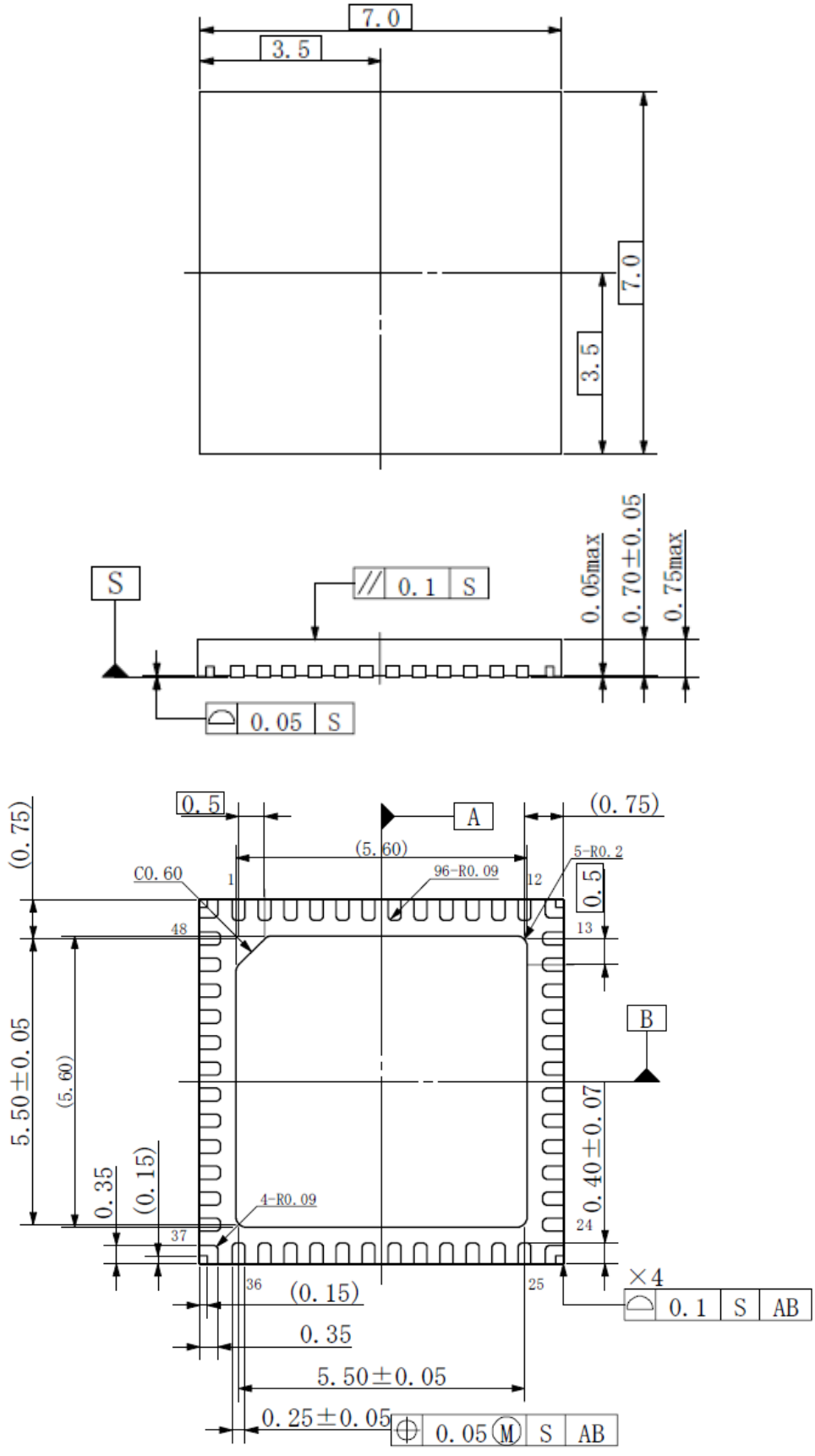
When using an IC with large current flow such as power amp, regulator or driver, design the device so that heat is appropriately radiated, in order not to exceed the specified junction temperature (TJ) at any time or under any condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, when designing the device, take into consideration the effect of IC heat radiation with peripheral components.

Back-EMF

When a motor rotates in the reverse direction, stops or slows abruptly, current flows back to the motor's power supply owing to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond the absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

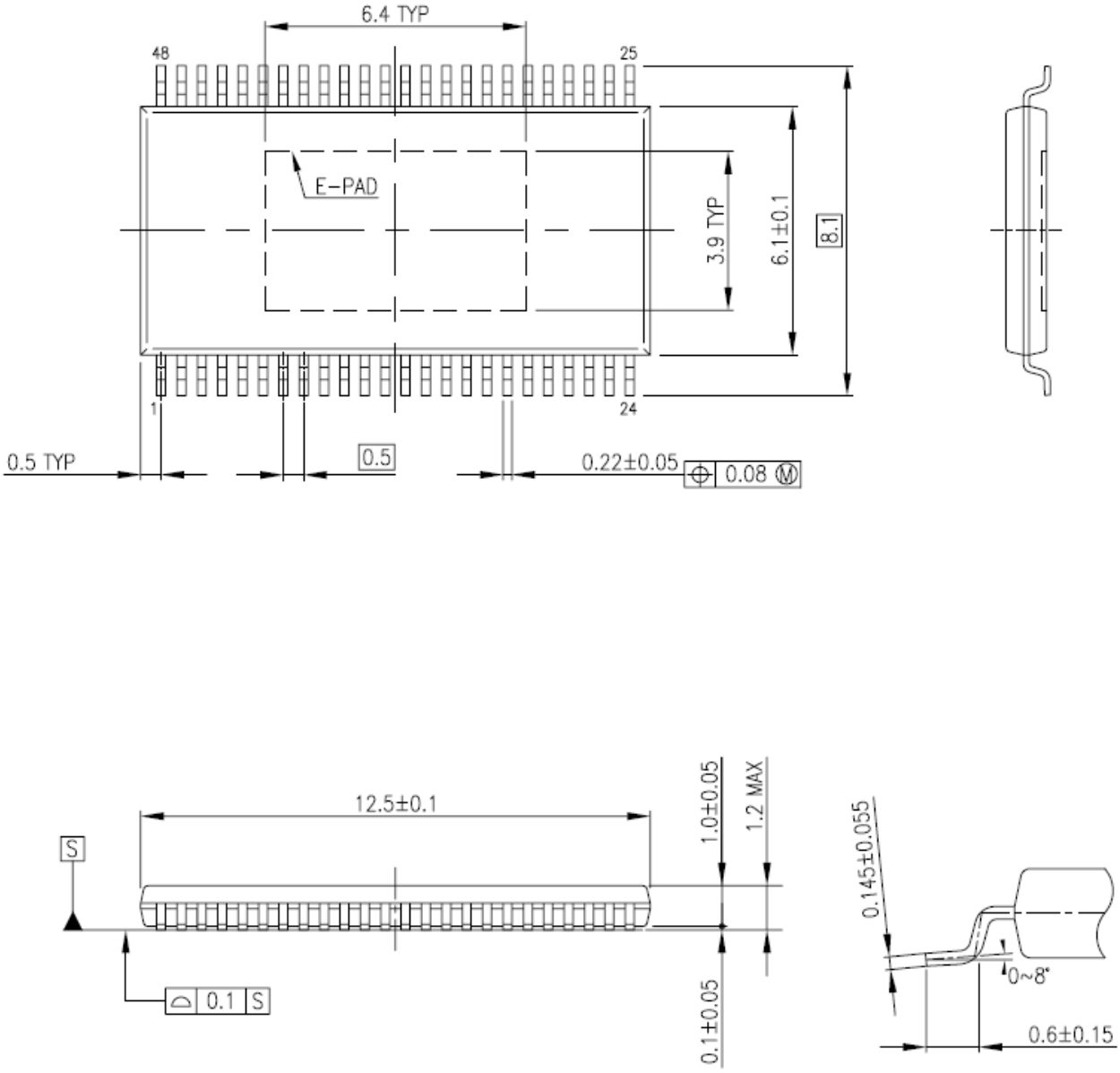
11. Package Information (unit :mm)

11.1. P-WQFN48-0707-0.50-003



weight 0.10 g（Typ.）

11.2. HTSSOP48-P-300-0.50



weight 0.21 g（Typ.）

RESTRICTIONS ON PRODUCT USE

Toshiba Corporation and its subsidiaries and affiliates are collectively referred to as “TOSHIBA”.
Hardware, software and systems described in this document are collectively referred to as “Product”.

- TOSHIBA reserves the right to make changes to the information in this document and related Product without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, lifesaving and/or life supporting medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, and devices related to power plant. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative or contact us via our website.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**