TC32168FTG

RF Transceiver for ETC

Ver. 1

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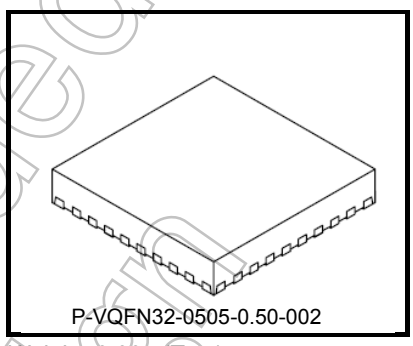
TOSHIBA CMOS Integrated Circuit Silicon Monolithic

TC32168FTG

5.8 GHz RF Transceiver for ETC including Modem/Wakeup

1. Abstract

TC32168FTG is a single-chip 5.8-GHz RF transceiver for ETC (Electronic Toll Collection) system. It is mainly used for OBU (On Board Unit) of automotive systems. Wakeup detector, Crystal oscillator, Mixer, IF amplifier, IF filter, RSSI (Received Signal Strength Indicator), ASK/OOK modulator/demodulator, Transmission band limiting filter, and PA are included in this IC.
Less than 5 μA of the current consumption has been achieved in Sleep mode (only WAKEUP block is active). Also this IC supports a fast boot sequence for MLFF (Multi-Lane Free Flow) and a dual band reception waiting (a data reception at both 5830 MHz and 5840 MHz).



Weight: 0.08g (Typ.)

2. Application

This IC can be used for ETC systems whose bit rate is 256 kbps or 512 kbps.

3. Features

- Low current consumption
- Fast boot sequence (Refer to Electrical Characteristics for details.)
- Small package: P-VQFN32-0505-0.50-002, 5.0 mm × 5.0 mm square
- Including Wakeup function
- Including Modem functions (Addition of CRC, Postamble, or Preamble is available.)
  - Modem mode: Data transmission through the internal modem
  - Direct mode: Data transmission or reception through INTRPT/DIO pin is available.
- MLFF (Multi-Lane Free Flow) is supported.
  - Boot control from MCU through CE pin
  - Auto-wakeup function using an auto-boot sequence is selectable.
- Including IF filter
  - High selection performance for a reception signal using the internal IF filter
- IC control from dedicated pins
  - Fast boot sequence from Sleep mode using CE pin
  - Fast switching between TX (Transmission) and RX (Reception) using TXRX pin
    - Switching between TX and RX can be also done by using SPI (Serial Peripheral Interface) bus
- IC control from SPI bus
  - Wakeup detection settings
    - Setting of a cycle number of the output pulses
    - Wakeup routine setting
  - Internal frequency settings (PLL frequency synchronizer); PLL = Phase Locked Loop
    - Transmission frequency setting
    - Reception frequency setting
  - Modem function setting
    - Switching between Modem mode and Direct mode

4. Block Diagram

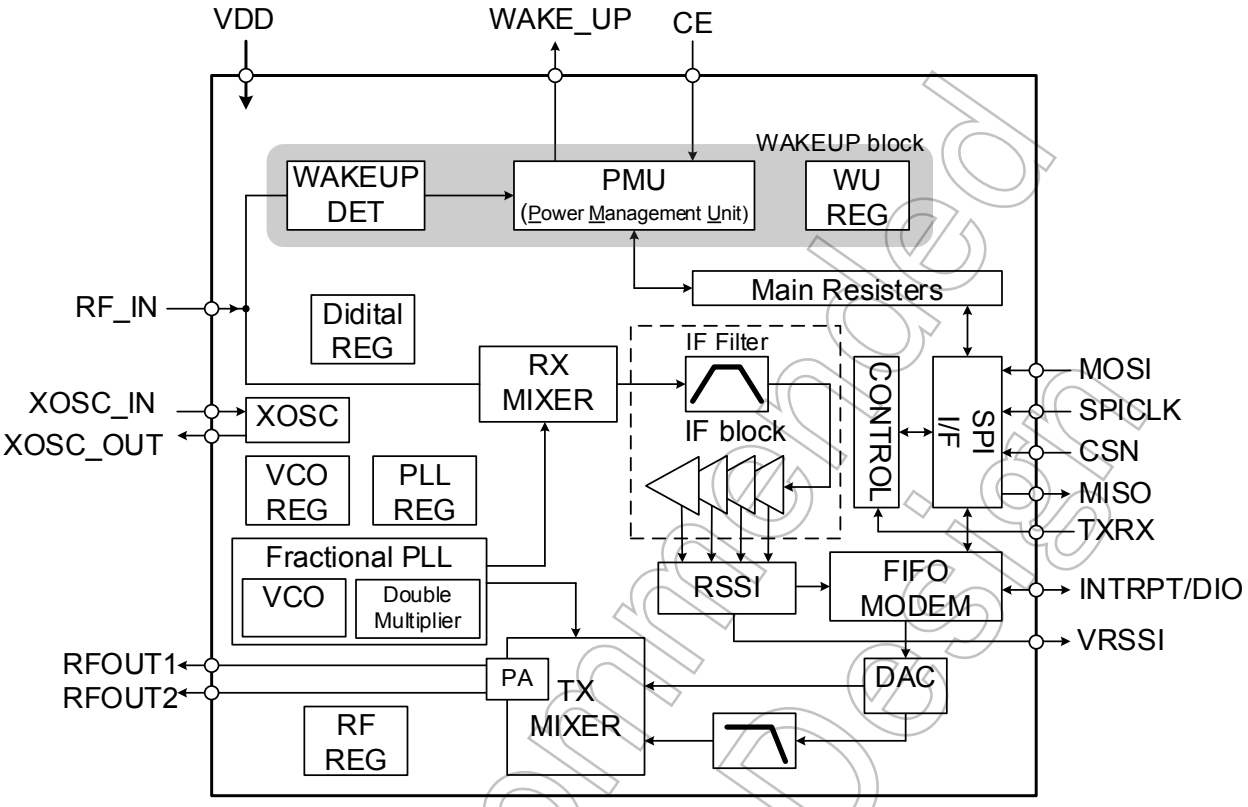


Figure 4-1 Block Diagram

Above figure is a schematic of this product. Some of the functional blocks and others in the block diagram may be omitted or simplified for explanatory purposes.
In this figure, only the circuits in the gray shaded block operate in Sleep mode.

5. Pin Assignment

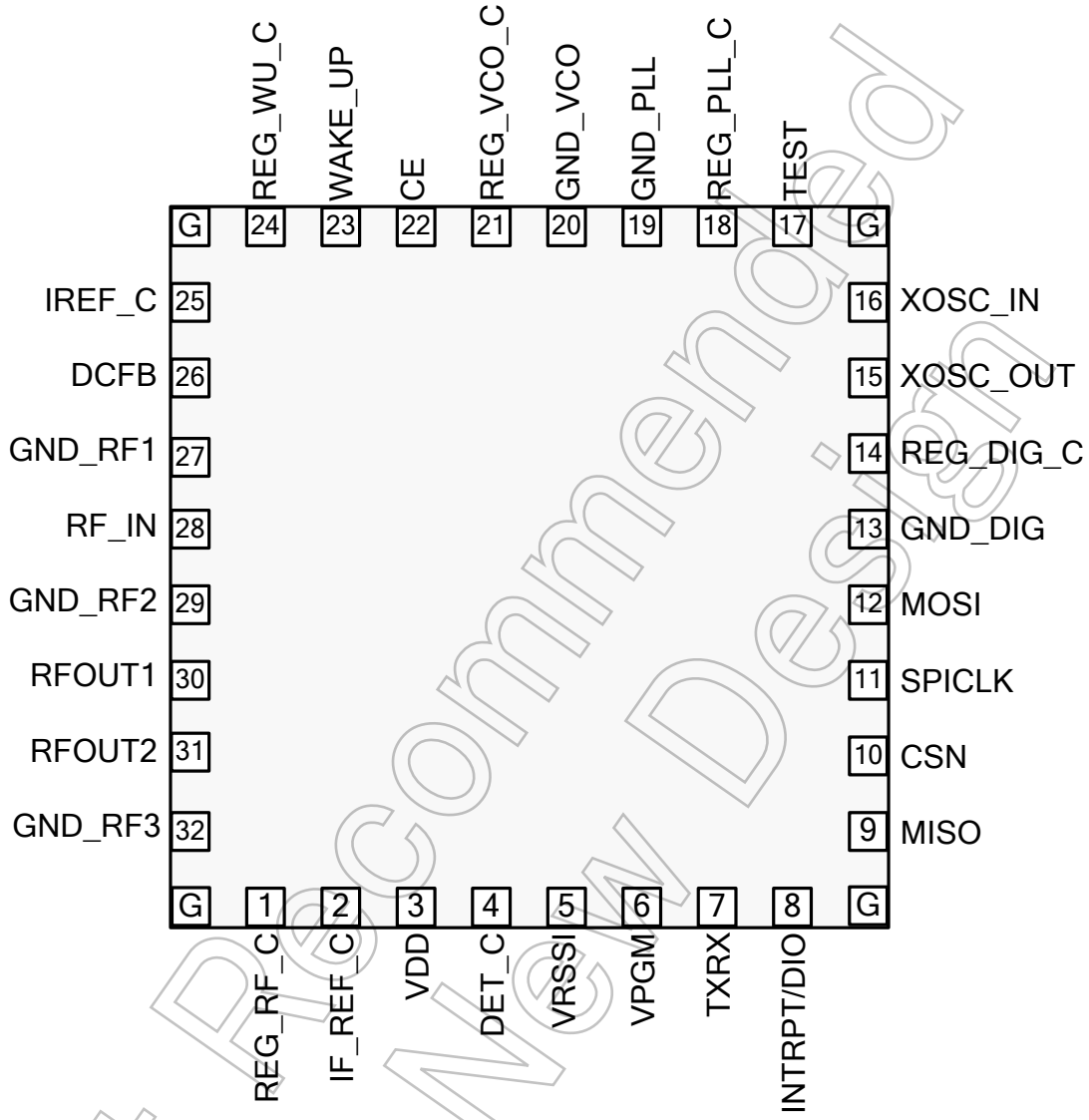


Figure 5-1 Pin Assignment (Top View)

Note: The G pins at the four corners of this IC package are internally connected to the substrate of this IC. It is recommended that those pins are connected to the ground on the printed-circuit board.

6. Pin Description

Table 6-1 Pin Description

Pin No.	Name	I/O	Description
1	REG_RF_C	—	Connect a bypass capacitor for internal regulator stabilization.
2	IF_REF_C	—	Connect a capacitor for IF filter circuit stabilization.
3	VDD	Power Supply	Supply voltage input pin. 3.0 V (Typ.). Connect a bypass capacitor.
4	DET_C	—	Connect a capacitor for ASK/OOK detector.
5	VRSSI	O	RSSI output.
6	VPGM	—	Connect to the ground directly (only for the test in Toshiba).
7	TXRX	I	Select Transmission or Reception. "1": Transmission/"0": Reception
8	INTRPT/DIO	I/O	Select the pin function by SPI control. Use for an interrupt: Set Modem mode by SPI. Use for Data I/O: Set Direct mode by SPI.
9	MISO	O	Master input/Slave output of SPI (Master In Slave Out).
10	CSN	I	Enable of SPI communication. "0": Communication enable. "1": Communication stop.
11	SPICLK	I	Clock of SPI. Input SPI clock for communication.
12	MOSI	I	Master output/Slave input of SPI (Master Out Slave In).
13	GND_DIG	—	Ground for digital blocks. Connect to GND.
14	REG_DIG_C	—	Connect a bypass capacitor for internal regulator stabilization.
15	XOSC_OUT	O	Connect a crystal oscillator. (When TCXO is used, this pin should be open.)
16	XOSC_IN	I	Connect a crystal oscillator. (When TCXO is used, connect it to this pin via a capacitor.)
17	TEST	—	Connect to the ground directly (only for the test in Toshiba).
18	REG_PLL_C	—	Connect a bypass capacitor for internal regulator stabilization.
19	GND_PLL	—	Ground for PLL. Connect to GND.
20	GND_VCO	—	Ground for VCO. Connect to GND.
21	REG_VCO_C	—	Connect a bypass capacitor for internal regulator stabilization.
22	CE	I	"1" setting means Transmission/Reception is enabled. After the power is supplied, this pin should be set to "0". And then set to "1". (Refer to 7.11.2.)
23	WAKE_UP	O	When 14-kHz Wakeup signal is detected, this pin outputs "1." Also when the Wakeup function is re-set up, this pin outputs "1."
24	REG_WU_C	—	Connect a bypass capacitor for internal regulator stabilization.
25	IREF_C	—	Connect an external capacitor for Wakeup detection. Note; The characteristics of this pin is affected by the value of the connected capacitor. Use a ceramic capacitor, and pay attention to condensation or dust to avoid the leak current.
26	DCFB	—	Connect an external capacitor for Wakeup detection. Note; The characteristics of this pin is affected by the value of the connected capacitor. Use a ceramic capacitor, and pay attention to condensation or dust to avoid the leak current.
27	GND_RF1	—	Ground for RF blocks. Connect to GND.
28	RF_IN	I	RF signal input. The input impedance is 50-Ω (Typ.).
29	GND_RF2	—	Ground for RF blocks. Connect to GND.
30	RFOUT1	O	RF signal output 1. Connect to a 50-Ω impedance signal line.
31	RFOUT2	O	RF signal output 2. Connect to a 50-Ω impedance signal line.
32	GND_RF3	—	Ground for RF blocks. Connect to GND.

Note: In the table above, "1" means the supply voltage level and "0," the ground level.

7. Functional Description

7.1 Power Supply

The power supply voltage of this product is in the range of 1.8 V to 3.6 V.
VDD pin should be connected to not only the power supply but also a bypass capacitor to reduce noises.
In this product, internal regulators deliver the voltage sources.
In Figure 4-1, “REG” boxes represent the regulators.
Circuits to control Wakeup operation (PMU, WAKEUP DET and WU REG in Figure 4-1) are always “ON” while the power is supplied.
The other circuits are controlled by the power supply voltage from the internal regulators.

7.2 RF Frequency

This product has a fractional PLL.
The internal oscillator consists of the fractional PLL, VCO, and the crystal oscillator circuit for PLL reference signal.
The oscillation frequency can be set to the value in the range of 5725 MHz to 5875 MHz via SPI bus.

(1) Reception frequency setting
The difference between the reception frequency and the LOCAL frequency should be set to +/-5 MHz.
Either Upper LOCAL or Lower LOCAL can be selected according to the application system or the radio surroundings.
The frequency calculation is shown as follows:

$f_{OPR}RX = f_{LO}$ +/-5 (MHz)
NRX[D20,D0] = f_{LO} (MHz) × 125
= NRX[D20] × 2^{20} + NRX[19] × 2^{19} + ・・・・ + NRX[D2] × 2^2 + NRX[D1] × 2^1 + NRX[D0] × 2^0
f_{OPR}.RX is the reception frequency. f_{LO} is the LOCAL frequency which is set by the register NRX[D20,D0] (= 04h[D15,D0] and 05h[D4,D0]).
The sign “+/-” depends on the selection of the Upper LOCAL or Lower LOCAL frequency.

The initial value of the reception LOCAL frequency is 5835 MHz.
If the reception local frequency is not set to the register, the PLL is locked to 5835 MHz and this IC can receive both Ch1 (5830 MHz) and Ch2 (5840 MHz) after CE pin becomes “1”.

The register setting is necessary to receive another frequency signal.
After a target frequency is set in NRX register, the register pll_reset (= 08h[D0]) should be set to “1” (refer to 8.9). Then the PLL locks at the frequency.
After that, it is not necessary to write "0" to the register pll_reset (= 08h[D0]).

(2) Transmission frequency setting
For a transmission frequency, a target frequency should be directly set.

$f_{OPR}TX = f_{LO}$ (MHz)
NTX[D20,D0] = f_{LO} (MHz) × 125
= NTX[D20] × 2^{20} + NTX[D19] × 2^{19} + ・・・・ + NTX[D2] × 2^2 + NTX[D1] × 2^1 + NTX[D0] × 2^0
f_{OPR}.TX is the transmission frequency. f_{LO} is the internal frequency which is set by the register NTX[D20,D0] (= 06h[D15,D0] and 07h[D4,D0]).

The initial value of the transmission frequency is 5790 MHz.
When the data reception changes to the data transmission, the PLL is locked to the transmission frequency.
In order to change the transmission frequency, the register pll_reset should be set to “1”, after a target frequency is set to the register NTX.
After that, it is not necessary to write "0" to the register pll_reset (= 08h[D0]).

7.3 System Clock generation

This product contains a crystal oscillator circuit. 32.768-MHz crystal oscillator should be used.
Heavy load capacity of the crystal oscillator may be the cause of slower oscillation starting. So, the crystal oscillator should be selected after enough evaluation on the system.
This datasheet shows the data values measured by using an evaluation board contained the crystal oscillator which is recommended by Toshiba.

7.4 Wakeup Operation

PMU and WAKEUP DET blocks are used for Wakeup operation.
PMU and WAKEUP DET are always “ON”.
PMU controls the operation of this product.
WAKEUP DET can detect a 14-kHz waveform in the 5.8-GHz frequency band.
PMU and WAKEUP DET operate with the clock which is generated by an internal oscillator. So, no special oscillators for them are necessary.

7.5 RF Demodulation

A received signal is demodulated.
In Modem mode, the signal is decoded by the FIFO modem and stored in a register. The data can be output from SPI bus.
In Direct mode, the demodulated signal is output asynchronously from INTRPT/DIO pin.
For the details of these Modem modes, refer to 7.7.
RSSI outputs a voltage level corresponding to the dB level of the input signal.

7.6 RF Modulation

This product modulates the amplitude of the input signal and outputs the modulated signal from RFOUT 1 and RFOUT 2 pins as a high-frequency signal.
In Modem mode, when data is input from SPI bus, the data can be coded by the FIFO modem.
In Direct mode, when data is input from INTRPT/DIO pin, the data can be modulated.
The data coding cannot be done in Direct mode. A transmission data should be input as it is.

For details of these Modem modes, refer to 7.7.
The detail settings for the ASK modulation waveform in this IC is set to a register via SPI bus.

7.7 MODEM

This product has two Modem modes as follows. The Modem modes can be selected by the registers dio_sel and dio_en (refer to 8.4). In Figure 4-1, the Modem is shown as FIFOMODEM.

(1) Modem Mode

In this mode an internal Modem of this IC is used. Full functions of this IC can be used and no external modem devices are necessary. In this mode, data input and output are done via SPI bus. INTRPT/DIO pin is used for an interrupt.

(2) Direct Mode

When the internal modem functions in this IC are not necessary, Direct mode should be set.
An external modem device should be prepared.
In this mode, INTRPT/DIO pin is used for data input and output.

The modem in this IC has following functions.
Reception:

(1) Bit synchronization by a preamble
(2) FM0 decoding
(3) Frame detection by a frame start mark
(4) Abort detection
(5) ZERO detection
(6) Generation of the frame length of the second layer in the information frame by a frame end mark
(7) Error detection by CRC16
(8) Clock recovery
(9) Determination of a non-standard bit length of a reception signal

Transmission:

(1) ZERO insertion
(2) Addition of a frame start and a frame end marks
(3) Addition of a preamble and a postamble
(4) FM0 encoding
(5) Frame check (CRC16)

7.8 System Control and Data Communication

The functions of this product are controlled by the combination of SPI bus and specified pin signals.
The function of the chip enable is controlled by CE pin.
If CE pin stays in “0,” the control via SPI bus is disabled.
The settings via SPI bus should be done after the CE pin is set to “1.”
The switching between the transmission and the reception is done by either the setting of TXRX pin or the register setting via SPI bus.

7.9 State Transition Diagram

This product has mainly three states, Sleep, Reception (RX), and Transmission (TX).

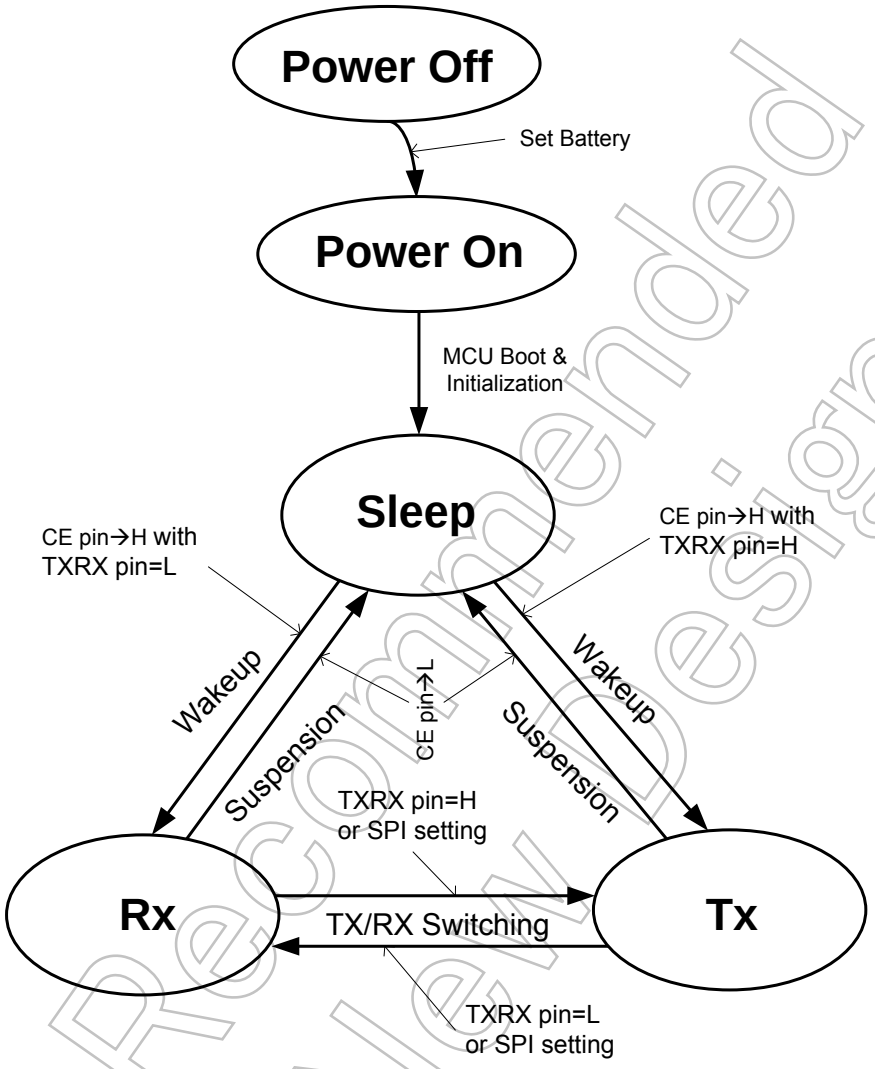


Figure 7-1 State Transition Diagram of TC32168FTG

7.10 State Description

7.10.1 Power Off and Power On States

In Power Off State, the power is not supplied to the OBU of ETC.
All functions stop because no power is supplied.
In Power On State, the power is supplied to the OBU of ETC.
The power is supplied to this IC and it is initialized.

7.10.2 Power On State to Sleep State

The MCU is waiting for the boot of itself.
The boot sequence for the MCU is supposed as follows: At first MCU is reset and initialized. Then MCU's pin assignment, I/O conditions and functions are set. Finally the MCU controls this IC.
After this product is reset and initialized by the MCU, this product enters one of the states, Sleep, RX or TX.
When this product is used on an OBU, Sleep state is recommended.

Note: CE pin should be kept "0" for 600 μs or more before it is set to "1" to initialize this IC surely. For details, refer to 7.11.2.

7.10.3 Sleep State

Only the Wakeup detection blocks of this product (PMU, WAKEUP DET and WU REG) are active.
The following instructions can execute:
Wakeup sensitivity setting, the number of cycles to start up the Wakeup signal, and the selection of Normal Wakeup or Auto Wakeup.
Other blocks of this IC are not supplied with power to reduce current consumption.
The external MCU is supposed to be in an idle state (a call sleep state, a low power state, and others) and is waiting for Wakeup interrupt from this IC.
The registers of PMU and WAKEUP DET keep their data during Sleep state.

7.10.4 RX State

This product can receive ASK or OOK modulated RF signal.
It can receive FM0 encoded 512 or 256-kbps ASK or OOK modulated RF signal at 5.8-GHz frequency band.
When TXRX pin is set to "0," this IC becomes RX State.
If using the register setting, the register TXRX_en (= 01h[D1]) shouod be set to "0" or the combination is done such as the register TXRX_en should be set to "1" and the register TXRX (= 01h[D0]), "0."
After that, this IC starts detecting the frame of the physical layer.
When the frame of the physical layer is detected, the information frame without FCS (Frame Check Sequence) is stored in the register TRXFIFO (= 10h[D2047,D0]). And rx_ready interrupt is asserted to the external MCU.

Note: The stored reception data in the register TRXFIFO should be read out. After the register becomes full with the reception data, a new reception data is overwritten and the previous data disappears. To avoid this, the register dettimer_dis (= 36h[D0]) is useful. It can control the flag error timer. The timer value is 2 ms. The stored data can be read during this 2 ms.
Note: If the FIFO data has been overwritten unintentionally, the register clr_fifo (= 43h[D8]) should be set to "0" to clear the register TRXFIFO.

7.10.5 TX State

This product can transmit ASK or OOK modulated signal.
It transmits FM0 encoded 512 or 256-kbps ASK or OOK modulated RF signal at 5.8-GHz frequency band.
Maximum RF output level is +3 dBm (Typ.).
When TXRX pin is set to "1," this IC becomes TX State.
If using the register setting, the register TXRX_en (= 01h[D1]) shouod be set to "0" or the combination is done such as the register TXRX_en should be set to "1" and the register TXRX (= 01h[D0]), "1."
After a transmission data is stored in the register TRXFIFO, the data transmission can start.
After transmission completes, tx_done interrupt is asserted to MCU.

7.10.6 Transition between RX State and TX State

In order to transit between RX state and TX state, TXRX pin is used or the combination of the register TXRX and the register TXRX_en is used. The selection is done by the register (0hXX).
When TXRX pin is used, the input data should be kept at least 1.3 μs to transit between TX state and RX state. Otherwise, the initialization of the PLL may not be done correctly and malfunction occurs.
It should be considered that PLL lock-up time which is approximately 30 μs is not included in the interval.
Appropriate frequencies should be set to the registers NRX and NTX just before the transition.
Whenever the transition between TX state and RX state occurs, the register TRXFIFO is cleared automatically.

Note: The signal durations described above depend on the frequency of the crystal oscillator.

7.11 Sequence Description

The abstract of the sequences for TC32168FTG is described here to implement suitable control. For details of the sequences, refer to 7.12 Flowchart Examples.

7.11.1 Chip Select and Reset

In the following cases, the chip enable and reset operations should be considered carefully.

- Periodic refreshing to recover from a register error caused by the cosmic ray, external noises, and others.
- Occurrence of unexpected operation in the system.
- Notice of an error from the interrupt register.
- No expected data can be acquired from the FIFO after receiving RF signal. Or reception failure occurs.

Some resets, such as PLL reset, will be used in the control routine of ETC.
It is also called the reset of Wakeup functon that the output setting of WAKE_UP pin is reset and this product enters Sleep state.
The explanation of the chip enable and the reset of this IC is described in Table 7-1.

Table 7-1 Chip Enable and Reset

Item	Description	Use Condition	Control
Wakeup Reset	Reset and initialization of Wakeup function. The initialization by this reset means to calibrate Wakeup detection timer to detect a 14-kHz waveform.	Wakeup function becomes available by this reset. That is, it is available in the following cases. - before entering Sleep state to prepare the next transmission. - after a fatal trouble occurs. - after a reception failure occurs.	Mandatory. Set the register wk_clr (=1Bh[D8]) to "1" to change WAKE_UP pin output from "1" to "0." Recommended. Set the register wk_reg_wen (= 1Ch[D8]) to "1". After the reset, the data of the register wk_reg_wen automatically returns to "0" (the initial value). For initialization, set the register wkcal_en (= 1Ah[D8]) to "1" while Wakeup function's reset is asserted. Set the registers w_s_set (=0Bh[D3,D0]), wk_num (=18h[D3,D0]), and autowk (=19h[D0]). Those register data are copied to registers in PMU and WAKEUP DET by setting the register wk_reg_wen to "1". After copying the data, the register data in PMU and WAKEUP DET become valid.
Chip Enable	This IC enters Convergence state* after the power is suppled. To escape from the state, the chip enable function should be controlled with CE pin input.	This chip enable shuold be asserted at the first connection of a battery (a voltage supply), after the ETC application system implementing this IC is manufactured.	Keep CE pin to "0" for 600 μs or more after the power is supplied. Then, change CE pin from "0" to "1."
		ETC system should be reset after a fatal trouble occurs.	Keep CE pin to "0" for 20 μs or more. Then, change CE pin from "0" to "1".
Software Reset	All registers and modems are reset. The registers are initialized.	The software reset is asserted during transition from Power On state to Sleep/TX/RX state. It is also asserted at the following cases. - At the refreshing of registers. - When the MCU detects an error or an abnormal situation.	Set the register RST (= 00h[D7]) to "1." After the reset, the data of the register RST automatically returns to "0" (the initial value). The modem can also be reset by CE pin operation.
PLL Reset	PLL circuit starts up and the PLL locks on the expected frequency.	- At changing between RX state and TX state. - At changing RF frequency.	Set the register PLL_RST (= 08h[D0]) to "1." PLL reset register is a trigger to initialize PLL circuit. After that, it is not necessary to write "0."

Note: For details of Convergence state*, refer to 7.11.2.
Note: The signal durations described in this table depend on the frequency of the crystal oscillator.

7.11.2 Operation after Power Supply

The ETC application system including TC32168FTG and MCU as a controller executes a system start routine after the power is supplied. "System" means here the unit which consists of this product and MCU as a controller.
At first, the reset should be asserted properly to both this IC and MCU to initialize them.
After the power is supplied, the states of this IC and MCU are indefinite. (The reset and initialization in the start routine of MCU is called "Boot.")
The MCU should reset and initialize (boot) itself after the supply voltage reaches the operation voltage of this product.
On the other hand, the state of PMU and WAKEUP DET in this IC is undefined (Sleep state, TX state, or RX state) after the power is supplied. MCU should set CE pin of this IC to "0" for 600 μs or more to determine the state of this IC. During the 600 μs duration this product is started up. Then this IC enters indefinite state temporarily.
The indefinite state means that the logical state of PMU and WAKEUP DET is indefinite, and it continues until the reset and the initialization by register setting are done.
Before the initialization is done by the register setting, MCU should wait 400 μs or more after the CE pin reset is deasserted.
An example of the timing chart of the system start sequence is shown below.

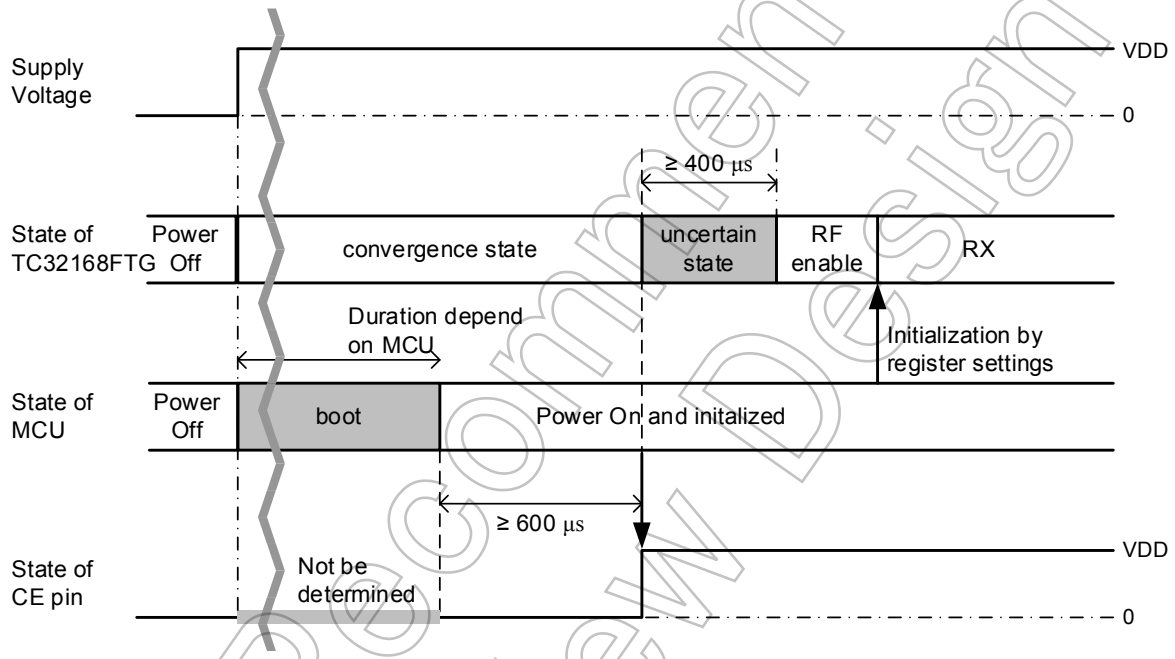


Figure 7-2 Example of a timing chart about System starting

Note: Signal durations described in this figure depend on the frequency of the crystal oscillator.
Note: Operations of this IC cannot be guaranteed without keeping time relationships between the signals expressed in the figure.

7.11.3 Wakeup Function

This product has a Wakeup function to detect a 14-kHz waveform in 5.8-GHz frequency band.
When a 14-kHz Wakeup signal is detected, WAKE_UP pin outputs "1" in Normal Wakeup mode.
After WAKE_UP pin outputs "1," this IC status should be checked via SPI bus, and then, the target settings should be done.
This IC supports Auto Wakeup function for MLFF when this product is used for ETC.
When Auto Wakeup function is selected, this IC can automatically start data reception after receiving 14-kHz Wakeup signal. And this IC can receive 5830 and 5840-MHz signal simultaneously without any external control.
When the reception completes correctly, the data is stored in FIFO register and is kept there.
If CE pin turns to "1," the reception data is discarded.
The setting which Wakeup sequence is used should be done to a register via SPI bus while CE pin is "1" as follows.
To set Normal Wakeup, the register autowk (= 19h[D0]) should be set to "0" in the initialization of PMU and WAKEUP DET.
If the register has not been written, the initial value is "0" which selects Normal Wakeup.
To set Auto Wakeup, the register autowk (= 19h[D0]) should be set to "1" in the initialization of PMU and WAKEUP DET.
Before entering Sleep state, Wakeup setting data should be transmitted (write-back) to the register for PMU and WAKEUP DET. The selected Wakeup function becomes valid.

(1) Normal Wakeup

This function is available only while CE pin is "0."
When Normal Wakeup is set, WAKE_UP pin outputs "1" when a 14-kHz Wakeup signal is detected.
The signal should be a trigger for this IC to be controlled by MCU. The system start-up time is the sum of the start-up times of this IC and MCU in Normal Wakeup operation.

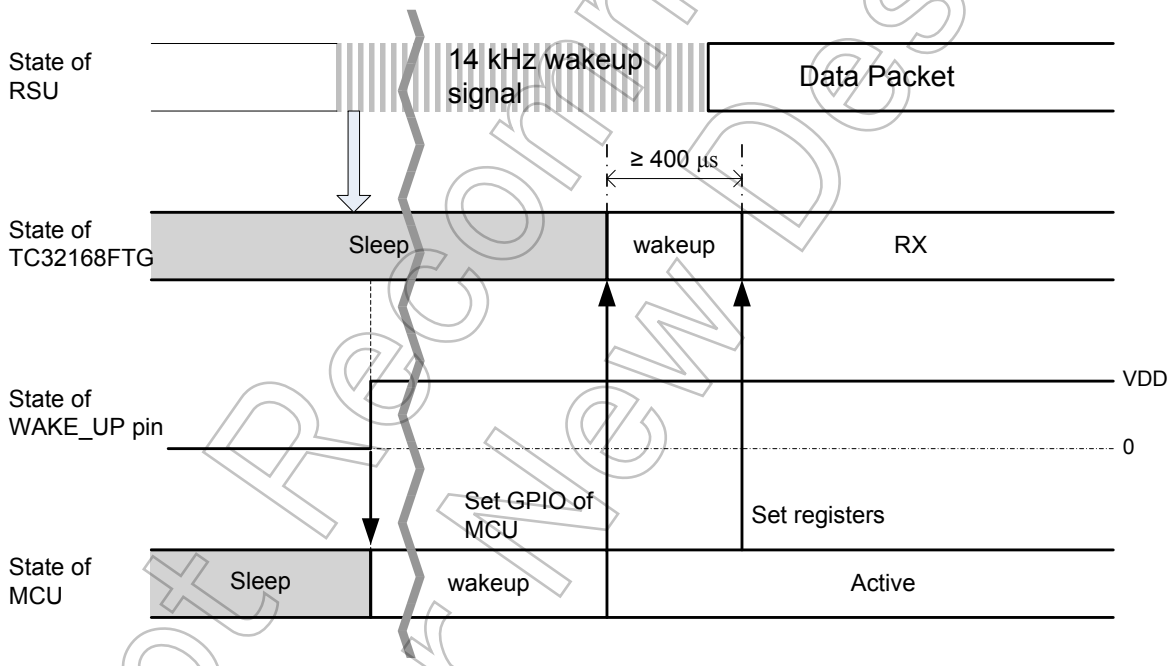


Figure 7-3 Normal Wakeup

Note: Signal durations described in this figure depend on the frequency of the crystal oscillator.

(2) Auto Wakeup

When Auto Wakeup is set, WAKE_UP pin outputs “1” when a 14-kHz Wakeup signal is detected, regardless of CE pin value.
This product becomes active and XOSC oscillation starts.
This IC will automatically return to Auto Wakeup if CE pin stays “0” for 20 μs or more after WAKE_UP pin becomes “1.”
This IC and MCU can start up in parallel in Auto Wakeup mode.
So the total time of the start-up can be shortened.
And the current consumption of the system can be reduced

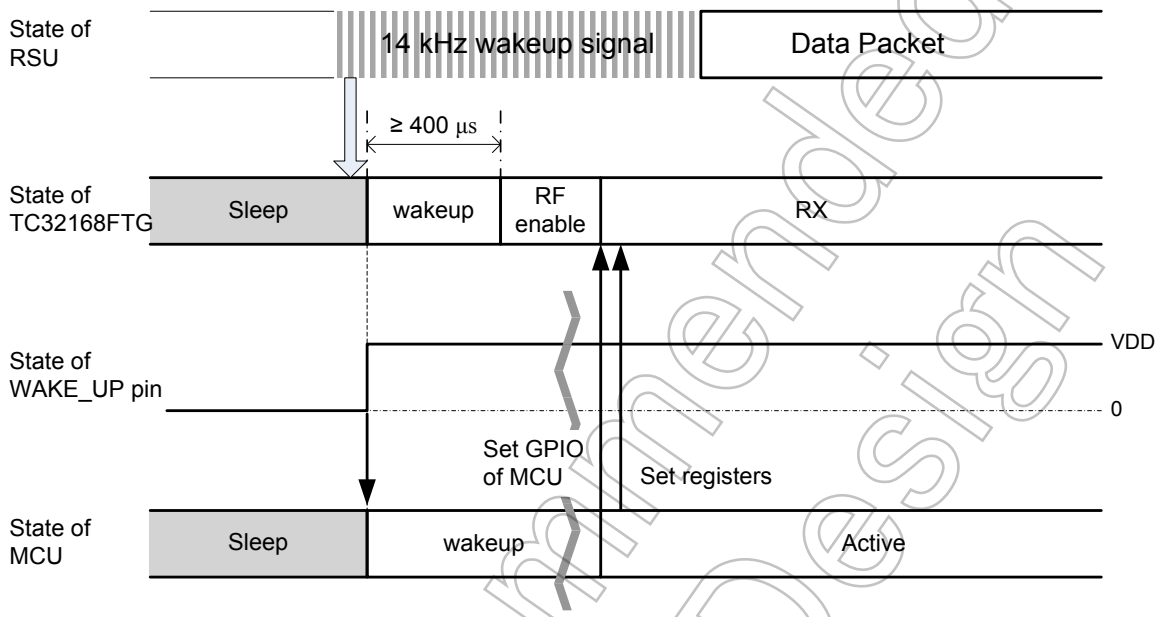


Figure 7-4 Auto Wakeup

Note: Communication between MCU and TC32168FTG should start after finishing those Wakeup durations.
Note: Signal durations described in this figure depend on the frequency of the crystal oscillator.

7.11.4 Suspension

When CE pin turns to “0,” this IC enters Sleep state regardless of the register settings.
Before entering Sleep state or when staying in TX state or RX state, Wakeup function which is used in Sleep state should be set, then CE pin should be changed to “0.”
This is called “write-back to Wakeup register.” If this write-back is omitted, the Wakeup function may not operate correctly at the next Wakeup signal input.
The timing chart of Suspension is shown in Figure 7-5.
Before MCU enters Sleep state, it should set the register wk_clr (= 1Bh[D8]) to “1.”
Then, WAKE_UP pin outputs “0” for 40 μs or more.
After that, CE pin should be set to “0.”

Following reset and initialization of Wakeup function should be done during TX/RX state.

- Set the register wk_reg_wen (= 1Ch[D8]) to "1."
- Set the register wkcal_en (= 1Ah[D8]) to "1."
- Set the register w_s_set (= 0Bh[D3,D0]) to the expected value for the application system.
- Set the register wk_num (= 18h[D3,D0]) to the expected value for the application system.
- Set the register autowk (= 19h[D0]) to the expected value according to the type of Wakeup (Normal/Auto).

In addition, the reset and initialization of Wakeup function is useful at the occurrence of a reception failure. For the reset and initialization, also refer to Table 7-1.

Note: If CE pin is set to “0” before WAKE_UP pin turns to “0”, WAKE_UP pin output keeps “1” during Sleep state.
As a result, the operation of WAKE_UP pin will fail when the next reception starts.

Note: In order not to fail the next reception, MCU should check the output of WAKE_UP pin before entering Idle state.

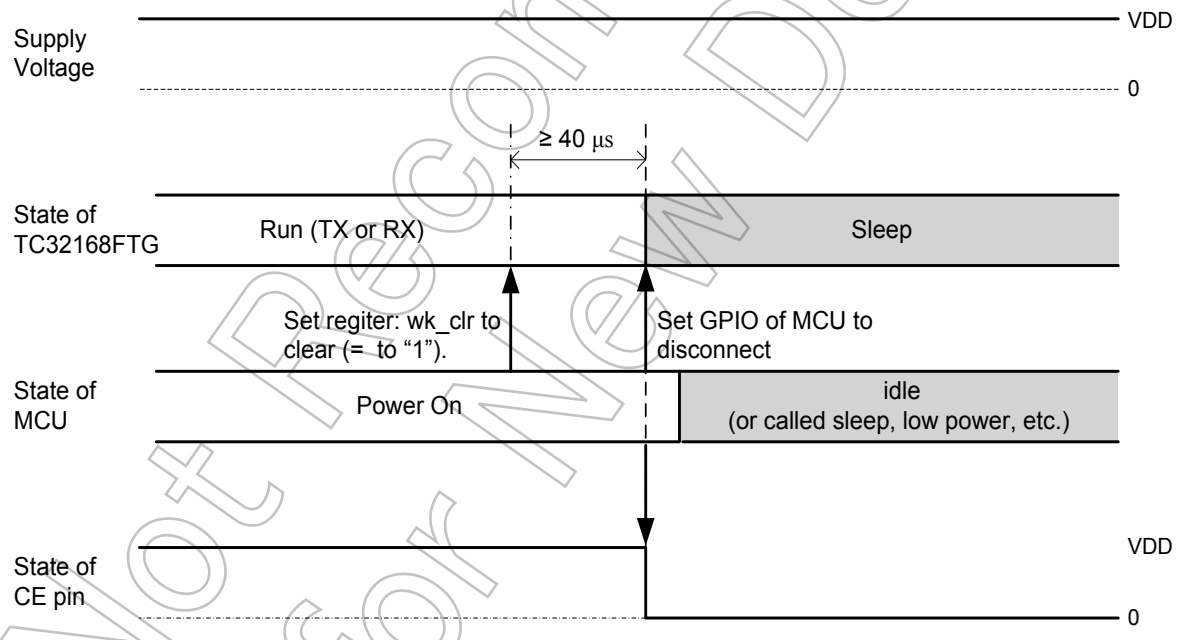


Figure 7-5 Sleep timing diagram

Note: The reset and initialization of Wakeup function described in this section should also be executed, which is not shown in the figure.
Note: Signal durations described in this figure depend on the frequency of the crystal oscillator.

7.11.5 Use of Modem in TX/RX

This product has 4 combinations of Modem operations (Modem mode / Direct mode) and TX/RX states.

(1) Modem Mode and RX State

Modem mode is selected via SPI bus and RX state is also selected by TXRX pin or SPI setting. After completing to receive data, this IC stops data reception, INTRPT/DIO pin (used for an interrupt) becomes "1," and an interrupt is generated. The type of the interrupt can be checked via SPI bus. The reception data can also be read out via SPI bus. When the interrupt completes, this IC re-starts data reception.

If TXRX pin is "0" and the setting is the default one, RF frequency of 5830 MHz or 5840 MHz is automatically received. To receive another frequency signal, the setting of the reception internal frequency and PLL setting should be changed properly.

(2) Modem Mode and TX State

Modem mode is selected via SPI bus and TX state is also selected by TXRX pin or SPI setting. For starting transmission, the transmission frequency should be set via SPI bus and the transmission data should be written to the transmission data register. 5790-MHz RF signal is transmitted in the default setting in this IC.

After completing to transmit data, this IC stops data transmission, INTRPT/DIO pin (used for an interrupt) becomes "1," and an interrupt is generated. The type of the interrupt can be checked via SPI bus. It is recommended that the next transmission should be done after the generation of the interrupt is confirmed. After the next transmission data is written to the transmission data register, this IC can re-start transmitting.

(3) Direct Mode and RX State

Direct mode is selected via SPI bus and RX state is also selected by TXRX pin or SPI setting. This IC outputs a bit stream of the received ASK/OOK RF signal from INTRPT/DIO pin (used for DIO pin). A large amplitude of RF signal of ASK/OOK causes the output "1" from INTRPT/DIO pin, and a small amplitude of RF signal of ASK/OOK causes the output "0."

If TXRX pin is "0" and the setting is the default one, RF frequency of 5830 MHz or 5840 MHz is automatically received. To receive another frequency signal, the setting of the reception internal frequency and PLL setting should be changed properly.

The bit rate of transmission RF output is a fixed value (512/256 kHz) or a divided value (an integer) of 512 kHz.

(4) Direct Mode and TX State

Direct mode is selected via SPI bus and TX state is also selected by TXRX pin or SPI setting. This IC can output RF signal. "1" input to INTRPT/DIO pin generates a large amplitude output of ASK/OOK RF signal, and "0" generates a small amplitude output of ASK/OOK RF signal.

The bit error rate of the received RF signal can be measured in this mode.

7.11.6 Interrupt

The signal of an interrupt is output from INTRPT/DIO pin. When an interrupt is asserted, the interrupt register should be read to identify the type of the interrupt.
The interrupt signal is a level sense one, not an edge sense one. So MCU should detect a level sense interrupt.
There are 10 interrupts asserted to MCU.
When rx_ready, pre_err, flag_err, rxlen_err, fm0_err, crc_ng, rx_abort, or post_err interrupt is asserted, data reception re-starts with the preamble detection. When txlen_err or tx_done interrupt is asserted, MCU should clear these interrupts to transmit the next frame.
The purpose of each interrupt is described as follows. For the register map, refer to 8.14.

Note: Interrupt Mask
Each interrupt is maskable separately. If an interrupt mask is set, the corresponding output of INTRPT/DIO pin is masked. An interrupt operation still executes even though the interrupt mask is set. For the register map, refer to 8.15.

Note: Clearing of Interrupt
Each interrupt can be cleared separately. The output of INTRPT/DIO pin becomes “0” after all asserted interrupts are cleared. The interrupt register should be checked to prepare the next interrupt. For the register map, refer to 8.16.

Note: Interrupt Polarity
The polarity of INTRPT/DIO output signal for the interrupts can be selected by the register int_inv. In this document, the assertion of an interrupt is assumed to "1" output of INTRPT/DIO pin. For the control of the interrupt polarity, refer to 8.17.

Table 7-2 Interrupt types

Item	Register Address	Description
rx_ready	11h[D0]	When the 2nd layer of the information frame is received correctly, rx_ready interrupt is asserted. MCU can read the 2nd layer of the information frame from TRXFIFO.
tx_done	11h[D1]	When the transmission of a frame completes, tx_done interrupt is asserted. tx_done interrupt should be cleared for MCU to transfer the next frame.
pre_err	11h[D2]	If no preambles are detected within 2 ms in RX state, pre_err interrupt is asserted.
flag_err	11h[D3]	If no frame start marks are detected within 2 ms in RX state, flag_err interrupt is asserted.
rxlen_err	11h[D4]	When the reception frame length is larger than the value in the register (Address: 17h), rxlen_err interrupt is asserted.
fm0_err	11h[D5]	If FM0 decoder error occurs during data reception, fm0_err interrupt is asserted.
crc_ng	11h[D6]	If the result of CRC check is incorrect, crc_ng interrupt is asserted.
rx_abort	11h[D7]	When an abort pattern is detected during frame reception, rx_abort interrupt is asserted.
post_err	11h[D8]	When the postamble detection option is active, this interrupt can be asserted. If no postambles are detected, post_err interrupt is asserted. The postamble is not detected in the default setting.
txlen_err	11h[D9]	If the transmission frame length is irregular, txlen_err interrupt is asserted. The irregular length means that the length is not the byte unit or the length is less than 2 bytes.

7.12 Flowchart Examples

The flowcharts for MCU are described here.
As an example, the flowcharts for China's ETC system are described.
Those examples use the initial register settings as much as possible.
In the following flowcharts, only the registers necessary for explanation are described.
For a different system, necessary registers may be different. The registers should be set according to Section 8 "Register Overview and Detail Description."

Note: Signal durations described in the following flowcharts depend on the frequency of the crystal oscillator.

7.12.1 Power On State to TX State (Direct Mode)

Direct mode is selected via SPI bus and TX state is also selected by TXRX pin or SPI setting. A modulated signal should be input to INTRPT/DIO pin (used for DIO pin).

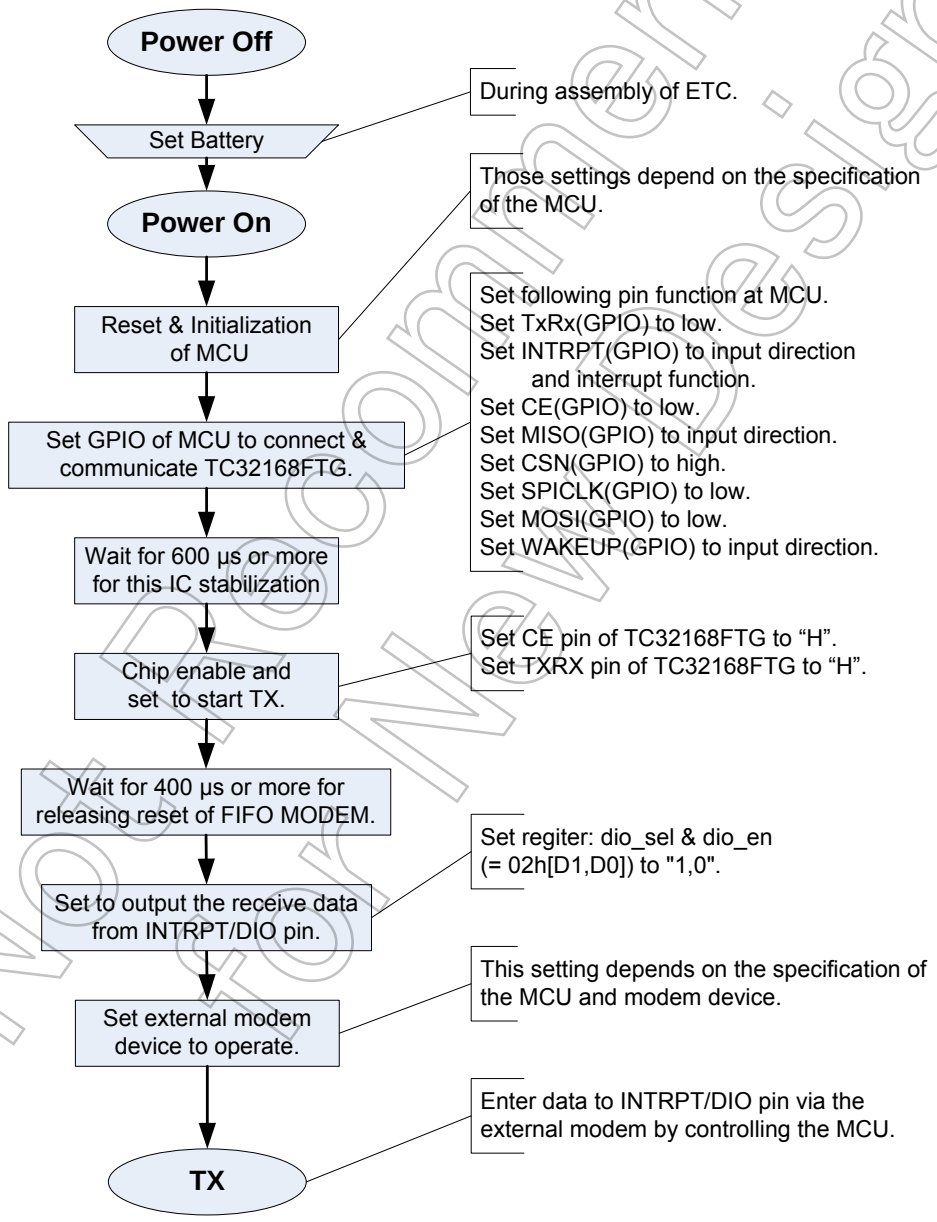


Figure 7-6 Flowchart of Power On state to TX state (Direct mode)

7.12.2 Power On State to RX State (Direct Mode)

Direct mode is selected via SPI bus and RX state is also selected by TXRX pin or SPI setting.
This IC outputs a bit stream of the received ASK/OOK signal from INTRPT/DIO pin (used for DIO pin).

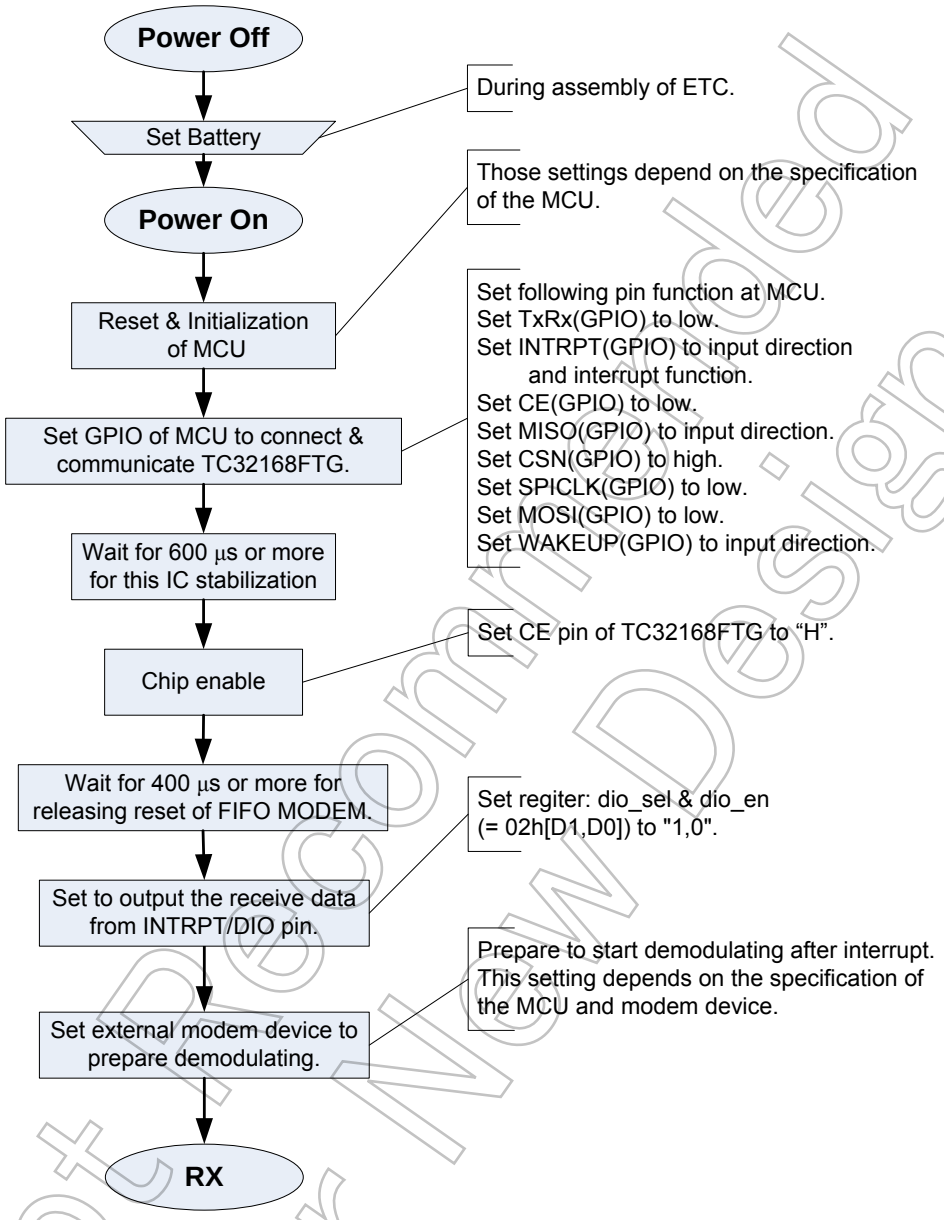


Figure 7-7 Flowchart of Power On state to RX state (Direct Mode)

7.12.3 Power On State to Sleep State to Prepare RX State (Normal/Auto Wakeup)

A conventional sequence which sets up Sleep state to prepare RX state is described here. This IC has two ways to start receiving a signal, Normal Wakeup and Auto Wakeup. This flow contains both. (Refer to the following notes.)

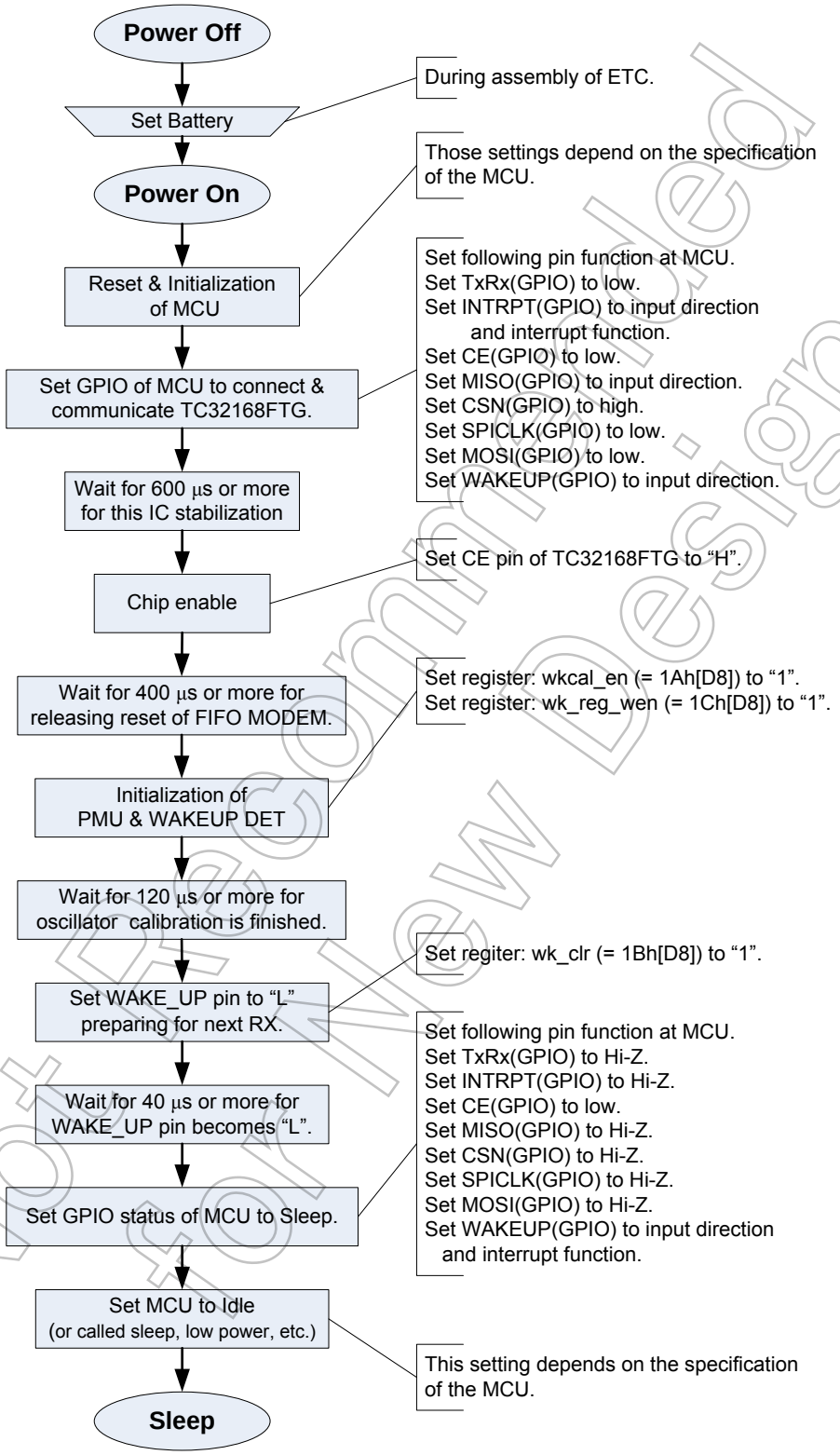


Figure 7-8 Power On state to Sleep state to prepare RX state (Normal or Auto Wakeup)

Note: In order to start Auto Wakeup operation in RX state, it is necessary to set the register autowk (= 19h[D0]) to "1" at the initialization of PMU and WAKEUP DET.

Note: "Hi-Z" means high impedance. This setting reduces leakage current.

7.12.4 Suspension

When CE pin turns to “0,” this IC enters Sleep state.
The register settings are ignored.
The preparation of the next reception or transmission should be done before executing the suspension.

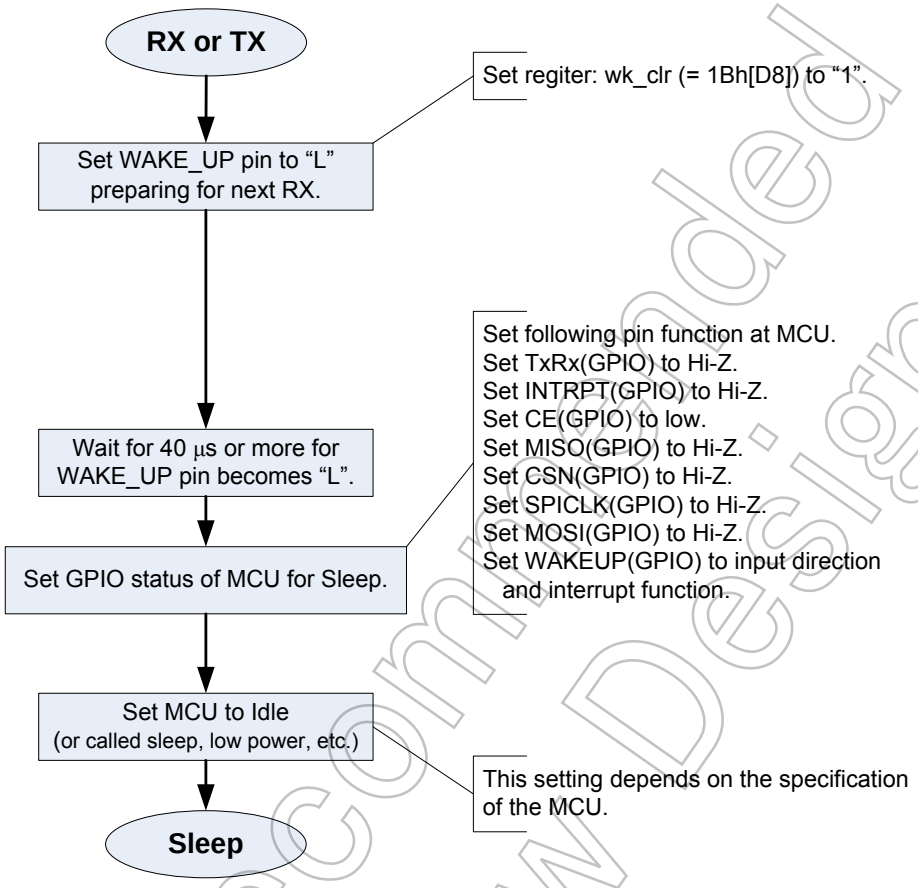


Figure 7-9 TX/RX state to Sleep state

Note: When Wakeup operation is changed, the register autowk (= 19h[D0]) should be updated here.
Note: Before entering Sleep state, WAKEUP (GPIO) should be kept in an input to execute an interrupt surely.
Otherwise, MCU cannot be started up by WAKE_UP pin output at the next reception.
Note: “Hi-Z” means high impedance. This setting reduces leakage current.

7.12.5 Sleep State to RX State (Normal Wakeup)

This product has a Wakeup function to detect a 14-kHz waveform in 5.8-GHz frequency band.
When a detected signal matches the expected signal, WAKE_UP pin outputs “1.”
There are two Wakeup operations, Normal Wakeup and Auto Wakeup.
In Normal Wakeup, MCU starts up this device when it sets CE pin to "1."

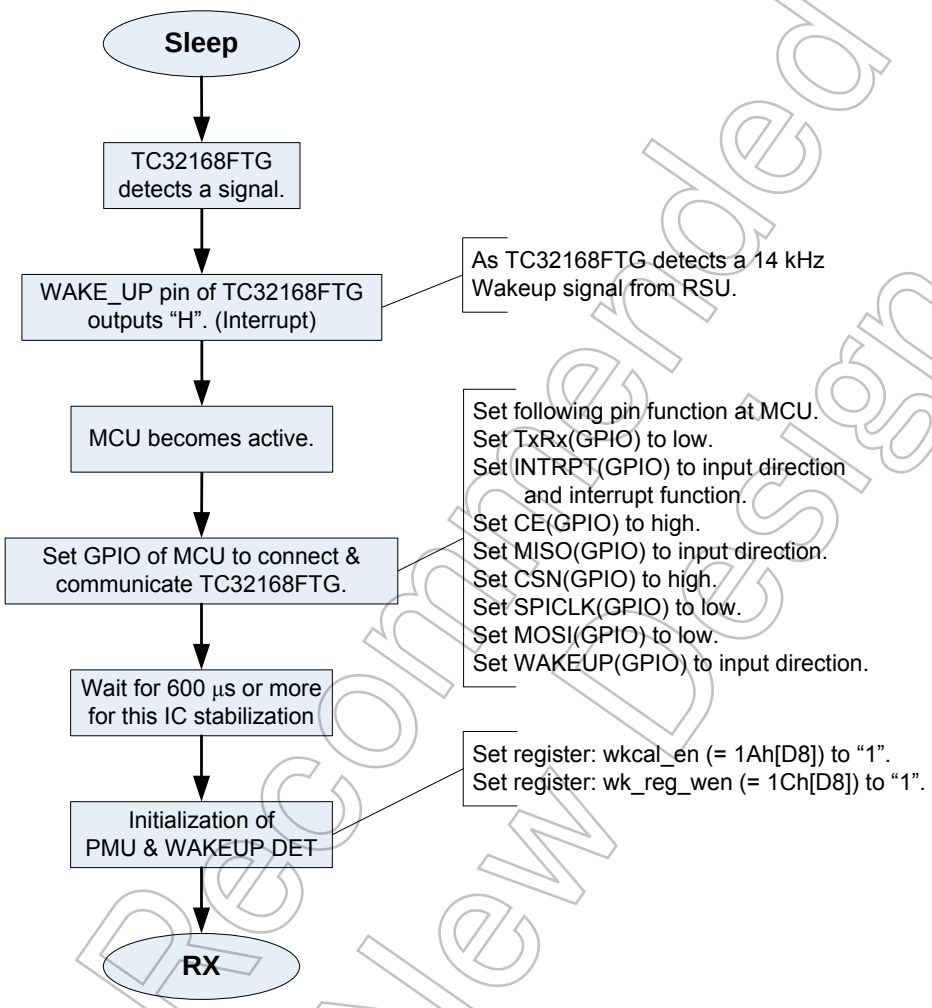


Figure 7-10 Transition from Sleep state to RX state by Normal Wakeup

Note: In the previous Suspension state, WAKEUP (GPIO) should be kept in an input to execute an interrupt surely. Otherwise, MCU cannot be started up by this Normal Wakeup sequence.

7.12.6 Sleep state to RX state (Auto Wakeup)

In Auto Wakeup sequence, this product becomes active automatically when a 14-kHz waveform in 5.8-GHz frequency band is detected and the detected signal matches the expected signal.
MCU starts up when WAKE_UP pin becomes "1."

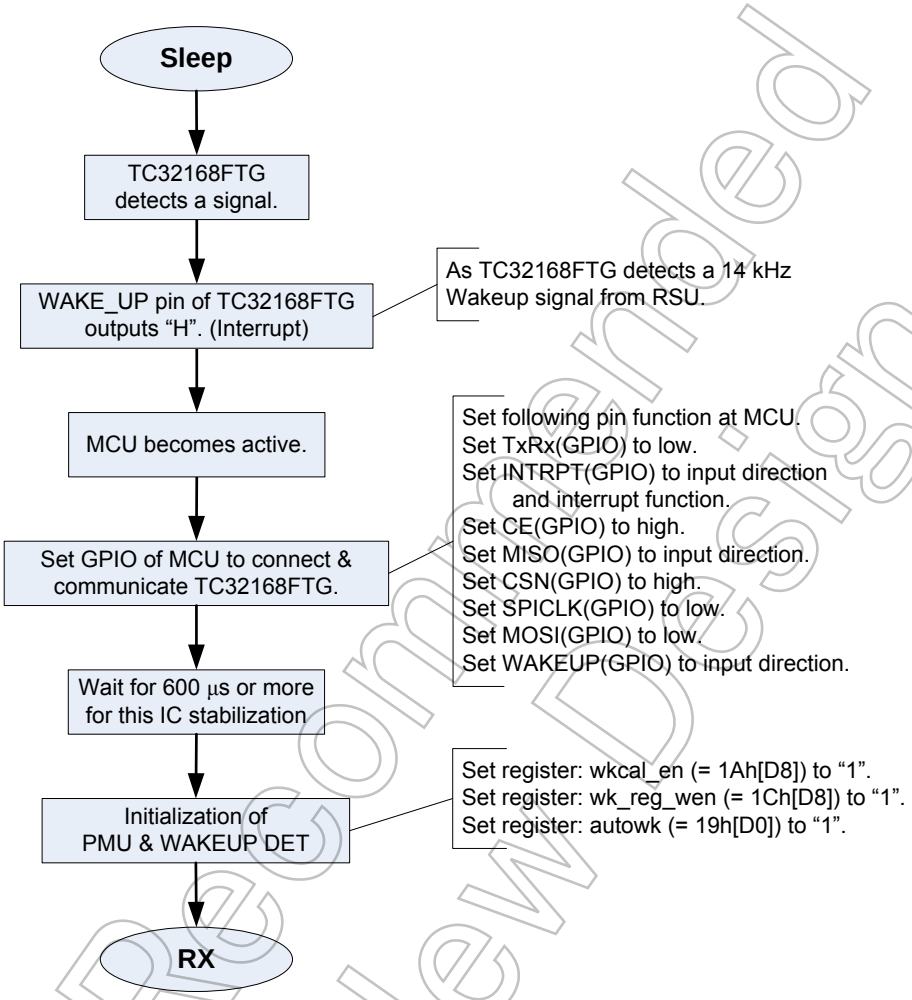


Figure 7-11 Transition from Sleep state to RX state by Auto Wakeup

Note: In the previous Suspension state, WAKEUP (GPIO) should be kept in an input to execute an interrupt surely. Otherwise, MCU cannot be started up by this Auto Wakeup sequence.

7.12.7 Sleep State to TX State

In the transition sequence from Sleep state to TX state, the MCU controls TC32168FTG and the application system.

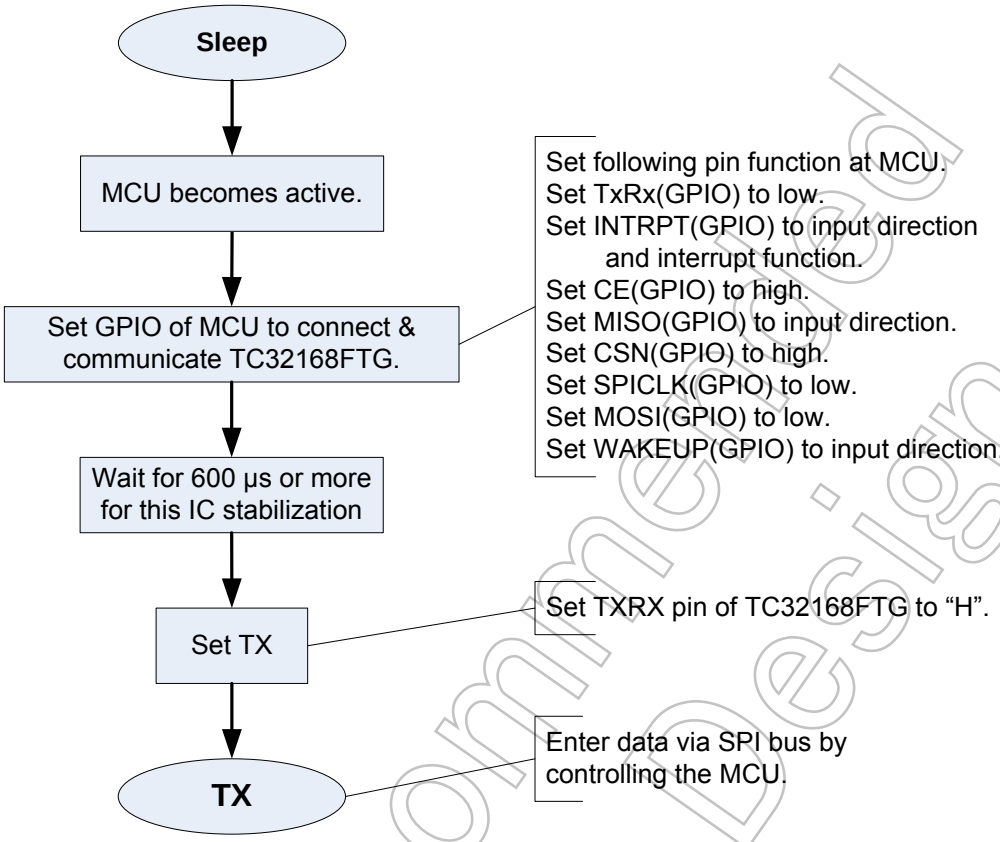


Figure 7-12 Transition from Sleep state to TX state controlled by MCU

7.12.8 RX State

The following flow shows waiting for a signal, receiving the signal, detecting, and data transmission to MCU.

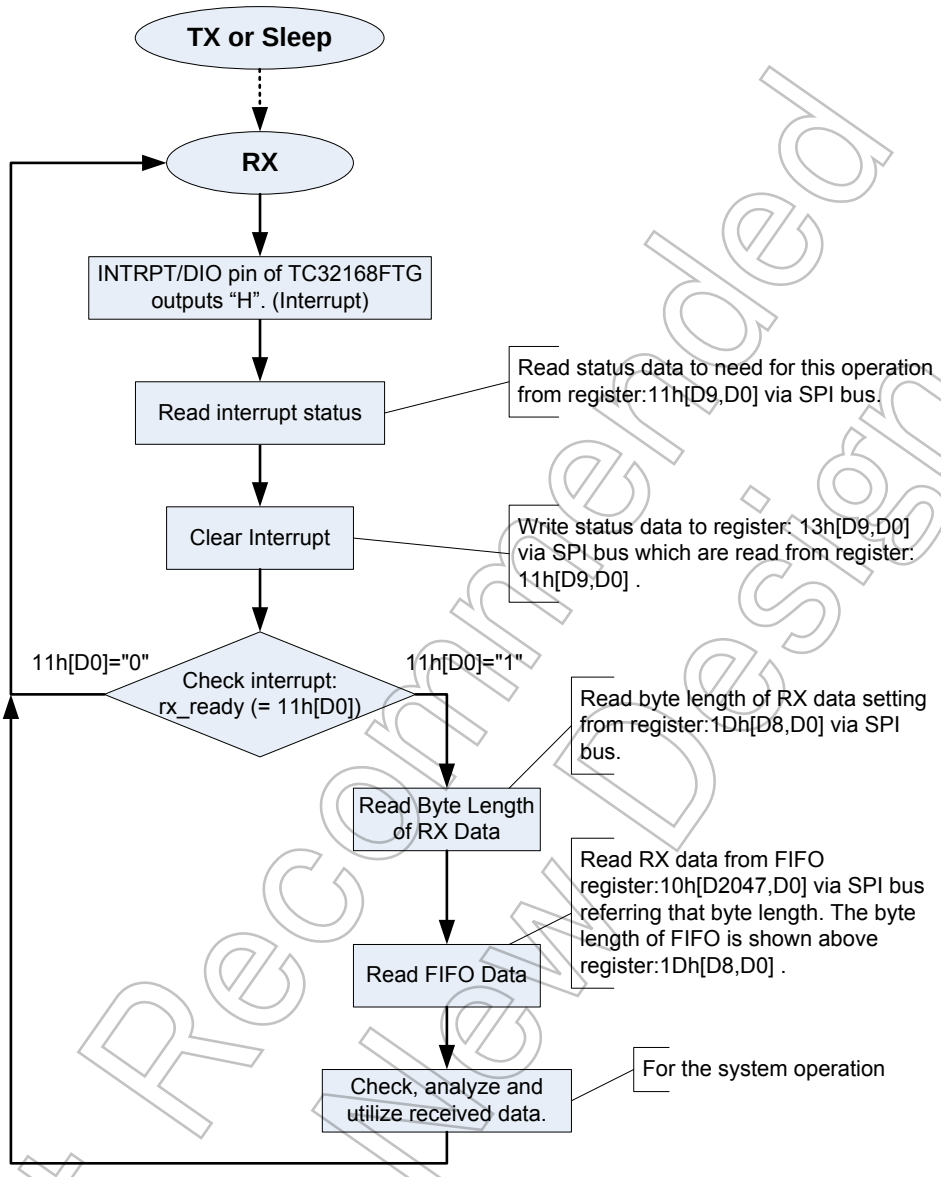


Figure 7-13 Signal wait and reception

7.12.9 RX State at BST Reception

As a special case, the following flow shows waiting for a signal, receiving the signal, detecting, and data transmission to MCU in Beijing's ETC system.

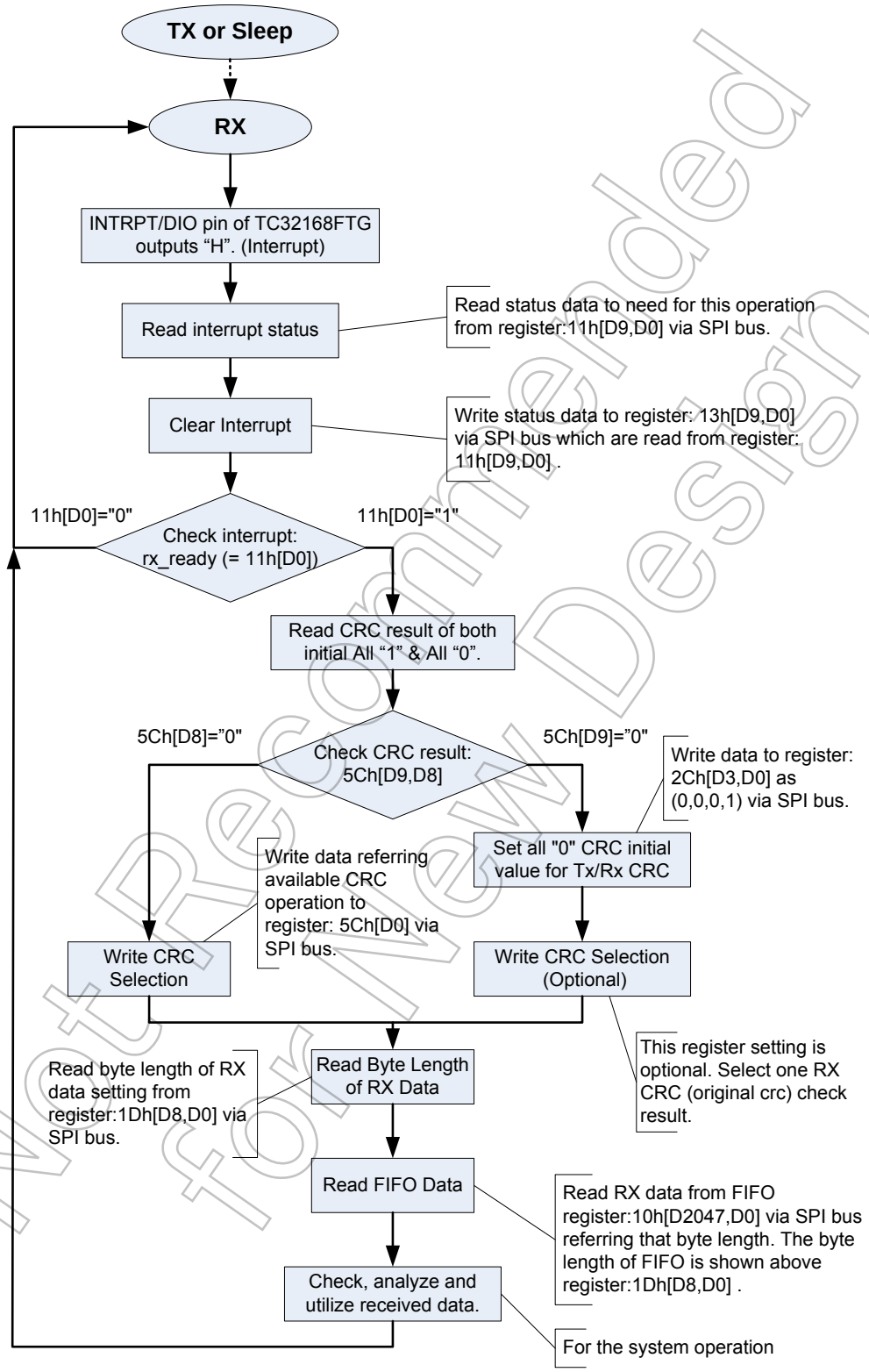


Figure 7-14 Signal wait and reception for BST reception (CRC rejection sequence in Beijing ETC System)

Note: rx_ready interrupt can check that the register crc_rslt_b (= 5Ch[D9]) is "1" or the register crc_rslt_a (= 5Ch[D8]) is "1." Both cases are loop back paths. So, before CRC result is checked, it is necessary to set that neither cases should occur.

Note: For the detail of "Write of CRC Selection," refer to 7.15.

7.12.10 Reception Frequency Change

The following flow shows the sequence to change the reception frequency during RX state.

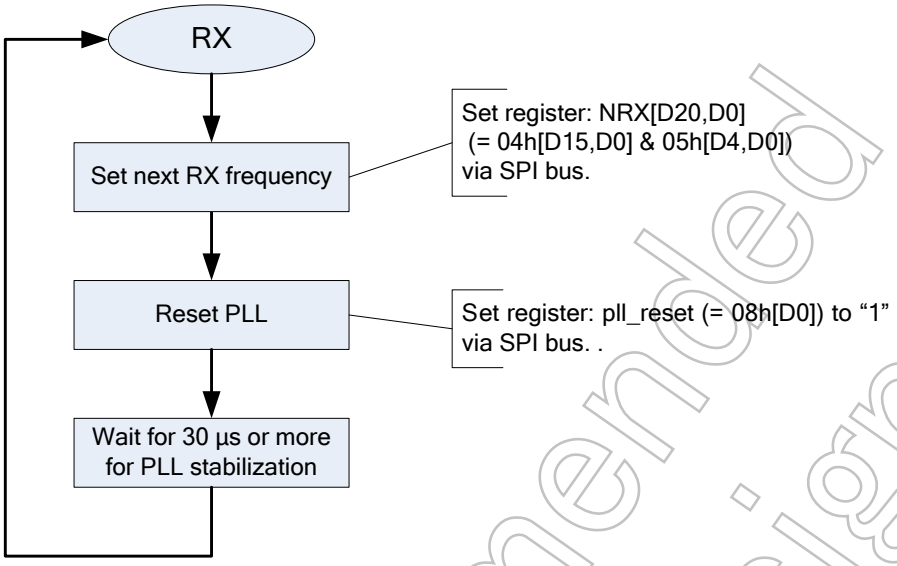


Figure 7-15 Reception frequency change during RX state

Note: The calculation of the reception frequency is shown in 7.2.

Note: When the initial reception frequency is not used, the PLL should be reset by setting the register NRX via SPI bus before starting data reception.

7.12.11 TX state

The following flow shows the sequence of data transmission and MCU checking.

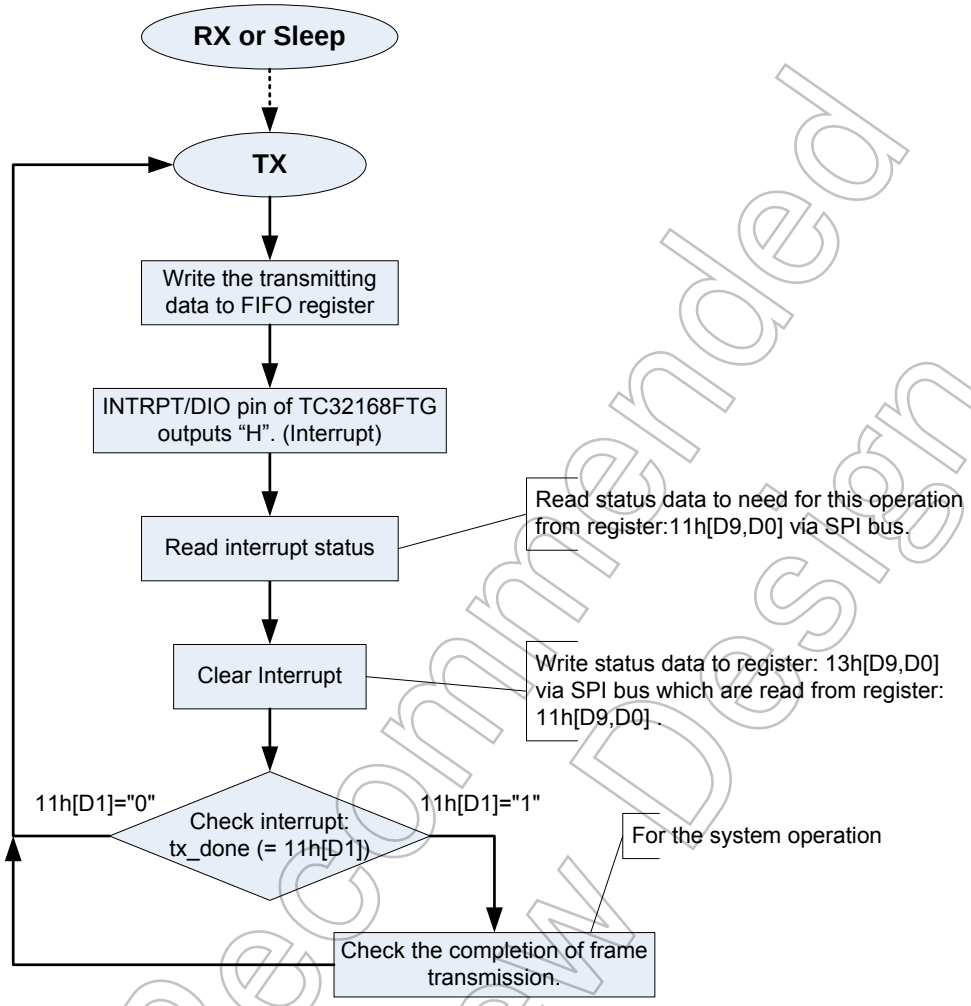


Figure 7-16 Sequence of data transmission and checking

7.12.12 Transmission Frequency Change

The following flow shows the sequence to change the transmission frequency during TX state.

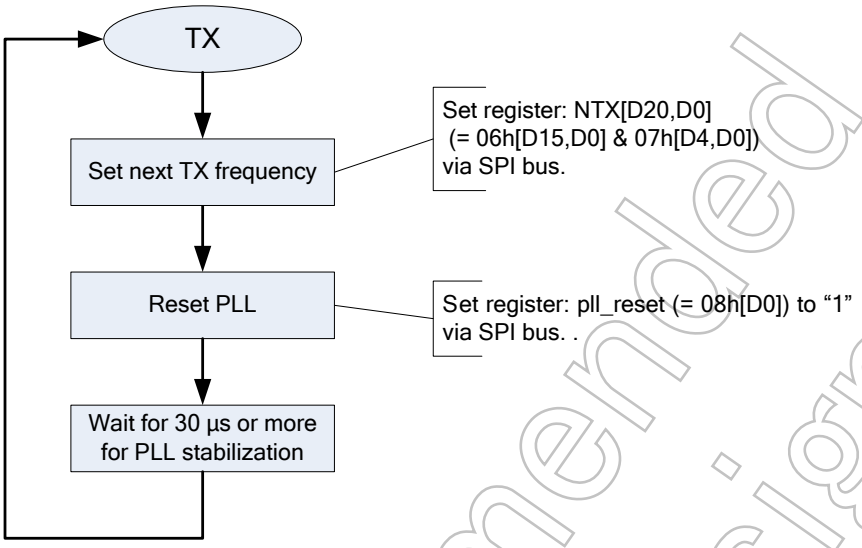


Figure 7-17 Transmission frequency change during TX state

Note: The calculation of the transmission frequency is shown in 7.2.

Note: When the initial transmission frequency is not used, the PLL should be reset by setting the register NTX via SPI bus before starting data transmission.

7.12.13 RX State to TX State

When the RF signal direction is changed, TXRX pin or SPI bus control is used.

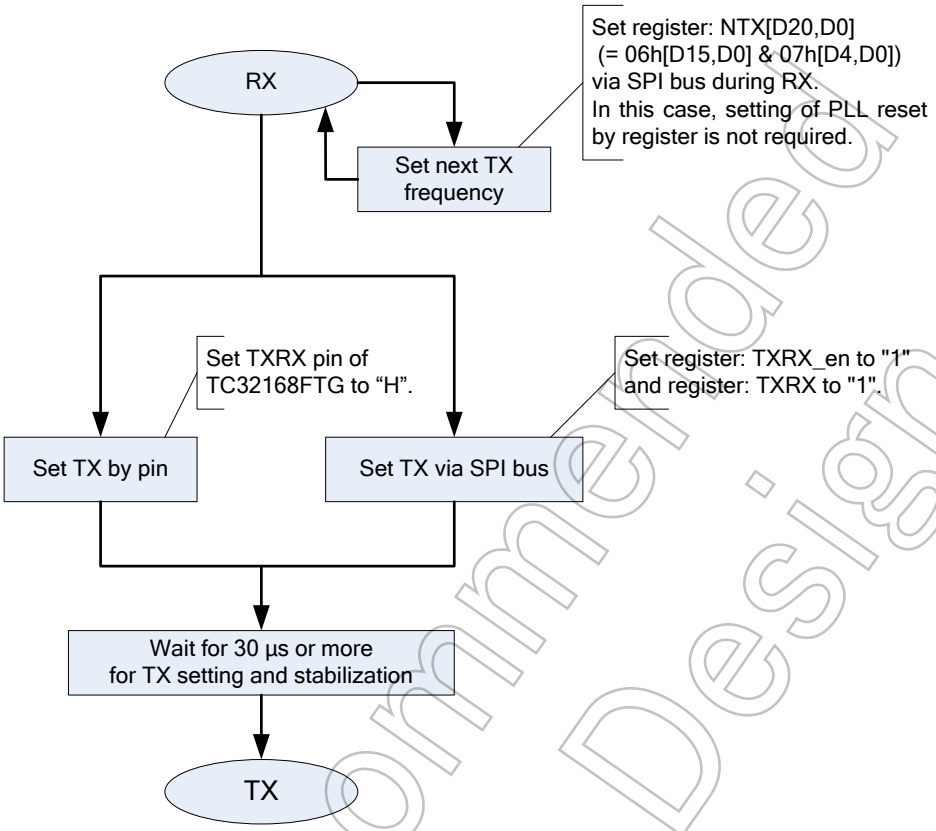


Figure 7-18 RX state to TX state

7.12.14 TX State to RX State

When the RF signal direction is changed, TXRX pin or SPI bus control is used.

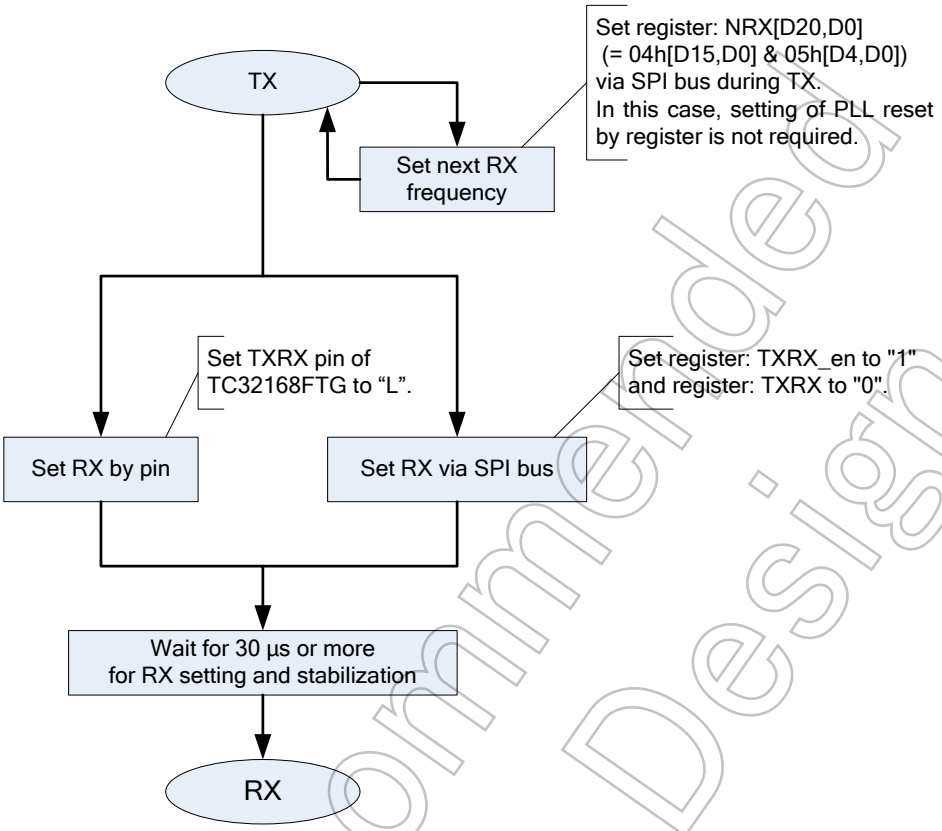


Figure 7-19 TX state to RX state

7.13 Sequential Reception of Downlink Frames

When two downlink frames are transmitted subsequently with the minimum interval (10 μs), the read timing of the register for the reception data is shown as follows.

Case1:
Both the first frame and the subsequent frame are received.

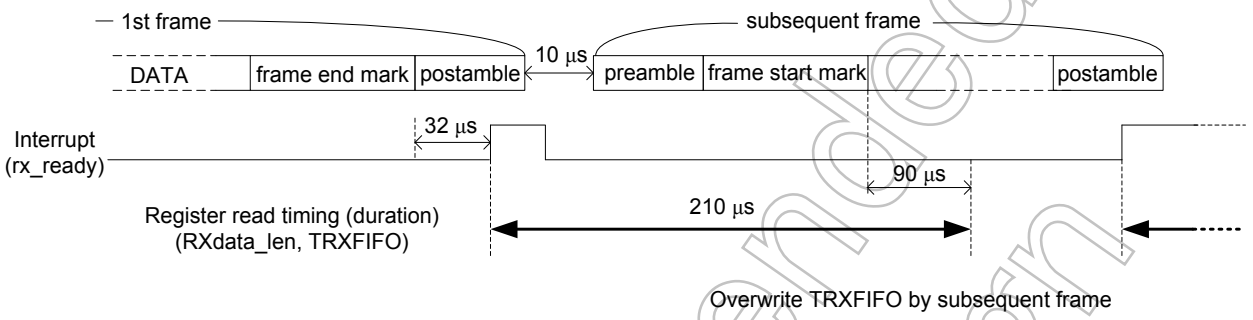


Figure 7-20 TRXFIFO timing for two frame reception

The register RXdata_len (= 1Dh[D8.D0]) and the register TRXFIFO (= 10h[D2047.D0]) have to be read in the interval between rx_ready (= 11h[D0]) interrupt assertion and 90 μs after the head of the next transmission data (210 μs).

Case2:
Only the 1st frame is received. And TC32168FTG enters TX State.

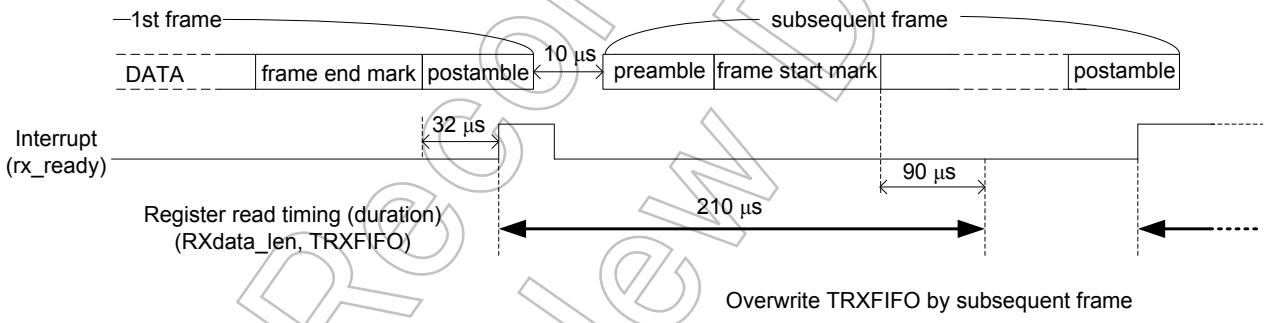


Figure 7-21 TRXFIFO timing for one frame reception

The register RXdata_len and the register TRXFIFO have to be read in the interval between rx_ready interrupt assertion and 90 μs after the head of the next transmitted data (210 μs). When transiting to TX state, the register TRXFIFO is cleared.

7.14 Reception of CRC Error Frame

Even though CRC result is not correct, MCU can read the received frame and the CRC result if the frame end mark is correct. Reading method is the same as the case of the correct CRC result.

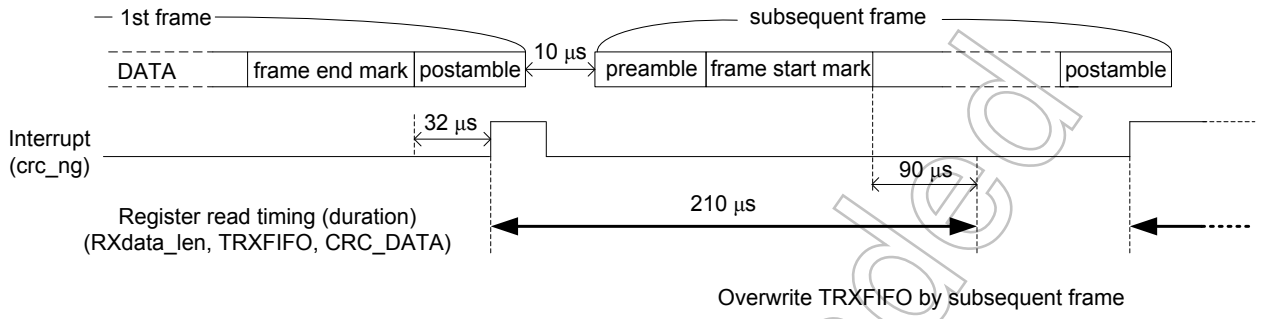


Figure 7-22 Reception of CRC error frame

7.15 CRC Selection

When the register sel_crc (= 5Ch[D0]) is set to "0" and the register crc_inv/lsb_msb/crc_pol/crc_ini (= 2Ch[D3,D0]) is set to (0,0,0,0), both CRC results whose initial values are all "1" and all "0" can be received. That means both CRC values are calculated simultaneously. "1" CRC check parameter can be set to the register crc_ini (= 2Ch[D3,D0]). And the other CRC check parameters are determined according to the CRC result whose initial value is all "1."

The results of CRC calculation are stored to the registers crc_rslt_b and crc_rslt_a (= 5Ch[D9,D8]). Which CRC result should be used is decided after the registers crc_rslt_b and crc_rslt_a are read in rx_ready interrupt sequence. When the register crc_rslt_b is "0," the CRC frame whose initial value is all "0" is received. When the register crc_rslt_a is "0," the CRC frame whose initial value is all "1" is received. According to the CRC results, the register crc_ini (= 2Ch[D0]) should be set appropriately. When the register sel_crc is set to "1," only "1" CRC check is effective, and the parameters for CRC with the initial value of all "0" become invalid. So the result of the CRC whose initial value is all "0" becomes incorrect. After the CRC selection, the register sel_crc should be set to "1" to use only “1” CRC check.

For the CRC selection, refer to Figure 7-23.

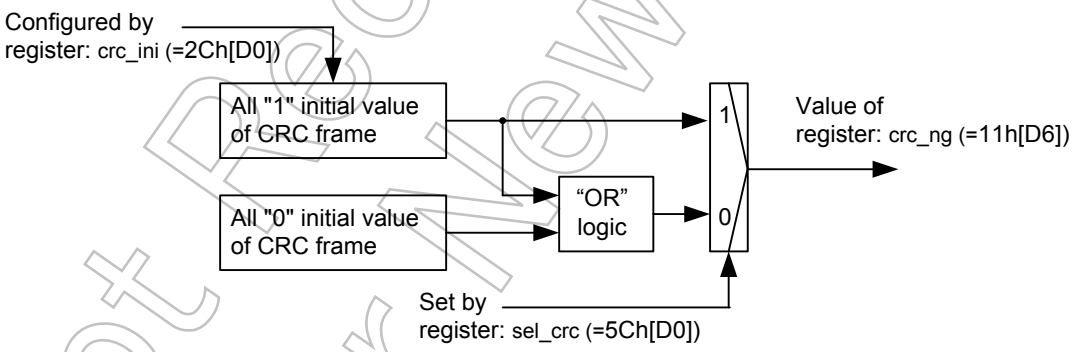


Figure 7-23 CRC selection

Note: The contents in 7.13, 7.14 and 7.15 are useful to construct a system for Beijing's ETC.

7.16 Register Access for System Control

7.16.1 SPI Control Data Format

The conceptual diagrams of SPI control data format are shown as follows. The format consists of an address (8 bits) and a data (16 bits). The read or write is instructed in the value of the third bit. The bit "0" means data read and "1," data write. To separate each communication data, "1" duration which is 1-cycle or more length of SPI clock is inserted between the data.

(1) SPI Write Access Format

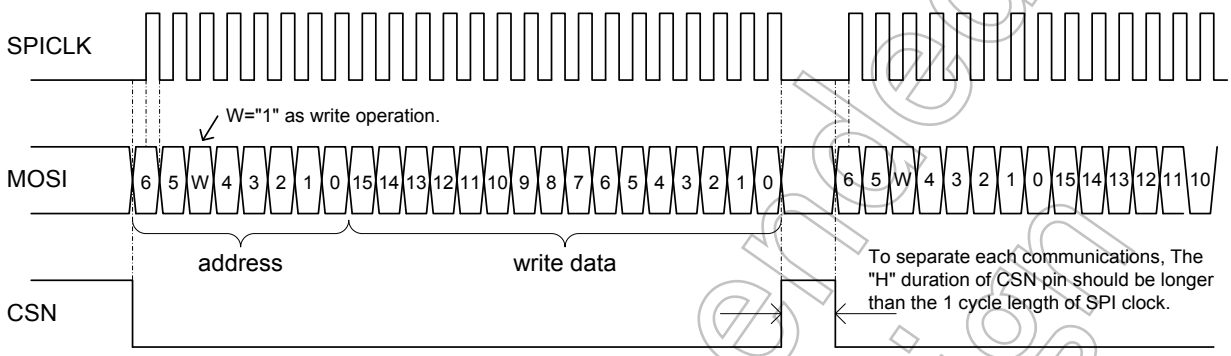


Figure 7-24 SPI write format

(2) SPI Read Access Format

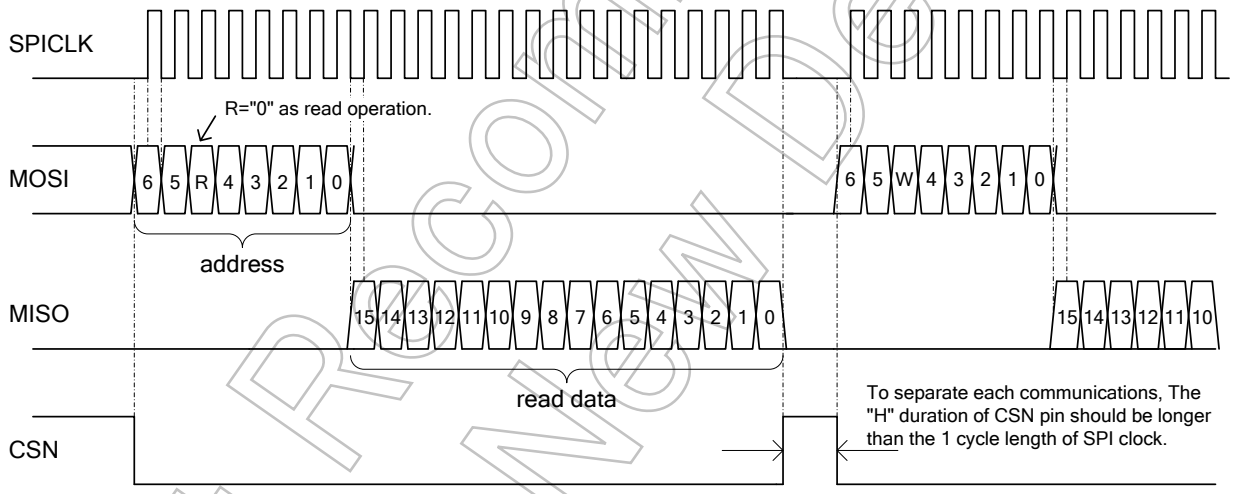


Figure 7-25 SPI read format

The conceptual diagrams of SPI FIFO data format are shown as follows. The format consists of an address (8 bits) and a data (2048 bits). The length of FIFO data is an 8-byte unit. The data length is 128 bytes or less. The instruction of read or write and the separating each communication data are the same as those of SPI control data format. The address of the SPI FIFO data format is fixed to 10h (TRXFIFO register).

(3) SPI FIFO Data Write Access Format

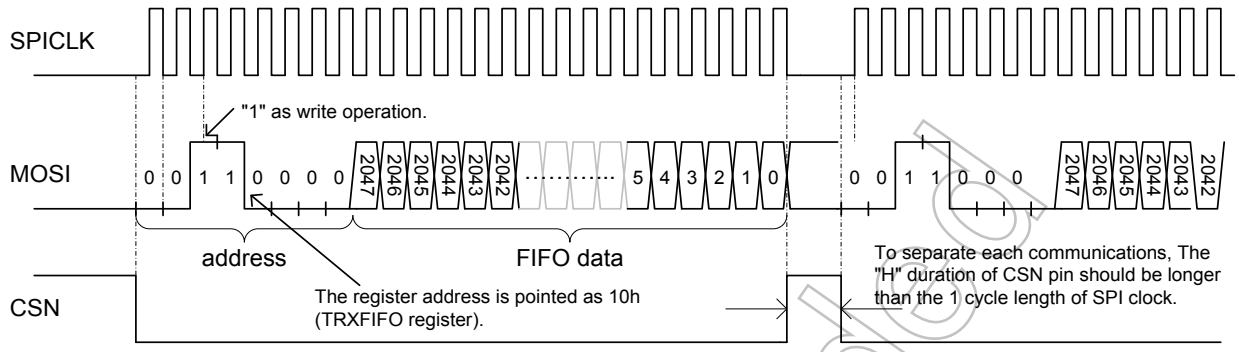


Figure 7-26 SPI FIFO data write format

(4) SPI FIFO Data Read Access Format

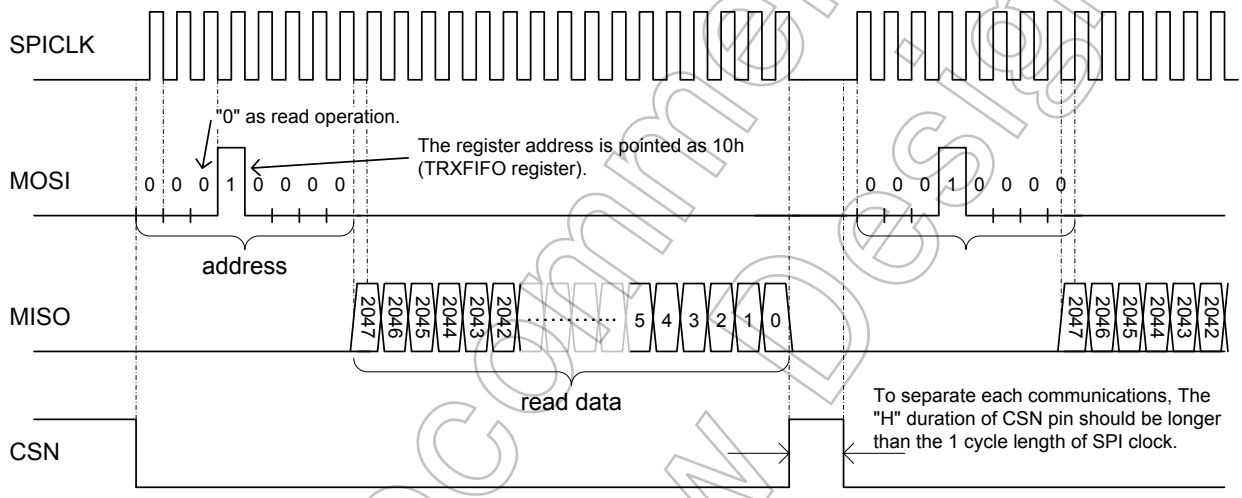


Figure 7-27 SPI FIFO data read format

7.16.2 SPI Signal Timing Specification

The conceptual diagrams of TC32168FTG's SPI signal timing specification is shown as follows. The figure shows the simplified operation for explanation.

The interrelationship among the signal timings should be compliant to specified values. The frequency of SPICLK should be 8 MHz or less not to fail the communication between this IC and MCU. The gray areas in the following figure show no influence on the communication.

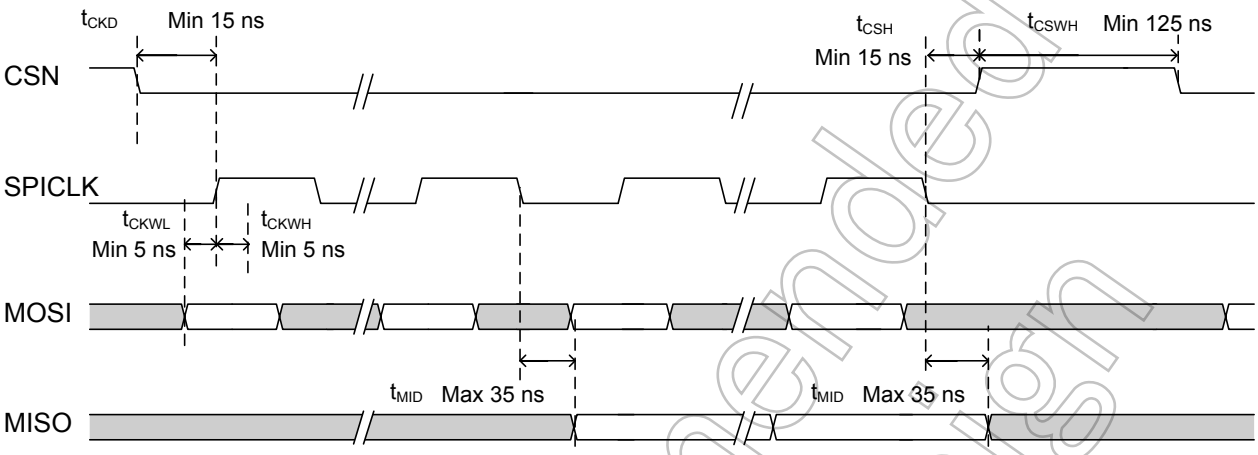


Figure 7-28 SPI signal timing specification

Table 7-3 SPI signal timing

Item	Symbol	Min	Typ.	Max	Unit
SPI CLK Frequency	f_{SPI}	0.05	8.0	8.192	MHz
CLK "H" Time	t_{CKWH}	5	—	—	ns
CLK "L" Time	t_{CKWL}	5	—	—	ns
CLK Delay Time	t_{CKD}	15	—	—	ns
CS "H" Time	t_{CSWH}	125	—	—	ns
CS Hold Time	t_{CSH}	15	—	—	ns
MISO Delay Time	t_{MID}	—	—	35	ns

Note: The values above should be used for the time values of SPI bus.

8. Register Overview and Detail Description

8.1 Register Overview

The contents of Table 8-1 show the register overview in TC32168FTG for China's ETC application system.
For the details, refer to the following sections.

Table 8-1 Register Overview

Sec.	Address	Function	Name	Used Bit	R/W	Description
8.2	00h	SWRST	RST	D7	W	Software reset.
8.3	01h	TX RX Status	TXRX_en	D1	W	Select transmission or reception
8.4	02h	DIO ENABLE	dio_sel	D1	R/W	Select the function of INTRPT/DIO pin.
			dio_en	D0	R/W	Enable INTRPT/DIO pin.
8.5	04h	PLL_RX1	NRX	[D15,D0]	R/W	Set the reception PLL frequency (LSB).
8.6	05h	PLL_RX2	NRX	[D20,D16]	R/W	Set the reception PLL frequency (MSB).
8.7	06h	PLL_TX1	NTX	[D15,D0]	R/W	Set the transmission PLL frequency (LSB).
8.8	07h	PLL_TX2	NTX	[D20,D16]	R/W	Set the transmission PLL frequency (MSB).
8.9	08h	PLL_RST	pll_reset	D0	W	Reset of PLL block.
8.10	09h	TX_Power_Control	outctrl	[D11,D0]	R/W	Control of transmission power.
8.11	0Ah	Analog_Settings	bw	D8	W	Select IF filter band width.
			ook	D7	W	Select to use the anti-aliasing filter for modulation.
			ph	D6	W	Select RSSI peak hold operation.
			mr	[D4,D0]	W	Set the modulation index.
8.12	0Bh	Analog_Settings_WU	w_s_set	[D3,D0]	R/W	Set Wakeup sensitivity.
8.13	10h	TRXFIFO	txdata	[D2047,D0]	R/W	Read/Write data of Transmission/Reception FIFO
8.14	11h	INTR_ST	txlen_err	D9	R	Transmission frame length is invalid.
			post_err	D8	R	No postambles are detected.
			rx_abort	D7	R	Abort sequence is detected.
			crc_ng	D6	R	CRC check result is not correct.
			fm0dec_err	D5	R	FM0 decode error occurs.
			rxlen_err	D4	R	Reception frame length is invalid.
			flag_err	D3	R	No frame start marks are detected.
			pre_err	D2	R	No preambles are detected.
			tx_done	D1	R	Complete transmission of a frame.
			rx_ready	D0	R	Reception frame is received.
8.15	12h	INTR_MK	txlen_err_mask	D9	R/W	Set an interrupt mask.
			post_err_mask	D8	R/W	
			rx_abort_mask	D7	R/W	
			crc_ng_mask	D6	R/W	
			fm0dec_err_mask	D5	R/W	
			rxlen_err_mask	D4	R/W	
			flag_err_mask	D3	R/W	
			pre_err_mask	D2	R/W	
			tx_done_mask	D1	R/W	
			rx_ready_mask	D0	R/W	

Sec.	Address	Function	Name	Used Bit	R/W	Description
8.16	13h	INTR_CLR	txlen_err_clr	D9	W	Clear an interrupt.
			post_err_clr	D8	W	
			rx_abort_clr	D7	W	
			crc_ng_clr	D6	W	
			fm0dec_err_clr	D5	W	
			rxlen_err_clr	D4	W	
			flag_err_clr	D3	W	
			pre_err_clr	D2	W	
			tx_done_clr	D1	W	
			rx_ready_clr	D0	W	
8.17	14h	INTR_INV	int_inv	D0	R/W	Invert the output of the interrupt pin.
8.18	15h	BIT_RATE	txrate	[D9,D8]	R/W	Set the transmission bit rate.
8.18	15h	BIT_RATE	rxrate	D0	R/W	Set the reception bit rate.
8.19	16h	RAMP FIFO	rmpup	[D255,D128]	R/W	Set the ramp-up coefficient.
8.19	16h	RAMP FIFO	rmpdwn	[D127,D0]	R/W	Set the ramp-down coefficient.
8.20	17h	MAX_RXDATALEN	rxlen	[D8,D0]	R/W	Set the maximum reception data length.
8.21	18h	WK_DET_NUM	wk_num	[D3,D0]	R/W	Set the number of Wakeup detection cycles.
8.22	19h	WakeUP_REG_SETS	autowk	D0	R/W	Select Wakeup operation.
8.23	1Ah	CAL_WakeUp	wkcal_en	D8	W	Start calibration of Wakeup detection timer.
8.24	1Bh	WakeUP_CLR	wk_clr	D8	W	Clear the output of WAKE_UP pin.
8.25	1Ch	Wakeup_reg_write	wk_reg_wen	D8	W	Write data to Wakeup register.
8.26	1Dh	RXdata_len	rxdatalen	[D8,D0]	R	Byte number of the received data in the reception FIFO.
8.27	2Ch	CRC_INI	crc_inv	D3	R/W	Invert CRC result.
			lsb_msb	D2	R/W	Select MSB first or LSB first for transmission data.
			crc_pol	D1	R/W	Select CRC generating polynomial.
			crc_ini	D0	R/W	Select the initial value of CRC shift register.
8.28	36h	RX_DET_TIMER_DIS	dettimer_dis	D0	R/W	Control the reception detection timer.
8.29	3Ch	TEST SEL	txbit_sel	[D5,D4]	R/W	Generate the transmission data pattern for test.
			fir_sel	[D2,D0]	R/W	Select the transmission data for test.
8.30	3Dh	WK_FREQ_SET	wk_high_det	[D11,D8]	R/W	Set Wakeup detection pulse frequency to 20 kHz or more.
			wk_low_det	[D4,D0]	R/W	Set Wakeup detection pulse frequency to 10 kHz or less.
8.31	3Eh	WK_FREQ_SET_WEN	wk_freq_wen	D8	W	Write a frequency data to Wakeup register.
8.32	43h	RX FIFO CLEAR	rxfifocls	D8	W	Clear the reception FIFO register.
8.33	56h	XOSC_TRIM	xosc_ctrim	[D11,D8]	R/W	Trim the crystal oscillator circuit.
8.34	5Ch	SEL_RX_CRC	crc_rslt_b	D9	R	Check the CRC result whose initial value is all "0."
			crc_rslt_a	D8	R	Check the CRC result whose initial value is all "1."
			sel_crc	D0	R/W	Select CRC operation.
8.35	5Dh	CRC_DATA	crc_data	[D15,D0]	R	Received CRC data.

8.2 00h; Software Reset

Address	Function	Name		R/W	Initial Value.	Description
00h	SWRST	D15	—	W	0	Don't care. (Recommended to set to “0.”)
		D14	—	W	0	Don't care. (Recommended to set to “0.”)
		D13	—	W	0	Don't care. (Recommended to set to “0.”)
		D12	—	W	0	Don't care. (Recommended to set to “0.”)
		D11	—	W	0	Don't care. (Recommended to set to “0.”)
		D10	—	W	0	Don't care. (Recommended to set to “0.”)
		D9	—	W	0	Don't care. (Recommended to set to “0.”)
		D8	—	W	0	Don't care. (Recommended to set to “0.”)
		D7	RST	W	0	Reset operation during register write access. 1: Reset **0: No Operation <Initial value>** When the register 00h[D7] is set to “1,” the software reset is asserted. So, this bit is automatically cleared. By this software reset, the main registers and the modem are reset,
		D6	—	W	0	Don't care. (Recommended to set to “0.”)
		D5	—	W	0	Don't care. (Recommended to set to “0.”)
		D4	—	W	0	Don't care. (Recommended to set to “0.”)
		D3	—	W	0	Don't care. (Recommended to set to “0.”)
		D2	—	W	0	Don't care. (Recommended to set to “0.”)
		D1	—	W	0	Don't care. (Recommended to set to “0.”)
		D0	—	W	0	Don't care. (Recommended to set to “0.”)

Note: PMU and WAKEUP DET are not reset by this software reset.

8.3 01h; TX/RX State Selection

Address	Function	Name		R/W	Initial Value	Description
01h	TX or RX State	D15	—	W	0	Don't care. (Recommended to set to “0.”)
		D14	—	W	0	Don't care. (Recommended to set to “0.”)
		D13	—	W	0	Don't care. (Recommended to set to “0.”)
		D12	—	W	0	Don't care. (Recommended to set to “0.”)
		D11	—	W	0	Don't care. (Recommended to set to “0.”)
		D10	—	W	0	Don't care. (Recommended to set to “0.”)
		D9	—	W	0	Don't care. (Recommended to set to “0.”)
		D8	—	W	0	Don't care. (Recommended to set to “0.”)
		D7	—	W	0	Don't care. (Recommended to set to “0.”)
		D6	—	W	0	Don't care. (Recommended to set to “0.”)
		D5	—	W	0	Don't care. (Recommended to set to “0.”)
		D4	—	W	0	Don't care. (Recommended to set to “0.”)
		D3	—	W	0	Don't care. (Recommended to set to “0.”)
		D2	—	W	0	Don't care. (Recommended to set to “0.”)
		D1	TXRX_en	W	0	Select the way to switch between TX state and RX state. **0: Setting by TXRX pin is enabled. <Initial value>** 1: Setting by the register 01h[D0] is enabled.
		D0	TXRX	W	0	TX state of RX state selection. **0: RX state <Initial value>** 1: TX state

8.4 02h; Selection of Function of INTRPT/DIO Pin

Address	Function	Name		R/W	Initial Value	Description
02h	DIO ENABLE	D15	—	W	0	Don't care. (Recommended to set to “0.”)
		D14	—	W	0	Don't care. (Recommended to set to “0.”)
		D13	—	W	0	Don't care. (Recommended to set to “0.”)
		D12	—	W	0	Don't care. (Recommended to set to “0.”)
		D11	—	W	0	Don't care. (Recommended to set to “0.”)
		D10	—	W	0	Don't care. (Recommended to set to “0.”)
		D9	—	W	0	Don't care. (Recommended to set to “0.”)
		D8	—	W	0	Don't care. (Recommended to set to “0.”)
		D7	—	W	0	Don't care. (Recommended to set to “0.”)
		D6	—	W	0	Don't care. (Recommended to set to “0.”)
		D5	—	W	0	Don't care. (Recommended to set to “0.”)
		D4	—	W	0	Don't care. (Recommended to set to “0.”)
		D3	—	W	0	Don't care. (Recommended to set to “0.”)
		D2	—	W	0	Don't care. (Recommended to set to “0.”)
		D1	dio_sel	W	0	Select the signal direction of INTRPT/DIO pin used for a digital I/O (the register dio_en is set to "1") in Direct mode. 0: INTRPT/DIO pin is an output. 1: INTRPT/DIO pin is an input.
		D0	dio_en	W	0	Select the function of INTRPT/DIO pin. **0: INTRPT/DIO pin is used for an interrupt. <Initial Value>** 1: INTRPT/DIO pin is used for a data input/output pin.

8.5 04h; Reception PLL Frequency Setting (LSB)

Address	Function	Name		R/W	Initial Value	Description
04h	PLL_RX1	D15	NRX[15]	W	0	Set the reception PLL frequency (LSB). Set the value of f_{LO} MHz × 125. (f_{LO} is the internal frequency.) **Initial frequency: 5835 MHz** (The initial value of the register is “211Fh.”)
		D14	NRX[14]	W	0	
		D13	NRX[13]	W	1	
		D12	NRX[12]	W	0	
		D11	NRX[11]	W	0	
		D10	NRX[10]	W	0	
		D9	NRX[9]	W	0	
		D8	NRX[8]	W	1	
		D7	NRX[7]	W	0	
		D6	NRX[6]	W	0	
		D5	NRX[5]	W	0	
		D4	NRX[4]	W	1	
		D3	NRX[3]	W	1	
		D2	NRX[2]	W	1	
		D1	NRX[1]	W	1	
		D0	NRX[0]	W	1	

Note: Unless the register is set via SPI, the register data is set to the initial value.

8.6 05h; Reception PLL Frequency Setting (MSB)

Address	Function	Name		R/W	Initial Value	Description
05h	PLL_RX2	D15	—	W	0	Don't care. (Recommended to set to “0.”)
		D14	—	W	0	Don't care. (Recommended to set to “0.”)
		D13	—	W	0	Don't care. (Recommended to set to “0.”)
		D12	—	W	0	Don't care. (Recommended to set to “0.”)
		D11	—	W	0	Don't care. (Recommended to set to “0.”)
		D10	—	W	0	Don't care. (Recommended to set to “0.”)
		D9	—	W	0	Don't care. (Recommended to set to “0.”)
		D8	—	W	0	Don't care. (Recommended to set to “0.”)
		D7	—	W	0	Don't care. (Recommended to set to “0.”)
		D6	—	W	0	Don't care. (Recommended to set to “0.”)
		D5	—	W	0	Don't care. (Recommended to set to “0.”)
		D4	NRX[20]	W	0	Set the reception PLL frequency (MSB). Set the value of f_{LO} MHz × 125. (f_{LO} is the internal frequency.) **Initial frequency: 5835 MHz** (The initial value of the register is “000Bh.”)
		D3	NRX[19]	W	1	
		D2	NRX[18]	W	0	
		D1	NRX[17]	W	1	
		D0	NRX[16]	W	1	

Note: Unless the register is set via SPI, the register data is set to the initial value.

8.7 06h; Transmission PLL Frequency Setting (LSB)

Address	Function	Name		R/W	Initial Value	Description
06h	PLL_TX1	D15	NTX[15]	W	0	Set the transmission PLL frequency (LSB). Set the value of f_{LO} MHz × 125. (f_{LO} is the internal frequency.) **Initial frequency: 5790 MHz** (The initial value of the register is "0B26h.")
		D14	NTX[14]	W	0	
		D13	NTX[13]	W	0	
		D12	NTX[12]	W	0	
		D11	NTX[11]	W	1	
		D10	NTX[10]	W	0	
		D9	NTX[9]	W	1	
		D8	NTX[8]	W	1	
		D7	NTX[7]	W	0	
		D6	NTX[6]	W	0	
		D5	NTX[5]	W	1	
		D4	NTX[4]	W	0	
		D3	NTX[3]	W	0	
		D2	NTX[2]	W	1	
		D1	NTX[1]	W	1	
		D0	NTX[0]	W	0	

Note: Unless the register is set via SPI, the register data is set to the initial value.

8.8 07h; Transmission PLL Frequency Setting (MSB)

Address	Function	Name		R/W	Initial Value	Description
07h	PLL_TX2	D15	—	W	0	Don't care. (Recommended to set to “0.”)
		D14	—	W	0	Don't care. (Recommended to set to “0.”)
		D13	—	W	0	Don't care. (Recommended to set to “0.”)
		D12	—	W	0	Don't care. (Recommended to set to “0.”)
		D11	—	W	0	Don't care. (Recommended to set to “0.”)
		D10	—	W	0	Don't care. (Recommended to set to “0.”)
		D9	—	W	0	Don't care. (Recommended to set to “0.”)
		D8	—	W	0	Don't care. (Recommended to set to “0.”)
		D7	—	W	0	Don't care. (Recommended to set to “0.”)
		D6	—	W	0	Don't care. (Recommended to set to “0.”)
		D5	—	W	0	Don't care. (Recommended to set to “0.”)
		D4	NTX[20]	W	0	Set the transmission PLL frequency (MSB). Set the value of f_{LO} MHz × 125. (f_{LO} is the internal frequency.) **Initial frequency: 5790 MHz** (The initial value of the register is “000Bh.”)
		D3	NTX[19]	W	1	
		D2	NTX[18]	W	0	
		D1	NTX[17]	W	1	
		D0	NTX[16]	W	1	

Note: Unless the register is set via SPI, the register data is set to the initial value.

8.9 08h; Reset for PLL Block

Address	Function	Name		R/W	Initial Value	Description
08h	PLL_RST	D15	—	W	0	Don't care. (Recommended to set to “0.”)
		D14	—	W	0	Don't care. (Recommended to set to “0.”)
		D13	—	W	0	Don't care. (Recommended to set to “0.”)
		D12	—	W	0	Don't care. (Recommended to set to “0.”)
		D11	—	W	0	Don't care. (Recommended to set to “0.”)
		D10	—	W	0	Don't care. (Recommended to set to “0.”)
		D9	—	W	0	Don't care. (Recommended to set to “0.”)
		D8	—	W	0	Don't care. (Recommended to set to “0.”)
		D7	—	W	0	Don't care. (Recommended to set to “0.”)
		D6	—	W	0	Don't care. (Recommended to set to “0.”)
		D5	—	W	0	Don't care. (Recommended to set to “0.”)
		D4	—	W	0	Don't care. (Recommended to set to “0.”)
		D3	—	W	0	Don't care. (Recommended to set to “0.”)
		D2	—	W	0	Don't care. (Recommended to set to “0.”)
		D1	—	W	0	Don't care. (Recommended to set to “0.”)
		D0	pll_reset	W	0	PLL reset and lock-up operations during register write access. PLL reset register is a trigger to initialize PLL circuit. It is not necessary to clear this bit after the reset operation completes. 1: PLL circuit starts the lock-up. **0: No Operation <Initial value>**

Note: When TC32168FTG starts from Sleep state or the transition between TX state and RX state occurs, the PLL reset is asserted automatically.

8.10 09h; Transmission Power Control

Address	Function	Name		R/W	Initial Value	Description
09h	TX_Power_Control	D15	—	W	0	Don't care. (Recommended to set to “0.”)
		D14	—	W	0	Don't care. (Recommended to set to “0.”)
		D13	—	W	0	Don't care. (Recommended to set to “0.”)
		D12	—	W	0	Don't care. (Recommended to set to “0.”)
		D11	outctrl[11]	W	0	Output power control for transmission. **Initial value: All "0"** For the control level, refer to Table 8-2 and Section 13.
		D10	outctrl[10]	W	0	
		D9	outctrl[9]	W	0	
		D8	outctrl[8]	W	0	
		D7	outctrl[7]	W	0	
		D6	outctrl[6]	W	0	
		D5	outctrl[5]	W	0	
		D4	outctrl[4]	W	0	
		D3	outctrl[3]	W	0	
		D2	outctrl[2]	W	0	
		D1	outctrl[1]	W	0	
		D0	outctrl[0]	W	0	

Note: For the relationship between the register value and the transmission output power, refer to the figure “TX Output Power vs. Register Control Setting” in Section 13.

Note: The control input values of the register outctrl are shown in the following table. The setting of the values which are not shown in the Table 8-2 is prohibited.

Table 8-2 Input value of Register outctrl

Value of Register outctrl[D11,D0]	
111111111111	0xFFF
011111111111	0x7FF
001111111111	0x3FF
000111111111	0x1FF
000011111111	0x0FF
000001111111	0x07F
000000111111	0x03F
000000011111	0x01F
000000001111	0x00F
000000000111	0x007
000000000011	0x003
000000000001	0x001
000000000000	0x000

8.11 0Ah; Modulation and IF Filter Settings

Address	Function	Name		R/W	Initial Value	Description
0Ah	Analog_Settings	D15	—	W	0	Don't care. (Recommended to set to “0.”)
		D14	—	W	0	Don't care. (Recommended to set to “0.”)
		D13	—	W	0	Don't care. (Recommended to set to “0.”)
		D12	—	W	0	Don't care. (Recommended to set to “0.”)
		D11	—	W	0	Don't care. (Recommended to set to “0.”)
		D10	—	W	0	Don't care. (Recommended to set to “0.”)
		D9	—	W	0	Don't care. (Recommended to set to “0.”)
		D8	bw	W	0	Select IF filter band width. **0: Normal <Initial value>** 1: Narrow band width
		D7	ook	W	0	Enable to use the anti-aliasing filter. **0: Use the anti-aliasing filter for ASK <Initial value>** 1: Bypath the filter for OOK
		D6	ph	W	0	Select RSSI peak hold function. **0: Normal <Initial value> This should be selected.** 1: Slow (for the system using less than 128-kbps data)
		D5	—	W	0	Don't care. (Recommended to set to “0.”)
		D4	mr[4]	W	0	Set Modulation index. **Initial value: All "0"** For Modulation index, refer to Section 13.
		D3	mr[3]	W	0	
		D2	mr[2]	W	0	
		D1	mr[1]	W	0	
		D0	mr[0]	W	0	

Note: The register ook sets only using the anti-aliasing filter or not. To select the modulation (ASK/OOK), it is necessary that “Ramp Up/Down Coefficients” are set to the registers rmpup (=16h[D255,D128]) and rmpdwn (=16h[D127,D0]). For the Ramp Up/Down Coefficients, refer to 8.19.

Note: For the relationship between the register value and the modulation index, refer to the figure, “Modulation Index vs. Register Setting Characterisitcs” in Section 13.

8.12 0Bh; Wakeup Sensitivity Setting

This register data is copied to the register for PMU and WAKEUP DET by setting the register wk_reg_wen (= 1C[D8]) to “1.” After copying the data, this register value becomes valid.

Address	Function	Name		R/W	Initial Value	Description
0Bh	Analog_Settings_WU	D15	—	W	0	Don't care. (Recommended to set to “0.”)
		D14	—	W	0	Don't care. (Recommended to set to “0.”)
		D13	—	W	0	Don't care. (Recommended to set to “0.”)
		D12	—	W	0	Don't care. (Recommended to set to “0.”)
		D11	—	W	0	Don't care. (Recommended to set to “0.”)
		D10	—	W	0	Don't care. (Recommended to set to “0.”)
		D9	—	W	0	Don't care. (Recommended to set to “0.”)
		D8	—	W	0	Don't care. (Recommended to set to “0.”)
		D7	—	W	0	Don't care. (Recommended to set to “0.”)
		D6	—	W	0	Don't care. (Recommended to set to “0.”)
		D5	—	W	0	Don't care. (Recommended to set to “0.”)
		D4	—	W	0	Don't care. (Recommended to set to “0.”)
		D3	w_s_set[3]	W	0	Set Wakeup sensitivity.
		D2	w_s_set[2]	W	0	**Initial value: All "0"**
		D1	w_s_set[1]	W	0	**Set the register w_s_set to (0,1,0,1) at the**
		D0	w_s_set[0]	W	0	**operation.**

8.13 10h; Read/Write Data of Transmission/Reception FIFO

The selection of the transmission FIFO or the reception FIFO is determined by the selection of TX state or RX State, respectively. When the transition between TX state and RX state occurs, the data of the register TRXFIFO is cleared automatically.

Address	Function	Name		R/W	Initial Value	Description
10h	TRXFIFO	D2047	txdata_2047	R/W	0	Read data of the reception FIFO/Write data of the transmission FIFO. The length of FIFO data is in the units of 8 bytes. The maximum length is 256 bytes. The length is usually 128 bytes or less. It should be set to the register rxlen (= 17h[D8,D0]). For the details of the register, refer to 8.20. **Initial value: All "0"**
		D2046	txdata_2046	R/W	0	
		D2045	txdata_2045	R/W	0	
		In this address, the 2048-bit continuous data area exists.				
		D10	txdata_10	R/W	0	
		D9	txdata_9	R/W	0	
		D8	txdata_8	R/W	0	
		D7	txdata_7	R/W	0	
		D6	txdata_6	R/W	0	
		D5	txdata_5	R/W	0	
		D4	txdata_4	R/W	0	
		D3	txdata_3	R/W	0	
		D2	txdata_2	R/W	0	
		D1	txdata_1	R/W	0	
		D0	txdata_0	R/W	0	

8.14 11h; Interrupts

When an interrupt occurs, its status can be read by MCU via SPI bus. For the details of the interrupts, refer to 7.11.6.

Address	Function	Name		R/W	Initial Value	Description
11h	INTR_ST	D15	—	R	0	—
		D14	—	R	0	—
		D13	—	R	0	—
		D12	—	R	0	—
		D11	—	R	0	—
		D10	—	R	0	—
		D9	txlen_err	R	0	Transmission frame length is invalid. 0: No errors. / 1: The error occurs.
		D8	post_err	R	0	No postambles are detected. 0: No errors. / 1: The error occurs.
		D7	rx_abort	R	0	Abort sequence is detected. 0: No errors. / 1: The error occurs.
		D6	crc_ng	R	0	CRC check result is not correct. 0: No errors. / 1: The error occurs.
		D5	fm0dec_err	R	0	FM0 decode error occurs. 0: No errors. / 1: The error occurs.
		D4	rxlen_err	R	0	Reception frame length is invalid. 0: No errors. / 1: The error occurs.
		D3	flag_err	R	0	No frame start marks are detected. 0: No errors. / 1: The error occurs.
		D2	pre_err	R	0	No preambles are detected. 0: No errors. / 1: The error occurs.
		D1	tx_done	R	0	Transmission of a frame completes. 0: No errors. / 1: The error occurs.
		D0	rx_ready	R	0	A frame is received. 0: No errors. / 1: The error occurs.

Note: The interrupt register should be cleared as soon as possible to wait for the next interrupt. Otherwise, the register is overwritten at the generation of the next interrupt, which cannot detect the interrupt.

8.15 12h; Interrupt Mask Setting

Address	Function	Name		R/W	Initial Value	Description
12h	INTR_MK	D15	—	W	0	Don't care. (Recommended to set to “0.”)
		D14	—	W	0	Don't care. (Recommended to set to “0.”)
		D13	—	W	0	Don't care. (Recommended to set to “0.”)
		D12	—	W	0	Don't care. (Recommended to set to “0.”)
		D11	—	W	0	Don't care. (Recommended to set to “0.”)
		D10	—	W	0	Don't care. (Recommended to set to “0.”)
		D9	txlen_err_mask	W	0	Set an interrupt mask. **0: Mask is not set for the interrupt. <Initial value>** 1: Mask is set for the interrupt
		D8	post_err_mask	W	0	
		D7	rx_abort_mask	W	0	
		D6	crc_ng_mask	W	0	
		D5	fm0dec_err_mask	W	0	
		D4	rxlen_err_mask	W	0	
		D3	flag_err_mask	W	0	
		D2	pre_err_mask	W	0	
		D1	tx_done_mask	W	0	
		D0	rx_ready_mask	W	0	

Note: When an interrupt mask is set, the corresponding output of INTRPT/DIO is masked. But the interrupt operation itself executes. The MCU which controls ETC system containing TC32168FTG can use the status of the interrupt via SPI bus.

8.16 13h; Interrupt Clearing

When a bit in the register is set to “1”, the corresponding interrupt is cleared.

Address	Function	Name		R/W	Initial Value	Description
13h	INTR_CLR	D15	—	W	0	Don't care. (Recommended to set to “0.”)
		D14	—	W	0	Don't care. (Recommended to set to “0.”)
		D13	—	W	0	Don't care. (Recommended to set to “0.”)
		D12	—	W	0	Don't care. (Recommended to set to “0.”)
		D11	—	W	0	Don't care. (Recommended to set to “0.”)
		D10	—	W	0	Don't care. (Recommended to set to “0.”)
		D9	txlen_err_clr	W	0	Selection to clear an interrupt. **0: No operation = Not clear <Initial value>** 1: Clear
		D8	post_err_clr	W	0	
		D7	rx_abort_clr	W	0	
		D6	crc_ng_clr	W	0	
		D5	fm0dec_err_clr	W	0	
		D4	rxlen_err_clr	W	0	
		D3	flag_err_clr	W	0	
		D2	pre_err_clr	W	0	
		D1	tx_done_clr	W	0	
		D0	rx_ready_clr	W	0	

Note: The interrupt register should be cleared as soon as possible to wait for the next interrupt. Otherwise, the register is overwritten at the generation of the next interrupt, which cannot detect the interrupt.

Note: The output of INTRPT/DIO pin turns to “0” after all asserted interrupts are cleared.

8.17 14h; Inversion of Interrupt Pin Output

Address	Function	Name		R/W	Initial Value	Description
14h	INTR_INV	D15	—	W	0	Don't care. (Recommended to set to “0.”)
		D14	—	W	0	Don't care. (Recommended to set to “0.”)
		D13	—	W	0	Don't care. (Recommended to set to “0.”)
		D12	—	W	0	Don't care. (Recommended to set to “0.”)
		D11	—	W	0	Don't care. (Recommended to set to “0.”)
		D10	—	W	0	Don't care. (Recommended to set to “0.”)
		D9	—	W	0	Don't care. (Recommended to set to “0.”)
		D8	—	W	0	Don't care. (Recommended to set to “0.”)
		D7	—	W	0	Don't care. (Recommended to set to “0.”)
		D6	—	W	0	Don't care. (Recommended to set to “0.”)
		D5	—	W	0	Don't care. (Recommended to set to “0.”)
		D4	—	W	0	Don't care. (Recommended to set to “0.”)
		D3	—	W	0	Don't care. (Recommended to set to “0.”)
		D2	—	W	0	Don't care. (Recommended to set to “0.”)
		D1	—	W	0	Don't care. (Recommended to set to “0.”)
		D0	int_inv	W	0	Set the inversion of INTRPT/DIO pin output (used for an interrupt). **0: “1” active at an interrupt assertion. <Initial value>** 1: “0” active at an interrupt assertion.

Note: The output signal polarity of INTRPT/DIO pin at an interrupt assertion is set by this register.

8.18 15h; Transmission and Reception Bit Rate Settings

Address	Function	Name		R/W	Initial Value	Description
15h	BIT_RATE	D15	—	W	0	Don't care. (Recommended to set to “0.”)
		D14	—	W	0	Don't care. (Recommended to set to “0.”)
		D13	—	W	0	Don't care. (Recommended to set to “0.”)
		D12	—	W	0	Don't care. (Recommended to set to “0.”)
		D11	—	W	0	Don't care. (Recommended to set to “0.”)
		D10	—	W	0	Don't care. (Recommended to set to “0.”)
		D9	txrate[1]	W	0	Transmission data rate setting. txrate[1:0] = **00: 512 kbps <Initial value>** 01: 256 kbps 10: 128 kbps 11: 125 kbps
		D8	txrate[0]	W	0	
		D7	—	W	0	Don't care. (Recommended to set to “0.”)
		D6	—	W	0	Don't care. (Recommended to set to “0.”)
		D5	—	W	0	Don't care. (Recommended to set to “0.”)
		D4	—	W	0	Don't care. (Recommended to set to “0.”)
		D3	—	W	0	Don't care. (Recommended to set to “0.”)
		D2	—	W	0	Don't care. (Recommended to set to “0.”)
		D1	—	W	0	Don't care. (Recommended to set to “0.”)
		D0	rxrate	W	1	Reception data rate setting. 0: 512 kbps **1: 256 kbps <Initial value>**

8.19 16h; Ramp Up and Down Coefficient Setting

The recommended ramp up and ramp down coefficients should be set to the proper registers at the start of the operation of the system. The coefficient values above have been optimized.

It should be notified that the ramp up and the ramp down coefficients of ASK and OOK are different. In the table below, both coefficients are shown. When the modulation type is selected, such settigs should be also done as the ramp up and the ramp down coefficients and the enable or disable of the anti-aliasing filter.

In this address, the 256-byte continuous data area exists. The modulated output signal of TC32168FTG is shaped by the ramp up and ramp down coefficients in this address, and the digital signal is converted to the analog one. The frequency of the step of the ramp up and the ramp down is 16.384 MHz. Each coefficient is set individually. The data write to the register is done in units of byte. 8-bit (= 1 byte) area is assigned to each coefficient, but the 3 bits of MSB of a write data should be fixed to (0,0,0) in advance. So each register is written with 8-bit data, but the MSB 3 bits are ignored and only the lower 5 bits should be the actual data.

Those registers can be read to confirm the written data. The registers are read in units of byte. The 3 bits of MSB return (0,0,0), and the lower 5 bits return the written data. So the written value can be checked.

Address	Function	Name		R/W	Initial Value	Description	
						Recommended value for ASK	Recommended value for OOK
16h	RAMP FIFO	D255..248	rmpup[79:75]	R/W	1F	**Set to “1F.”**	**Set to “1F.”**
		D247..240	rmpup[74:70]	R/W	1F	**Set to “1F.”**	**Set to “1F.”**
		D239..232	rmpup[69:65]	R/W	1E	**Set to “1F.”**	**Set to “1F.”**
		D231..224	rmpup[64:60]	R/W	1C	**Set to “1F.”**	**Set to “1F.”**
		D223..216	rmpup[59:55]	R/W	1A	**Set to “1F.”**	**Set to “1F.”**
		D215..208	rmpup[54:50]	R/W	17	**Set to “1F.”**	**Set to “1F.”**
		D207..200	rmpup[49:45]	R/W	14	**Set to “1F.”**	**Set to “1F.”**
		D199..192	rmpup[44:40]	R/W	11	**Set to “1F.”**	**Set to “1F.”**
		D191..184	rmpup[39:35]	R/W	0E	**Set to “1F.”**	**Set to “1F.”**
		D183..176	rmpup[34:30]	R/W	0B	**Set to “1B.”**	**Set to “1F.”**
		D175..168	rmpup[29:25]	R/W	08	**Set to “12.”**	**Set to “1F.”**
		D167..160	rmpup[24:20]	R/W	05	**Set to “0E.”**	**Set to “1F.”**
		D159..152	rmpup[19:15]	R/W	03	**Set to “08.”**	**Set to “1F.”**
		D151..144	rmpup[14:10]	R/W	01	**Set to “07.”**	**Set to “1F.”**
		D143..136	rmpup[9:5]	R/W	00	**Set to “03.”**	**Set to “1F.”**
		D135..128	rmpup[4:0]	R/W	00	**Set to “00.”**	**Set to “1F.”**
		D127..120	rmpdwn[79:75]	R/W	00	**Set to “00.”**	**Set to “00.”**
		D119..112	rmpdwn[74:70]	R/W	00	**Set to “00.”**	**Set to “00.”**
		D111..104	rmpdwn[69:65]	R/W	01	**Set to “00.”**	**Set to “00.”**
		D103..96	rmpdwn[64:60]	R/W	03	**Set to “00.”**	**Set to “00.”**
		D95..88	rmpdwn[59:55]	R/W	05	**Set to “00.”**	**Set to “00.”**
		D87..80	rmpdwn[54:50]	R/W	08	**Set to “00.”**	**Set to “00.”**
		D79..72	rmpdwn[49:45]	R/W	0B	**Set to “00.”**	**Set to “00.”**
		D71..64	rmpdwn[44:40]	R/W	0E	**Set to “00.”**	**Set to “00.”**
		D63..56	rmpdwn[39:35]	R/W	11	**Set to “00.”**	**Set to “00.”**
		D55..48	rmpdwn[34:30]	R/W	14	**Set to “03.”**	**Set to “00.”**
		D47..40	rmpdwn[29:25]	R/W	17	**Set to “07.”**	**Set to “00.”**
		D39..32	rmpdwn[24:20]	R/W	1A	**Set to “08.”**	**Set to “00.”**
		D31..24	rmpdwn[19:15]	R/W	1C	**Set to “0E.”**	**Set to “00.”**
		D23..16	rmpdwn[14:10]	R/W	1E	**Set to “12.”**	**Set to “00.”**
		D15..8	rmpdwn[9:5]	R/W	1F	**Set to “1B.”**	**Set to “00.”**
		D7..0	rmpdwn[4:0]	R/W	1F	**Set to “1F.”**	**Set to “00.”**

Note: The followings are examples of the register data.
1B = (0,0,0,1,1,0,1,1)
07 = (0,0,0,0,0,1,1,1)
The 3 bits of MSB are usually (0,0,0).

Note: Actual modulated output waveform may not match the signal designed by the register setting due to the distortion in the modulation circuit. The waveform designed by the register setting should be tuned to be close to the desired modulation waveform carefully with monitoring the output waveform. For the designed waveform, refer to Figure 8-1.

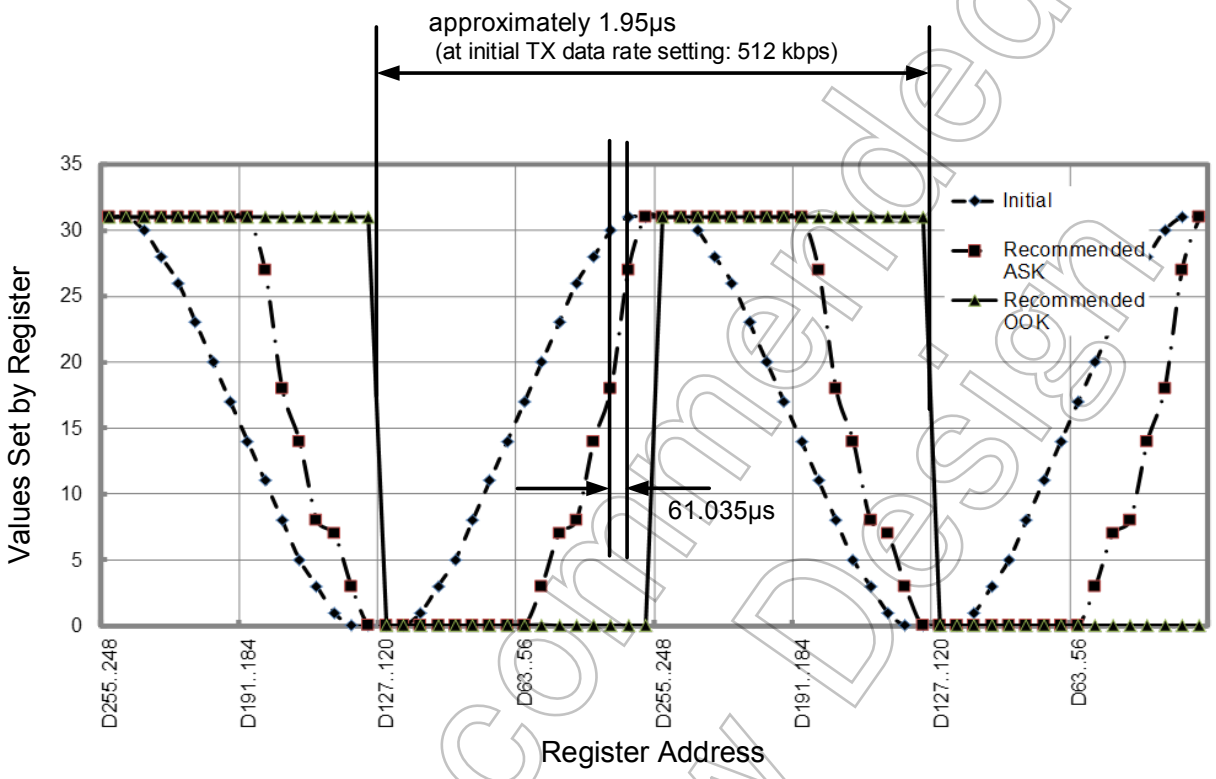


Figure 8-1 Waveform designed by Ramp up and Ramp down coefficient registers

8.20 17h; Maximum Reception Data Length Setting

When a reception frame (a reception data length) is longer than this setting value, rx_len_err interrupt is asserted in the register rx_len_err (= 11h[D4]).

Address	Function	Name		R/W	Initial Value	Description
17h	MAX_RXDATALEN	D15	—	W	0	Don't care. (Recommended to set to “0.”)
		D14	—	W	0	Don't care. (Recommended to set to “0.”)
		D13	—	W	0	Don't care. (Recommended to set to “0.”)
		D12	—	W	0	Don't care. (Recommended to set to “0.”)
		D11	—	W	0	Don't care. (Recommended to set to “0.”)
		D10	—	W	0	Don't care. (Recommended to set to “0.”)
		D9	—	W	0	Don't care. (Recommended to set to “0.”)
		D8	rxlen[8]	W	0	Set the maximum reception data length. **Initial value: 128 bytes** Register rxlen = (0,1,0,0,0,0,0,0,0)
		D7	rxlen[7]	W	1	
		D6	rxlen[6]	W	0	
		D5	rxlen[5]	W	0	
		D4	rxlen[4]	W	0	
		D3	rxlen[3]	W	0	
		D2	rxlen[2]	W	0	
		D1	rxlen[1]	W	0	
		D0	rxlen[0]	W	0	

8.21 18h; Setting of Cycle Number of Wakeup Detection

The initial value "3" means that WAKE_UP pin outputs "1" when the rising edge of the fourth cycle of 14-kHz Wakeup signal is detected. This register data is copied to the register for PMU and WAKEUP DET by setting the register wk_reg_wen (= 1C[D8]) to "1." After copying the data, this register value becomes valid.

Address	Function	Name		R/W	Initial Value	Description
18h	WK_DET_NUM	D15	—	W	0	Don't care. (Recommended to set to "0.")
		D14	—	W	0	Don't care. (Recommended to set to "0.")
		D13	—	W	0	Don't care. (Recommended to set to "0.")
		D12	—	W	0	Don't care. (Recommended to set to "0.")
		D11	—	W	0	Don't care. (Recommended to set to "0.")
		D10	—	W	0	Don't care. (Recommended to set to "0.")
		D9	—	W	0	Don't care. (Recommended to set to "0.")
		D8	—	W	0	Don't care. (Recommended to set to "0.")
		D7	—	W	0	Don't care. (Recommended to set to "0.")
		D6	—	W	0	Don't care. (Recommended to set to "0.")
		D5	—	W	0	Don't care. (Recommended to set to "0.")
		D4	—	W	0	Don't care. (Recommended to set to "0.")
		D3	wk_num[3]	W	0	Set the cycle number of Wakeup detection. The number of the rectangular waves for Wakeup (= 14 kHz Wakeup signal, refer to Figure 7-3) is checked. When the number of received Wakeup signal becomes larger than the value in the register wk_num, the output of WAKE_UP pin changes from "0" to "1." **Initial value: 03 = (0,0,1,1)**
		D2	wk_num[2]	W	0	
		D1	wk_num[1]	W	1	
		D0	wk_num[0]	W	1	

8.22 19h; Wakeup Operation Selection

This register data is copied to the register for PMU and WAKEUP DET by setting the register wk_reg_wen (= 1C[D8]) to “1.” After copying the data, this register value becomes valid.

Address	Function	Name		R/W	Initial Value	Description
19h	WakeUP_REG_SETS	D15	—	W	0	Don't care. (Recommended to set to “0.”)
		D14	—	W	0	Don't care. (Recommended to set to “0.”)
		D13	—	W	0	Don't care. (Recommended to set to “0.”)
		D12	—	W	0	Don't care. (Recommended to set to “0.”)
		D11	—	W	0	Don't care. (Recommended to set to “0.”)
		D10	—	W	0	Don't care. (Recommended to set to “0.”)
		D9	—	W	0	Don't care. (Recommended to set to “0.”)
		D8	—	W	0	Don't care. (Recommended to set to “0.”)
		D7	—	W	0	Don't care. (Recommended to set to “0.”)
		D6	—	W	0	Don't care. (Recommended to set to “0.”)
		D5	—	W	0	Don't care. (Recommended to set to “0.”)
		D4	—	W	0	Don't care. (Recommended to set to “0.”)
		D3	—	W	0	Don't care. (Recommended to set to “0.”)
		D2	—	W	0	Don't care. (Recommended to set to “0.”)
		D1	—	W	0	Don't care. (Recommended to set to “0.”)
		D0	autowk	W	0	Select Wakeup operation. **0: Normal Wakeup operation <Initial value>** 1: Auto Wakeup operation

8.23 1Ah; Calibration Start of Wakeup Detection Timer

The frequency of the internal oscillator for PMU and WAKEUP DET in one product is different from another one. In order to detect Wakeup signal correctly, it is necessary to calibrate the internal oscillator frequency.
The calibration takes 120 μs at maximum.

Address	Function	Name		R/W	Initial Value.	Description
1Ah	CAL_WakeUp	D15	—	W	0	Don't care. (Recommended to set to “0.”)
		D14	—	W	0	Don't care. (Recommended to set to “0.”)
		D13	—	W	0	Don't care. (Recommended to set to “0.”)
		D12	—	W	0	Don't care. (Recommended to set to “0.”)
		D11	—	W	0	Don't care. (Recommended to set to “0.”)
		D10	—	W	0	Don't care. (Recommended to set to “0.”)
		D9	—	W	0	Don't care. (Recommended to set to “0.”)
		D8	wkcal_en	W	0	Start the calibration of Wakeup detection timer. It operates during register write access. **0: No Operation <Initial value>** 1: Start the calibration of the internal oscillator for Wakeup waveform detection.
		D7	—	W	0	Don't care. (Recommended to set to “0.”)
		D6	—	W	0	Don't care. (Recommended to set to “0.”)
		D5	—	W	0	Don't care. (Recommended to set to “0.”)
		D4	—	W	0	Don't care. (Recommended to set to “0.”)
		D3	—	W	0	Don't care. (Recommended to set to “0.”)
		D2	—	W	0	Don't care. (Recommended to set to “0.”)
		D1	—	W	0	Don't care. (Recommended to set to “0.”)
		D0	—	W	0	Don't care. (Recommended to set to “0.”)

8.24 1Bh; Clearing of WAKE_UP Pin Output

Address	Function	Name		R/W	Initial Value.	Description
1Bh	WakeUP_CLR	D15	—	W	0	Don't care. (Recommended to set to “0.”)
		D14	—	W	0	Don't care. (Recommended to set to “0.”)
		D13	—	W	0	Don't care. (Recommended to set to “0.”)
		D12	—	W	0	Don't care. (Recommended to set to “0.”)
		D11	—	W	0	Don't care. (Recommended to set to “0.”)
		D10	—	W	0	Don't care. (Recommended to set to “0.”)
		D9	—	W	0	Don't care. (Recommended to set to “0.”)
		D8	wk_clr	W	0	Clear WAKE_UP pin output during register write access. **0: No Operation <Initial value>** 1: Clear (Set WAKE_UP pin output from "1" to "0".)
		D7	—	W	0	Don't care. (Recommended to set to “0.”)
		D6	—	W	0	Don't care. (Recommended to set to “0.”)
		D5	—	W	0	Don't care. (Recommended to set to “0.”)
		D4	—	W	0	Don't care. (Recommended to set to “0.”)
		D3	—	W	0	Don't care. (Recommended to set to “0.”)
		D2	—	W	0	Don't care. (Recommended to set to “0.”)
		D1	—	W	0	Don't care. (Recommended to set to “0.”)
		D0	—	W	0	Don't care. (Recommended to set to “0.”)

Note: This register should be set just before entering Sleep state.

8.25 1Ch; Data Write to Wakeup Register

The registers for PMU and WAKEUP DET keep the copied data during Sleep state in TC32168FTG. When ETC system MCU starts booting, the resisters for PMU and WAKEUP DET are recommended to be refreshed by this register to keep Wakeup operation settings.

Address	Function	Name		R/W	Initial Value	Description
1Ch	Wakeup_reg_write	D15	—	W	0	Don't care. (Recommended to set to “0.”)
		D14	—	W	0	Don't care. (Recommended to set to “0.”)
		D13	—	W	0	Don't care. (Recommended to set to “0.”)
		D12	—	W	0	Don't care. (Recommended to set to “0.”)
		D11	—	W	0	Don't care. (Recommended to set to “0.”)
		D10	—	W	0	Don't care. (Recommended to set to “0.”)
		D9	—	W	0	Don't care. (Recommended to set to “0.”)
		D8	wk_reg_wen	W	0	The data of the registers w_s_set (= 0Bh[D3,D0]) / wk_num (= 18h[D3,D0]) / autowk (= 19h[D0]) are copied to the registers for PMU and WAKEUP DET during register write access. **0: No Operation <Initial value>** 1: Copy operation
		D7	—	W	0	Don't care. (Recommended to set to “0.”)
		D6	—	W	0	Don't care. (Recommended to set to “0.”)
		D5	—	W	0	Don't care. (Recommended to set to “0.”)
		D4	—	W	0	Don't care. (Recommended to set to “0.”)
		D3	—	W	0	Don't care. (Recommended to set to “0.”)
		D2	—	W	0	Don't care. (Recommended to set to “0.”)
		D1	—	W	0	Don't care. (Recommended to set to “0.”)
		D0	—	W	0	Don't care. (Recommended to set to “0.”)

8.26 1Dh; Byte Length Setting of Reception Data

After the interrupt is asserted by the register rx_ready (= 11h[D0]), the data length of the reception FIFO is written to this register. Before reading data in the reception FIFO, ETC system MCU should know the length of the reception frame.

Address	Function	Name		R/W	Initial Value	Description
1Dh	RXdata_len	D15	—	R	0	—
		D14	—	R	0	—
		D13	—	R	0	—
		D12	—	R	0	—
		D11	—	R	0	—
		D10	—	R	0	—
		D9	—	R	0	—
		D8	rxdatalen[8]	R	0	The byte length of the reception data in the reception FIFO can be checked.
		D7	rxdatalen[7]	R	0	
		D6	rxdatalen[6]	R	0	
		D5	rxdatalen[5]	R	0	
		D4	rxdatalen[4]	R	0	
		D3	rxdatalen[3]	R	0	
		D2	rxdatalen[2]	R	0	
		D1	rxdatalen[1]	R	0	
		D0	rxdatalen[0]	R	0	

8.27 2Ch; CRC Setting

Those CRC parameters are applied to both the reception and the transmission.
Those parameter values are not kept in Sleep state.
This register setting is for Beijing's ETC system.
Refer to 7.12.9 and 7.15.

Address	Function	Name		R/W	Initial Value	Description
2Ch	CRC_INI	D15	—	R/W	0	Set to “0.”
		D14	—	R/W	0	Set to “0.”
		D13	—	R/W	0	Set to “0.”
		D12	—	R/W	0	Set to “0.”
		D11	—	R/W	0	Set to “0.”
		D10	—	R/W	0	Set to “0.”
		D9	—	R/W	0	Set to “0.”
		D8	—	R/W	0	Set to “0.”
		D7	—	R/W	0	Set to “0.”
		D6	—	R/W	0	Set to “0.”
		D5	—	R/W	0	Set to “0.”
		D4	—	R/W	0	Set to “0.”
		D3	crc_inv	R/W	0	Inverse CRC result. 0: Inverse. 1: Not inverse.
		D2	lsb_msb	R/W	0	Select the transmission way of MSB first or LSB first. (At reading the transmission FIFO or writing the reception FIFO) 0: LSB first 1: MSB first
		D1	crc_pol	R/W	0	Select CRC generating polynomial. 0: $X^{16} + X^{12} + X^5 + X^0$ 1: $X^{16} + X^{15} + X^2 + X^0$
		D0	crc_ini	R/W	0	Select the initial value of CRC shift register. 0: Initial value is all "1." 1: Initial value is all "0."

8.28 36h; Reception Detection Timer Setting

The FIFO data which are received and stored in the register TRXFIFO are cleared by the timeout (2 ms) of the frame start mark interrupt and the postamble detection interrupt.
To avoid this, the register dettimer_dis should be set to "1."

Address	Function	Name		R/W	Initial Value	Description
36h	RX_DET_TIMER_DIS	D15	—	R/W	0	—
		D14	—	R/W	0	—
		D13	—	R/W	0	—
		D12	—	R/W	0	—
		D11	—	R/W	0	—
		D10	—	R/W	0	—
		D9	—	R/W	0	—
		D8	—	R/W	0	—
		D7	—	R/W	0	—
		D6	—	R/W	0	—
		D5	—	R/W	0	—
		D4	—	R/W	0	—
		D3	—	R/W	0	—
		D2	—	R/W	0	—
		D1	—	R/W	0	—
		D0	dettimer_dis	R/W	0	Control the reception detection timer. Control the timer to disable the frame start mark interrupt and the postamble interrupt. When this register is set to "1," those interrupts cannot be asserted after 2-ms duration defined by the timer has passed. **0: Enable the timer. <Initial value>** 1: Disable the timer. The interrupt status can be read from the registers flag_err (= 11h[D3]) and post_err (= 11h[D8]). Refer to 8.14.

8.29 3Ch; Tests Selection

Address	Function	Name		R/W	Initial Value	Description
3Ch	TEST SEL	D15	—	W	0	Set to “0.”
		D14	—	W	0	Set to “0.”
		D13	—	W	0	Set to “0.”
		D12	—	W	0	Set to “0.”
		D11	—	W	0	Set to “0.”
		D10	—	W	0	Set to “0.”
		D9	—	W	0	Set to “0.”
		D8	—	W	0	Set to “0.”
		D7	—	W	0	Set to “0.”
		D6	—	W	0	Set to “0.”
		D5	txbit_sel[1]	W	0	Generate a transmission data pattern of FM0 coding for test. Refer to Table 8-3. **00: Disable the test operation <Initial value>**
		D4	txbit_sel[0]	W	0	
		D3	—	W	0	Set to “0.”
		D2	fir_sel[2]	W	0	Select a transmission data for test. Refer to Table 8-3. **000: Disable the test operation <Initial value>**
		D1	fir_sel[1]	W	0	
		D0	fir_sel[0]	W	0	

The test data selection in the table above is shown in the Table 8-3.

Table 8-3 Test operations for ASK at TX state

Register: fir_sel	Register: txbit_sel	Generated transmission data pattern of RF ASK signal
000	00	Disable the test operation <Initial value> (Used for an actual ETC system.)
	11	PN9 in FM0 coding (Used for ACPR measurement.)
001	don't care	All "0" of ASK without FM0 coding (a continuous waveform)
010	don't care	All "1" of ASK without FM0 coding (a continuous waveform)
101	don't care	ASK signal has been FM0-modulated using the data input from INTRPT/DIO pin.
011 / 110 / 111	don't care	Prohibited.

Note: To use the data input from INTRPT/DIO pin, both registers dio_en and dio_sel should be set to "1". For the pin usage, refer to 8.4.
Note: The bit rate of the communication data is set in the register txrate (= 15h[D9,D8]). (Refer to 8.18.)

8.30 3Dh; Frequency Setting of Wakeup Detection

The frequency tolerance of 14-kHz Wakeup signal is controlled by this register.

Address	Function	Name		R/W	Initial Value	Description
3Dh	WK_FREQ_SET	D15	—	W	0	Set to “0.”
		D14	—	W	0	Set to “0.”
		D13	—	W	0	Set to “0.”
		D12	—	W	0	Set to “0.”
		D11	wk_high_det[3]	W	0	Set Wakeup detection pulse frequency to 20 kHz or more. **Initial value: (0,1,0,1)**
		D10	wk_high_det[2]	W	1	
		D9	wk_high_det[1]	W	0	
		D8	wk_high_det[0]	W	1	
		D7	—	W	0	Set to “0.”
		D6	—	W	0	Set to “0.”
		D5	—	W	0	Set to “0.”
		D4	wk_low_det[4]	W	1	Set Wakeup detection pulse frequency to 10 kHz or less. **Initial value: (1,1,1,1,0)**
		D3	wk_low_det[3]	W	1	
		D2	wk_low_det[2]	W	1	
		D1	wk_low_det[1]	W	1	
		D0	wk_low_det[0]	W	0	

8.31 3Eh; Wakeup Frequency Register Control

The registers for PMU and WAKEUP DET keep the copied data during Sleep state in TC32168FTG.

Address	Function	Name		R/W	Initial Value	Description
3Eh	WK_FREQ_SET_WEN	D15	—	W	0	Set to “0.”
		D14	—	W	0	Set to “0.”
		D13	—	W	0	Set to “0.”
		D12	—	W	0	Set to “0.”
		D11	—	W	0	Set to “0.”
		D10	—	W	0	Set to “0.”
		D9	—	W	0	Set to “0.”
		D8	wk_freq_wen	W	0	Write the frequency data to Wakeup register. The data in the registers wk_high_det (= 3D[D11,D8]) and wk_low_det (= 3Dh(D4,D0]) are copied to the registers for PMU and WAKEUP DET during register write access. **0: No Operation <Initial value>** 1: Copy operation
		D7	—	W	0	Set to “0.”
		D6	—	W	0	Set to “0.”
		D5	—	W	0	Set to “0.”
		D4	—	W	0	Set to “0.”
		D3	—	W	0	Set to “0.”
		D2	—	W	0	Set to “0.”
		D1	—	W	0	Set to “0.”
		D0	—	W	0	Set to “0.”

8.32 43h; Reception FIFO Register Clearing

This function is useful after the FIFO data has been overwritten in RX state.
If this register is set to "1," the data in the register TRXFIFO (= 10h[D2047,D0]) are cleared.

Address	Function	Name		R/W	Initial Value.	Description
43h	RX FIFO CLEAR	D15	—	W	0	Set to "0."
		D14	—	W	0	Set to "0."
		D13	—	W	0	Set to "0."
		D12	—	W	0	Set to "0."
		D11	—	W	0	Set to "0."
		D10	—	W	0	Set to "0."
		D9	—	W	0	Set to "0."
		D8	rxfifocls	W	0	Clear the reception FIFO register during register write access. **0: No Operation = Not clear <Initial value>** 1: Clear
		D7	—	W	0	Set to "0."
		D6	—	W	0	Set to "0."
		D5	—	W	0	Set to "0."
		D4	—	W	0	Set to "0."
		D3	—	W	0	Set to "0."
		D2	—	W	0	Set to "0."
		D1	—	W	0	Set to "0."
		D0	—	W	0	Set to "0."

8.33 56h; Crystal Oscillator Trimming

Address	Function	Name		R/W	Initial Value	Description
56h	XOSC_TRIM	D15	—	W	0	Set to “0.”
		D14	—	W	0	Set to “0.”
		D13	—	W	0	Set to “0.”
		D12	—	W	0	Set to “0.”
		D11	xosc_ctrim[3]	W	0	Crystal oscillator trimming. **Initial value: All “0”**
		D10	xosc_ctrim[2]	W	0	
		D9	xosc_ctrim[1]	W	0	
		D8	xosc_ctrim[0]	W	0	
		D7	—	W	0	Set to “0.”
		D6	—	W	0	Set to “0.”
		D5	—	W	0	Set to “0.”
		D4	—	W	0	Set to “0.”
		D3	—	W	0	Set to “0.”
		D2	—	W	0	Set to “0.”
		D1	—	W	0	Set to “0.”
		D0	—	W	0	Set to “0.”

Note: Toshiba measures the electrical data of TC32168FTG using the crystal oscillator “FCX-04-32.768MHz-J20997 (RIVER ELETEC CORPORATION).”

Note: When this crystal oscillator is used, the recommended value of the register xosc_ctrim (= 56h[D11,D8]) is (0,0,0,1).

8.34 5Ch; Reception CRC Selection

This register setting is used for Beijing's ETC system.
For the details, refer to 7.15 and Figure 7-23.

Address	Function	Name		R/W	Initial Value	Description
5Ch	SEL_RX_CRC	D15	—	R/W	0	Set to “0.”
		D14	—	R/W	0	Set to “0.”
		D13	—	R/W	0	Set to “0.”
		D12	—	R/W	0	Set to “0.”
		D11	—	R/W	0	Set to “0.”
		D10	—	R/W	0	Set to “0.”
		D9	crc_rslt_b	R	0	Check the result of the CRC whose initial value is all “0.” 0: Correct. / 1: Not correct.
		D8	crc_rslt_a	R	0	Check the result of the CRC whose initial value is all “1.” 0: Correct. / 1: Not correct.
		D7	—	R/W	0	Set to “0.”
		D6	—	R/W	0	Set to “0.”
		D5	—	R/W	0	Set to “0.”
		D4	—	R/W	0	Set to “0.”
		D3	—	R/W	0	Set to “0.”
		D2	—	R/W	0	Set to “0.”
		D1	—	R/W	0	Set to “0.”
		D0	sel_crc	R/W	0	Select CRC operation. 0: Logical OR is done for the result of the CRC whose initial value is all “0” and the result of the CRC whose initial value is all “1.” 1: Select the result of the CRC whose initial value is all “1.” The logical OR value is not used. The CRC result is configured by the register crc_ini (= 2Ch[D0]). The default setting of this register is consistent with China's ETC standard

8.35 5Dh; CRC Data Information

The data of this register is used for Beijing's ETC system.
For the details, refer to 7.15.

Address	Function	Name		R/W	Initial Value	Description
5Dh	CRC_DATA	D15	crc_data[15]	R	0	Reception CRC data
		D14	crc_data[14]	R	0	
		D13	crc_data[13]	R	0	
		D12	crc_data[12]	R	0	
		D11	crc_data[11]	R	0	
		D10	crc_data[10]	R	0	
		D9	crc_data[9]	R	0	
		D8	crc_data[8]	R	0	
		D7	crc_data[7]	R	0	
		D6	crc_data[6]	R	0	
		D5	crc_data[5]	R	0	
		D4	crc_data[4]	R	0	
		D3	crc_data[3]	R	0	
		D2	crc_data[2]	R	0	
		D1	crc_data[1]	R	0	
		D0	crc_data[0]	R	0	

9. Absolute Maximum Ratings

The absolute maximum ratings of a semiconductor device are a set of specified parameter values which must not be exceeded during operation, even for an instant.
If any of these ratings would be exceeded during operation, the device electrical characteristics may be irreparably altered, and the reliability and lifetime of the device can no longer be guaranteed.
Moreover, the operations with exceeding the ratings may cause break down, damage, or degradation to any other equipment.
Applications using the device should be designed such that each rating will never be exceeded in any operating conditions.
Before using this product, and creating and designing a system, the precautions and the use conditions in this document should be referred to and complied with.

Table 9-1 Absolute maximum ratings

(Unless otherwise specified, Ta = 25°C and the referenced voltage is the ground.)

Item	Symbol / Pin Name	Rating	Unit
Supply voltage	V_{DD}	-0.2 to 6.0	V
Input voltage (I/O pin)	MOSI, SPICLK, CSN, INTRPT/DIO, TXRX, CE, and TEST	-0.2 to 6.0	V
Signal Input voltage	RF_IN	10	dBm
Power dissipation	P_D	250	mW
Storage temperature range	Tstg	-40 to 125	°C

10. Operation Range

The operation range indicates the conditions under which the basic operation is possible even when there is some fluctuation in the electrical characteristics of a product.

Table 10-1 Operation Range

(Unless otherwise specified, Ta = 25°C and the referenced voltage is the ground.)

Item	Symbol / Pin Name	Rating	Unit
Supply voltage	V_{DD}	1.8 to 3.6	V
Operation temperature range The specifications are not guaranteed.	Ta	-40 to 85	°C
High level output current	I_{OH}; MISO, INTRPT/DIO, and WAKE_UP	0 to 10	μA
Low level output current	I_{OL}; MISO, INTRPT/DIO, and WAKE_UP	-10 to 0	μA

11. Electrical Characteristics

Table 11-1 Electrical characteristics

(Unless otherwise specified, V_{DD}= 3.0 V, f = 5830 MHz, Ta = 25°C and the referenced voltage is the ground.)

Item	Symbol	Test Condition	Min	Typ.	Max	Unit
Current						
Current consumption in Sleep 1 (Room temperature)	I_{DDS1}	V_{DD} = 3.0 V and Ta = +25°C in Sleep state	—	4.4	6	μA
Current consumption in Sleep 2 (High temperature)	I_{DDS2}	V_{DD} = 3.0 V and Ta = +85°C in Sleep State	—	4.9	10	μA
Current consumption in RX state	I_{DDR}	RX state, V_{DD} = 3.0 V, and RF input level = 0 dBm,	—	31	37	mA
Current consumption in TX state	I_{DDT}	TX State, V_{DD} = 3.0 V, PN9, and FM0 modulation. Set the register: mr (= 0Ah[D4,D0]) to (0,0,0,0,0). Set the register: outctrl (= 09h[D11,D0]) to all "1."	—	40	50	mA
Pin Input (TXRX, INTRPT/DIO [as Input], CSN, SPICLK, MOSI, and CE)						
Input high voltage	V_{IH}	—	V_{DD} × 0.8	V_{DD}	V_{DD} + 0.2	V
Input low voltage	V_{IL}	—	-0.2	GND	0.3	V
Leakage current 1 (Input high voltage)	I_{IH}	Pin input = V_{DD}	-3	0	3	μA
Leakage current 2 (Input low voltage)	I_{IL}	Pin input = GND	-3	0	3	μA
Pin Output (INTRPT/DIO [as Output], MISO, and WAKE_UP)						
Output high voltage	V_{OH}	—	V_{DD} × 0.8	V_{DD}	—	V
Output low voltage	V_{OL}	—	-0.3	GND	0.3	V
Drive current 1 (Source current: Output high voltage)	I_{OH}	The source current at "$V_{OH} \geq V_{DD} \times 0.8$."	200	—	—	μA
Drive current 2 (Sink current: Output low voltage)	I_{OL}	The sink current at "$V_{OL} \leq +0.3$ V."	—	—	200	μA
Crystal Oscillator						
Crystal oscillator frequency	f_{XOSC}	—	—	32.768	—	MHz
Crystal oscillator startup time	t_{XOSC}	Startup time of the system clock from the switching of CE pin (L → H). Assumed the use of "FCX-04-32.768MHz-J20997" (RIVER ELETEC CORPORATION).	—	—	500	μs
Load capacitance	C_L	Load capacitance to keep the startup time which is 500 μs or less. (Refer to Section 12.)	6	—	7	pF
SPI Bus						
SPI operating frequency range	f_{SPI}	Clock frequency to transfer data,	0.05	8	8.192	MHz
Frequency Synthesizer						
Available frequency range	f_{VFO}	$f_{VFO} = f_{VCO} \times 2$ (f_{VCO} = VCO frequency)	5725	5835	5875	MHz
Frequency switching time	t_{LOCK}	$f_{LOCK} \leq$ +/-100 kHz, Duration from the change (setting to “1”) of the register pll_reset to the completion of PLL frequency locking.	—	25	30	μs
Frequency step	f_{STEP}	Minimum frequency step of PLL	—	5	—	MHz

Item	Symbol	Test Condition	Min	Typ.	Max	Unit
Wakeup						
Operating frequency range	$f_{OPR}WU$	At RF_IN pin	5775	5830	5845	MHz
Frequency range of Wakeup pulse	$f_{PR}WU$	At RF_IN pin, Pulse frequency to enter Wakeup state surely.	(10.4)	14	(15.7)	kHz
Wakeup sensitivity 1	WU sens1	Ta = +25°C and Modulation index = 1.00. Set the register w_s_set (= 0Bh[D3,D0]) to (0,1,0,1).	-51	-49	-46	dBm
Wakeup sensitivity 2	WU sens2	Ta = +85°C and Modulation index = 1.00. Set the register w_s_set to (0,1,0,1).	-50	-48	-45	dBm
Wakeup maximum input level 1	WU max1	Ta = +25°C and Modulation index = 0.75, Set the register w_s_set to (0,1,0,1).	2	7	—	dBm
Wakeup maximum input level 2	WU max2	Ta = +85°C and Modulation index = 0.75, Set the register w_s_set to (0,1,0,1).	2	8	—	dBm
Data Reception						
Reception operating frequency range	$f_{OPR}RX$	Frequency at RF_IN pin. Set the internal frequency to the reception frequency +/-5 MHz.	5725	5830	5875	MHz
Reception sensitivity 1	RX sens1	IF filter = Normal, Reception BER = 10×10^{-6}, Ta = +25°C, Internal frequency = 5835 MHz, and Modulation index = 0.80	(-66)	-64.5	-60	dBm
Reception sensitivity 2	RX sens2	IF filter = Normal, Reception BER = 10×10^{-6}, Ta = +85°C, Internal frequency = 5835 MHz, and Modulation index = 0.80	(-62)	-61	-58	dBm
Reception maximum input level 1	RX max1	IF filter = Normal, Reception BER = 10×10^{-6}, Ta = +25°C, Internal frequency = 5835 MHz, and Modulation index = 0.80	-9	-5	(-4)	dBm
Reception maximum input level 2	RX max2	IF filter = Normal, Reception BER = 10×10^{-6}, Ta = -40 °C, Internal frequency = 5835 MHz, and Modulation index = 0.80	-10	-6	(-5)	dBm
Leakage Power 1	P_{OFF}-OUT	At RFOUT2 pin in RX state.	—	-62	-59	dBm
Leakage Power 2	P_{OFF}-IN	At RF_IN pin in RX state.	—	-60	-50	dBm
RSSI output voltage 1	$V_{RSSI}1$	RF input level = -60 dBm at RF_IN pin. CW	0.52	0.60	0.66	V
RSSI output voltage 2	$V_{RSSI}2$	RF input level = -40 dBm at RF_IN pin. CW	0.80	0.85	0.90	V
RSSI output voltage 3	$V_{RSSI}3$	RF input level = -20 dBm at RF_IN pin. CW	1.06	1.12	1.18	V
RSSI output voltage 4	$V_{RSSI}4$	RF input level = 0 dBm at RF_IN pin. CW	1.10	1.17	1.24	V
RSSI linearity	L_{RSSI}	Average slope of RSSI between $V_{RSSI}3$ and $V_{RSSI}2$.	11	14	17	mV/dBm
VRSSI current performance	I_{RSSI}	When the RSSI output voltage is 0.75 V and RSSI pin has no loads. The swings exceeding RSSI output voltage is +/-50 mV or less.	-45	0	45	μA

Item	Symbol	Test Condition	Min	Typ.	Max	Unit
Data Transmission						
Transmission operating frequency range	f_{OPR}TX	f_{OPR}TX = f_{VFO} (fVCO = VCO frequency)	5725	5790	5875	MHz
Maximum RF output power 1	P_{OUTMAX}S1	Single output of RFOUT2 pin. Set the maximum output power (Set the register outctrl (= 09h[D11,D0]) to all "1."). CW. Ta = + 25°C and Transmission frequency = 5790 MHz,	0	2	—	dBm
Maximum RF output power 2	P_{OUTMAX}S2	Single output of RFOUT2 pin. Set the maximum output power (Set the register outctrl (= 09h[D11,D0]) to all "1."). CW. Ta = + 85°C and Transmission frequency = 5790 MHz,	-2	0	—	dBm
Maximum RF output power 3	P_{OUTMAX}D3	Simultaneous outputs of RFOUT1 and 2 pins. Set the maximum output power (Set the register outctrl to all "1."). CW. Ta = + 25°C and Transmission frequency = 5790 MHz,	3	5	—	dBm
Maximum RF output power 4	P_{OUTMAX}D4	Simultaneous outputs of RFOUT1 and 2 pins. Set the maximum output power (Set the register outctrl to all "1."). CW. Ta = + 85°C and Transmission frequency = 5790 MHz,	1	3	—	dBm
Minimum RF output power 1	P_{OUTMIN}S1	Single output of RFOUT2 pin. Set the minimum output power (Set the register outctrl (= 09h[D11,D0]) to all "0."). CW. Ta = + 25°C and Transmission frequency = 5790 MHz,	—	-6	-5	dBm
Minimum RF output power 2	P_{OUTMIN}S2	Single output of RFOUT2 pin. Set the minimum output power (Set the register outctrl (= 09h[D11,D0]) to all "0."). CW. Ta = + 85°C and Transmission frequency = 5790 MHz,	—	-7	-6	dBm
Minimum RF output power 3	P_{OUTMIN}D3	Simultaneous outputs of RFOUT1 and 2 pins. Set the minimum output power (Set the register outctrl to all "0."). CW. Ta = + 25°C and Transmission frequency = 5790 MHz,	—	-3	-2	dBm
Minimum RF output power 4	P_{OUTMIN}D4	Simultaneous outputs of RFOUT1 and 2 pins. Set the minimum output power (Set the register outctrl to all "0."). CW. Ta = + 85°C and Transmission frequency = 5790 MHz,	—	-4	-3	dBm
Modulation rate frequency 1	f_{MOD}1	Transmission data rate setting = 512 kbps (Set the register txrate (= 15h[D9,D8]) to (0,0).). Set the recommended ramp up/down coefficients.	—	512	—	kHz
Modulation rate frequency 2	f_{MOD}2	Transmission data rate setting = 256 kbps (Set the register txrate to (0,1).). Set the recommended ramp up/down coefficients.	—	256	—	kHz
Occupied band width	OBW	Transmission data rate setting = 512 kbps (Set the register txrate to (0,0).). Set ASK recommended ramp up/down coefficients. 99 % occupied frequency band.	—	1.4	2.2	MHz
Adjacent channel power ratio	ACPR	Transmission data rate setting = 512 kbps (Set the register txrate to (0,0).). Set ASK recommended ramp up/down coefficients. Frequency offset = +/-10 MHz. Set the register mr (=	—	-45	-40	dBc

Item	Symbol	Test Condition	Min	Typ.	Max	Unit
		0Ah[D4,D0]) to (0,0,0,0,0).				
Transmission eye pattern (Time ratio)	EYE T	Time axis. Transmission data rate setting = 512 kbps (Set the register txrate to (0,0).). Set ASK recommended ramp up/down coefficients.	80	97	100	%
Transmission eye pattern (Amplitude ratio)	EYE A	Amplitude axis. Transmission data rate setting = 512 kbps (Set the register txrate to (0,0).). Set ASK recommended ramp up/down coefficients.	80	97	100	%
Modulation index 1	MOD INDEX1	Transmission data rate setting = 512 kbps (Set the register txrate to (0,0).). Set ASK recommended ramp up/down coefficients. Set the register mr to (0,0,1,0,1). (Set Modulation index to 0.85.)	0.80	0.85	0.90	—
Modulation index 2	MOD INDEX2	Transmission data rate setting = 512 kbps (Set the register txrate to (0,0).). Set ASK recommended ramp up/down coefficients.. Set the register mr to (0,1,0,0,1). (Set Modulation index to 0.70.)	0.65	0.70	0.75	—
Modulation index 3	MOD INDEX3	Transmission data rate setting = 512 kbps (Set the register txrate to (0,0).). Set OOK. (Set the register ook (= 0Ah[D7]) to "1.") Set OOK recommended ramp up/down coefficients.	0.95	0.98	1.00	—
Spurious level 1	Spr.1	Spurious frequency = Transmission frequency +/-32.768 MHz (32.768 MHz = XOSC frequency). Set the maximum output power. (Set the register outctrl to all "1."). CW. At RFOUT2 pin. Set the register mr to (0,0,0,0,0).	—	-80	-60	dBc
Spurious level 2	Spr.2	Spurious frequency = Transmission frequency +/-16.384 MHz (16.384 MHz is used for the phase competition.) Set the maximum output power. (Set the register outctrl to all "1."). CW. At RFOUT2 pin. Set the register mr to (0,0,0,0,0).	—	-60	-52	dBc
Spurious level 3	Spr.3	Spurious frequency = Transmission frequency/2 (Half of Transmission frequency = VCO frequency). Set the maximum output power. (Set the register outctrl to all "1."). CW. At RFOUT2 pin. Set the register mr to (0,0,0,0,0).	—	-60	-52	dBc
Spurious level 4	Spr.4	Spurious frequency = Transmission frequency × 1.5 (It is the third harmonic of VCO frequency.) Set the maximum output power. (Set the register outctrl to all "1."). CW. At RFOUT2 pin. Set the register mr to (0,0,0,0,0).	—	-64	-58	dBc
Spurious level 5	Spr.5	Frequency components other than the above. Set the maximum output power. (Set the register outctrl to all "1."). CW. At RFOUT2 pin. Set the register mr to (0,0,0,0,0).	—	-25	-15	dBm

Note: "—" = Not specified

Note: CW is "Continuous Wave."

Note: The values enclosed in parentheses are reference data.

Note: The value of f_{VFO} is equal to that of f_{LO} (the internal frequency).

12. Typical Measurement Circuit

The components illustrated in the following test circuit are used only to check the characteristics of this product. Toshiba does not guarantee that these components will prevent malfunction or failure in a particular application system.

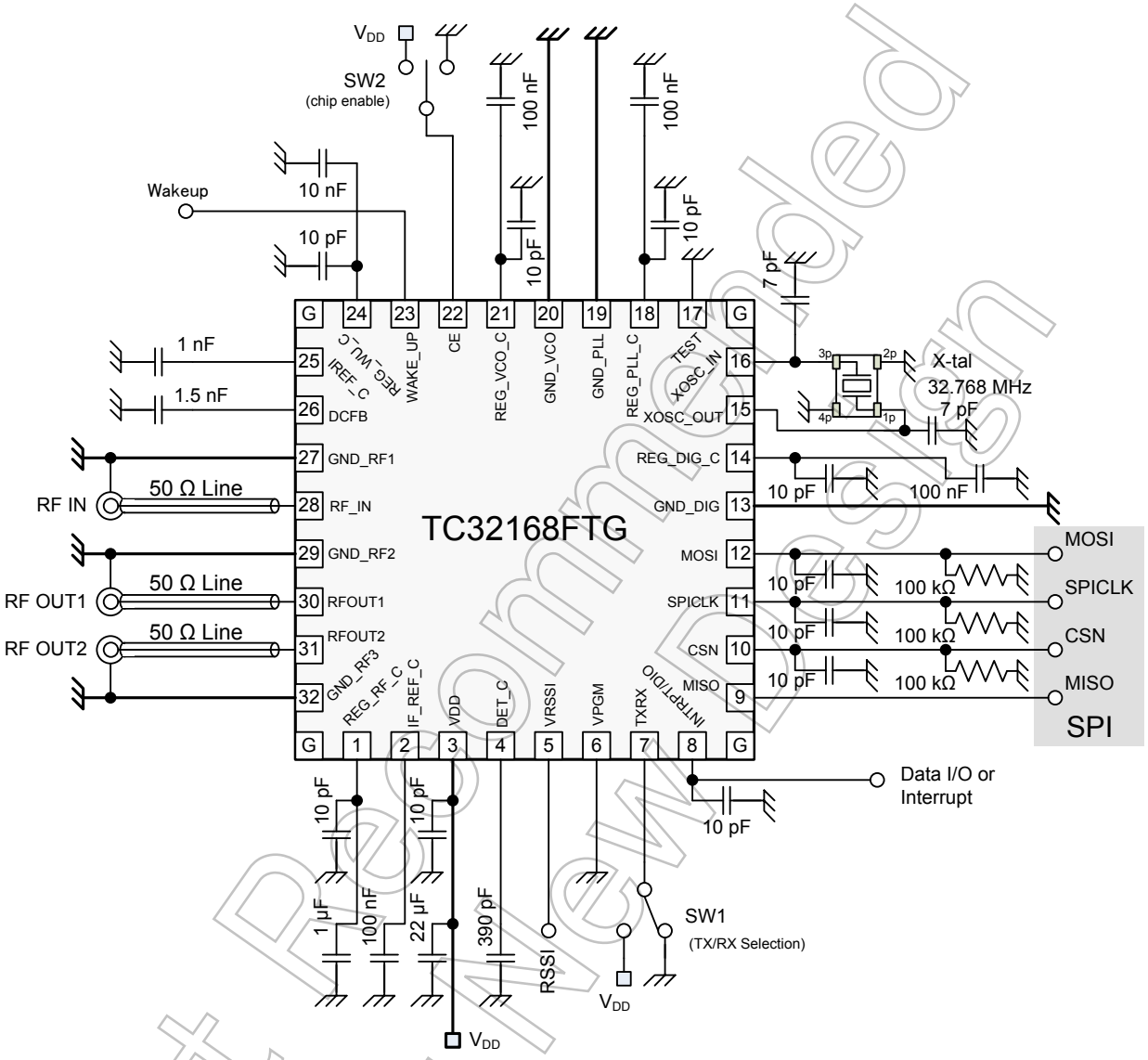


Figure 12-1 Typical Measurement Circuit of TC32168FTG

Note: In this circuit, the crystal oscillator "FCX-04-32.768MHz-J20997 (RIVER ELETEC CORPORATION)" is supposed to be used.

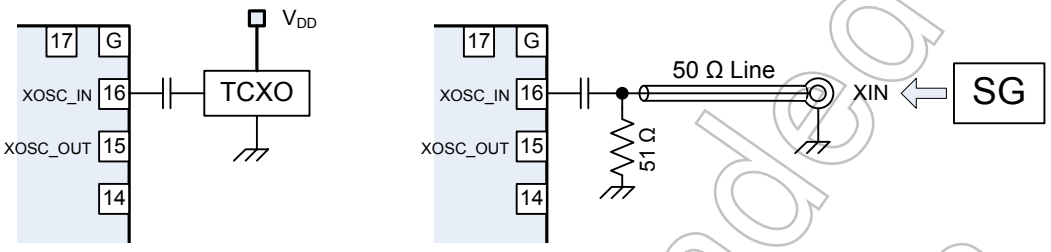
Note: The selection of Transmission or Reception is controlled by SW1. In the figure, Reception is selected.

Note: The operation of the chip enable is controlled by SW2. For the setting of SW2, refer to the flowcharts in 7.12.

Note: G pins at the four corners of this package are connected to the substrate of this IC internally. Those pins are recommended to be connected to GND on a printed-circuit board.

Note; The characteristics of IREF_C and DCFB pins are affected by the values of the connecting capacitors, respectively. A ceramic capacitor should be connected to each pin. Pay attention to condensation or dust to avoid the leak current.

When TCXO or an external signal generator is used, refer to Figure 12-2. The output of TCXO should be connected to XOSC_IN pin via a capacitor to cut DC voltage component, as shown in (a). And XOSC_OUT pin should be open. To use TCXO, any settings by SPI bus or specific pins are not necessary. It is not necessary to check its drive performance and impedance, either.
When an external signal generator is used, a 50-Ω impedance line should be connected to the capacitor to cut DC voltage component, as shown in (b). XOSC_OUT pin should be open.
The frequency accuracy of either TCXO or an external signal generator depends on its own characteristics.

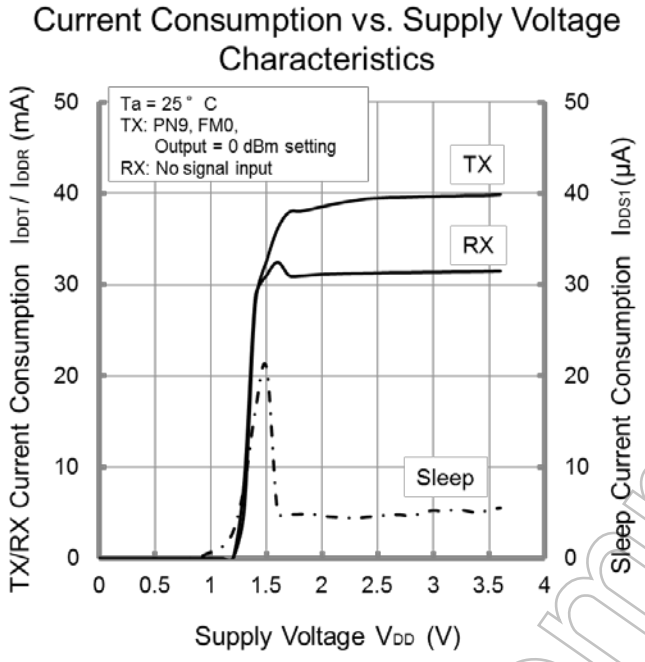


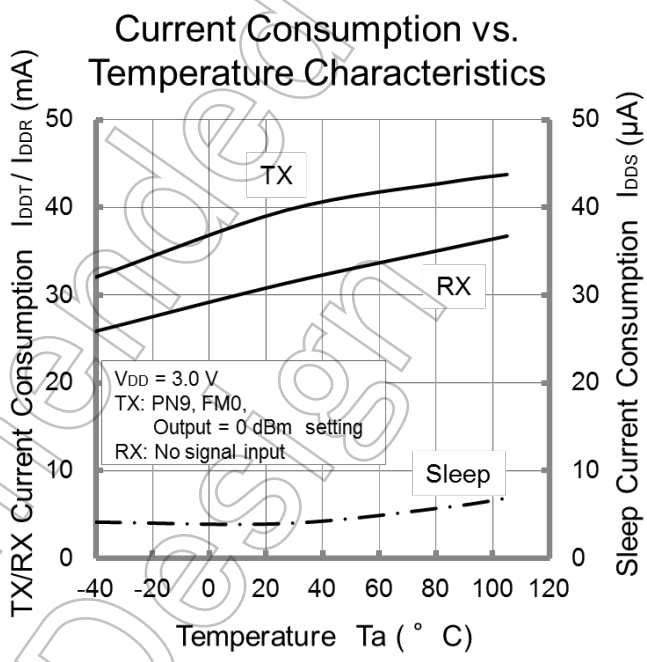
(a) (b)

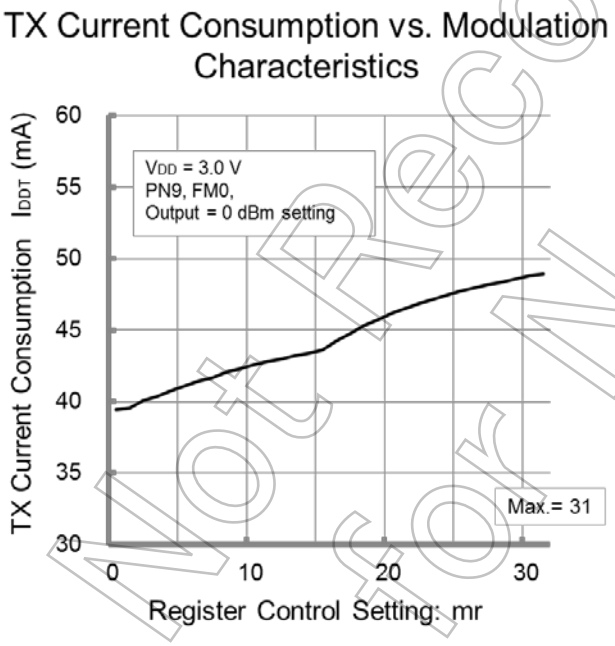
Figure 12-2 Measurement Circuit using TCXO or External signal generator

13. Reference Data

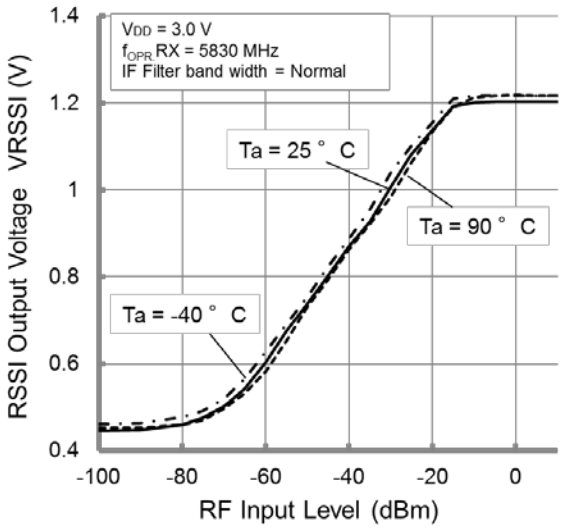
The temperature characteristics are acquired using Toshiba evaluation board "TC32168FTG ver1.0 hyoka." The crystal oscillator "FCX-04-32.768MHz-J20997 (RIVER ELETEC CORPORATION)" is used in those measurements. The operation is not guaranteed out of the ranges shown in the electrical characteristics



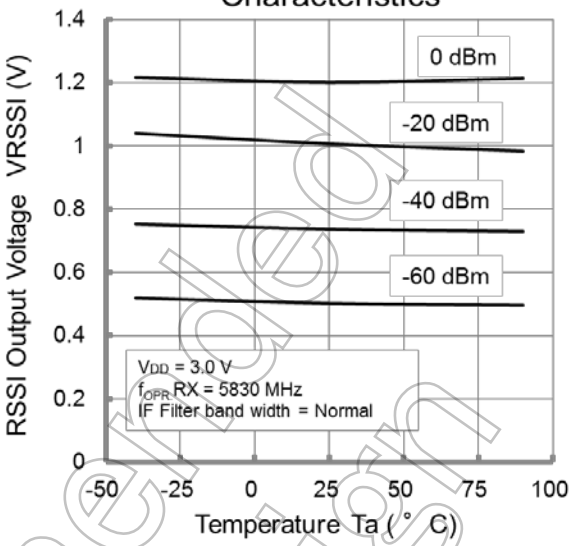




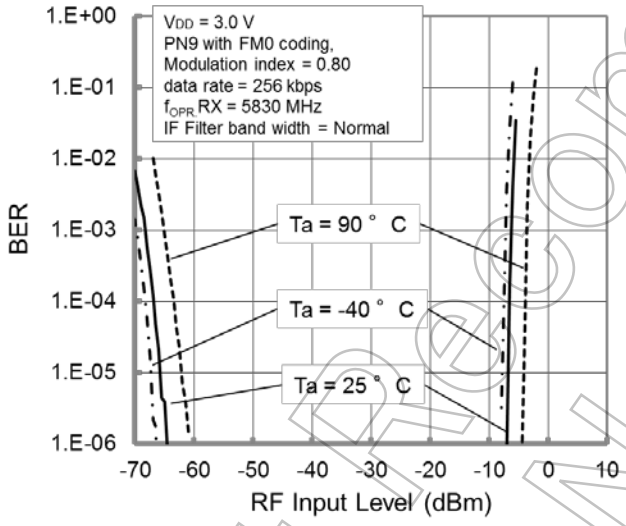
RSSI Output Voltage vs. Input Level Characteristics



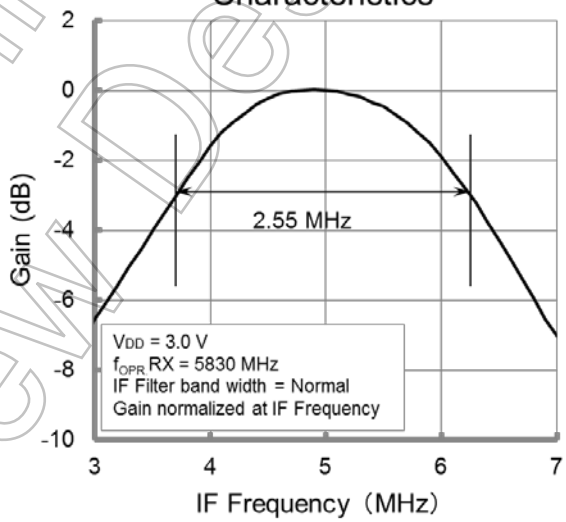
RSSI vs. Temperature Characteristics



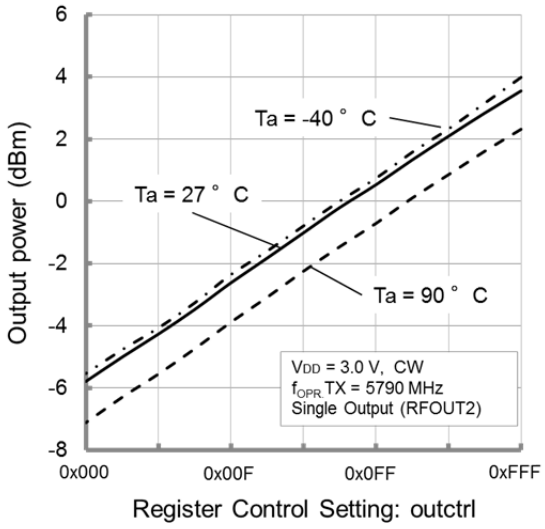
BER vs. RF Input Level Characteristics



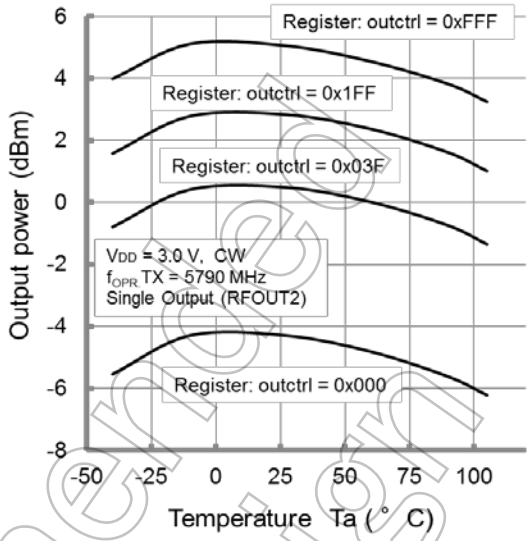
BPF vs. IF Frequency Characteristics



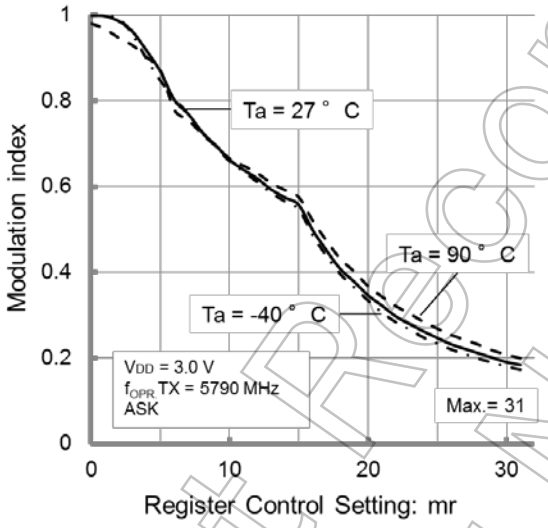
TX Output Power vs.
Register Control Setting



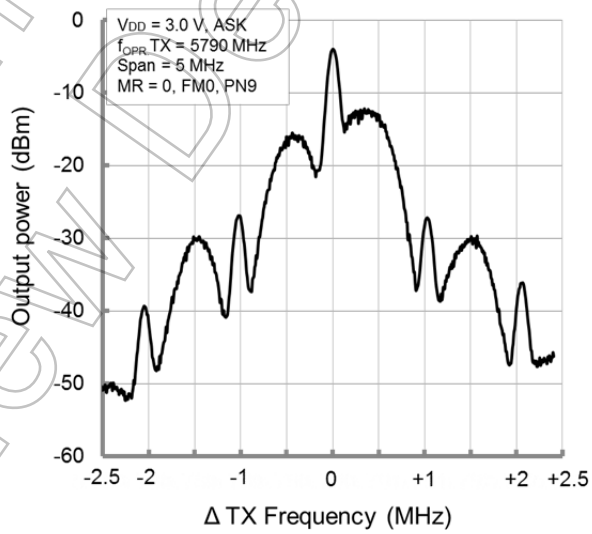
TX Output Power vs.
Temperature Characteristics



Modulation index vs.
Register Setting Characteristics



ASK Waveform Spectrum Characteristics



14. Example of Evaluation Circuit

Toshiba does not guarantee the operation of this evaluation circuit. When a production design is done, the design and the designed product should be evaluated carefully.

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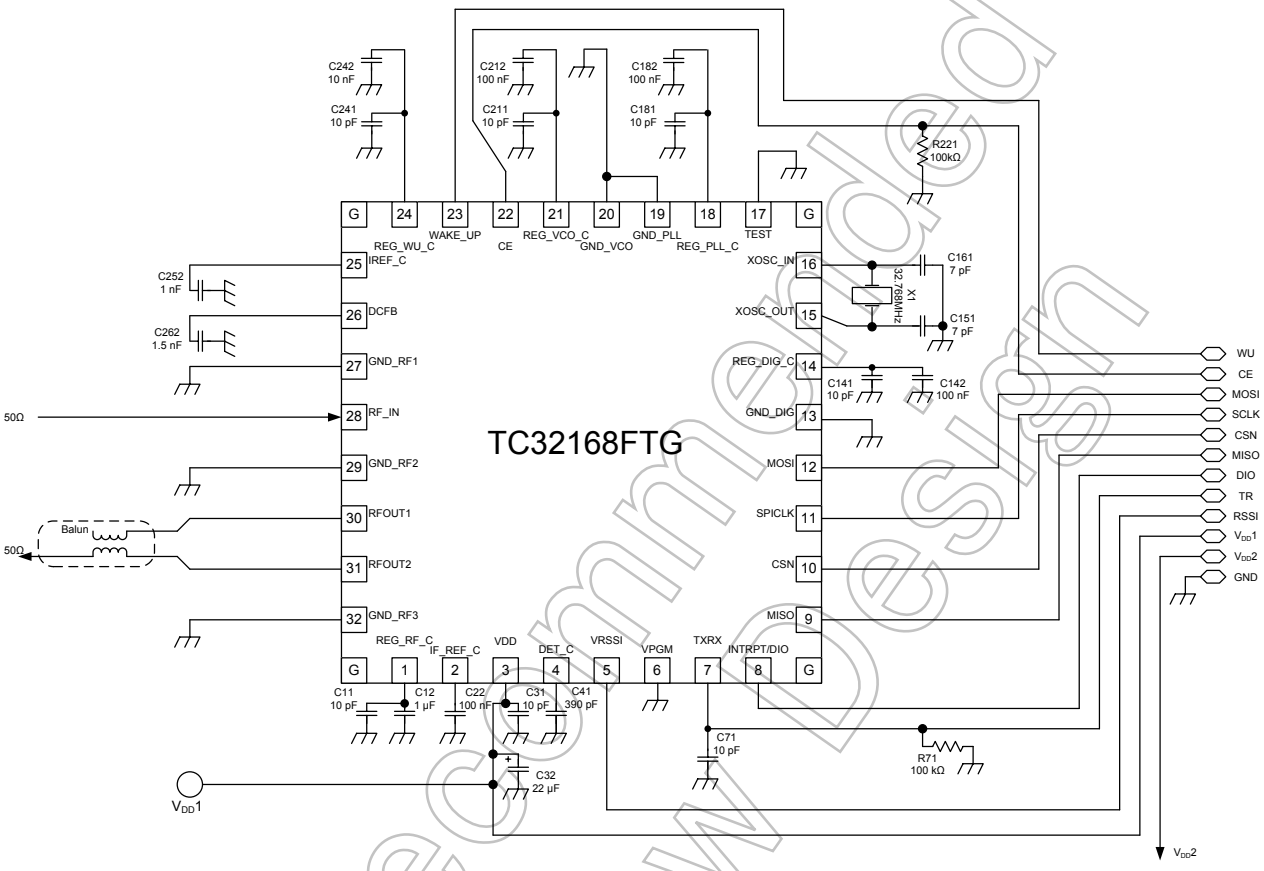


Figure 14-1 Example of Evaluation Circuit

Note: In this circuit, the crystal oscillator "FCX-04-32.768MHz-J20997 (RIVER ELETEC CORPORATION)" is supposed to be used.

Note: G pins at the four corners of this package are connected to the substrate of this IC internally. Those pins are recommended to be connected to GND on a printed-circuit board.

Note: In the circuit above, “Balun” converts balanced signal to unbalanced one. An appropriate Balun should be selected and checked according to the antenna or other RF circuit elements.

15. Application Circuit (Reference)

This is an example of an ETC system using TC32168FTG. Toshiba does not guarantee this application circuit example as a production design. When a production design is done, the design and the designed product should be evaluated carefully.

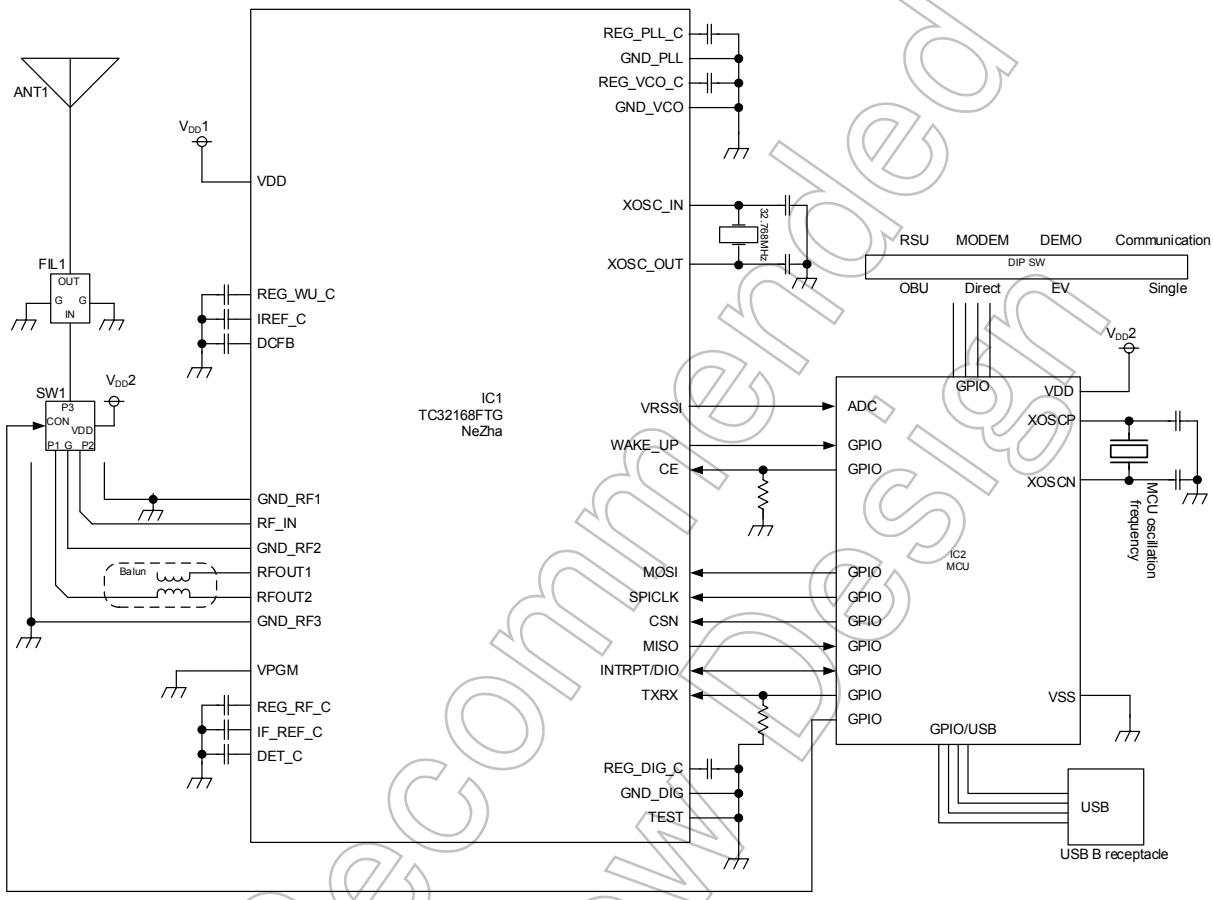


Figure 15-1 Example of ETC system using TC32168FTG

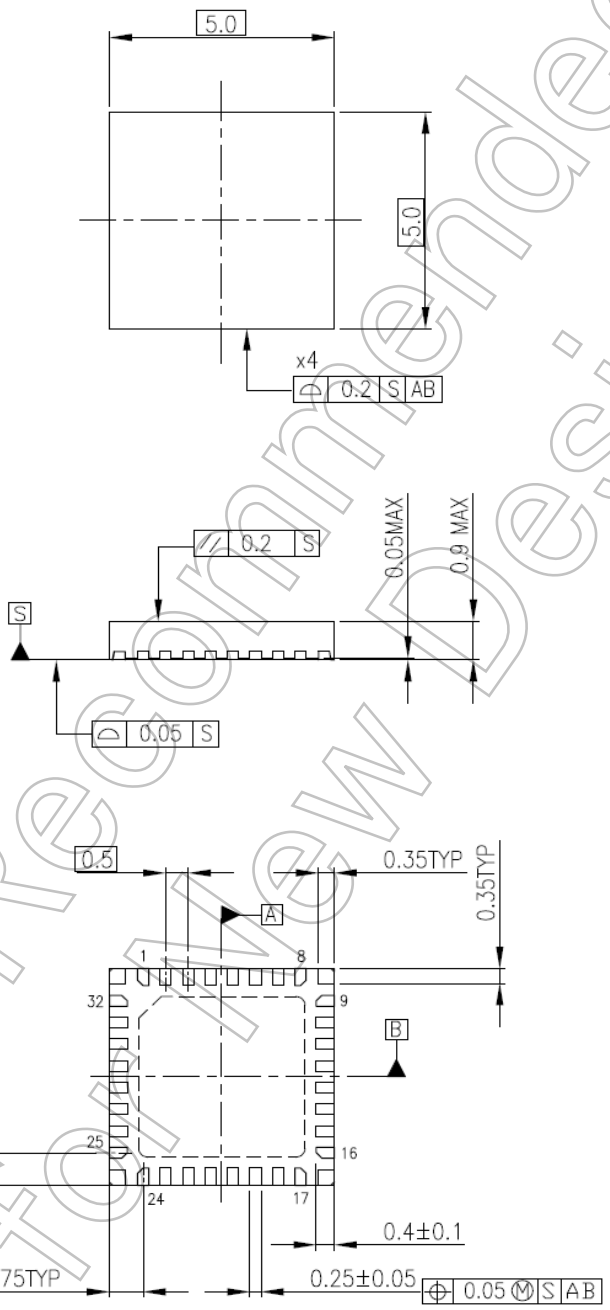
Note: In the figure, the system clock frequency of MCU is not specified. An appropriate frequency should be adopted for the system according to its specifications.

16. Package Figure

16.1 Package Dimensions

Package Type: P-VQFN32-0505-0.50-002

"Unit: mm"



Weight: 0.08g (Typ.)

Figure 16-1 Package dimensions

These drawings are used for explanation. About undescribed or detailed information of the package, please contact Toshiba sales.

16.2 Marking

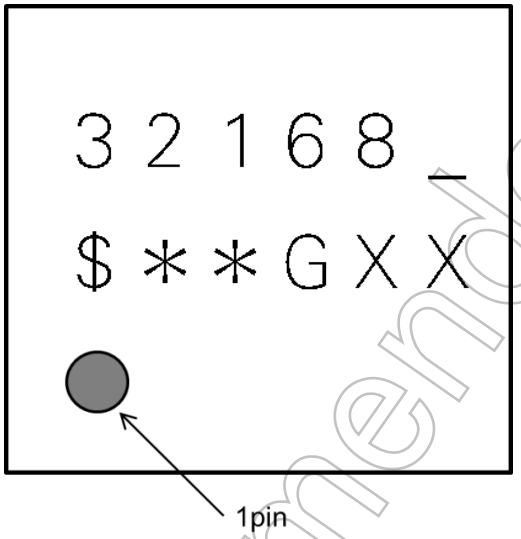


Figure 16-2 Marking

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