TPD7104AF
Application note

Description

TPD7104AF is a high-side gate driver IC for N-channel MOSFETs with 12 V power supply. The MOSFET is driven by an internal charge pump circuit. By selecting the optimum MOSFET for the operating condition, a high-side switch with suitable specifications can be configured for systems handling a wide range of currents. This IC is equipped with a power reverse connection protection function in addition to a load short protection function and a diagnostic function, all of which contribute to improved system safety. Additionally, it is available in a compact PS-8 surface-mount package (2.9 mm * 2.8 mm), enabling system miniaturization.

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1. Product overview

The TPD7104AF is a high-side gate driver IC for N-channel MOSFETs, designed for applications such as semiconductor relays and load switches. By selecting the most suitable MOSFET for the system, the IC can accommodate a wide range of applications. This IC incorporates power reverse connection protection and load short-circuit (overcurrent) detection circuits.

2. Application circuit example

2.1. Application example of load switch circuit (disable reverse polarity protection)

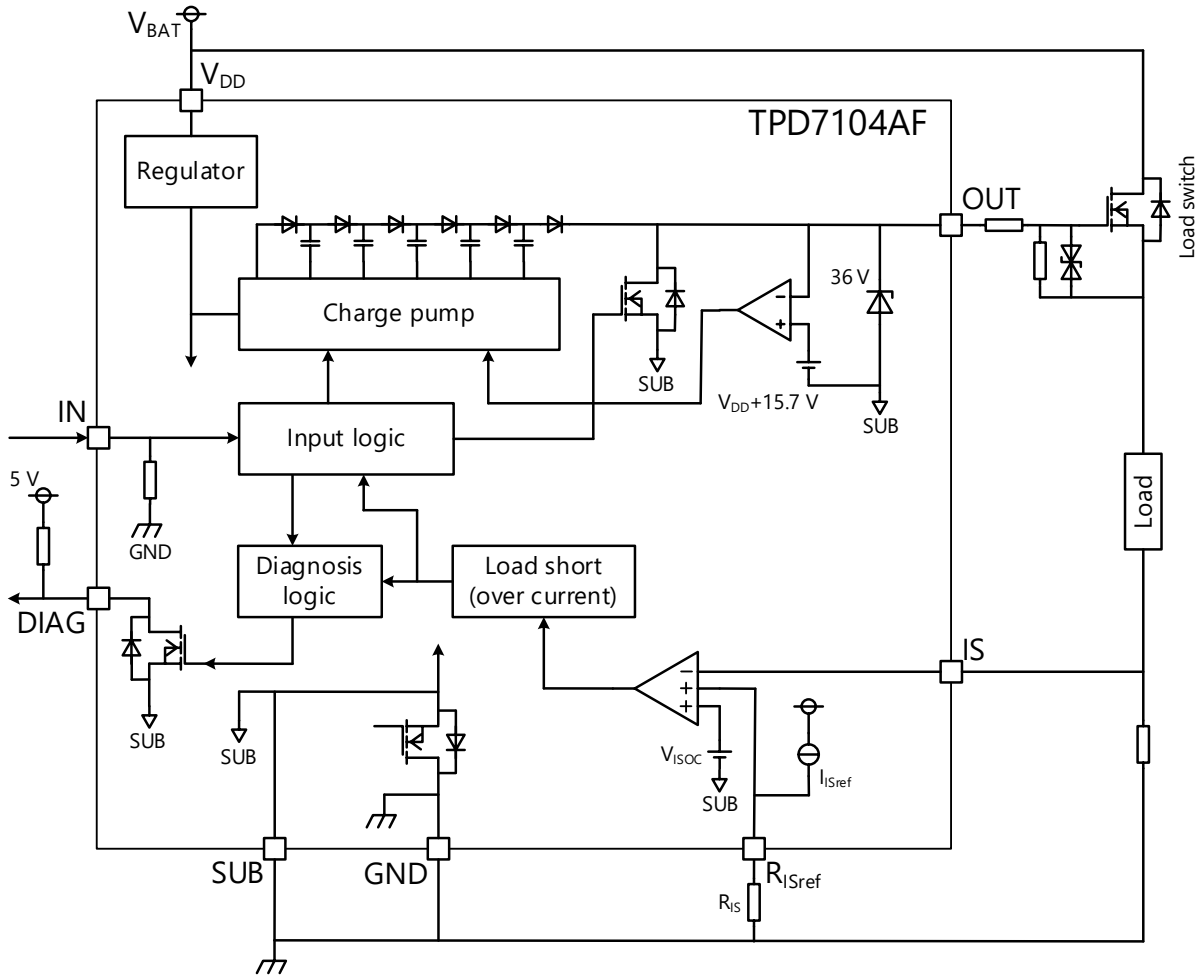


Fig. 2.1 Block diagram (load switch circuit)

2.2. Application example of reverse polarity protection circuit (enable reverse polarity protection)

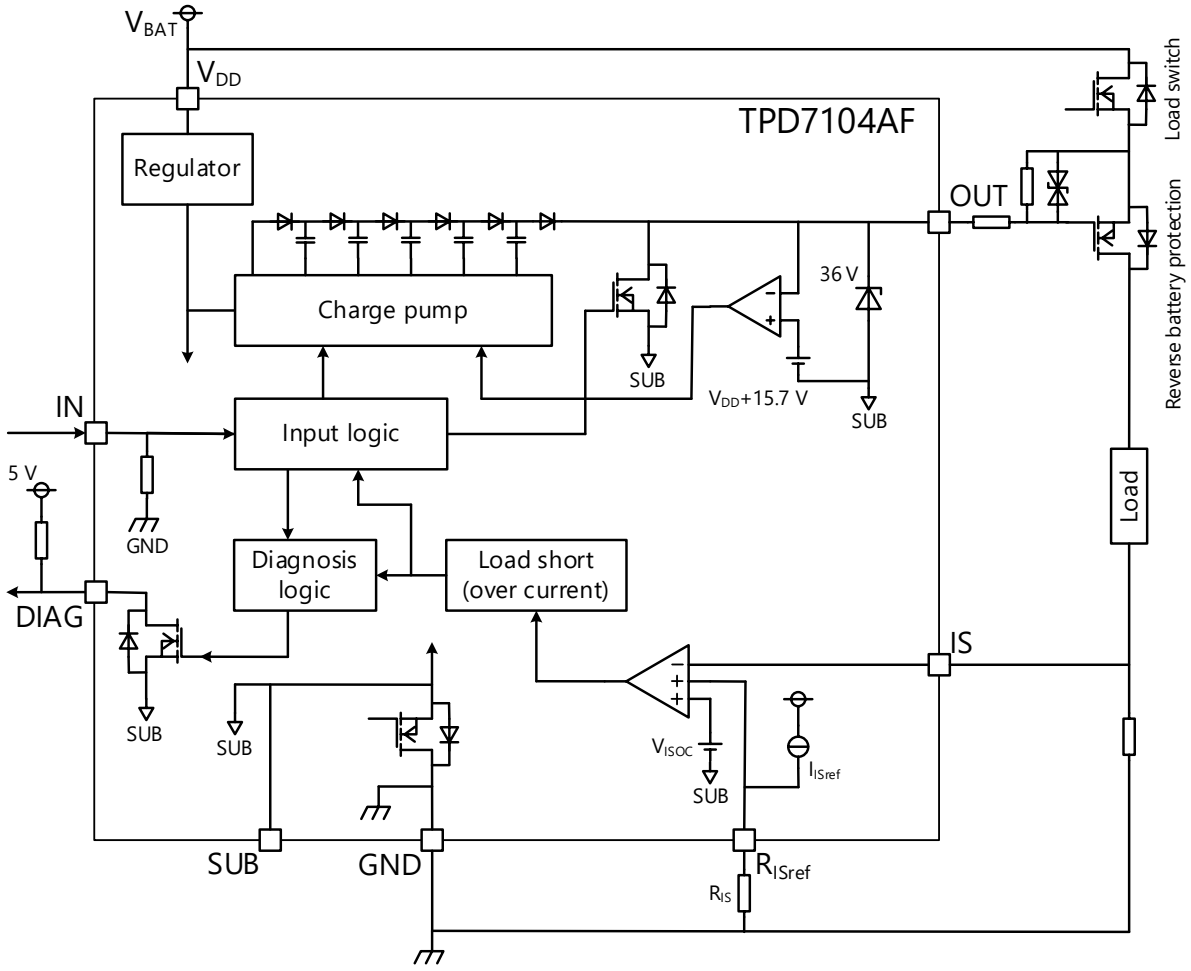


Fig. 2.2 Block diagram (reverse polarity protection)

3. Terminal equivalent circuit

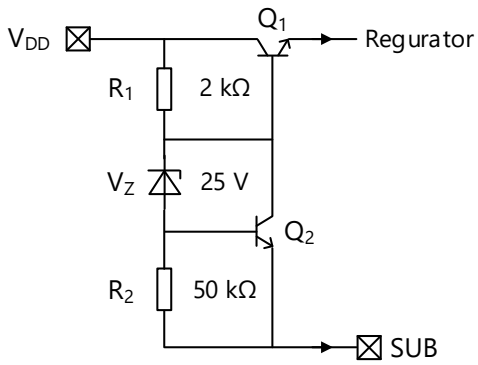


Fig. 3.1 Equivalent circuit of V_{DD} pin

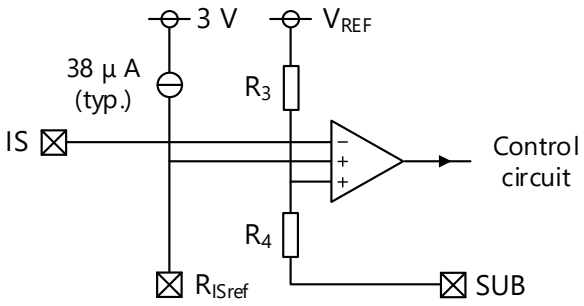


Fig. 3.2 Equivalent circuit of IS and R_{ISref} pins

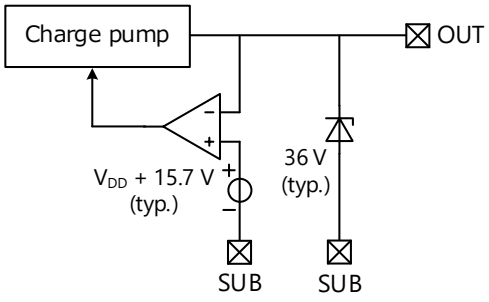


Fig. 3.3 Equivalent circuit of OUT pin

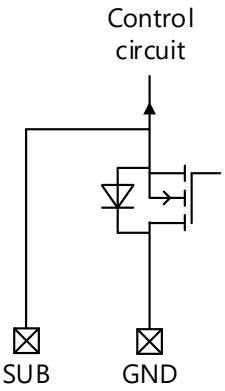


Fig. 3.4 Equivalent circuit of SUB and GND pins

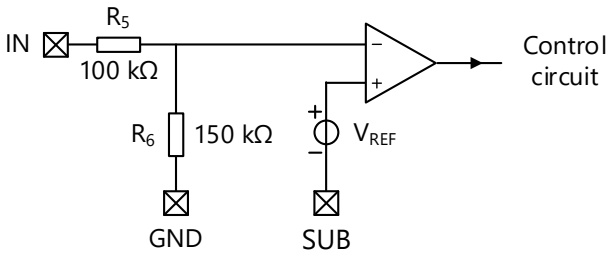


Fig. 3.5 Equivalent circuit of IN pin

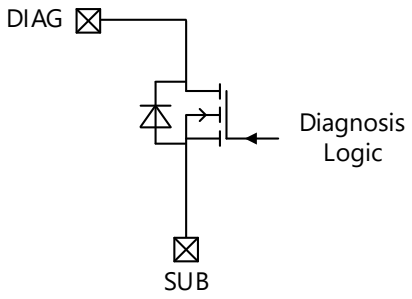


Fig. 3.6 Equivalent circuit of DIAG pin

4. Normal operation

TPD7104AF controls the output voltage at the OUT pin according to the input level at the IN pin, thereby driving an external N-channel MOSFET. When $V_{IN} = V_{IL}$, the OUT pin outputs Low, turning off the external N-channel MOSFET, and the DIAG pin outputs High. When $V_{IN} = V_{IH}$, the OUT pin outputs High, turning on the external N-channel MOSFET, and the DIAG pin outputs Low. Ensure that the voltage at the V_{DD} pin remains within the operating range (5 V to 18 V) during operation.

Table 4.1 Truth table of normal operation

V_{IN}	V_{OUT}	V_{DIAG}	External N-channel MOSFET
L	L	H (Note)	OFF
H	H	L	ON

Note: The DIAG output is configured as an N-channel open-drain MOSFET. When V_{DIAG} is 'H', the MOSFET is OFF.

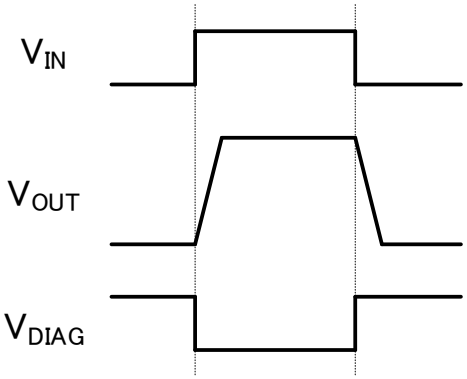


Fig. 4.1 Timing chart of normal operation

5. Description of each function or circuit

5.1. Reverse polarity protection function

TPD7104AF is equipped with a reverse polarity protection function. This function prevents current from flowing into the IC from the GND pin when the power supply is connected in reverse, thereby protecting the IC. In this case, ensure that the voltage at each pin does not exceed the absolute maximum ratings. In addition, since the OUT pin is pulled down to the V_{DD} pin through an internal resistor, the external N-channel MOSFET remains off. When using this function, leave the SUB pin open. If this function is not used, short the SUB pin and the GND pin externally.

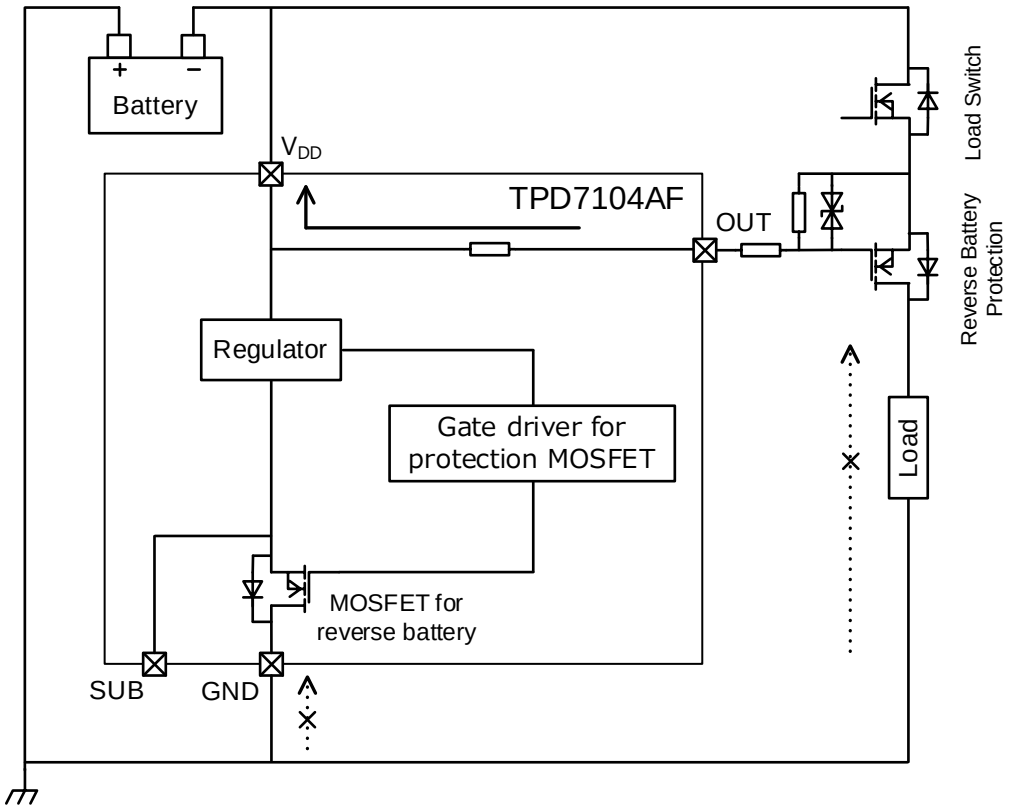


Fig. 5.1 Reverse polarity protection

5.2. Load short (overcurrent) protection function

TPD7104AF is equipped with a load short (overcurrent) protection function. This function latches VOUT output to Low, turns off the external N-channel MOSFET, and latches V_{DIAG} to High if V_{IS} remains at or above the load short detection voltage threshold V_{LSref} for the filter time of 1.8 µs (typical). V_{IS} is generated by passing the load current (I_{LOAD}) through the shunt resistor (R_{SHUNT}) inserted between the IS pin and GND. The threshold value V_{LSref} is determined as the smaller of the following two values: (1) V_{ISOC} (1.02 V (typ.)), which is a fixed voltage generated internally in the IC, and (2) V_{RISref} (the voltage at the R_{ISref} pin), which is the product of the resistance R_{IS} (variable) inserted between the R_{ISref} pin and GND and the internally generated current I_{ISref} (a fixed value of 38 µA (typ.)). If (2) is not used, leave the R_{ISref} pin open. To release the latch, set V_{IN} from V_{IL} to V_{IH}. In addition, if this function is not used, short the IS pin to GND.
The load short detection current threshold can be calculated using the following (Eq. 5-1) to (Eq. 5-2-2).

(1) When the R_{ISref} pin is left open:

$$\text{Load short detection current threshold} = \frac{V_{ISOC}}{R_{SHUNT}} \qquad \text{(Eq. 5-1)}$$

(2) When a resistor is connected to the R_{ISref} pin:

(2 - 1) If V_{RISref} (= I_{ISref} * R_{IS}) < V_{ISOC}:

$$\text{Load short detection current threshold} = \frac{V_{RISref}}{R_{SHUNT}} \qquad \text{(Eq. 5–2-1)}$$

(2 - 2) If V_{ISOC} < V_{RISref} (= I_{ISref} * R_{IS}):

$$\text{Load short detection current threshold} = \frac{V_{ISOC}}{R_{SHUNT}} \qquad \text{(Eq.5-2-2)}$$

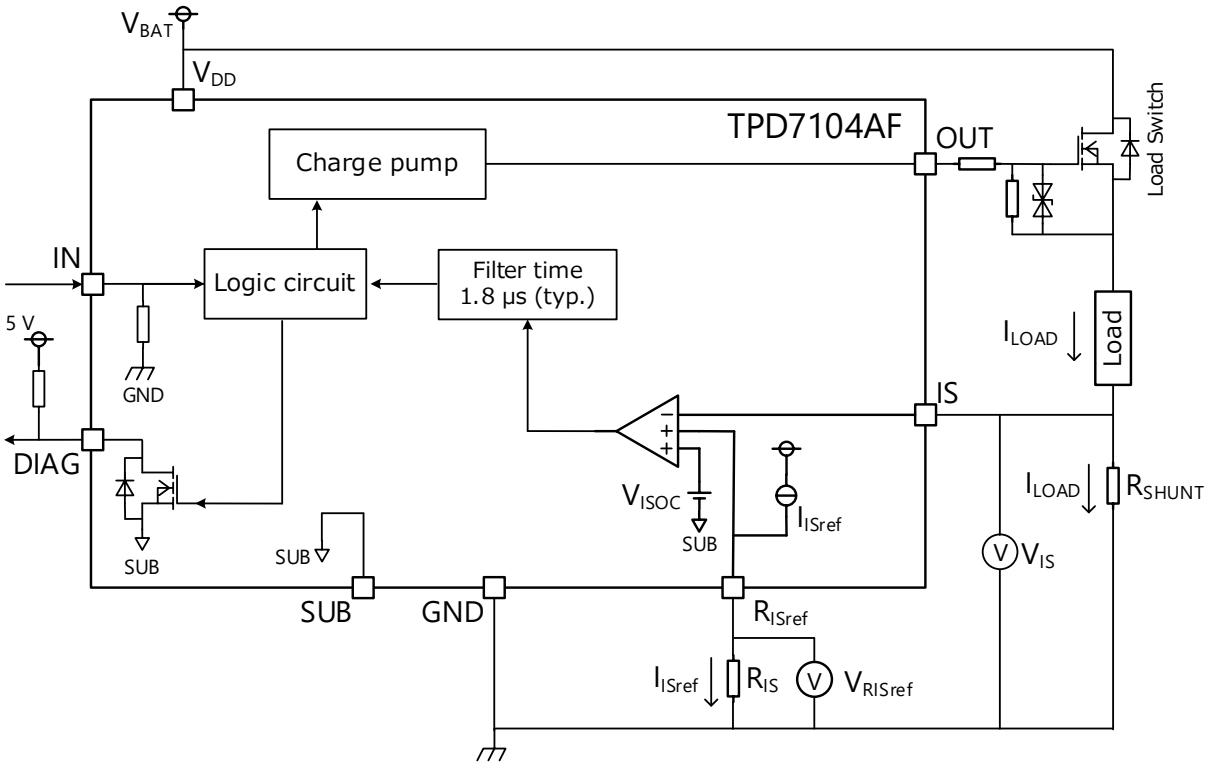


Fig. 5.2 Load short detection

Table 5.1 Truth table of load short detection operation

V_{IN}	V_{IS}	V_{OUT}	V_{DIAG}	External N-channel MOSFET	Notes
H	< V_{LSref}	H	L	ON	Normal operation
H	> V_{LSref}	L (latch)	H (latch)	OFF	Load short detection operation

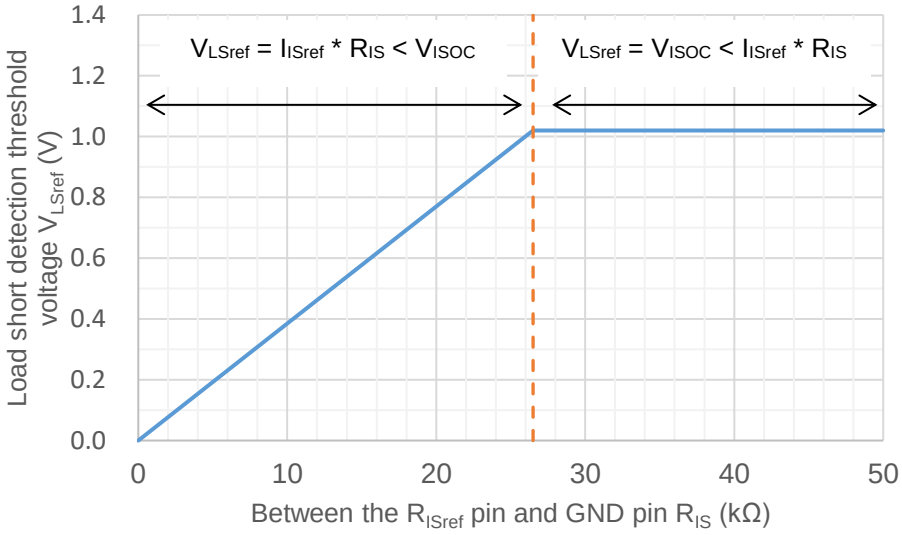


Fig. 5.3 V_{RISref} - R_{IS}

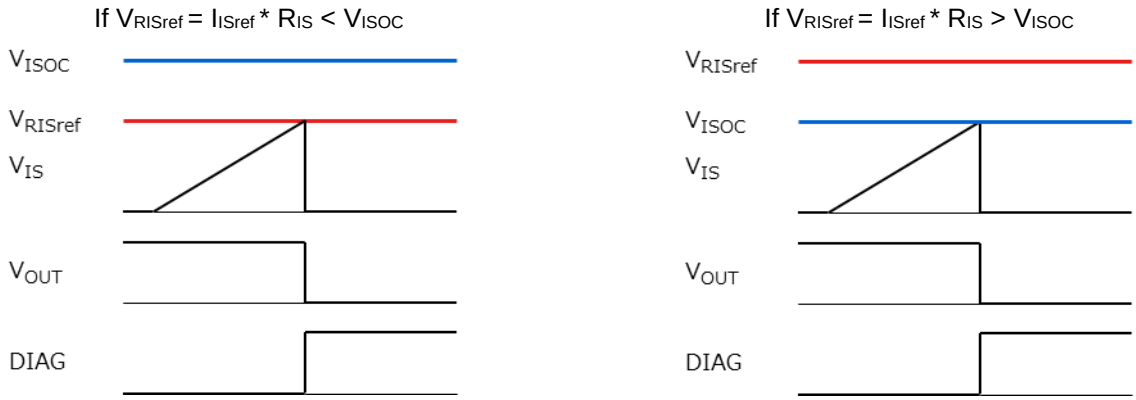


Fig. 5.4 Relationship between V_{RISref} and V_{ISOC}

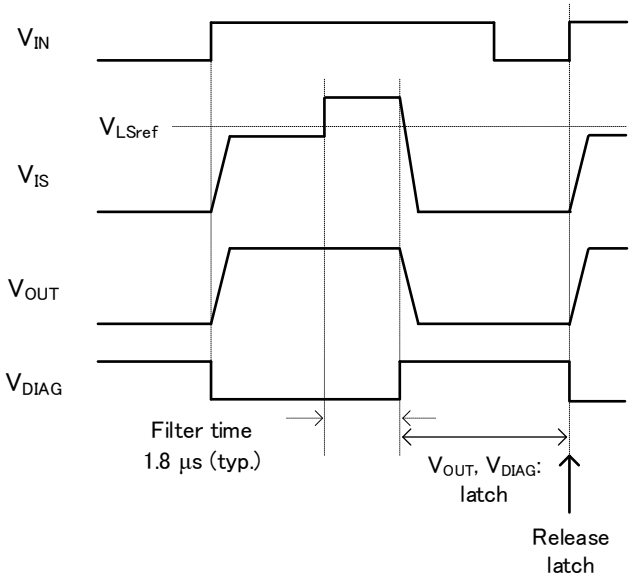


Fig. 5.5 Timing chart of load short detection operation

5.3. Charge pump circuit

The charge pump circuit is a boost power supply circuit for generating the gate-driving voltage of an external N-channel MOSFET. For high-side switches, when the external N-channel MOSFET is turned on, the source potential becomes nearly equal to the supply voltage. Therefore, to maintain the on-state, it is necessary to apply a voltage plus 10 to 15 V to the gate terminal. The charge pump circuit generates this voltage inside the IC. TPD7104AF incorporates a Dickson-type charge pump circuit, which consists of diodes, capacitors, and inverter circuits as shown in Fig. 5.6. The boosted voltage $V_{CP(OUT)}$ can be calculated using (Eq. 5-3).

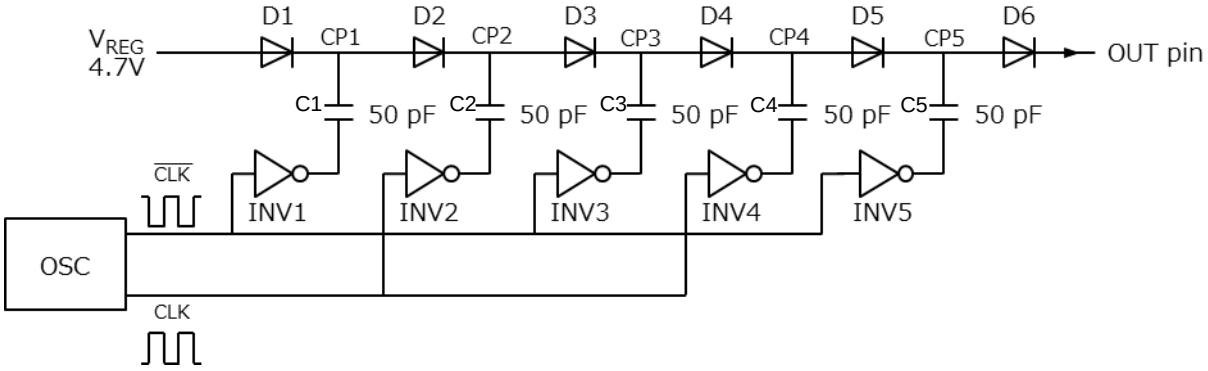


Fig. 5.6 Charge pump equivalent circuit

$$V_{CP(OUT)} = N * (V_{REG} - V_F) \qquad \text{(Eq. 5-3)}$$

N	: Number of stages
V_{REG}	: Power supply voltage for control circuit (V)
V_F	: Diode forward voltage (V)

Fig. 5.7 illustrates the operation of the Dickson-type charge pump circuit. Here, it is assumed that the voltage amplitudes of CLK and $\overline{CLK}$ are equal to that of V_{REG}.

Operation 1

When $\overline{CLK}$ is at the "L" level, capacitor C1 is charged from V_{REG} through diode D1, causing the voltage across C1 to become V_{REG} - V_F and voltage across CP1 swings between $2V_{REG}$ - V_F and V_{REG} - V_F.

Operation 2

When $\overline{CLK}$ is at the "H" level and CLK is at the "L" level, the charge stored in C1 charges C2 through D2, causing the voltage across C2 to become $2V_{REG}$ to $2V_F$, and voltage across CP2 swings between $3V_{REG}$ -$2V_F$ and $2V_{REG}$ - $2V_F$.

Operation 3

When $\overline{CLK}$ is at the "L" level and CLK is at the "H" level, the charge stored in C2 charges C3 through D3, causing the voltage across C3 to become $3V_{REG}$ to $3V_F$, and voltage across CP3 swings between $4V_{REG}$ - $3V_F$ and $3V_{REG}$ - $3V_F$.

Operation 4

When $\overline{CLK}$ is at the "H" level and CLK is at the "L" level, the charge stored in C3 charges C4 through D4, causing the voltage across C4 to become $4V_{REG} - 4V_F$, and voltage across CP4 swings between $5V_{REG} - 4V_F$ and $4V_{REG} - 4V_F$.

Operation 5

When $\overline{CLK}$ is at the "L" level and CLK is at the "H" level, the charge stored in C4 charges C5 through D5, causing the voltage across C5 to become $5V_{REG} - 5V_F$, and voltage across CP5 swings between $6V_{REG} - 5V_F$ and $5V_{REG} - 5V_F$.

Operation 6

The charge stored in C5 drives the gate of the external N-channel MOSFET with the voltage that is eventually boosted to 6 * ($V_{REG} - V_F$) through D6.

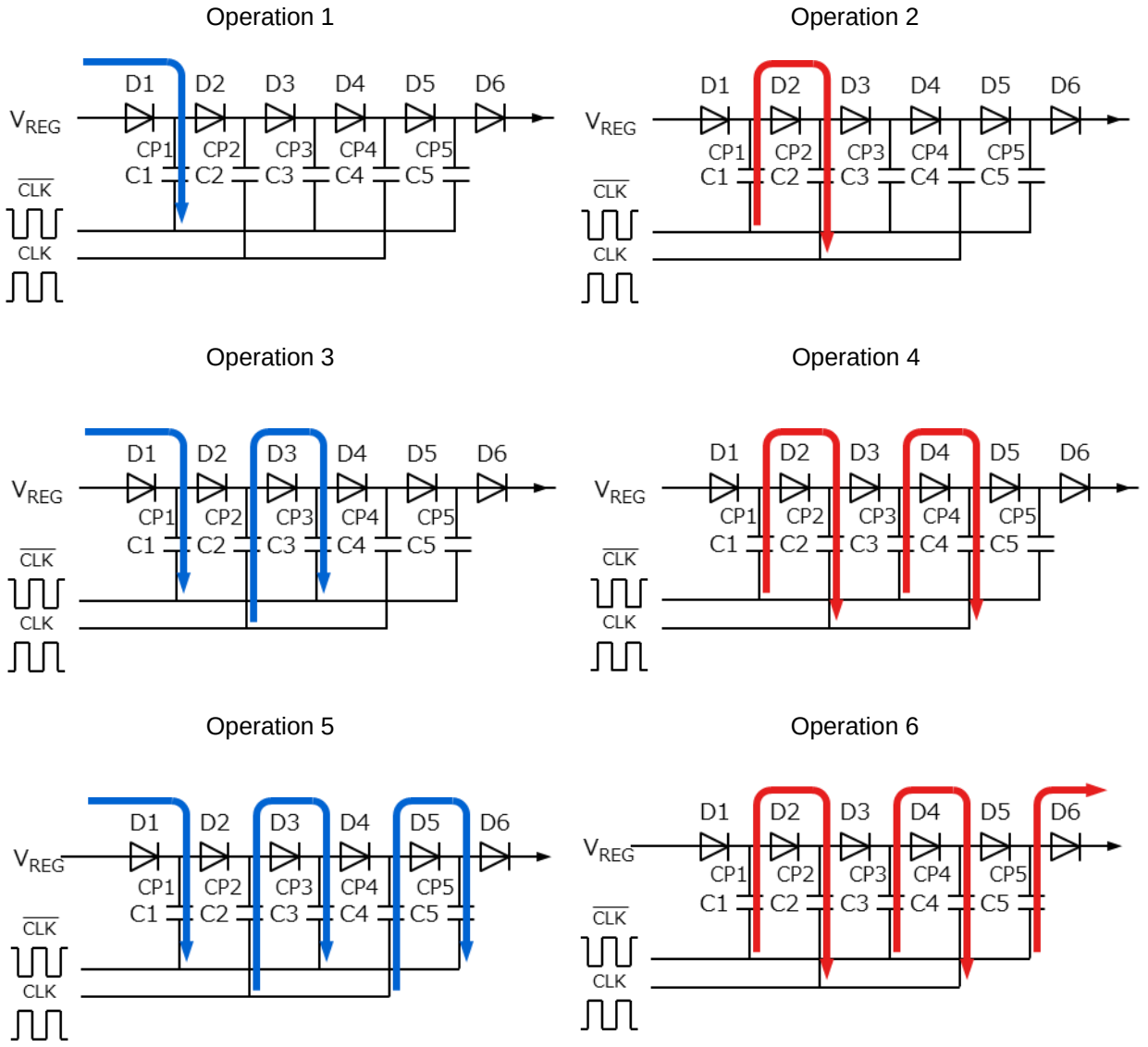


Fig. 5.7 Charge pump circuit operation

The voltage waveforms at the nodes of the charge pump circuit are ~~as~~ shown in Fig. 5.8. When V_{REG} = 4.7 V and V_F = 0.7 V, the output voltage calculated from (Eq. 5-3) becomes $V_{CP(OUT)}$ = 24 V, which is almost the same as the $V_{CP(OUT)}$ value shown in Fig. 5.8.

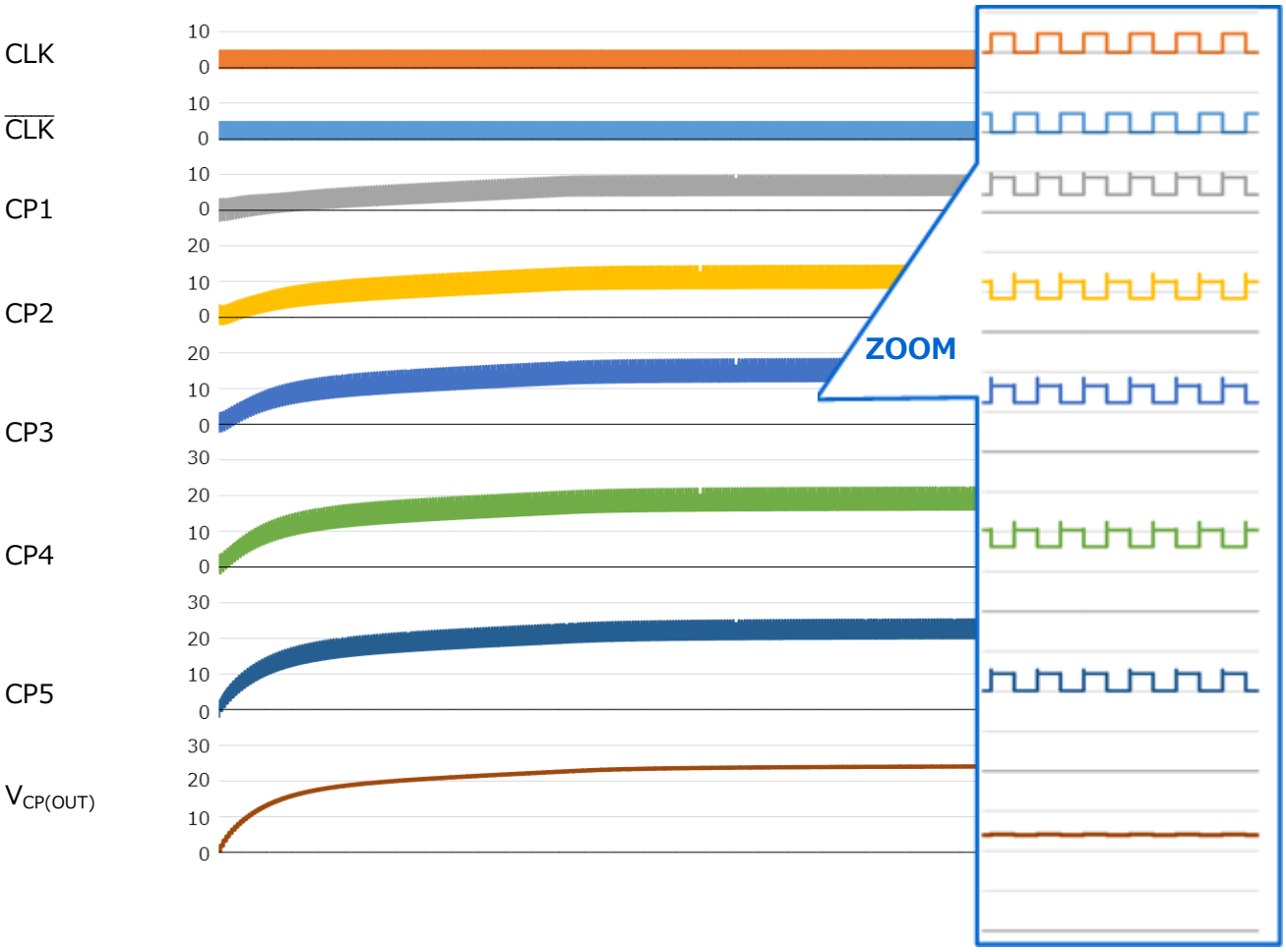


Fig. 5.8 Operation waveforms of each node in charge pump circuit

5.4. Charge pump voltage monitor circuit

TPD7104AF incorporates a charge pump voltage monitor circuit inside the OUT pin. This circuit stops the charge pump operation to protect the external N-channel MOSFET if the charge pump output voltage rises above V_{DD} + 15.7 V (typ.) due to external noise or other factors. A 36 V (typ.) Zener diode is also incorporated between the OUT and the SUB pins to protect the internal elements.

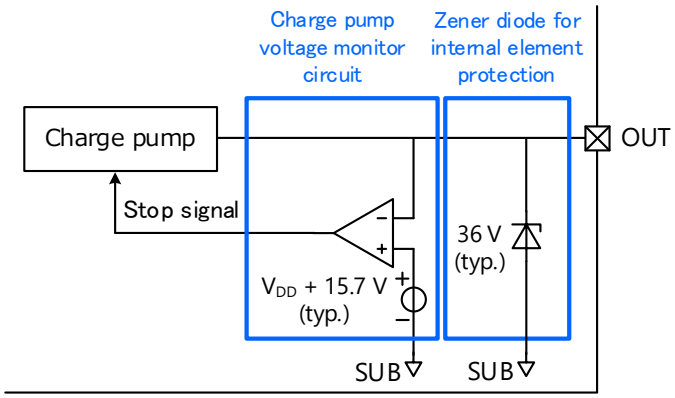


Fig. 5.9 Charge pump voltage monitor circuit

5.5. V_{DD} pin overvoltage protection circuit

TPD7104AF incorporates a series regulator, as shown in Figure 5.10, inside the V_{DD} pin to protect the internal elements when an overvoltage is applied to the V_{DD} pin. The output voltage of this regulator can be calculated using (Eq. 5-4). The power supply voltage for each control circuit is provided from the power supply for the control circuits connected to the subsequent stage through this regulator. When V_{DD} rises above 25 V, the output voltage of the series regulator is clamped at approximately 25 V, as shown in Figure 5.11.

$$V_{OUT(reg)} \approx V_Z + V_{BE(Q2)} - V_{BE(Q1)} \qquad \text{(Eq. 5-4)}$$

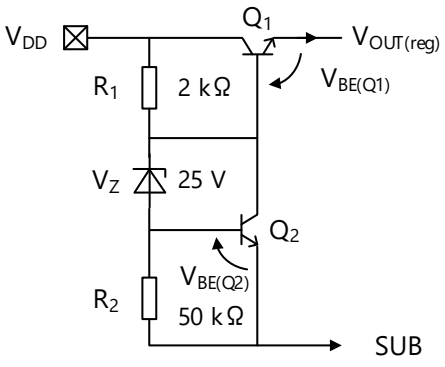


Fig. 5.10 V_{DD} pin overvoltage protection circuit

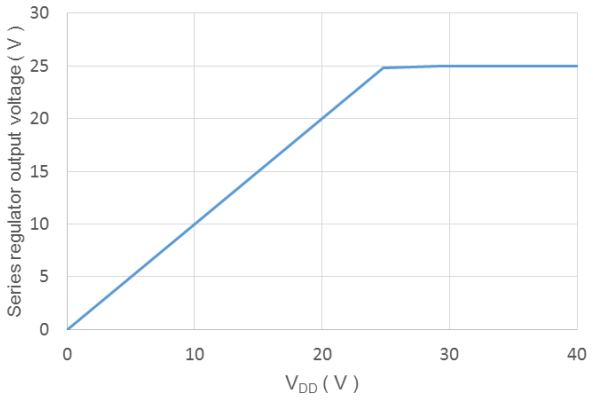


Fig. 5.11 Image of V_{DD} pin overvoltage protection operation

6. Electrical characteristics measurement circuit

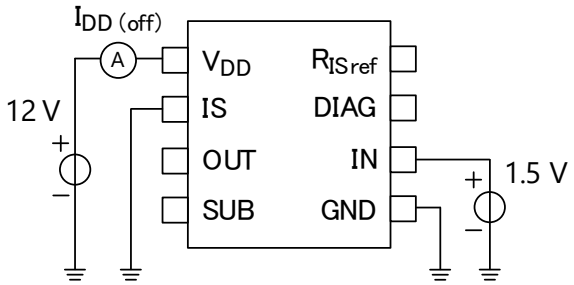


Fig. 6.1 Supply current $I_{DD(off)}$ measurement circuit

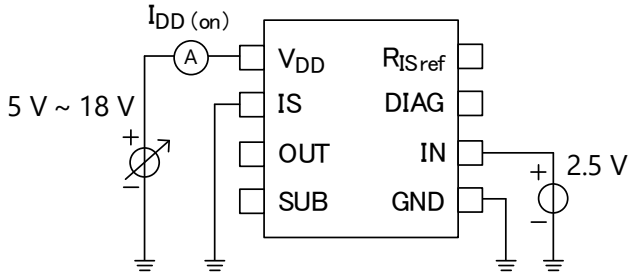
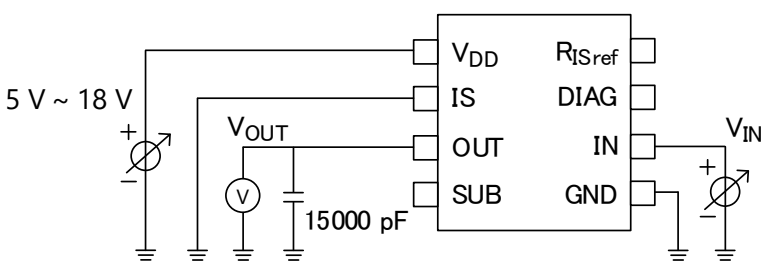


Fig. 6.2 Supply current $I_{DD(on)}$ measurement circuit



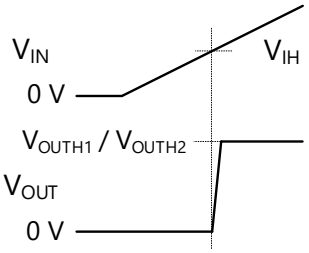
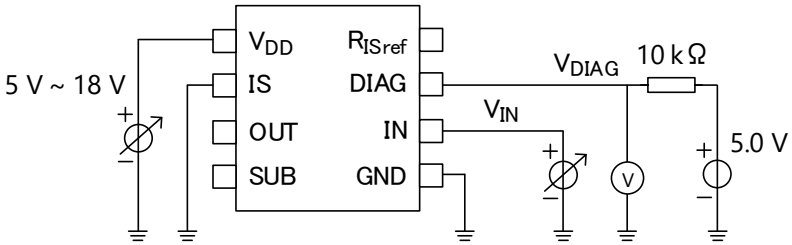


Fig. 6.3 High-level input voltage V_{IH} measurement circuit



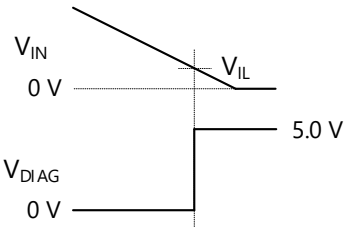


Fig. 6.4 Low-level input voltage V_{IL} measurement circuit

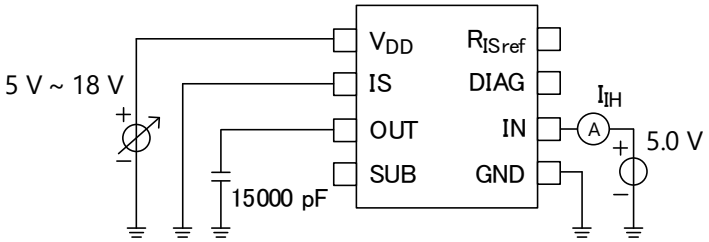


Fig. 6.5 Input current I_{IH} measurement circuit

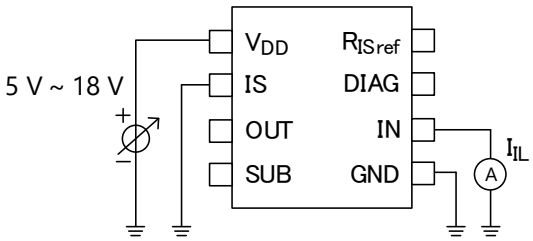


Fig. 6.6 Input current I_{IL} measurement circuit

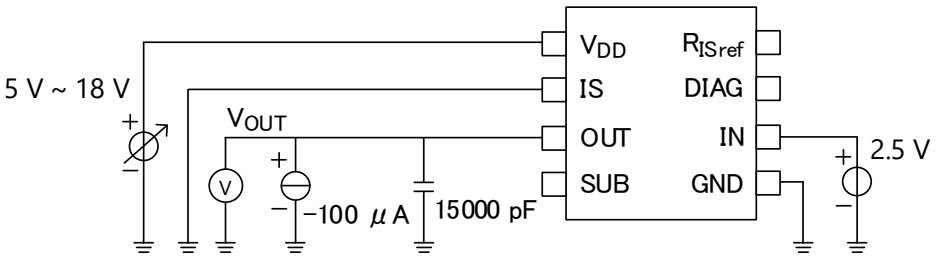


Fig. 6.7 Output voltage $V_{OUT1,2}$ measurement circuit

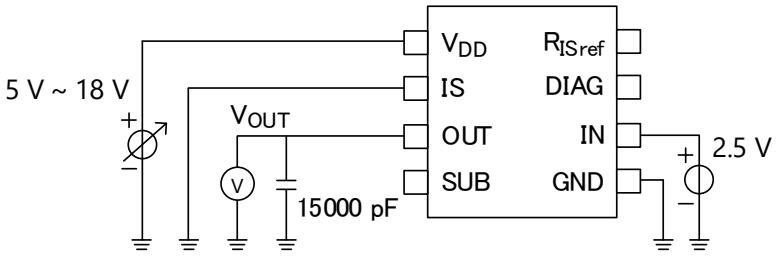


Fig. 6.8 Output clamp voltage V_{clamp} measurement circuit

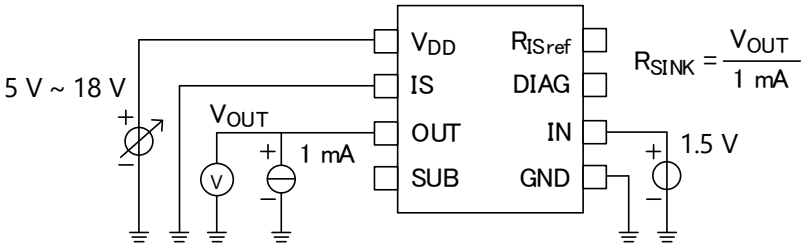


Fig. 6.9 Output resistance R_{SINK} measurement circuit

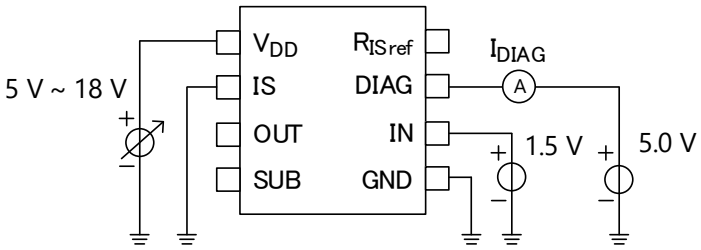


Fig. 6.10 Diagnosis output leakage current I_{DIAGH} measurement circuit

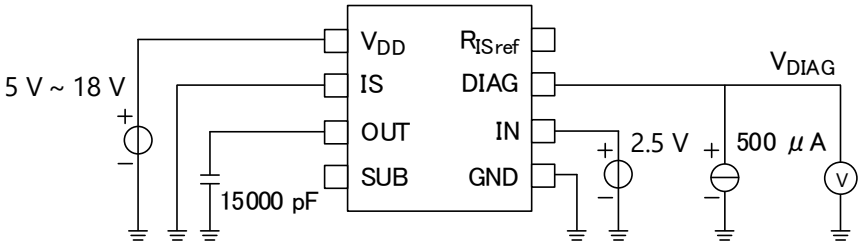


Fig. 6.11 Diagnosis output voltage V_{DIAGL} measurement circuit

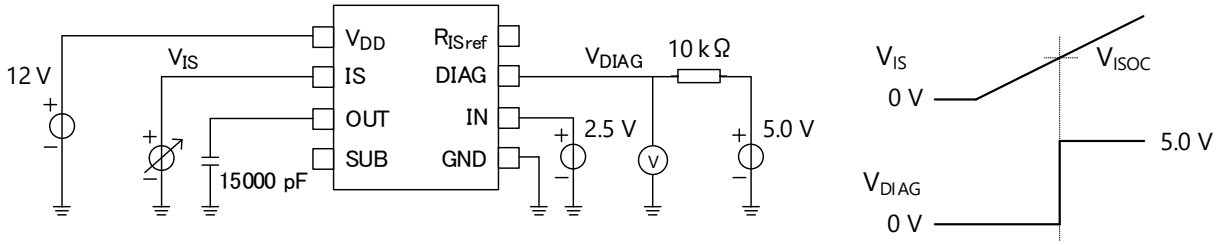


Fig. 6.12 Short circuit detection voltage V_{ISOC} measurement circuit

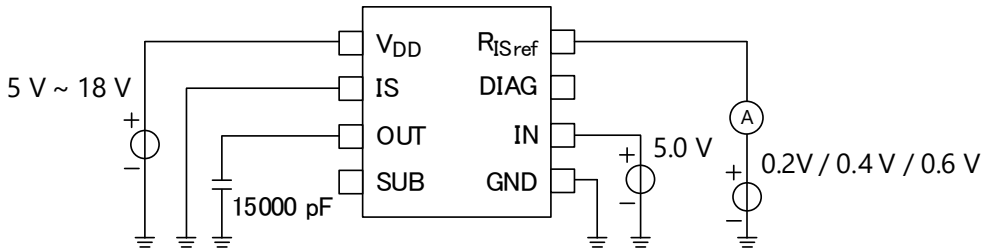


Fig. 6.13 R_{ISref} pin output current $I_{ISref(1),(2),(3)}$ measurement circuit

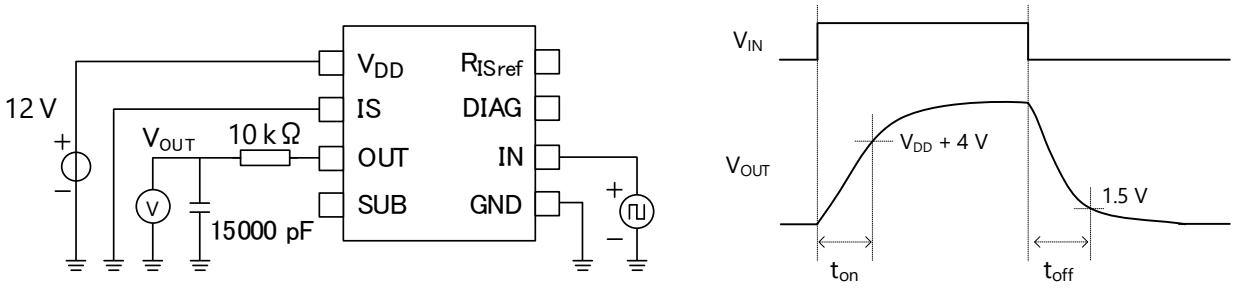


Fig. 6.14 Switching time t_{on}, t_{off} measurement circuit

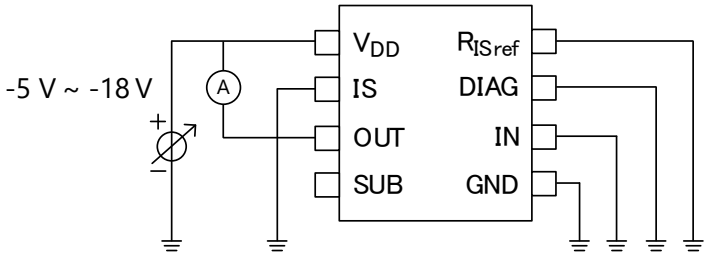


Fig. 6.15 Output current under reverse power connection $I_{REV(1),\ (2)}$ measurement circuit

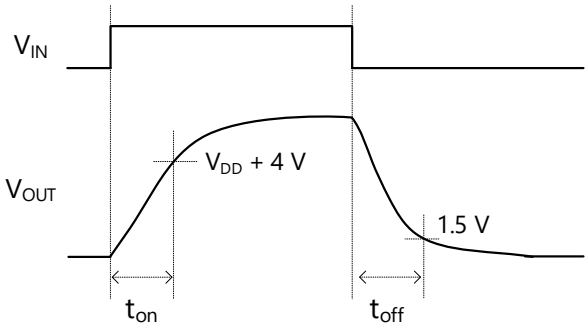
7. Definition and terminology

7.1. Absolute maximum rating

Term	Symbol	Description
Power supply voltage (DC)	$V_{DD(1)}$	DC voltage rating applied to the V_{DD} pin ensuring no IC destruction, characteristic degradation, or reliability deterioration.
Power supply voltage (pulse)	$V_{DD(2)}$	Pulse voltage rating applied to the V_{DD} pin ensuring no IC destruction, characteristic degradation, or reliability deterioration.
Power supply reverse connection	$-V_{DD(3)}$	Voltage rating applied to the V_{DD} pin ensuring no IC destruction, characteristic degradation, or reliability deterioration, even when a positive power supply is applied to the GND pin and a negative power supply is applied to the V_{DD} pin.
Input voltage	V_{IN}	Voltage rating applied to the IN pin ensuring no IC destruction, characteristic degradation, or reliability deterioration.
Output source current	$I_{OUT(-)}$	Current rating applied to the OUT pin (source current) ensuring no IC destruction, characteristic degradation, or reliability deterioration.
Output sink current	$I_{OUT(+)}$	Current rating applied to the OUT pin (sink current) ensuring no IC destruction, characteristic degradation, or reliability deterioration.
IS pin Voltage	V_{IS}	Voltage rating applied to the IS pin ensuring no IC destruction, characteristic degradation, or reliability deterioration.
Diagnosis output voltage	V_{DIAG}	Voltage rating applied to the DIAG pin ensuring no IC destruction, characteristic degradation, or reliability deterioration.
Diagnosis pin current	I_{DIAG}	Current rating applied to the DIAG pin ensuring no IC destruction, characteristic degradation, or reliability deterioration.
Power dissipation	P_D	Maximum allowable power dissipation throughout the operating range, ensuring no IC damage.
Operating temperature	T_{opr}	Ambient temperature range required for proper IC operation.
Junction temperature	T_j	Maximum allowable junction temperature during IC operation.
Storage temperature	T_{stg}	Ambient temperature range for storage or transportation without applied voltage applied to IC.

7.2. Electrical characteristics

Term	Symbol	Description
Operating supply voltage	$V_{DD(opr)}$	The supply voltage range that guarantees the normal operation and electrical characteristics of this IC within the specified junction temperature range.
Supply current	$I_{DD(off)}$	The current flowing into the V_{DD} pin when the IC is turned off by setting V_{IN} to V_{IL} within the specified junction temperature range.
Supply current	$I_{DD(on)}$	The current flowing into the V_{DD} pin when the IC is turned on by setting V_{IN} to V_{IH} within the specified junction temperature range.
High level input voltage	V_{IH}	The voltage at the IN pin that ensures the internal control circuit operates normally and the external N-channel MOSFET turns on within the specified junction temperature range.
Low level input voltage	V_{IL}	The voltage at the IN pin that ensures the internal control circuit operates normally and the external N-channel MOSFET turns off within the specified junction temperature range.
Input current	I_{IH}	The current flowing into the IN pin when the voltage specified in the measurement condition is applied to the IN pin within the specified junction temperature range.
Input current	I_{IL}	The current flowing into the IN pin when the voltage specified in the measurement condition is applied to the IN pin within the specified junction temperature range.
High level output voltage	V_{OUTH1} V_{OUTH2}	The output voltage at the OUT pin when the voltage and current specified in the measurement conditions are applied within the specified junction temperature range.
Output clamp voltage	V_{clamp}	The clamp voltage at the OUT pin when the voltage specified in the measurement conditions is applied within the specified junction temperature range.
Output resistance	R_{SINK}	The resistance value between the OUT pin and the GND pin when the voltage and current specified in the measurement conditions are applied within the specified junction temperature range.
Diagnostic output leakage current	I_{DIAGH}	The leakage current flowing into the DIAG pin when the voltage specified in the measurement conditions is applied within the specified junction temperature range.
Diagnostic output voltage	V_{DIAGL}	The on-voltage at the DIAG pin when the voltage and current specified in the measuring conditions are applied within the specified junction temperature range.
Short circuit detection voltage	V_{ISOC}	The reference voltage for load short detection inside the IC when the voltage specified in the measurement conditions is applied within the specified junction temperature range.
R_{ISref} pin output current	I_{ISref}	The current flowing into the R_{ISref} pin when the voltage specified in the measurement conditions is applied within the specified junction temperature range.

Term	Symbol	Description
Switching time	t_{on} t_{off}	ton: delay time from V_{IN} = V_{IH} (rising) to V_{OUT} = V_{DD} + 4 V toff: delay time from V_{IN} = V_{IL} (falling) to V_{OUT} = 1.5 V 
Output current for reverse connection	$I_{REV(1)}$ $I_{REV(2)}$	The value of current flowing into the OUT pin when the voltage specified by the measurement condition is applied within the specified junction temperature range.

8. Evaluation board

8.1. Appearance of evaluation board

We provide this product along with an evaluation board equipped with peripheral devices. By using this board, you can check the operation and the protection diagnosis function when using an actual load.

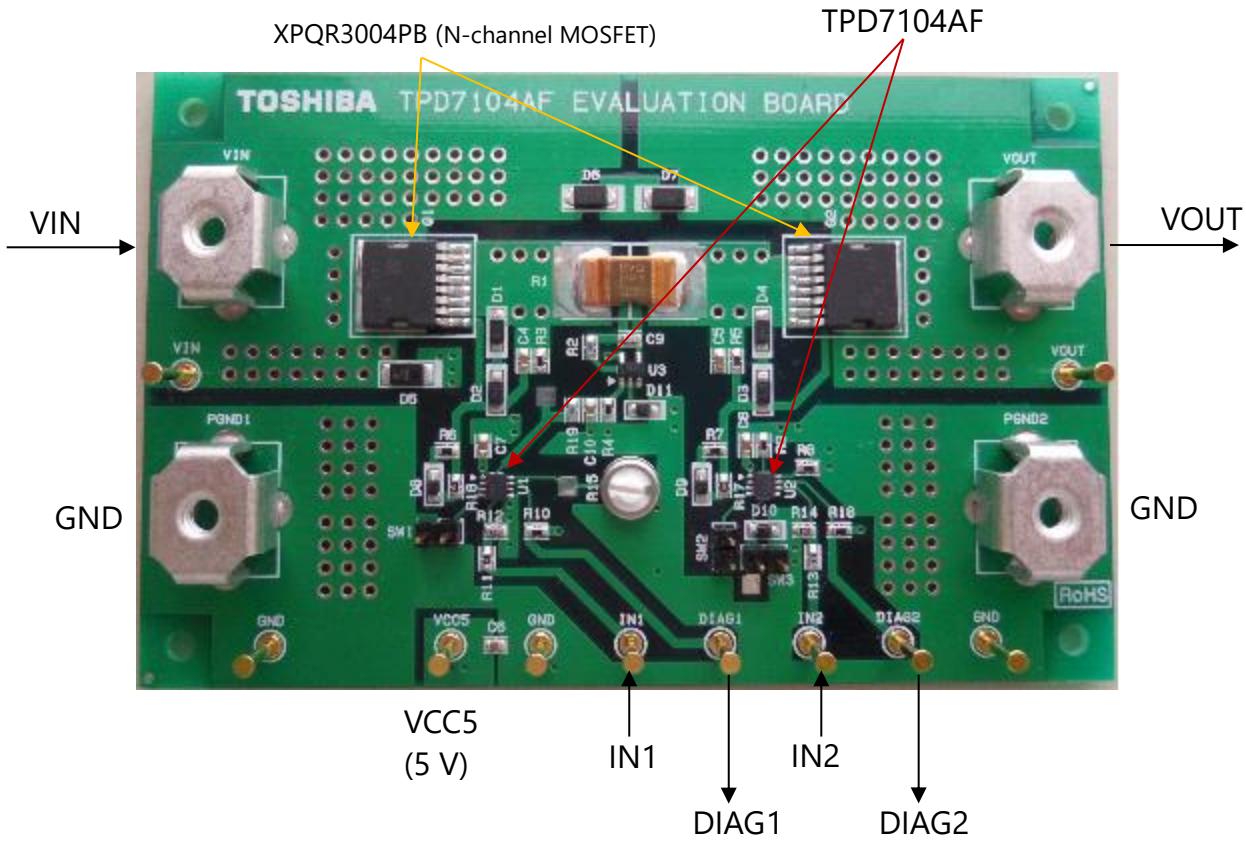


Fig. 8.1 TPD7104AF evaluation board

8.2. Circuit diagram for evaluation board

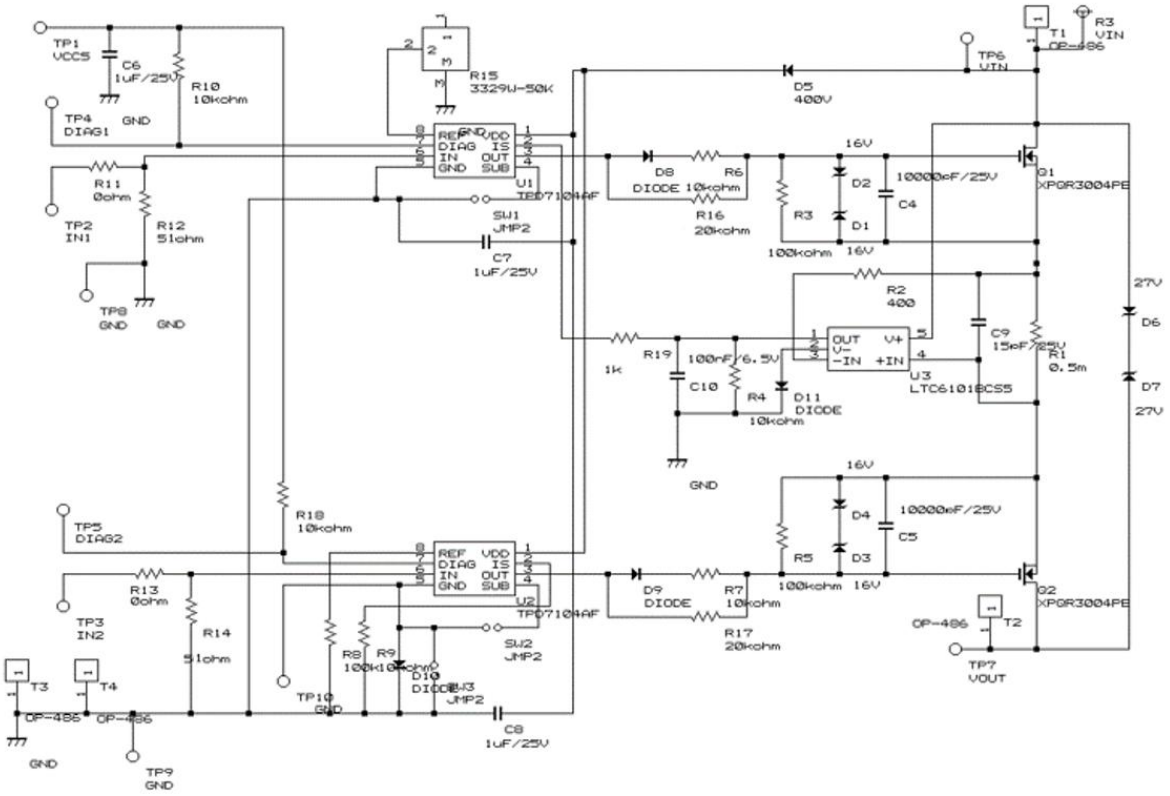


Fig. 8.2 Circuit diagram of TPD7104AF evaluation board

8.3. Bill of materials

Table 8.1 BOM list

No.	item	p/n	maker	spec.	location	PKG	QTY	Note.
1	IC	TPD7104AF	Toshiba	driver IC	U1, U2	PS-8	2	
2		LTC6101HVACS5	LT	sense amp.	U3	TSOT-23	1	
3	Power MOS	XPQR3004PB	Toshiba	Nch / 40V	Q1, Q2	L-TOGL	2	
4	R	BVS-M-R0005-1.0	Isabellenhuette	0.5 mΩ	R1		1	
5				300 Ω	R2	1608	1	
6		ERJP03F1003V	Panasonic	100 kΩ	R3, R5, R8	1608	3	
7		ERJP03F1002V	Panasonic	10 kΩ	R4, R6, R7, R9, R10, R18	1608	5	
8		ERJ3GEY0R00V	Panasonic	0 Ω	R11, R13	1608	2	
9		RR0816Q-510-D	Susumu	51 Ω	R12, R14	1608	2	
10		3329H	BOURNS	0 to 50 kΩ	R15	-	1	
11		CR0603-FX-2002ELF	BOURNS	20 kΩ	R16, R17	1608	2	
12				1 kΩ	R19	1608	1	
13	C	GRM155B11E103KA01D	Murata	10000pF / 25V	C4, C5	1005	2	
14		GRM188B31E105KA	Murata	1 μF / 25V	C6, C7, C8	1608	3	
15		C0603CH1E150J	TDK	15pF / 25V	C9	0603	1	
16				100 nF	C10	1608	1	
17	TP	ST2-2-2			TP1 to TP10		10	
18	D	CRZ16	Toshiba	16 V Zdi	D1 to D4	S-FLAT	4	
19		CMG06A	Toshiba	400 V / 1A	D5	M-FLAT	1	
20		CMZ27	Toshiba	27V / 1W	D6, D7	S-FLAT	2	
21		1SS352	Toshiba	80 V / 100 mA	D8 to D11	SOD-323	4	
22	terminal	OP-486	Osada	40 A DC max	T1 to T4		4	
23	jumper	XJ8T	Omron	2 poles / 2.54 mm	SW1 to SW3		3	

8.4. **Board layout**

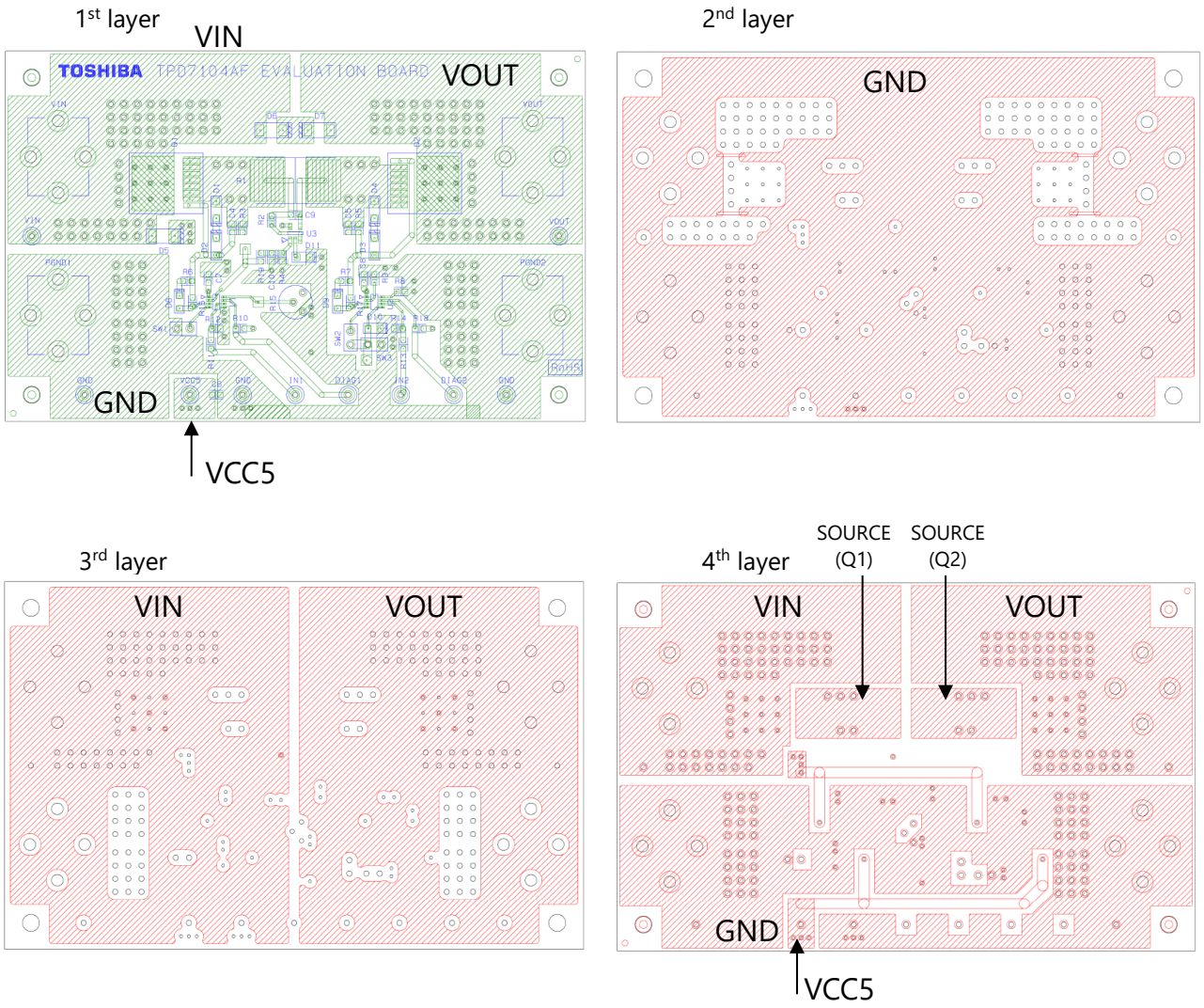


Fig. 8.3 Layout of TPD7104AF evaluation board

Points to note in the description

1. Block diagram
   Function blocks, circuits, constants, etc. in the block diagram are partially omitted or simplified for explanation of functions.

2. Equivalent circuit
   The equivalent circuit may be partially omitted or simplified for explanation of the circuit.

3. Measurement circuit
   The measurement circuit may be partially omitted or simplified for explanation of the measurement conditions.

IC usage consideration

Notes on handing of ICs

The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Exceeding the maximum rating may cause destruction, damage, and deterioration, and may result in injury due to explosion or burning.

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