

Toshiba Intelligent Power Device Silicon Monolithic MOS Integrated Circuit

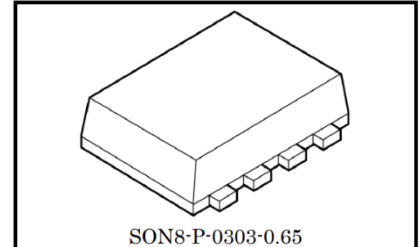
TPD1054F

Low-Side Switch for Solenoid, Mechanical relay and Lamp Drive

1. Description

TPD1054F is a low-side switch.

The IC has a MOSFET (D-MOS) output which can be directly driven from a CMOS or TTL logic circuit (e.g., an MPU). This IC is a monolithic power IC with intelligent features of protection and diagnostic functions.



Weight: 0.017 g (typ.)

2. Applications

Solenoid drive, mechanical relay drive and lamp drive.

3. Features

- A monolithic power IC with a structure combining a control block and a power MOSFET (D-MOS) on single chip.
- Can directly drive a power load from a CMOS or TTL logic (5 V, 3.3 V input compatible).
- Built-in overcurrent (Load short circuit), overtemperature (Thermal shutdown) and overvoltage (Active clamp) protection circuits.
- Incorporates a diagnosis function that allows diagnosis output to be read externally at overcurrent (load short circuit), overtemperature or load opening.
- Low Drain-Source ON-resistance:
 $R_{DS(ON)} = 0.8 \Omega$ (max) (@ $V_{DD} = 5 \text{ V}$, $V_{STBY} = 5 \text{ V}$, $V_{IN} = 5 \text{ V}$, $I_o = 0.5 \text{ A}$, $T_{ch} = 25 \text{ }^\circ\text{C}$)
- Low Leakage Current:
 $I_{DD1} = 10 \mu\text{A}$ (max) (@ $V_{IN} = 0 \text{ V}$, $V_{STBY} = 0 \text{ V}$, $V_{DD} = 5 \text{ V}$, $T_{ch} = -40$ to $125 \text{ }^\circ\text{C}$)
 $I_{OL} = 10 \mu\text{A}$ (max) (@ $V_{IN} = 0 \text{ V}$, $V_{STBY} = 0 \text{ V}$, $V_{DD} = 5 \text{ V}$, $V_{OUT} = 8$ to 16 V , $T_{ch} = -40$ to $125 \text{ }^\circ\text{C}$)
- AEC-Q100 qualified.
- It is a surface-mounted package "PS-8" (named by Toshiba), and the packing is embossed-tape packing.

Note: Due to its MOS structure. This product is sensitive to static electricity.

Start of commercial production
2013-12

4. Block Diagram

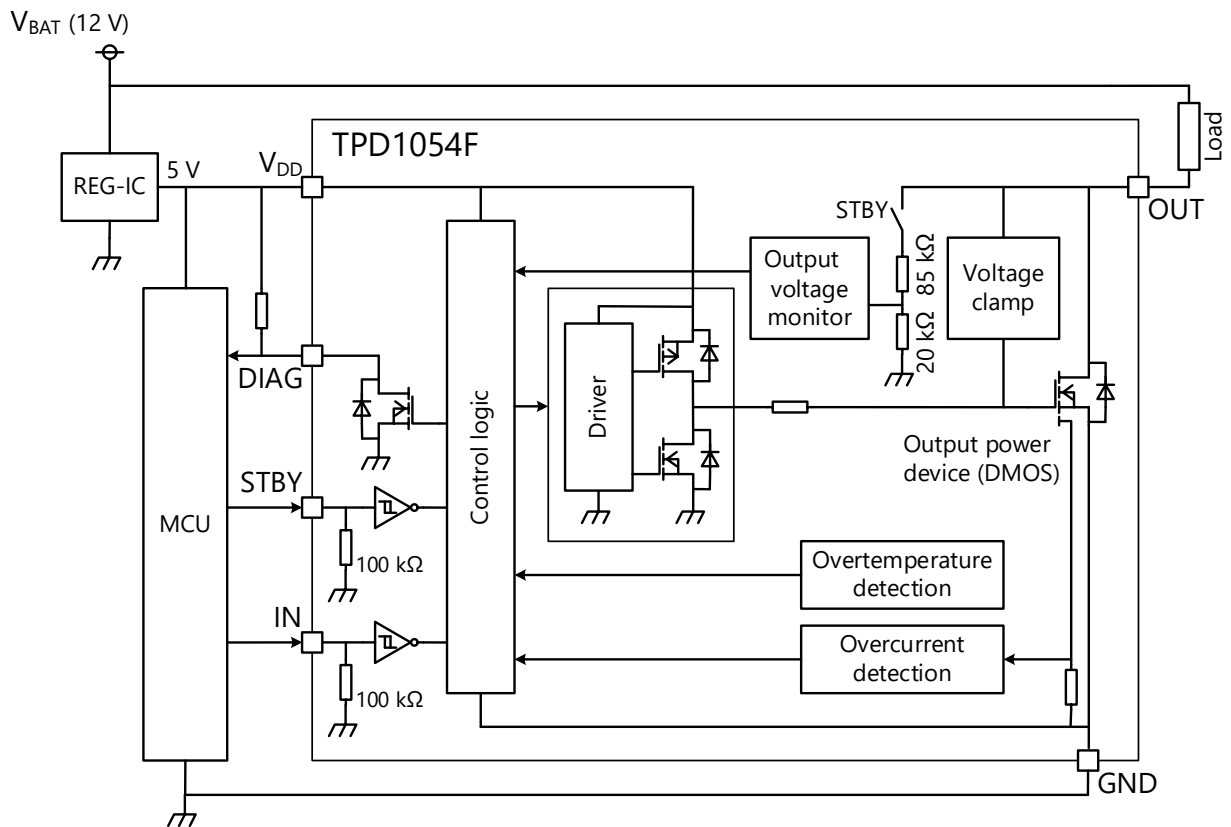


Figure 4.1 Block Diagram

Note: Numerical values in the block diagram are typical values.

5. Pin Assignments

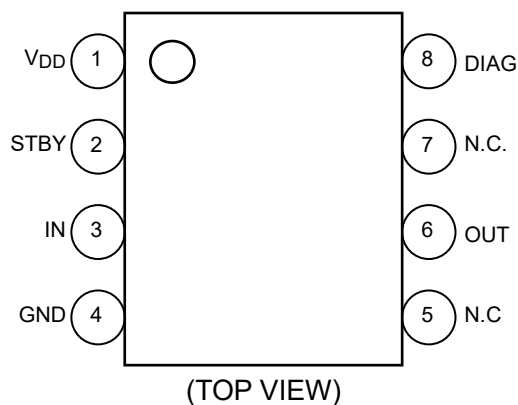


Figure 5.1 Pin Assignments

6. Pin Description

Table 6.1 Pin Description

Pin No.	Symbol	I/O	Pin Description
1	V _{DD}	—	Power supply pin.
2	STBY	IN	STBY pin. V _{STBY} =L/Open : I _{DD} ≤10 μA (Standby mode) V _{STBY} =H : Active control
3	IN	IN	Input pin. The IN pin has an internal pull-down resistor. Even if the IN pin is open, the output will not accidentally turn on.
4	GND	—	Ground pin.
5	N.C	—	No-Connect pin. (Not connected to the chip.)
6	OUT	OUT	Output pin. When a load short-circuit causes an overcurrent (1.0A min) to flow into a device, output current is limited in order to protect the IC.
7	N.C	—	No-Connect pin. (Not connected to the chip.)
8	DIAG	OUT	Diagnosis detection pin. It is open drain composition. When Input is "H" (Output on), and Overcurrent or Overtemperature is detected, DIAG becomes low level and it is latched. When input is low level, the state of latch is reset. When Input is "L" (Output off), the output is disconnected (load open is detected), V _{DIAG} =H output.

7. Functional Description

7.1. Timing chart

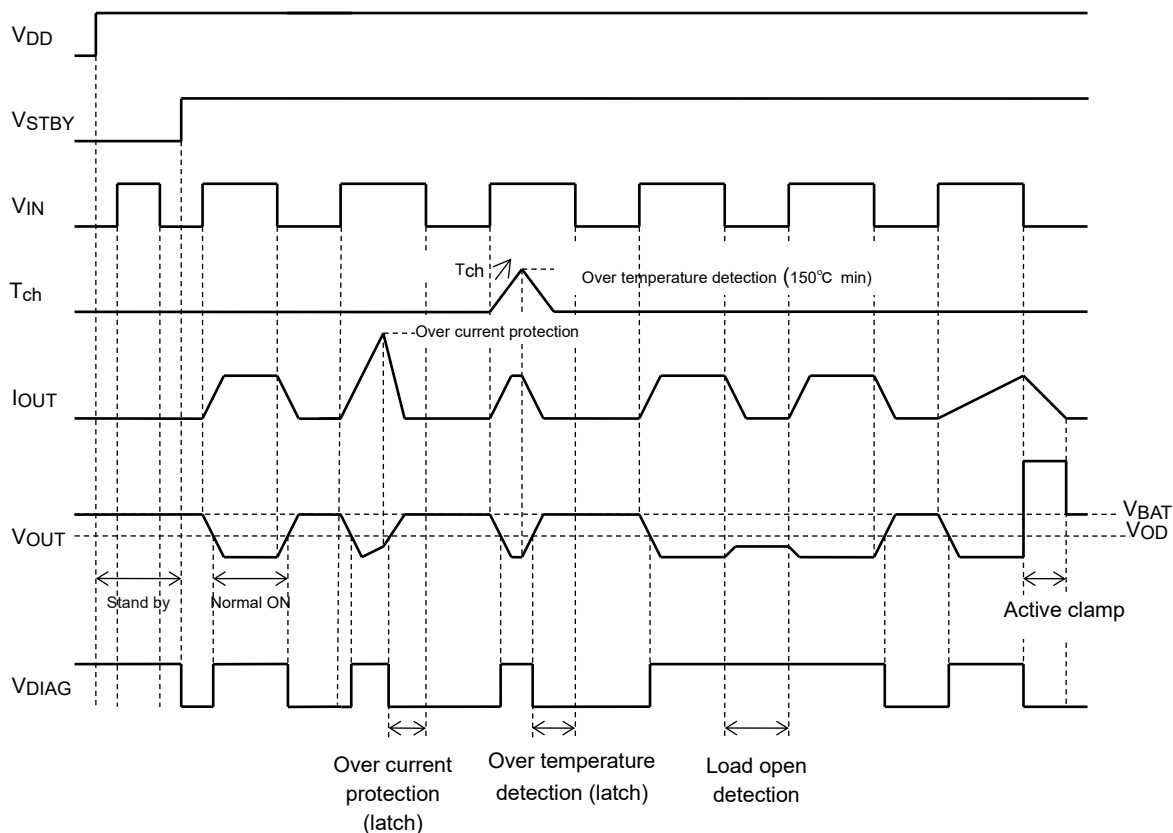


Figure 7.1 Timing chart

7.2. Truth table

Table 7.1 Truth table

STBY	IN	Output DMOS state	Output voltage V _{OUT} (Note 1)	DIAG output	Operating state
L	L	OFF	H	H	Standby mode
L	H	OFF	H	H	
H	L	OFF	H	L	Normal OFF
H	H	ON	L	H	Normal ON
H	H	OFF (latch*)	H	L (latch*)	Overcurrent (load short)
H	H	OFF (latch*)	H	L (latch*)	Over temperature
H	L	OFF	L	H	Load open (output is disconnected)

Note 1: H state is $V_{OUT} \geq V_{OD}$. L state is $V_{OUT} < V_{OD}$.

*Latch reset condition: $V_{STBY} < V_{IL}$ or $V_{STBY} < V_{IL}$.

8. Absolute Maximum Ratings (Note)

Table 8.1 Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	PIN	Rating	Unit	Note
Supply voltage	V_{DD}	V_{DD}	-0.3 to 6.0	V	-
Input voltage	V_{IN}, V_{STBY}	IN, STBY	-0.3 to 6.0	V	-
Diagnosis output voltage	V_{DIAG}	DIAG	-0.3 to 6.0	V	-
Diagnosis output current	I_{DIAG}	DIAG	5.0	mA	-
Output voltage	V_{OUT}	OUT	-0.3 to 40.0	V	-
Output current	I_{OUT}	OUT	Internally Limited	A	-
Power dissipation	$P_{D(1)}$	-	0.70	W	Refer to Figure 9.1
	$P_{D(2)}$	-	0.35	W	Refer to Figure 9.2
Single pulse active clamp capability (Note 1)	E_{AS}	-	125	mJ	-
Active clamp current	I_{AR}	-	1.0	A	-
Operating temperature	T_{opr}	-	-40 to 125	$^\circ\text{C}$	-
Channel temperature	T_{ch}	-	150	$^\circ\text{C}$	-
Storage temperature	T_{stg}	-	-55 to 150	$^\circ\text{C}$	-

Note : Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

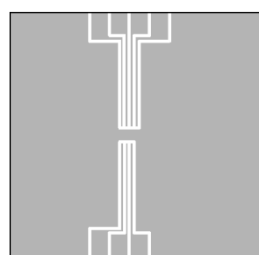
Note 1: Active clamp capability (single pulse) test condition
 $V_{BAT}=40\text{ V}$, $T_{ch}=25^\circ\text{C}$ (initial), $L=50\text{ mH}$, $I_{AR}=1\text{ A}$

9. Thermal Characteristics

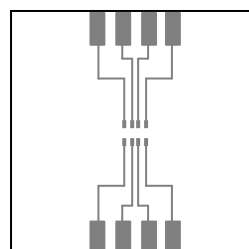
Table 9.1 Thermal characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to ambient	$R_{th(ch-a)}$	178.6 (Figure 9.1)	$^\circ\text{C/W}$
		357.2 (Figure 9.2)	

$$P_D = (T_{ch} - T_a) / R_{th(ch-a)}$$



Glass epoxy board
 Material: FR-4
 25.4 mm × 25.4 mm × 0.8 mm



Glass epoxy board
 Material: FR-4
 25.4 mm × 25.4 mm × 0.8 mm

Figure 9.1 Glass epoxy board (a)

Figure 9.2 Glass epoxy board (b)

10. Operating Ranges

Table 10.1 Operating Ranges

Characteristics	Symbol	Pin	Condition	Min	Typ.	Max	Unit
Drain-source clamp voltage	$V_{(CL)DSS}$	OUT	$I_O=1\text{ mA}$, $V_{STBY}=5\text{ V}$, $V_{IN}=0\text{ V}$	40	45	50	V
Operating supply voltage	$V_{DD(opr)}$	V_{DD}	-	4.5	5.0	5.5	V

11. Electrical Characteristics

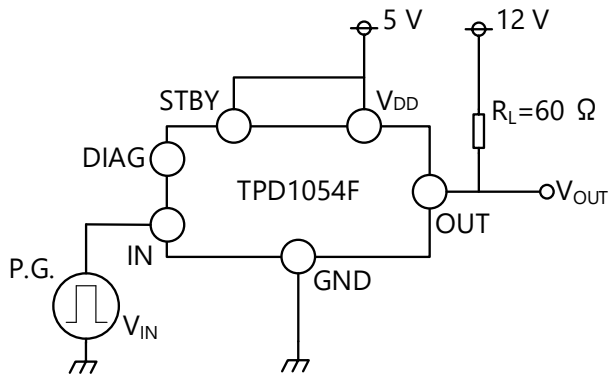
Table 11.1 Electrical Characteristics

(Unless otherwise specified $T_{ch} = -40\text{ to }125\text{ }^\circ\text{C}$, $V_{DD} = 4.5\text{ to }5.5\text{ V}$)

Characteristics	Symbol	Pin	Test circuit	Test condition	Min	Typ. (Note 1)	Max	Unit
Supply current	I_{DD1}	V_{DD}	-	$V_{STBY}=0\text{ V}$, $V_{IN}=0\text{ V}$, $V_{DD}=5\text{ V}$	-	-	10	μA
	I_{DD2}	V_{DD}	-	$V_{STBY}=5\text{ V}$, $V_{IN}=0\text{ V}$, $V_{DD}=5\text{ V}$	-	0.5	2.0	mA
	I_{DD3}	V_{DD}	-	$V_{STBY}=5\text{ V}$, $V_{IN}=5\text{ V}$, $V_{DD}=5\text{ V}$	-	0.5	2.0	mA
Output leakage current	I_{OL1}	OUT	-	$V_{STBY}=V_{IL}$, $V_{IN}=V_{IL}$, $V_{OUT}=8\text{ to }16\text{ V}$	-	-	10	μA
	I_{OL2}	OUT	-	$V_{STBY}=V_{IH}$, $V_{IN}=V_{IL}$, $V_{OUT}=8\text{ to }16\text{ V}$	-	120	300	μA
High level input voltage	V_{IH}	IN,STBY	-	-	2.3	-	-	V
Low level input voltage	V_{IL}	IN,STBY	-	-	-	-	0.8	V
High level input current	I_{IH}	IN,STBY	-	$V_{IN}(V_{STBY})=5\text{ V}$, $V_{DD}=5\text{ V}$	-	-	200	μA
Low level input current	I_{IL}	IN,STBY	-	$V_{IN}(V_{STBY})=0\text{ V}$, $V_{DD}=5\text{ V}$	-1	-	1	μA
Diagnosis output voltage	V_{DL}	DIAG	-	$I_{DIAG}=1\text{ mA}$	-	0.1	0.5	V
Diagnosis output current	I_{DH}	DIAG	-	$V_{DIAG}=5.5\text{ V}$	-	-	10	μA
Drain-source ON-resistance	$R_{DS(ON)1}$	OUT	-	$I_O=+0.5\text{ A}$, $T_{ch}=25\text{ }^\circ\text{C}$, $V_{DD}=5\text{ V}$, $V_{STBY}=V_{IH}$, $V_{IN}=V_{IH}$	-	0.45	0.80	Ω
	$R_{DS(ON)2}$	OUT	-	$I_O=+0.5\text{ A}$, $T_{ch}=-40\text{ to }125\text{ }^\circ\text{C}$, $V_{DD}=5\text{ V}$, $V_{STBY}=V_{IH}$, $V_{IN}=V_{IH}$	-	-	1.2	Ω
Overtemperature detection	T_{OT}	-	-	$V_{STBY}=5\text{ V}$, $V_{IN}=5\text{ V}$,	150	175	200	$^\circ\text{C}$
Overcurrent detection	I_{OC}	OUT	-	$V_{STBY}=5\text{ V}$, $V_{IN}=5\text{ V}$,	1.0	2.2	3.5	A
Load open threshold resistance	R_{OP}	OUT	-	$V_{STBY}=5\text{ V}$, $V_{IN}=0\text{ V}$, $V_{BAT}=8\text{ to }16\text{ V}$	10	300	1000	k Ω
	ΔR_{OP}	OUT	-	$V_{STBY}=5\text{ V}$, $V_{IN}=0\text{ V}$, $V_{BAT}=8\text{ to }16\text{ V}$	-	30	-	k Ω
Diagnosis output threshold voltage	V_{OD}	OUT	-	$V_{STBY}=5\text{ V}$	2	3	4	V
	ΔV_{OD}	OUT	-	$V_{STBY}=5\text{ V}$	-	0.3	-	V
OUT-GND internal resistance	R_{OUT1}	OUT	-	$V_{STBY}=5\text{ V}$, $V_{IN}=0\text{ V}$, $T_{ch}=25\text{ }^\circ\text{C}$	50	105	170	k Ω
	R_{OUT2}	OUT	-	$V_{STBY}=5\text{ V}$, $V_{IN}=0\text{ V}$, $T_{ch}=-40\text{ to }125\text{ }^\circ\text{C}$	40	105	200	k Ω
Switching time	t_{on}	OUT	1	$V_{STBY}=5\text{ V}$, $V_{IN}=0\rightarrow 5\text{ V}$, $V_{DD}=5\text{ V}$, $T_{ch}=25\text{ }^\circ\text{C}$, $V_{BAT}=12\text{ V}$, $R_L=60\text{ }\Omega$	-	0.5	1	μs
	t_{off}	OUT	1	$V_{STBY}=5\text{ V}$, $V_{IN}=5\rightarrow 0\text{ V}$, $V_{DD}=5\text{ V}$, $T_{ch}=25\text{ }^\circ\text{C}$, $V_{BAT}=12\text{ V}$, $R_L=60\text{ }\Omega$	-	0.5	1	μs

Note 1: The condition of the typical value is $T_{ch}=25\text{ }^\circ\text{C}$, $V_{DD}=5\text{ V}$.

12. Test Circuit



**Figure 12.1 Test circuit 1
(Switching time test circuit)**

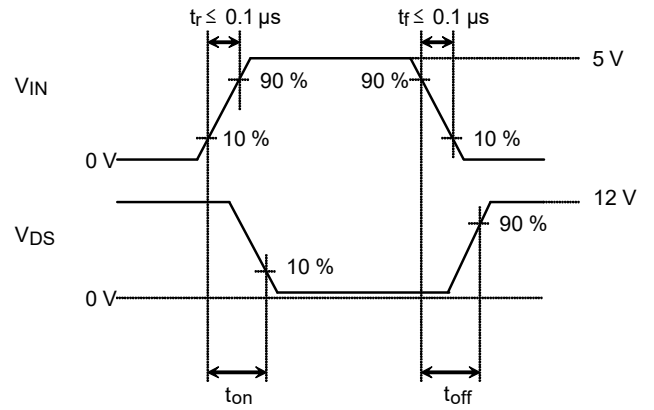


Figure 12.2 Switching time waveforms

13. Characteristic curves

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

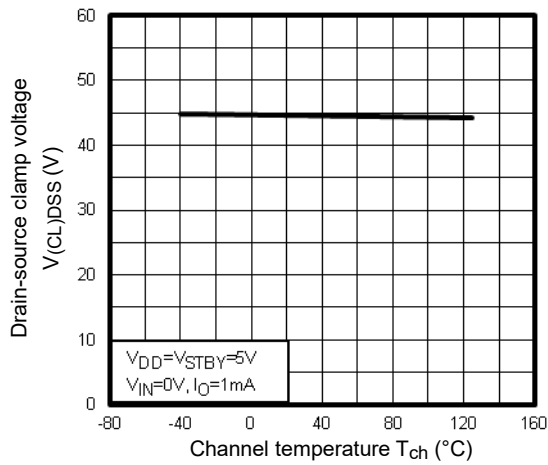


Figure 13.1 $V_{(CL)DSS} - T_{ch}$

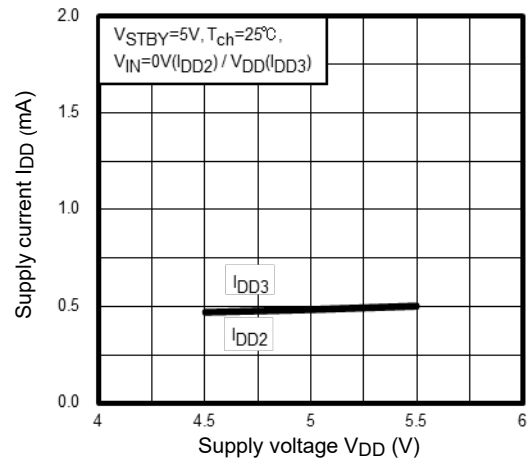


Figure 13.2 $I_{DD} - V_{DD}$

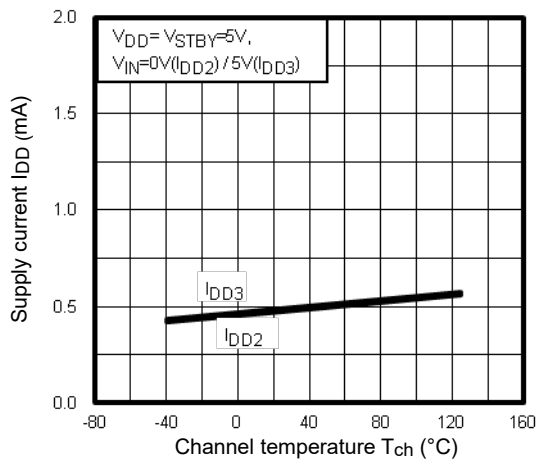


Figure 13.3 $I_{DD} - T_{ch}$

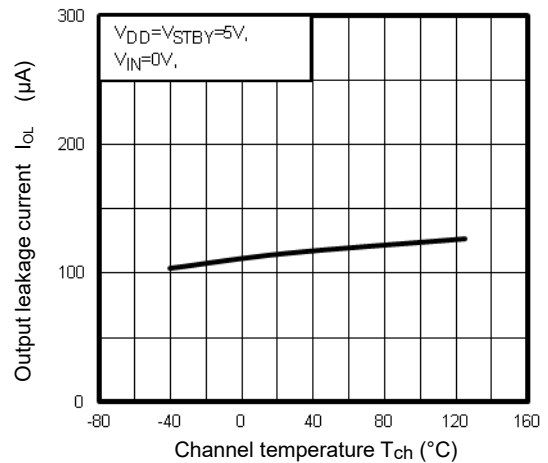


Figure 13.4 $I_{OL} - T_{ch}$

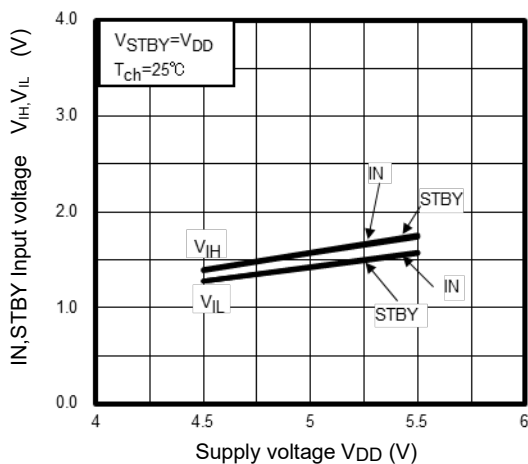


Figure 13.5 $V_{IH}, V_{IL} - V_{DD}$

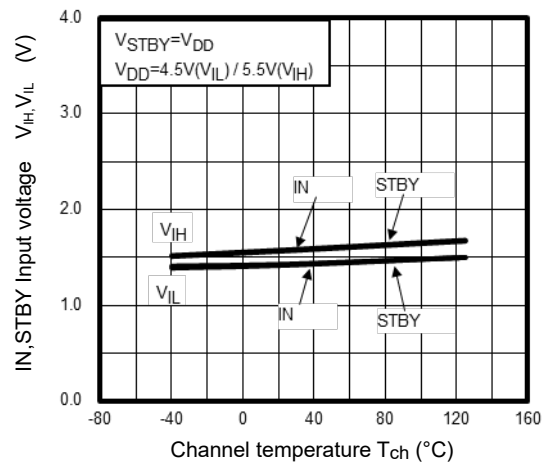


Figure 13.6 $V_{IH}, V_{IL} - T_{ch}$

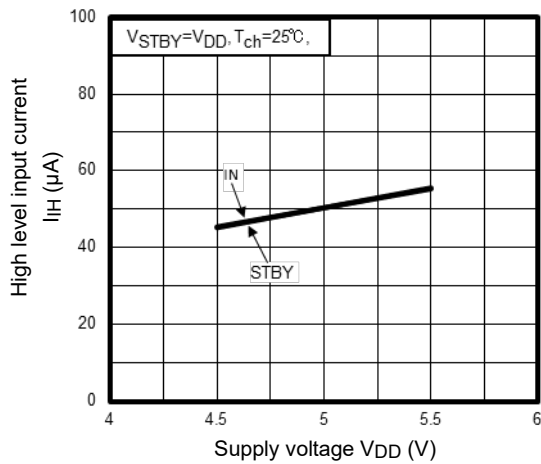


Figure 13.7 $I_{IH} - V_{DD}$

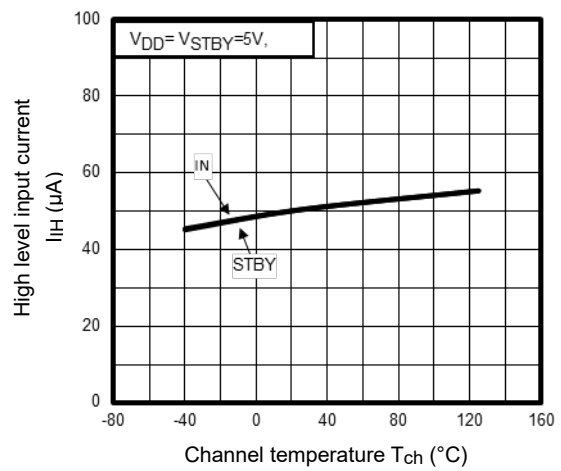


Figure 13.8 $I_{IH} - T_{ch}$

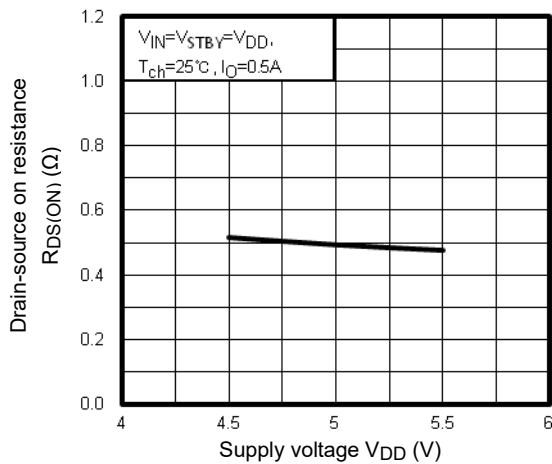


Figure 13.9 $R_{DS(ON)} - V_{DD}$

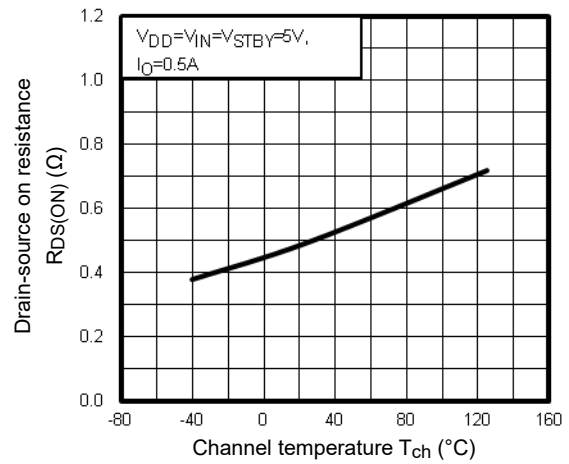


Figure 13.10 $R_{DS(ON)} - T_{ch}$

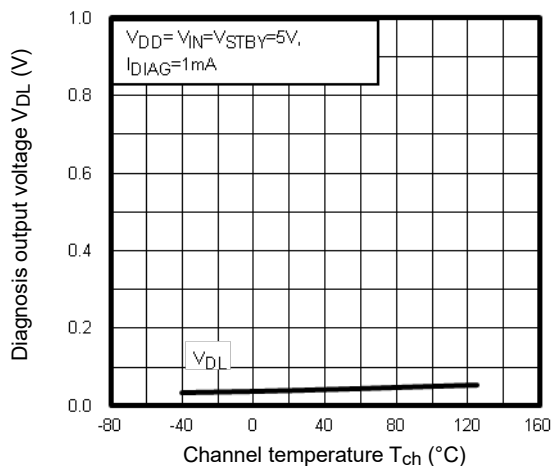


Figure 13.11 $V_{DL} - T_{ch}$

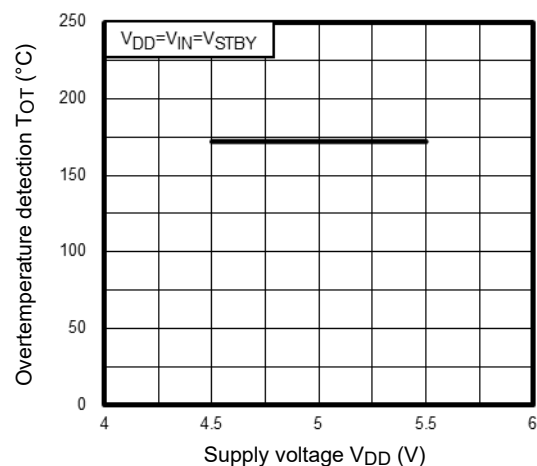


Figure 13.12 $T_{OT} - V_{DD}$

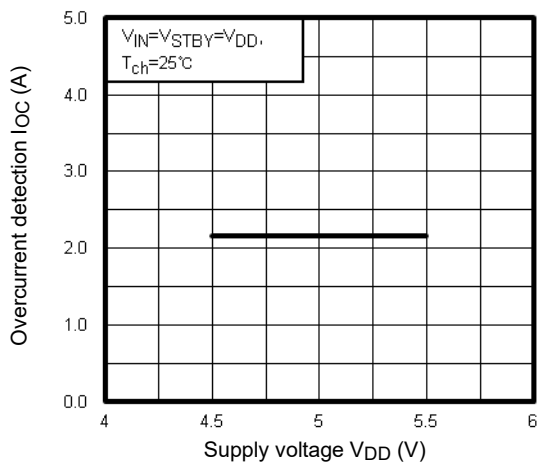


Figure 13.13 $I_{oc} - V_{DD}$

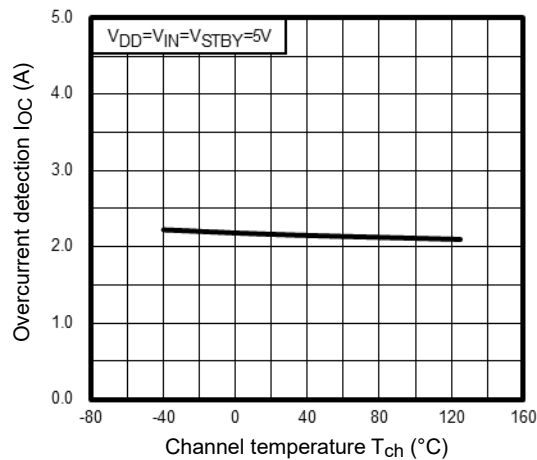


Figure 13.14 $I_{oc} - T_{ch}$

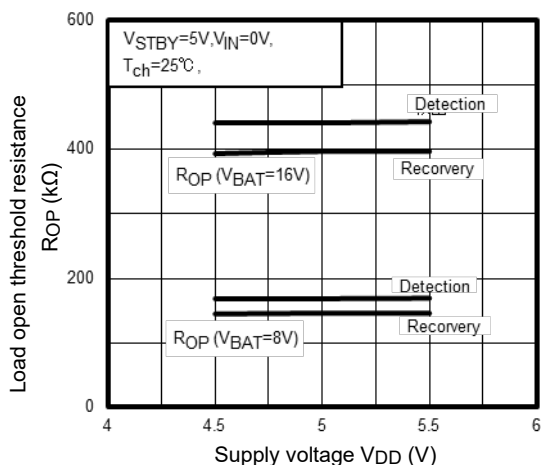


Figure 13.15 $R_{OP} - V_{DD}$

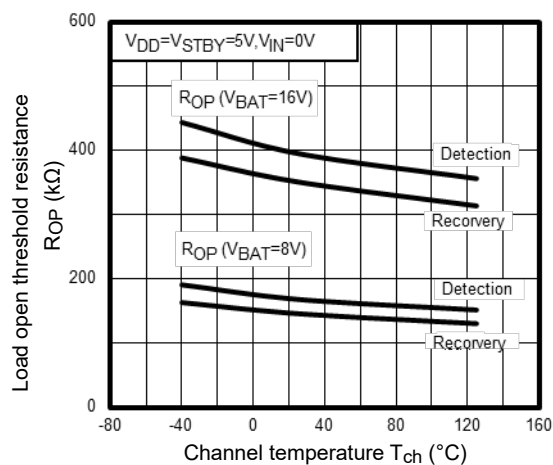


Figure 13.16 $R_{OP} - T_{ch}$

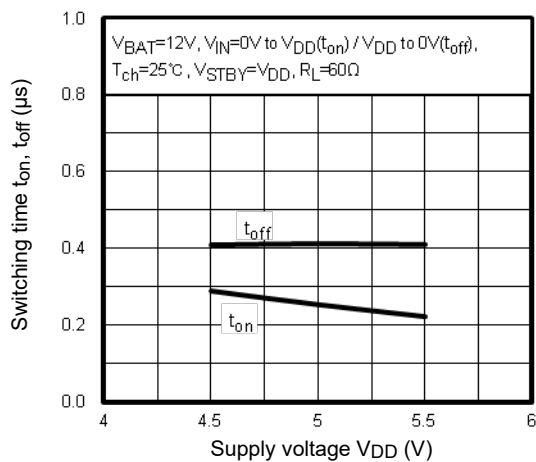


Figure 13.17 $t_{on}, t_{off} - V_{DD}$

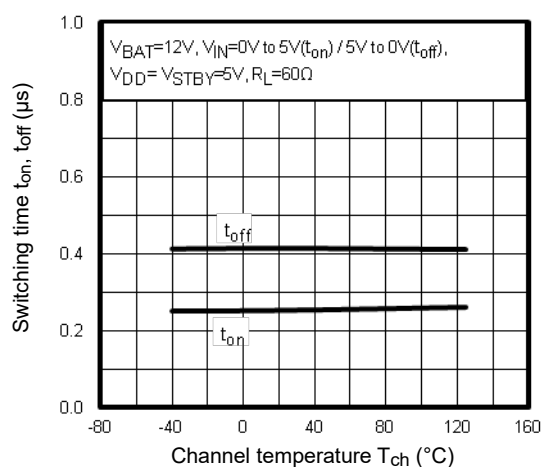


Figure 13.18 $t_{on}, t_{off} - T_{ch}$

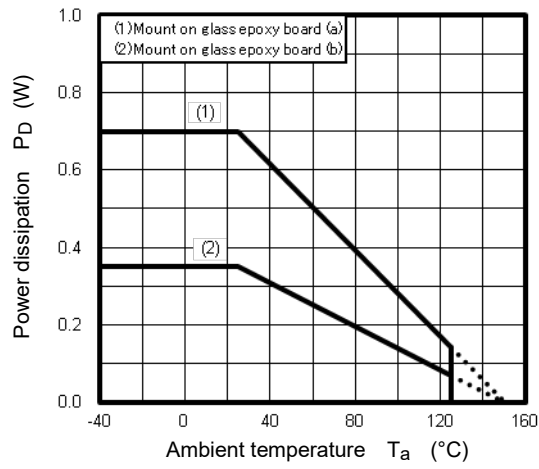
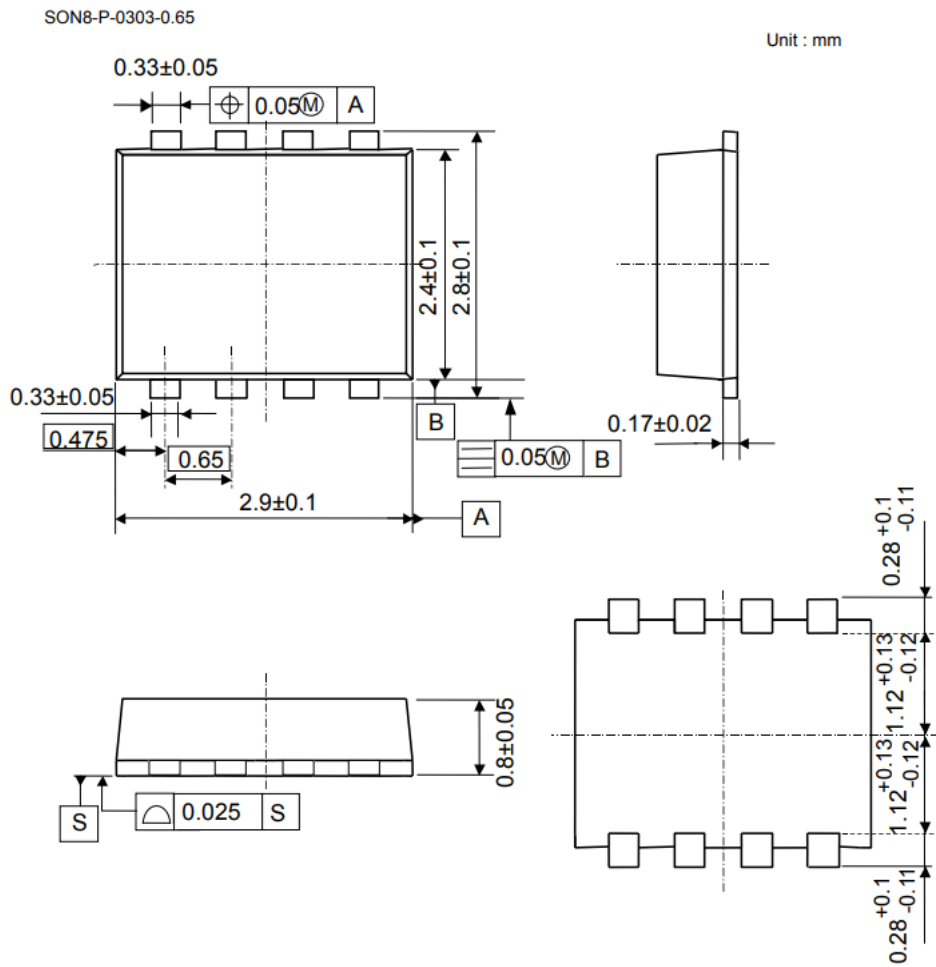


Figure 13.19 $P_D - T_a$

14. Package Information

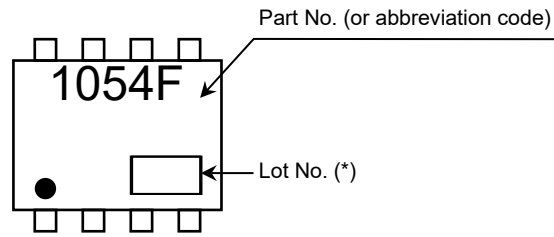
14.1. Package Dimensions



Weight: 0.017 g (Typ.)

Figure 14.1 Package Dimensions

14.2. Marking



Note: ● on the lower left of the marking indicates Pin 1

* Weekly code: (Three digits)



Week of manufacture

(01 for first week of year; continuing up to 52 or 53)

Year of manufacture

(The last digit of the calendar year)

Figure 14.2 Marking

14.3. Land Pattern Dimensions for Reference only

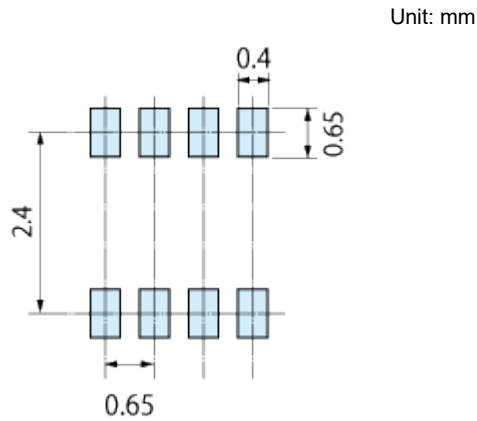


Figure 14.3 Land Pattern Dimensions for Reference only

15. IC Usage Considerations

15.1. Notes on Handling of ICs

The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. None of the multiple ratings can be exceeded. Exceeding the absolute maximum ratings may cause destruction, damage and deterioration, and may result in injury due to explosion or burning.

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