

TK2P90E

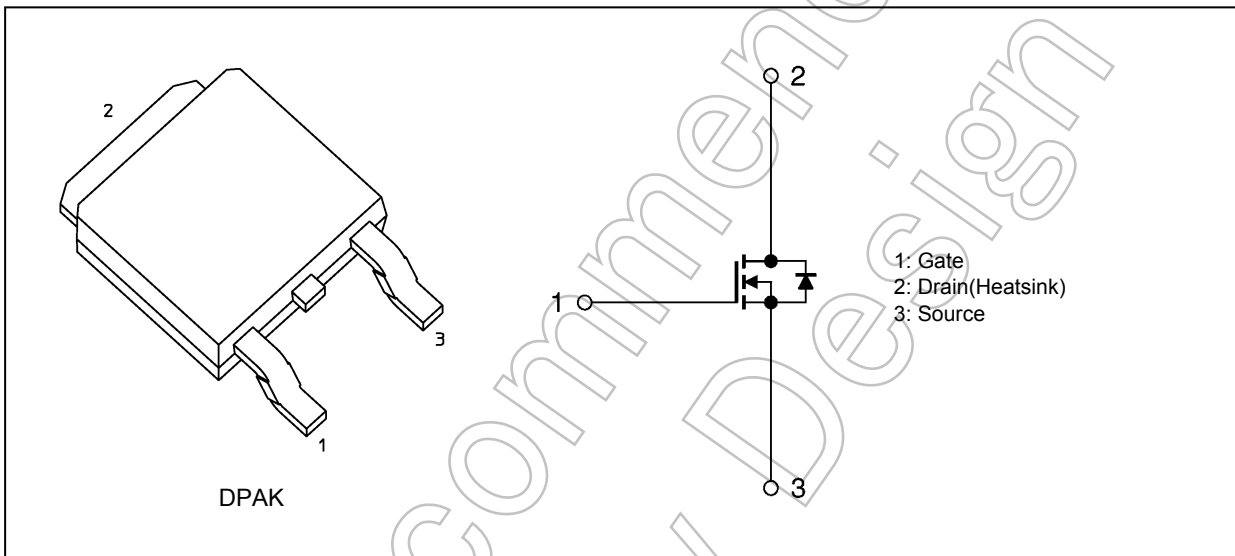
1. Applications

- Switching Voltage Regulators

2. Features

- (1) Low drain-source on-resistance: $R_{DS(ON)} = 4.7 \Omega$ (typ.)
- (2) Low leakage current : $I_{DSS} = 10 \mu A$ (max) ($V_{DS} = 720 V$)
- (3) Enhancement mode: $V_{th} = 2.5$ to $4.0 V$ ($V_{DS} = 10 V, I_D = 0.2 mA$)

3. Packaging and Internal Circuit



4. Absolute Maximum Ratings (Note) ($T_a = 25^\circ C$ unless otherwise specified)

Characteristics	Symbol	Rating	Unit
Drain-source voltage	V_{DSS}	900	V
Gate-source voltage	V_{GSS}	± 30	
Drain current (DC)	I_D (Note 1)	2	A
Drain current (pulsed)	I_{DP} (Note 1)	6	
Power dissipation	P_D ($T_c = 25^\circ C$)	80	W
Single-pulse avalanche energy	E_{AS} (Note 2)	157	mJ
Avalanche current	I_{AR}	2	A
Reverse drain current (DC)	I_{DR} (Note 1)	2	
Reverse drain current (pulsed)	I_{DRP} (Note 1)	6	
Channel temperature	T_{ch}	150	$^\circ C$
Storage temperature	T_{stg}	-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Start of commercial production

2014-02

5. Thermal Characteristics

Characteristics	Symbol	Max	Unit
Channel-to-case thermal resistance	$R_{th(ch-c)}$	1.56	°C/W

Note 1: Ensure that the channel temperature does not exceed 150 °C.

Note 2: $V_{DD} = 90\text{ V}$, $T_{ch} = 25^\circ\text{C}$ (initial), $L = 72.3\text{ mH}$, $R_G = 25\ \Omega$, $I_{AR} = 2\text{ A}$

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

Not Recommended for New Design

6. Electrical Characteristics

6.1. Static Characteristics ($T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	I_{GSS}	$V_{GS} = \pm 30\text{ V}, V_{DS} = 0\text{ V}$	—	—	± 1	μA
Drain cut-off current	I_{DSS}	$V_{DS} = 720\text{ V}, V_{GS} = 0\text{ V}$	—	—	10	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 10\text{ mA}, V_{GS} = 0\text{ V}$	900	—	—	V
Gate threshold voltage	V_{th}	$V_{DS} = 10\text{ V}, I_D = 0.2\text{ mA}$	2.5	—	4.0	
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS} = 10\text{ V}, I_D = 1.0\text{ A}$	—	4.7	5.9	Ω

6.2. Dynamic Characteristics ($T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	C_{iss}	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	—	500	—	μF
Reverse transfer capacitance	C_{rss}		—	4	—	
Output capacitance	C_{oss}		—	40	—	
Gate resistance	r_g	$V_{DS} = \text{OPEN}, f = 1\text{ MHz}$	—	5	—	Ω
Switching time (rise time)	t_r	See Fig. 6.2.1.	—	25	—	ns
Switching time (turn-on time)	t_{on}		—	50	—	
Switching time (fall time)	t_f		—	22	—	
Switching time (turn-off time)	t_{off}		—	70	—	
MOSFET dv/dt ruggedness	dv/dt	$V_{DD} = 0\text{ to }400\text{ V}, I_D = 2\text{ A}$	10	—	—	V/ns

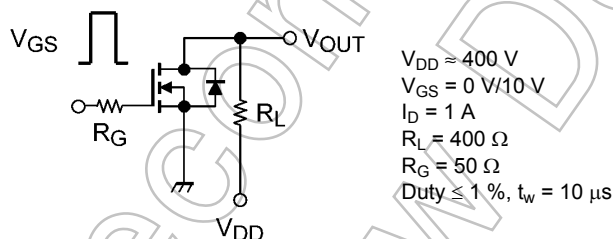


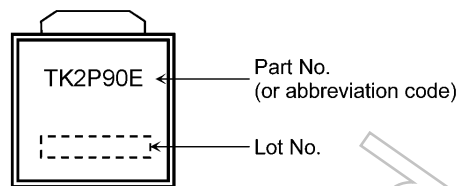
Fig. 6.2.1 Switching Time Test Circuit

6.3. Gate Charge Characteristics ($T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Q_g	$V_{DD} \approx 400\text{ V}, V_{GS} = 10\text{ V}, I_D = 2\text{ A}$	—	12	—	nC
Gate-source charge 1	Q_{gs1}		—	4	—	
Gate-drain charge	Q_{gd}		—	5	—	

6.4. Source-Drain Characteristics ($T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Diode forward voltage	V_{DSF}	$I_{DR} = 2\text{ A}, V_{GS} = 0\text{ V}$	—	—	-1.7	V
Reverse recovery time	t_{rr}	$I_{DR} = 2\text{ A}, V_{GS} = 0\text{ V}$ $-di_{DR}/dt = 100\text{ A}/\mu\text{s}$	—	800	—	ns
Reverse recovery charge	Q_{rr}		—	3.5	—	μC
Peak reverse recovery current	I_{rr}		—	11	—	A

7. Marking**Fig. 7.1 Marking**

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8. Characteristics Curves (Note)

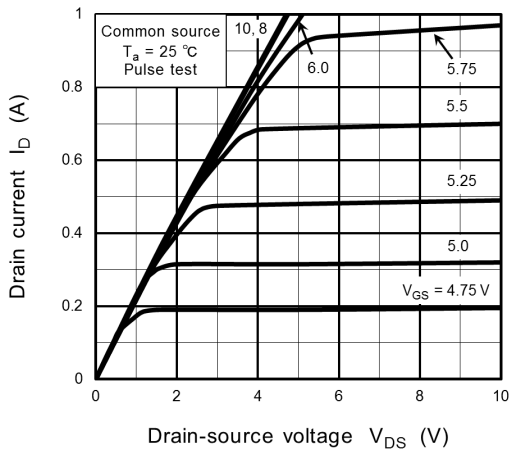


Fig. 8.1 $I_D - V_{DS}$

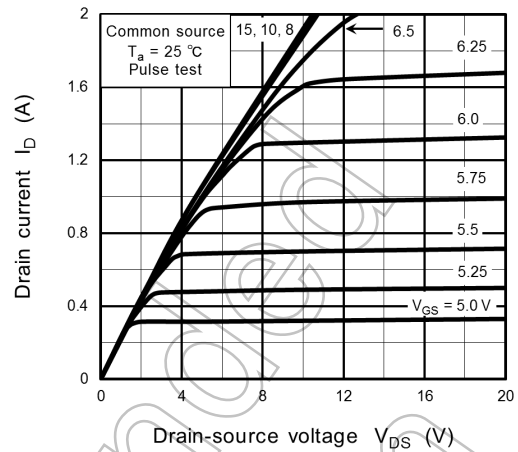


Fig. 8.2 $I_D - V_{DS}$

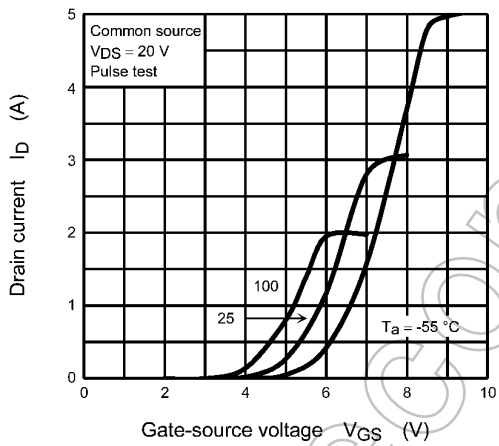


Fig. 8.3 $I_D - V_{GS}$

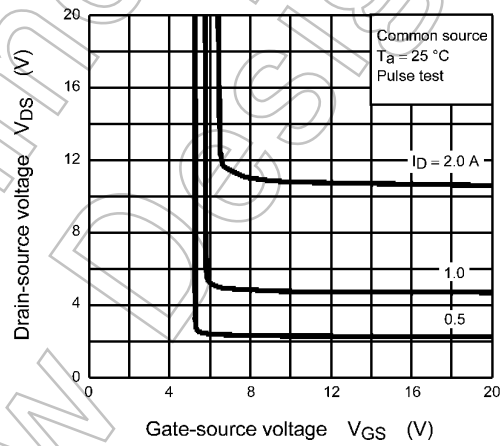


Fig. 8.4 $V_{DS} - V_{GS}$

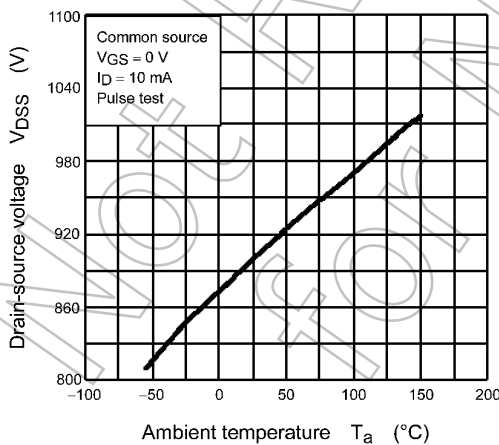


Fig. 8.5 $V_{DSS} - T_a$

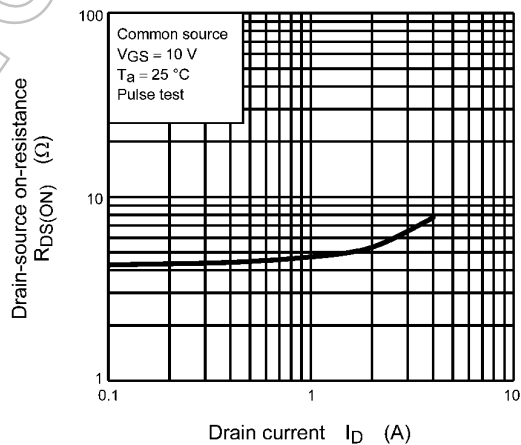


Fig. 8.6 $R_{DS(ON)} - I_D$

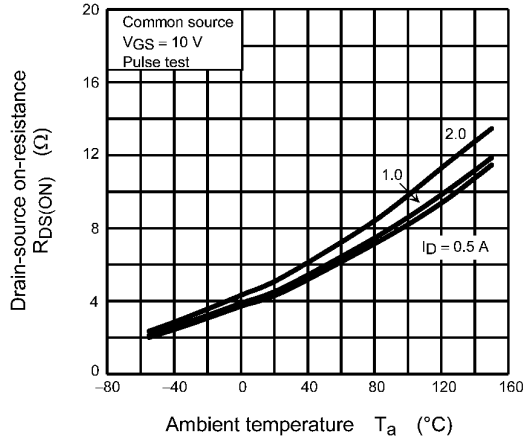


Fig. 8.7 $R_{DS(ON)} - T_a$

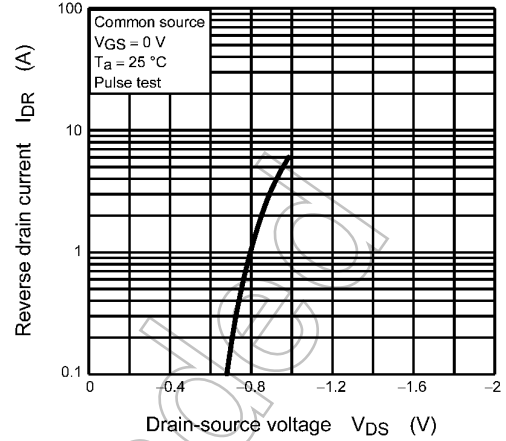


Fig. 8.8 $I_{DR} - V_{DS}$

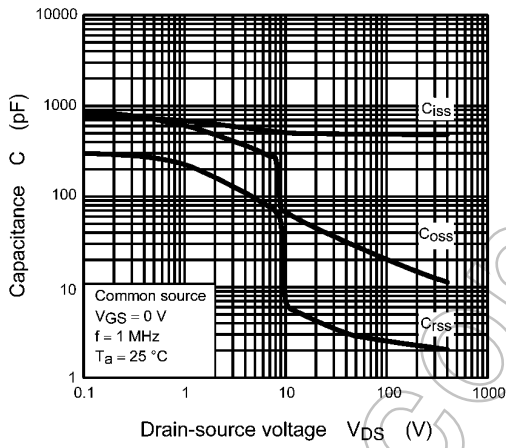


Fig. 8.9 $C - V_{DS}$

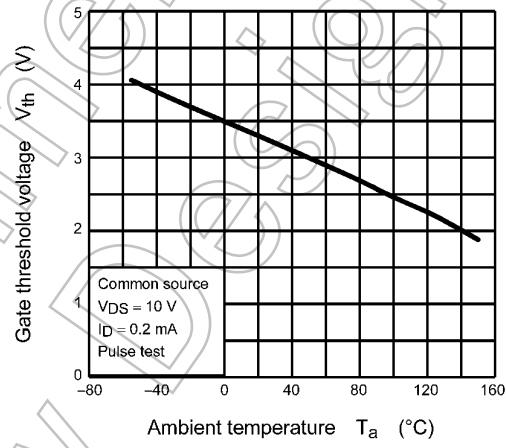


Fig. 8.10 $V_{th} - T_a$

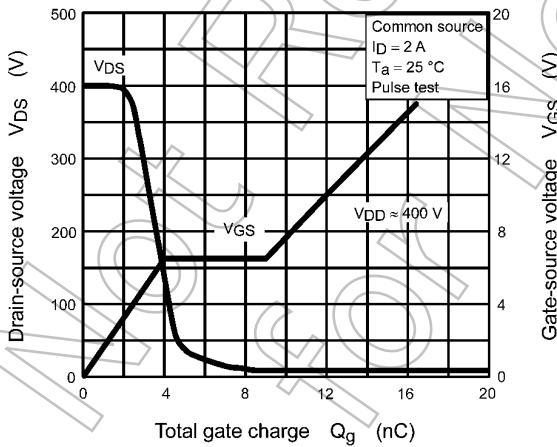


Fig. 8.11 Dynamic Input/Output Characteristics

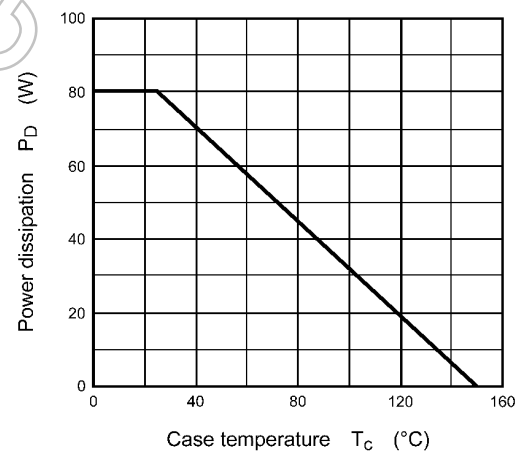


Fig. 8.12 $P_D - T_c$
(Guaranteed Maximum)

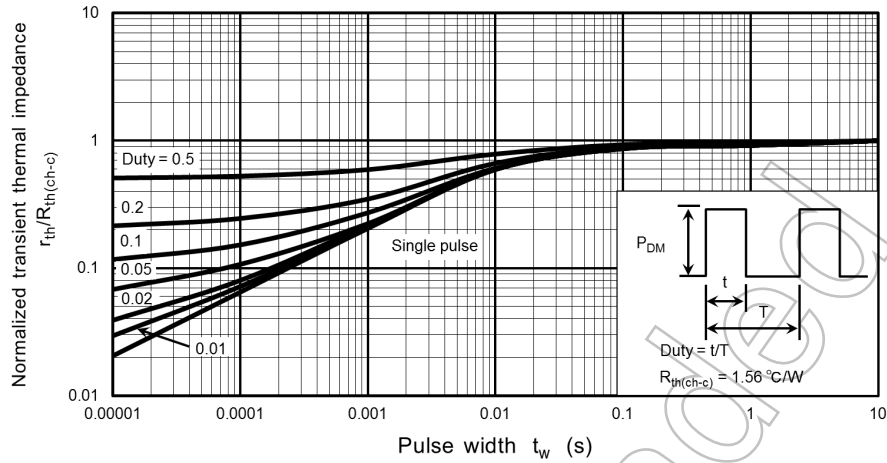


Fig. 8.13 $r_{th} - t_w$
(Guaranteed Maximum)

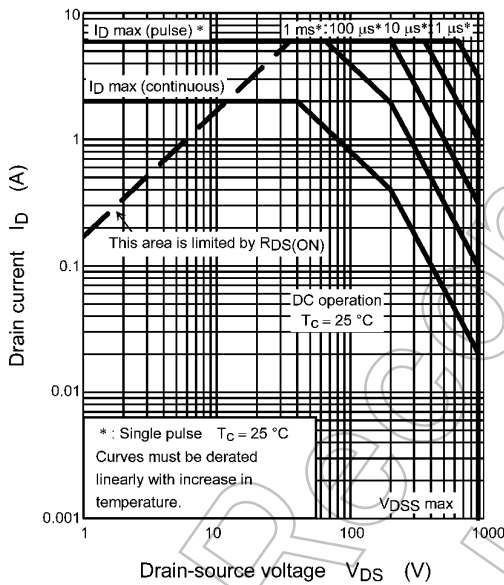


Fig. 8.14 Safe Operating Area
(Guaranteed Maximum)

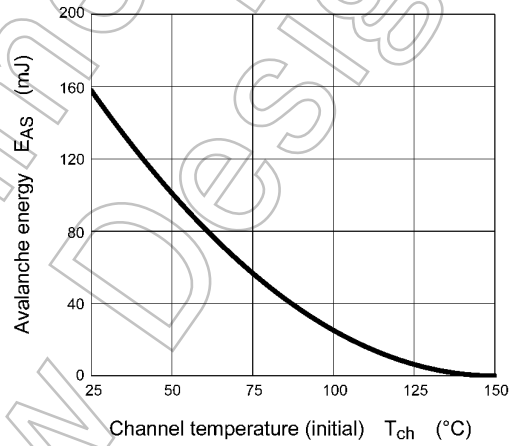
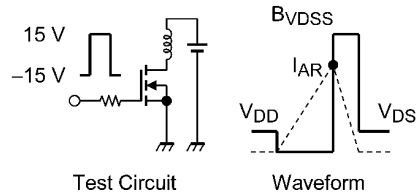


Fig. 8.15 $E_{AS} - T_{ch}$
(Guaranteed Maximum)



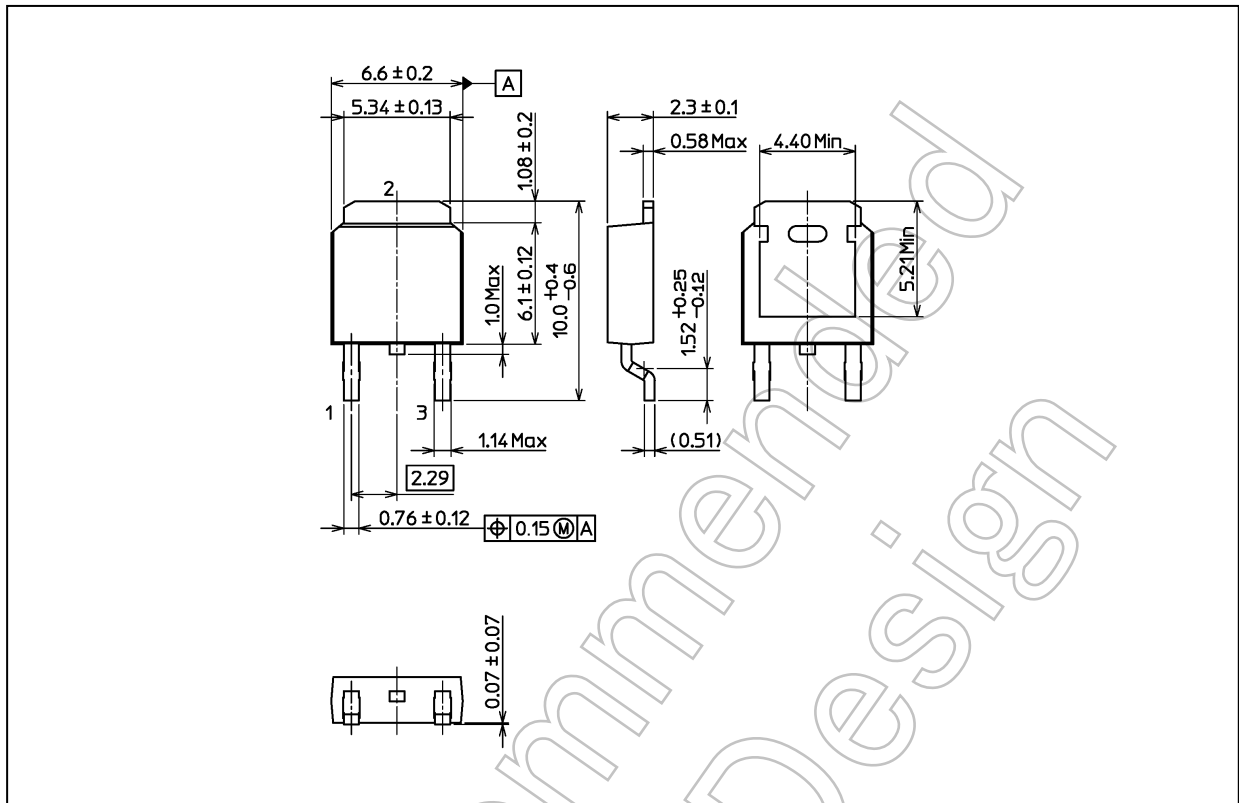
$$R_G = 25 \Omega, V_{DD} = 90 \text{ V } E_{AS} = \frac{1}{2} \cdot L \cdot I_{AR}^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

Fig. 8.16 Test Circuit/Waveform

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Package Dimensions

Unit: mm



Weight: 0.36 g (typ.)

Package Name(s)
TOSHIBA: 2-7K1S
Nickname: DPAK

Not Recommended for New Design

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