

Toshiba Intelligent Power Device Silicon Monolithic MOS Integrated Circuit

# TPD2017FN

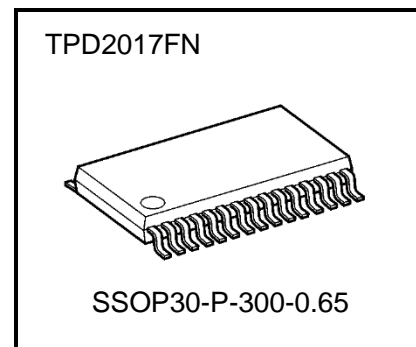
Low side switch (8-channels) for motors, solenoids, lamp drives

## 1. Description

TPD2017FN is a low-side switch (8 channels) with MOS FET out. This is the monolithic power IC that can be driven directly from CMOS, TTL logic circuitry (MCUs, etc.) and have overcurrent and thermal protection features.

## 2. Applications

- Programmable logic controller for Industrial Use.
- Driving resistant load and inductive loads.



Weight: 0.176 g (Typ.)

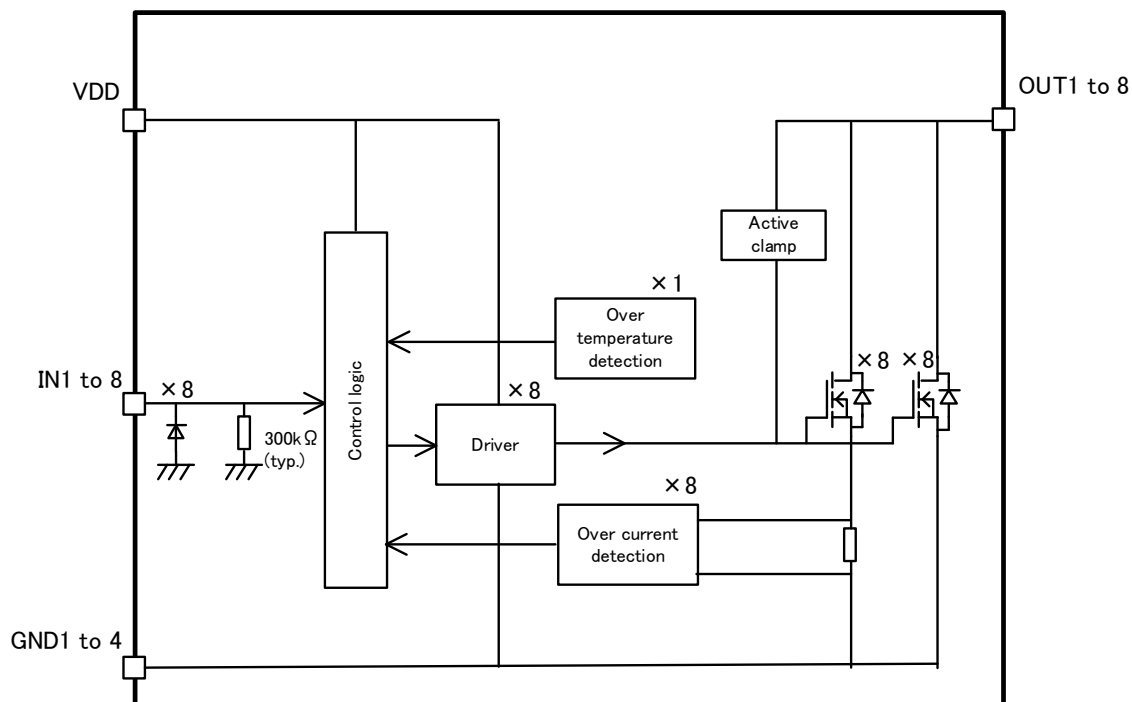
## 3. Features

- 8-channels of N-channel MOSFET are built-in.
- This IC can drive the power load directly.
- Built-in protection against over temperature and over current.
- 8-channels access enables space-saving design.
- Low voltage operation is possible : 2.7 V
- Low on resistance :  $0.55\Omega$  (max) @  $V_{IN} = 5V$ ,  $I_{OUT} = 0.5A$ ,  $T_j = 25^\circ C$  (per channels)
- Parallel operation is possible.
- Built-in active clamp circuit.
- SSOP30 packaging (300 mils) is embossed taping.

Note: This product has a MOS structure. Be careful of static electricity when handling it.

Start of commercial production  
2022-05

## 4. Block Diagram

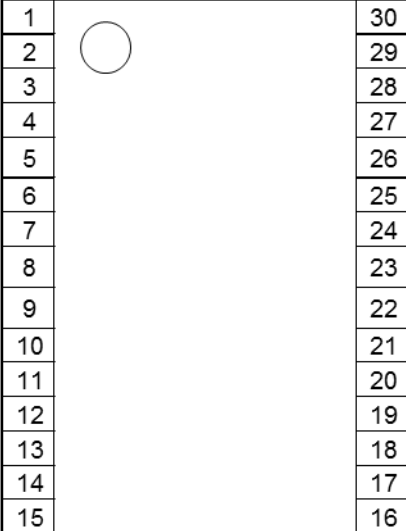


Note: Some of the functional blocks, circuits, constants, etc. in the block diagram are omitted and simplified.

Figure 4.1 Block Diagram

## 5. Pin Assignments

(TOP VIEW)



GND1	1	30	NC
GND2	2	29	NC
NC	3	28	NC
VDD	4	27	NC
IN1	5	26	OUT1
IN2	6	25	OUT2
IN3	7	24	OUT3
IN4	8	23	OUT4
IN5	9	22	OUT5
IN6	10	21	OUT6
IN7	11	20	OUT7
IN8	12	19	OUT8
NC	13	18	NC
GND3	14	17	NC
GND4	15	16	NC

**Figure 5.1 Pin Assignments**

## 6. Pin Description

**Table 6.1 Pin Description**

Pin No.	Symbol	I/O	Pin Description
1	GND1	-	GND pin.
2	GND2	-	GND pin.
3	NC	-	No-Connect pin.
4	VDD	-	Power supply pin.
5	IN1	IN	Input pin for channel 1. Built in pull down resistor (300kΩ typ.).
6	IN2	IN	Input pin for channel 2. Built in pull down resistor (300kΩ typ.).
7	IN3	IN	Input pin for channel 3. Built in pull down resistor (300kΩ typ.).
8	IN4	IN	Input pin for channel 4. Built in pull down resistor (300kΩ typ.).
9	IN5	IN	Input pin for channel 5. Built in pull down resistor (300kΩ typ.).
10	IN6	IN	Input pin for channel 6. Built in pull down resistor (300kΩ typ.).
11	IN7	IN	Input pin for channel 7. Built in pull down resistor (300kΩ typ.).
12	IN8	IN	Input pin for channel 8. Built in pull down resistor (300kΩ typ.).
13	NC	-	No-Connect pin.
14	GND3	-	GND pin.
15	GND4	-	GND pin.
16	NC	-	No-Connect pin.
17	NC	-	No-Connect pin.
18	NC	-	No-Connect pin.
19	OUT8	OUT	Output pin of channel 8.
20	OUT7	OUT	Output pin of channel 7.
21	OUT6	OUT	Output pin of channel 6.
22	OUT5	OUT	Output pin of channel 5.
23	OUT4	OUT	Output pin of channel 4.
24	OUT3	OUT	Output pin of channel 3.
25	OUT2	OUT	Output pin of channel 2.
26	OUT1	OUT	Output pin of channel 1.
27	NC	-	No-Connect pin.
28	NC	-	No-Connect pin.
29	NC	-	No-Connect pin.
30	NC	-	No-Connect pin.

## 7. Operational Description

### 7.1. Over temperature protection

To prevent destruction due to temperature rise, this product is equipped with one channel of a built-in over temperature detection circuit that turns off all outputs when the junction temperature exceeds the over temperature detection ( $T_{SD}$ ). When the junction temperature falls below the hysteresis set temperature ( $T_{SD}-\Delta T_{SD}$ ), the unit recovers to normal operation.

### 7.2. Over current protection

Each output has a built-in over current protection circuit. If the output current exceeds the over current detection value ( $I_{OC}$ ) due to a load short, etc., the output is turned off during the over current protection operating time ( $t_{OFF-DUTY}$ ). After that, the output returns, if the over current condition continues, the output will again be turned off for the over current protection operating time ( $t_{OFF-DUTY}$ ).

### 7.3. Timing chart

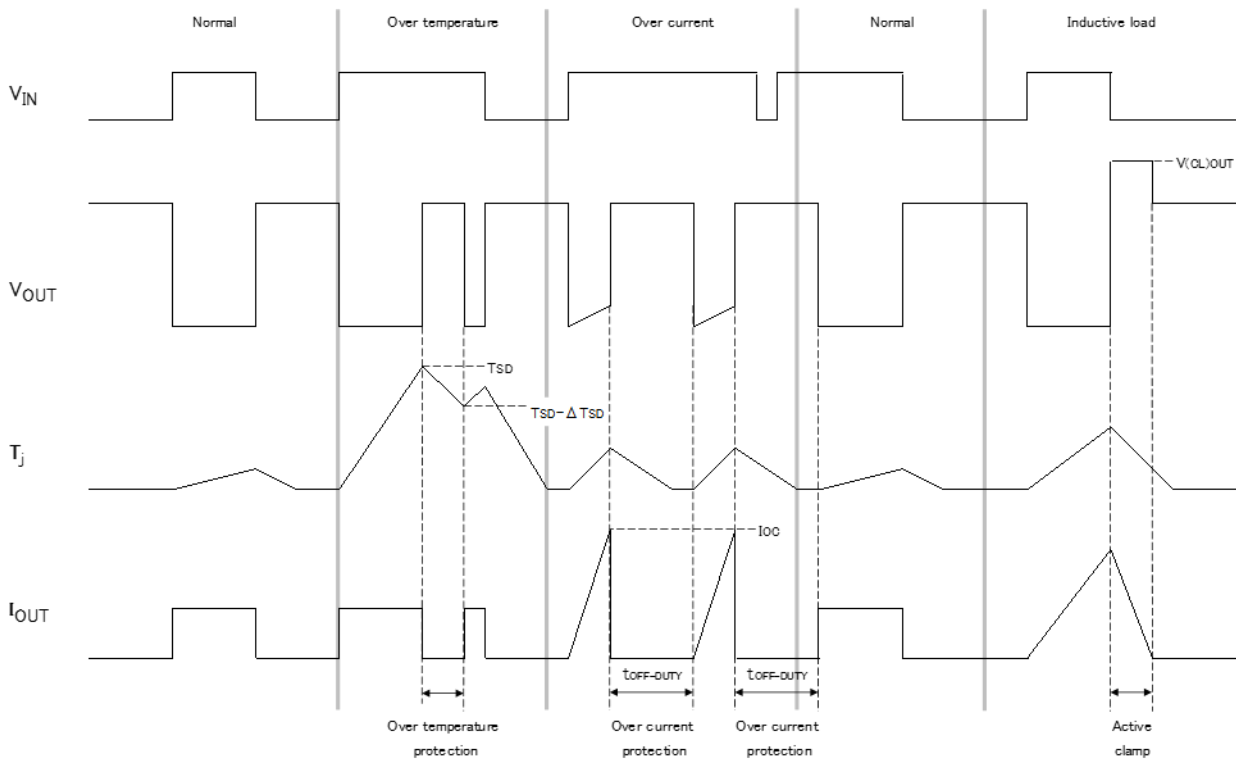


Figure 7.1 Timing chart

## 7.4. Truth table

**Table 7.1 Truth table**

Input	Output	Operating state
L	H	Normal
H	L	
L	H	Over current protection ( Load short circuit )
H	Switching	
L	H	Over temperature protection
H	H	

## 8. Absolute Maximum Ratings

**Table 8.1 Absolute Maximum Ratings (Note)**

 (T<sub>a</sub> = 25°C unless otherwise specified)

Characteristics	Symbol	Rating	Unit
Supply voltage	V <sub>DD</sub>	-0.3 to 6.0	V
Input voltage	V <sub>IN</sub>	-0.3 to 6.0	V
Output withstand voltage	V <sub>OUT</sub>	50.0 (Note 1)	V
Output current	I <sub>OUT</sub>	Internally limited	A
Power dissipation (operation all channels, T <sub>a</sub> =25°C )	P <sub>D</sub>	1.8	W
Operating temperature	T <sub>opr</sub>	-40 to 110	°C
Junction temperature	T <sub>j</sub>	150	°C
Storage temperature	T <sub>stg</sub>	-55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Not subject to production test.

### 8.1. Thermal Resistance

**Table 8.2 Thermal resistance**

Characteristics	Symbol	Rating	Unit
Thermal resistance ( junction to ambient )	R <sub>th(j-a)</sub>	70	°C / W

Note: JEDEC Standard.

Glass epoxy board

Material: FR-4(4 layer)

Board size: 76.2mm x 114.3mm x 1.6mm

## 9. Operating Ranges

**Table 9.1 Operating supply voltage**

Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
Operating supply voltage	$V_{DD(opr)}$	$T_j = 25^\circ\text{C}$	2.7	-	5.5	V

## 10. Electrical Characteristics

**Table 10.1 Electrical Characteristics**

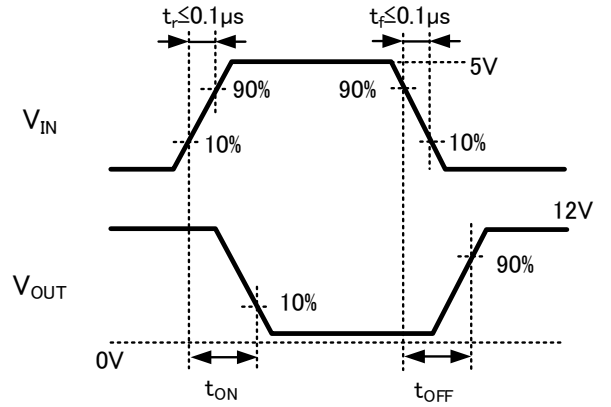
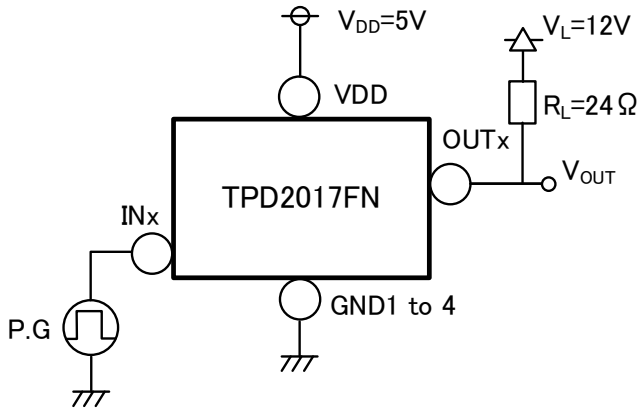
 ( $T_j = 25^\circ\text{C}$ ,  $V_{DD} = 2.7$  to  $5.5\text{V}$  unless otherwise specified)

Characteristics		Symbol	Test condition	Min	Typ.	Max	Unit
Output clamp voltage		$V_{(CL)OUT}$	$I_{OUT} = 10\text{mA}$ , $V_{IN} = 0\text{V}$	40	-	50	V
Supply current		$I_{DD(OFF)}$	$V_{DD} = 5\text{V}$ , $V_{IN} = 0\text{V}$	-	1.8	2.6	mA
		$I_{DD(ON)}$	$V_{DD} = 5\text{V}$ , $V_{IN} = 5\text{V}$ , All outputs open	-	2.2	3.1	mA
Input voltage	“L” level	$V_{IL}$	-	-	-	0.8	V
	“H” level	$V_{IH}$	-	2.0	-	-	
Input current		$I_{IL}$	$V_{IN} = 0\text{V}$	-1.0	-	1.0	$\mu\text{A}$
		$I_{IH}$	$V_{IN} = 5\text{V}$	-	17	23	
On resistance		$R_{DS(ON)}$	$V_{DD} = 5\text{V}$ , $V_{IN} = 5\text{V}$ , $I_{OUT} = 0.5\text{A}$	-	0.40	0.55	$\Omega$
Output leakage current		$I_{OL}$	$V_L = 40\text{V}$ , $V_{IN} = 0\text{V}$ , Per output	-	-	10	$\mu\text{A}$
Over current detection		$I_{OC}$	$V_{DD} = 5\text{V}$	1.0	1.5	2.5	A
Over current protection operation time		$t_{OFF-DUTY}$	$V_{DD} = 5\text{V}$	1.5	3.0	4.8	ms
Over temperature detection	Temperature	$T_{SD}$	$V_{DD} = 5\text{V}$	150	175	200	$^\circ\text{C}$
	Hysteresis	$\Delta T_{SD}$	$V_{DD} = 5\text{V}$	5	15	25	
Switching time		$t_{ON}$	Refer to test circuit 1	5	10	18	$\mu\text{s}$
		$t_{OFF}$		3	8	15	
Single pulse energy		$E_S$	$T_a = 25^\circ\text{C}$ , $I_{OUT} = 0.75\text{A}$ (1-channel operation)	30	150 <sup>(Note 2)</sup>	-	mJ

Note 2: Not subject to production test.

**11. Test circuit**

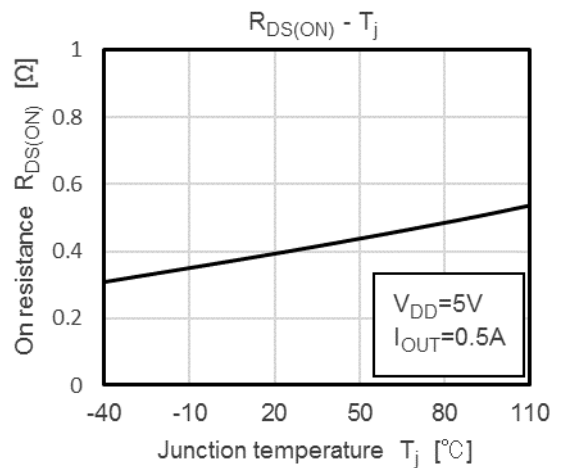
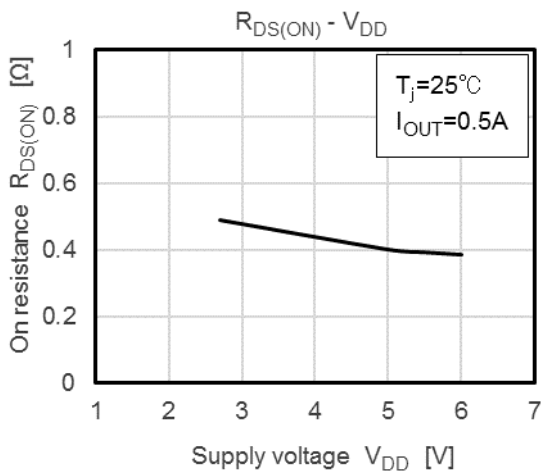
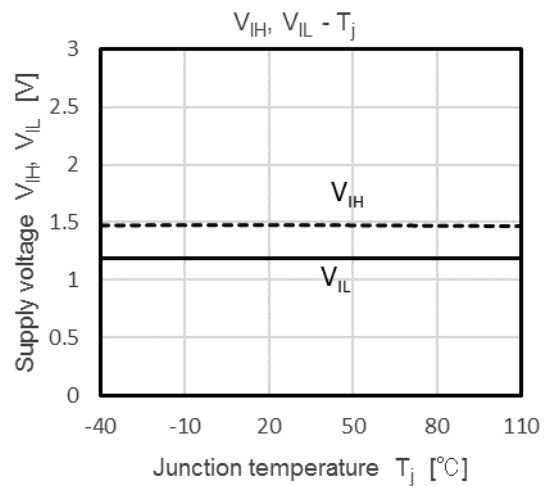
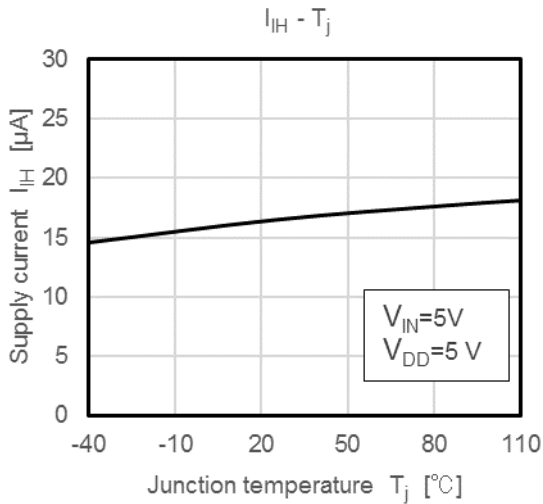
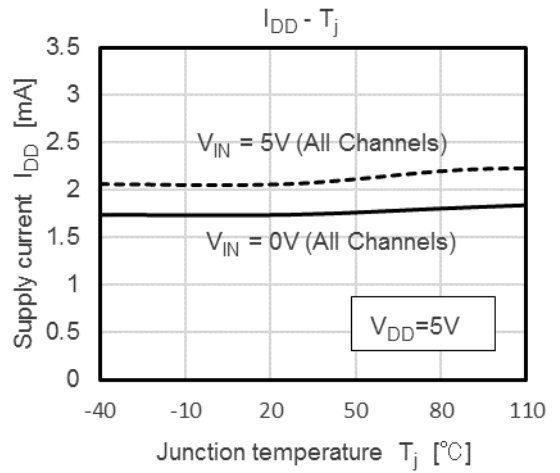
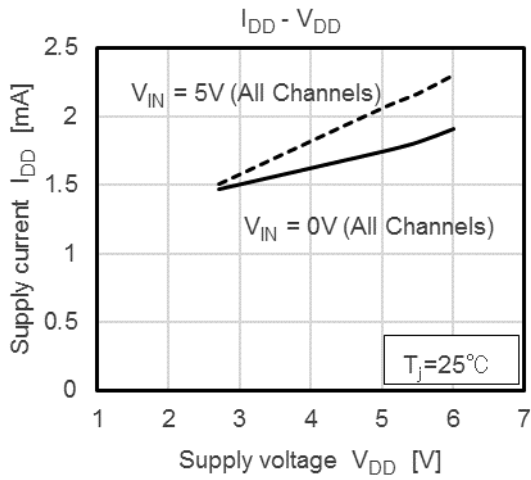
**11.1. Test circuit 1**

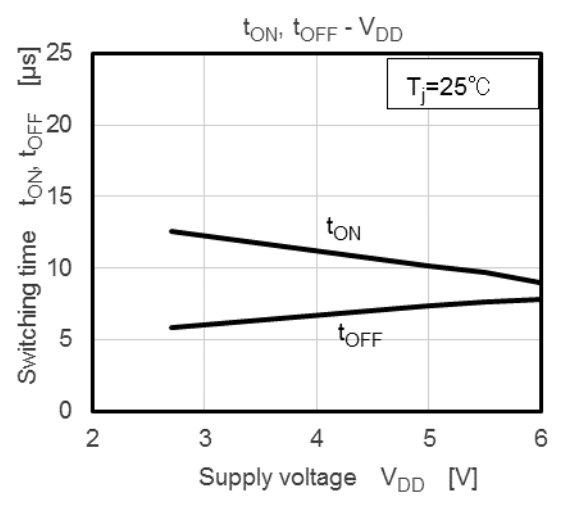
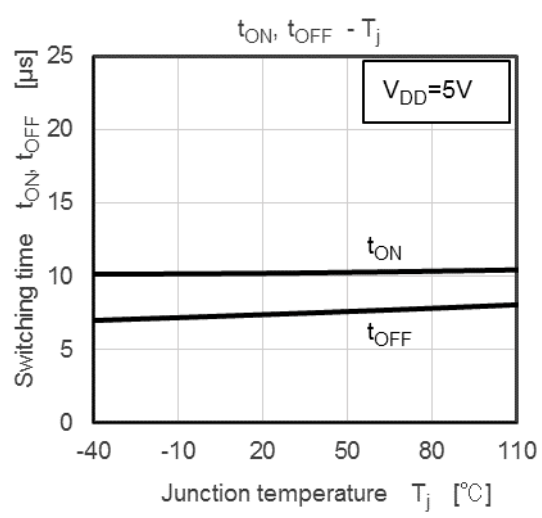
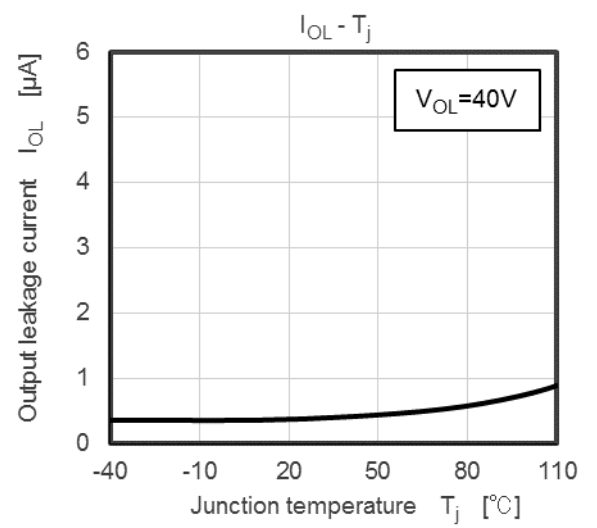
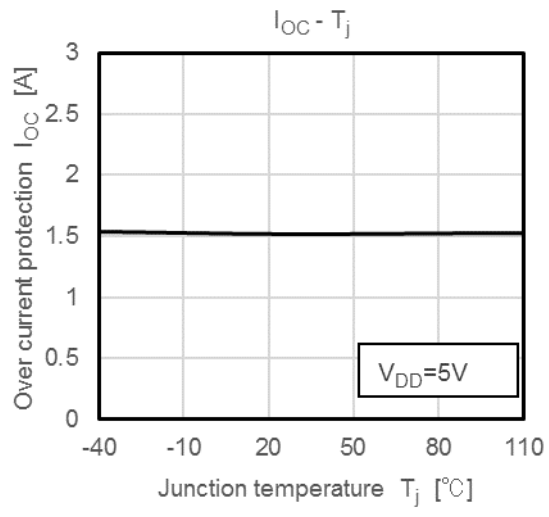
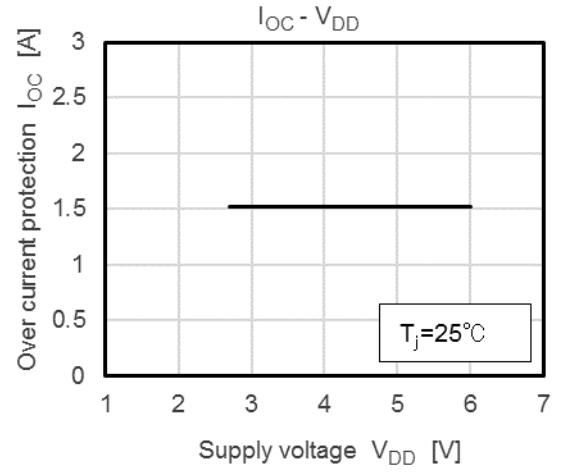
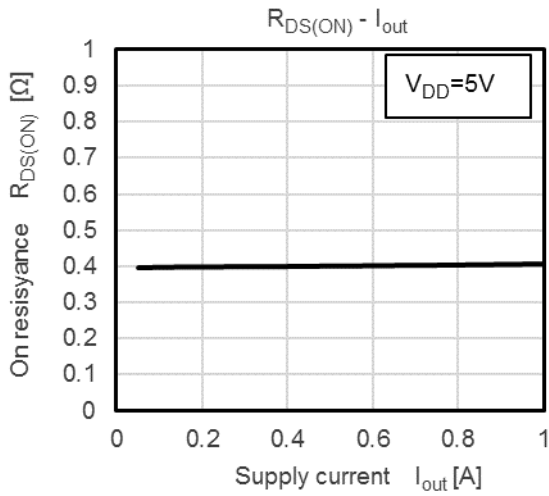


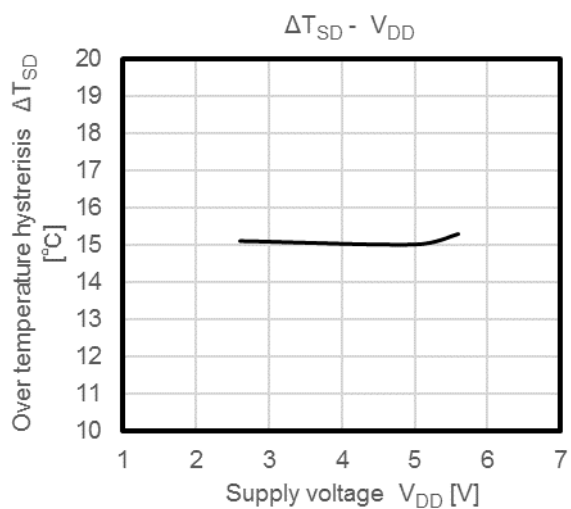
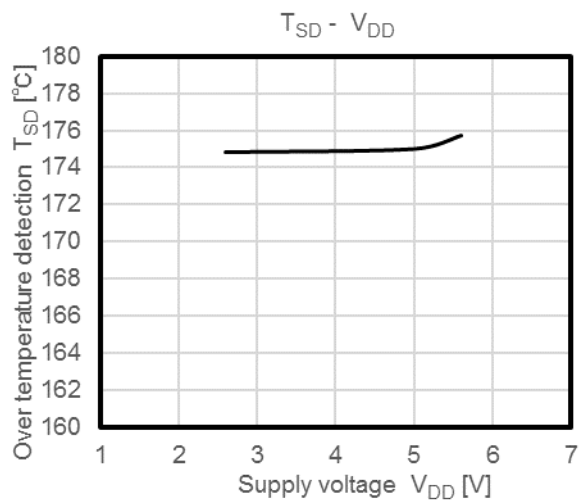
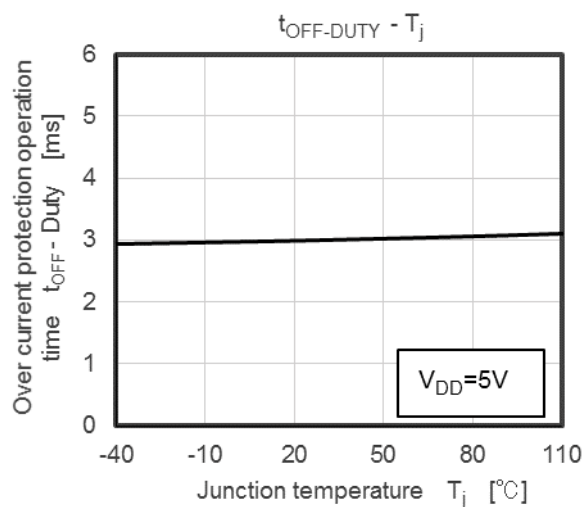
**Figure 11.1 Switching time measurement circuit**

**12. Characteristic curves**

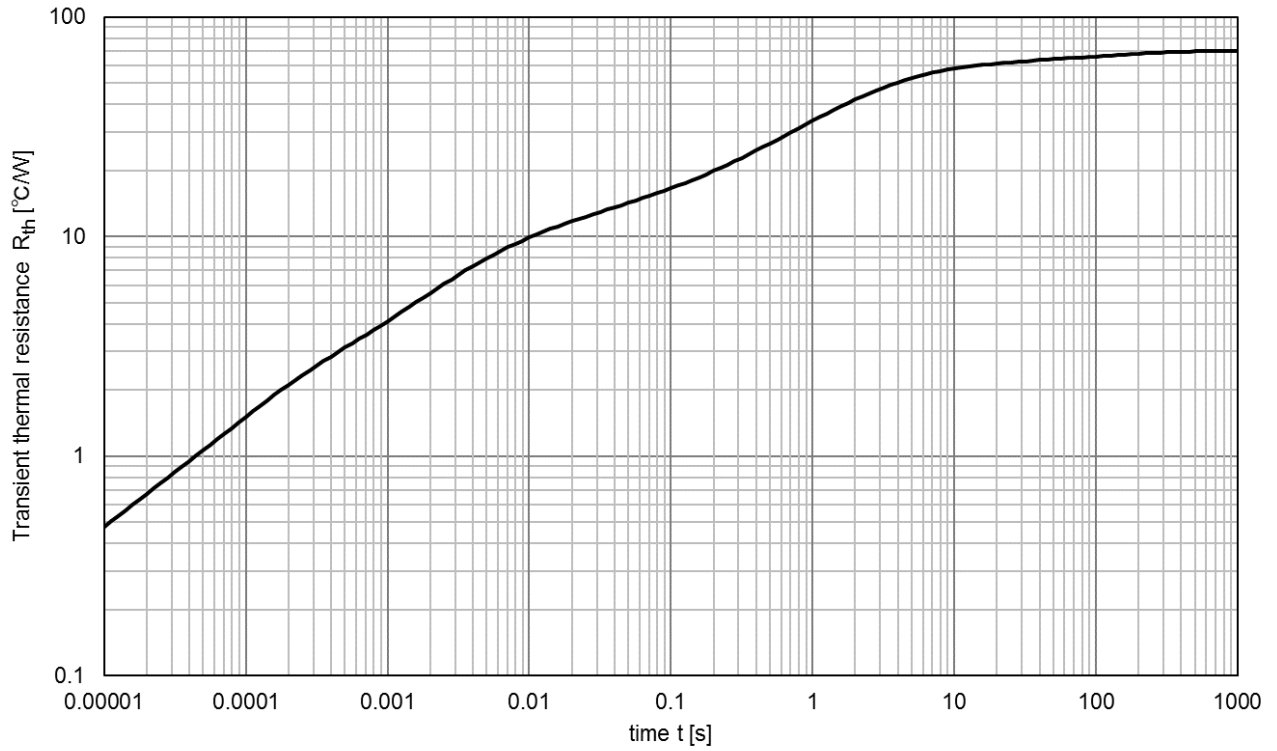
The values in the characteristic diagram are not guaranteed values unless otherwise specified, but reference values.







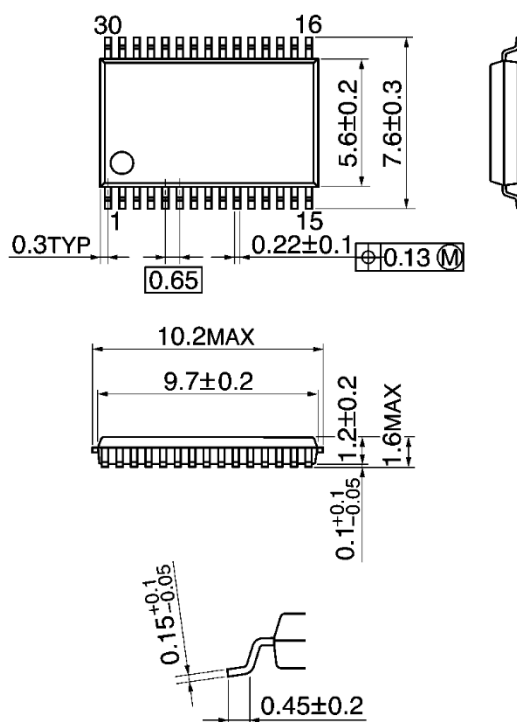
$R_{th} - t$  (1-channel operation)



## 13. Package Information

### 13.1. Package Dimensions

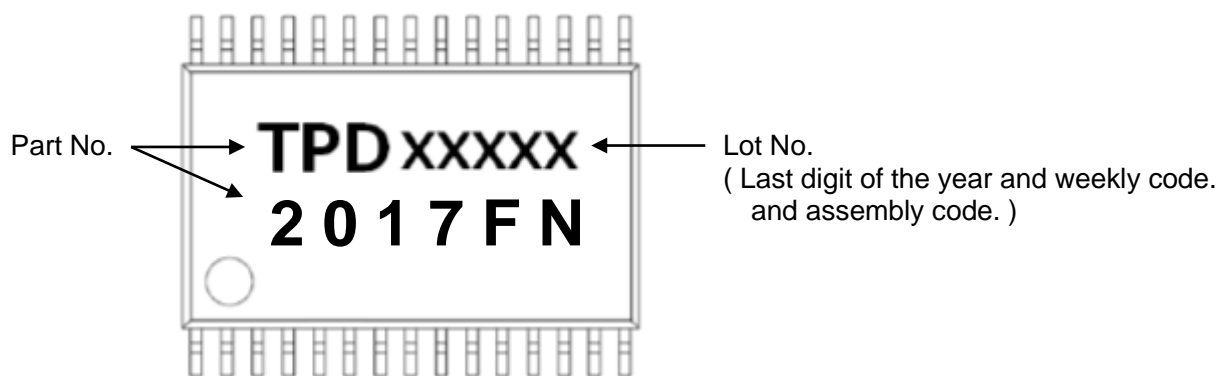
Unit : mm



Weight: 0.176 g (Typ.)

Figure 13.1 Package Dimensions

**13.2. Marking**

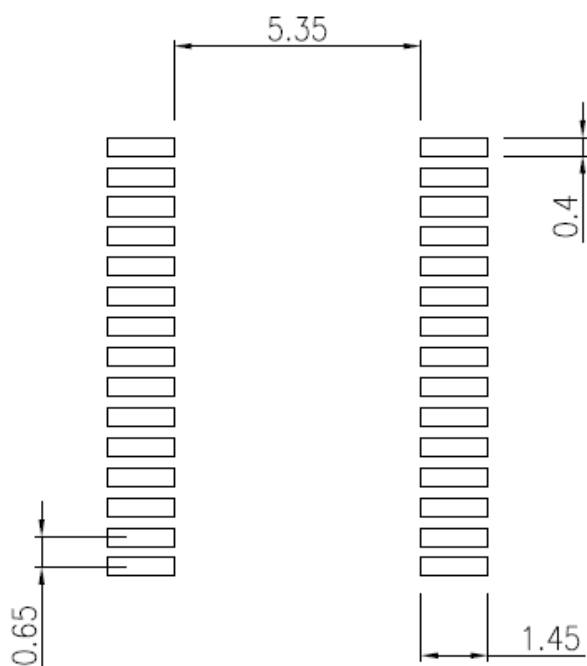


**Figure 13.2 Marking**

**13.3. Land Pattern Dimensions for Reference only**

SSOP30-P-300-0.65

"Unit: mm"



**Figure 13.3 Land Pattern Dimensions for Reference only**

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## 14. IC Usage Considerations

### 14.1. Notes on handling of ICs

The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment.

### 14.2. Notes on moisture-proof packaging

After opening the moisture-proof package, mount it within 168 hours in an environment of 30°C and RH 60% or less. Since it cannot be baked due to embossing, be sure to use it within the permissible range after opening the moisture-proof packaging. The standard packing quantity for taping is 2000 pieces / reel.

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