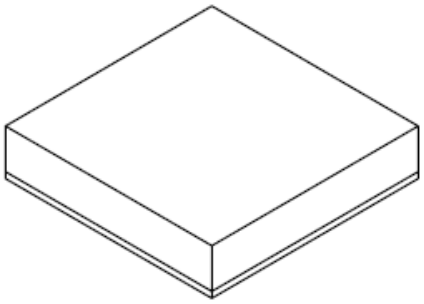
CDMOS Integrated Circuit Silicon Monolithic

# TC7710AWBG

IC for Battery Charger

## 1. Outline

The TC7710AWBG is a programmable battery charger for lithium-ion and lithium- polymer battery pack. The TC7710AWBG supports charge current up to 2.0A. For handheld devices with high capacity battery pack, this IC can charge the battery more quickly compared to the conventional devices.



S-WFBGA25-0303-0.40-001
S-WFBGA25-0303-0.40-002

## 2. Applications

Mobile phones
Devices with a single cell lithium-ion battery

## 3. Features

- Input voltage : 4.35V to 6.5V
- Battery Charging Specification 1.2 detection
- Battery shutdown current : 38μA(Typ.)
- Maximum charge current : 2.0A
- Protections and detections
  - Input over voltage protection (IOVP)
  - Under voltage lock out (UVLO)
  - Input current control
  - Battery voltage monitor
  - Battery temperature monitor
- Switching frequency : 3.0MHz
- Package : WCSP25 pin

## 4. Block Diagram

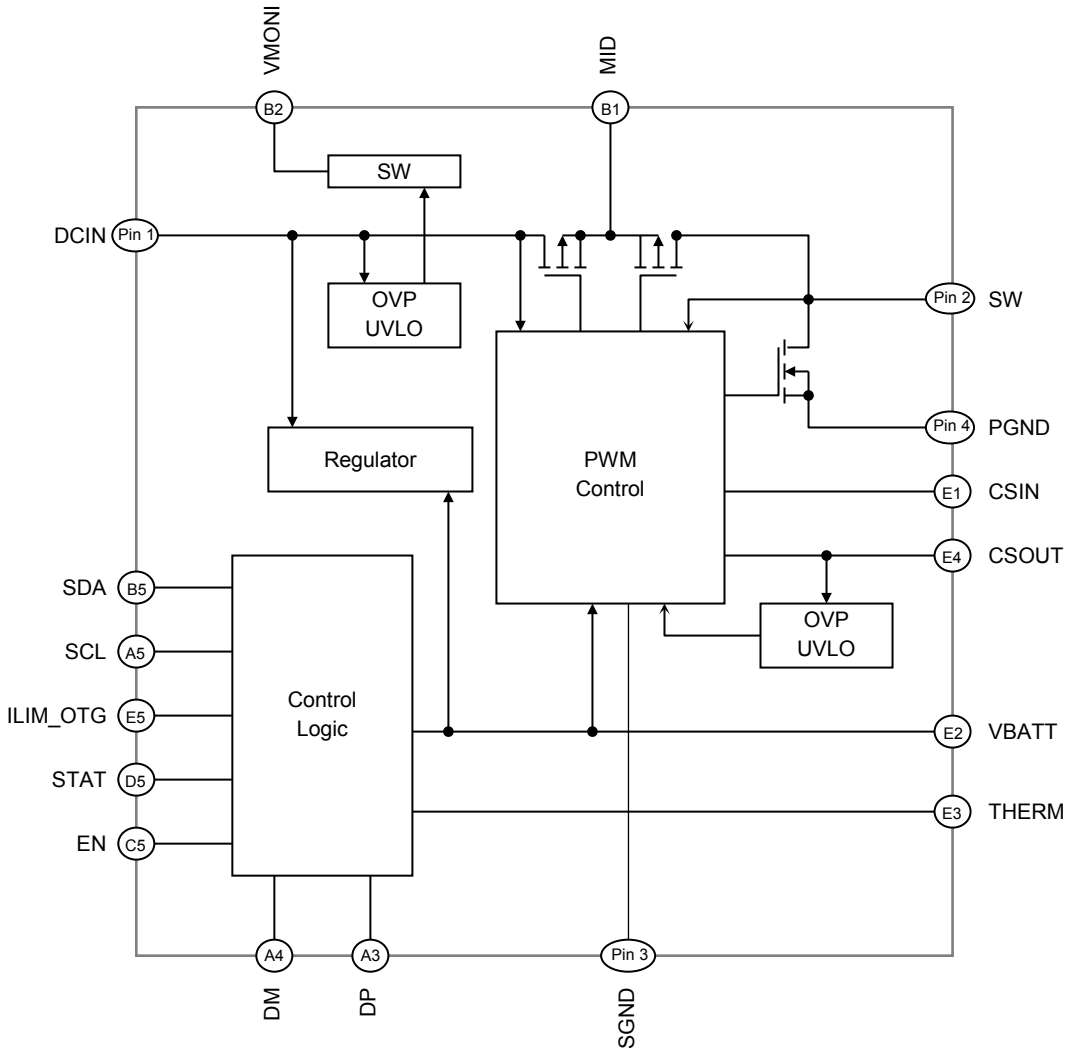



**Figure 4-1 Block Diagram**

Pin 1 : DCIN pin: A1 and A2.

Pin 2 : SW pin: C1 and C2.

Pin 3 : SGND pin: C3 and D3.

Pin 4 : PGND pin: D1 and D2.

Note. : Please refer to Application Circuit about parts and pin connection.

## 5. Pin Assignment

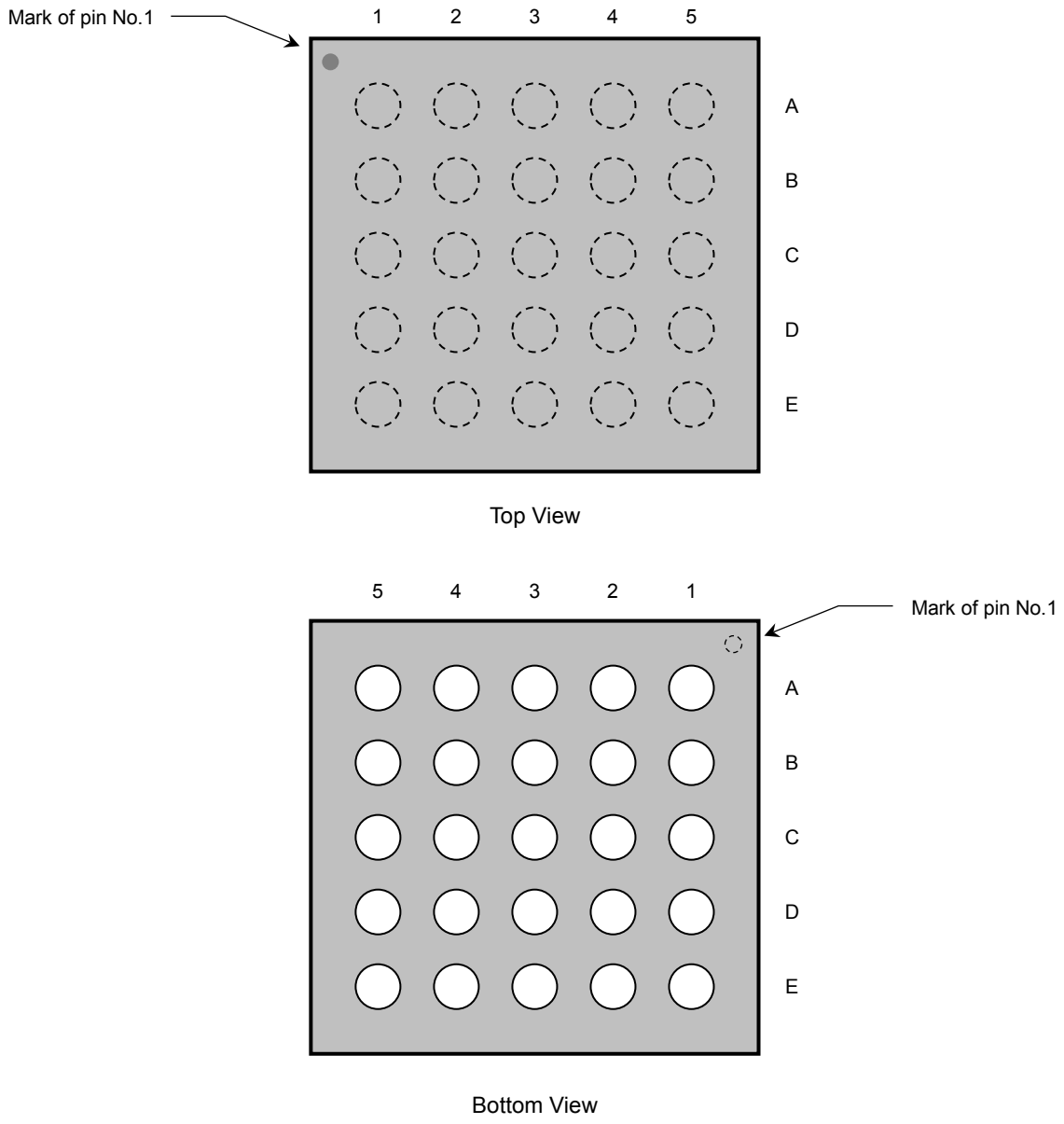



**Figure 5-1 Pin Assignment**

Note.: Please pay attention that corner pin which is next to the mark of No.1 is A1.

## 6. Pin Functions

**Table 6-1 Pin Functions (1)**

<table>
<tr><th>Pin No.</th><th>Pin name</th><th>I/O</th><th>Pin description</th></tr>
<tr><td>A1, A2</td><td>DCIN</td><td>I/O</td><td>I/O pin for USB VBUS / Input pin for AC adapter<br><table><tr><td>Charge</td><td>DC voltage input mode (+4.35V to +6.5V)</td></tr><tr><td>OTG</td><td>Voltage 5V output mode</td></tr></table>The capacitor of 1.0μF or more must be connected between DCIN pin and GND to stabilize the voltage.</td></tr>
<tr><td>A3</td><td>DP</td><td>I/O</td><td>I/O pin (+) for power source detection<br>It is connected to D+ pin of the USB connector.</td></tr>
<tr><td>A4</td><td>DM</td><td>I/O</td><td>I/O pin (-) for power source detection<br>It is connected to D- pin of the USB connector.</td></tr>
<tr><td>A5</td><td>SCL</td><td>I</td><td>Signal input pin for $I^2C$ bus clock<br>Input pin of clock signal for serial communication. Pull-up resistance should be connected to SCL pin because it is an open-drain pin.</td></tr>
<tr><td>B1</td><td>MID</td><td>I</td><td>FET midpoint input pin.<br>Middle-point voltage pin of high side MOSFET. The capacitor of 2.2μF or more should be connected between MID pin and GND to stabilize the voltage.</td></tr>
<tr><td>B2</td><td>VMONI</td><td>O</td><td>Input monitor for DC voltage<br>The voltage corresponding to DCIN is outputted and monitored in the range of UVLO to OVLO.</td></tr>
<tr><td>B5</td><td>SDA</td><td>I/O</td><td>I/O pin for $I^2C$ bus data signal.<br>Pull-up resistance should be connected to SDA pin because it is an open-drain pin.</td></tr>
<tr><td>C1, C2</td><td>SW</td><td>O</td><td>PWM signal output pin<br>PWM signal output pin for DCDC convertor. One-side of the inductor is connected to this pin.</td></tr>
<tr><td>C3, D3</td><td>SGND</td><td>-</td><td>Power supply pin for small signal (GND).</td></tr>
<tr><td>C5</td><td>EN</td><td>I</td><td>Input pin for enable signal.<br>This is a charge control pin for enable and resume. As for setting logic, polarity can be converted by register data.<br><table><tr><td rowspan="2">ENPINPOL<br>(11H,bit0)</td><td colspan="2">EN signal</td></tr><tr><td>Low</td><td>High</td></tr><tr><td>0</td><td>Charge</td><td>Stop charge</td></tr><tr><td>1</td><td>Stop charge</td><td>Charge</td></tr></table>Pay attention that validity of EN pin changes depending on ENSEL (11H, bit2).</td></tr>
<tr><td>D1, D2</td><td>PGND</td><td>-</td><td>Power supply pin (GND) for large signal.</td></tr>
<tr><td>D5</td><td>STAT</td><td>O</td><td>Status signal output pin<br>Error and operation state set by register are outputted from STAT pin. When error is generated, the TC7710AWBG outputs logic low. Pull-up resistance should be connected to STAT pin because it is an open-drain pin.</td></tr>
</table>

**Table 6-2 Pin Functions (2)**

| Pin No. | Pin name | I/O | Pin description |
|---|---|---|---|
| E1 | CSIN | I | Current sense input pin<br>Connect high side of the current sense resistance. |
| E2 | VBATT | I | Sub power supply / Kelvin sense input pin<br>Connect + pin of battery directly. |
| E3 | THERM | I | Battery thermistor sense input pin<br>Temperature can be detected by connecting this pin to “T pin” of ordinary battery pack.<br>Connect this pin to one-side of the thermistor (10 / 25 / 50 / 100kΩ NTC thermistor)<br>which is inside of the battery pack or on the PCB. |
| E4 | CSOUT | I/O | Current sense I/O pin<br>Connect low side of the current sense resistance. |
| E5 | ILIM_OTG | I | Input pin for control input current or Input pin for switching OTG operation<br>This pin sets input current and switches OTG operation. Current level of charging mode is controlled (USB mode / AC mode)<br>or<br>Valid of invalid or OTG mode is switched. |
| B3, B4, C4, D4 | TEST | - | IC test pin.<br>TOSHIBA test pin. It must be open. |

# 7. Functions

## 7.1 Input current limit

Input current from DCIN pin can be limited to the value set by ILIM_OTG pin or I²C (Refer to the table below.). When input current exceeds the preset value, the TC7710AWBG limits current to below the preset value automatically. When DCIN voltage turns into below the threshold voltage set by I²C, the TC7710AWBG limits current to the USB100 level (Max 100mA) and indicates an interrupt signal. To resume the current limit to the former level, the interrupt signal must be cleared (Refer to the command: INTCLR5 (15H, bit5).). After clearing the interrupt signal, input current limit is set to the former level quickly. For safe use, input current limit is set to lower value and the interrupt signal can be cleared.

**Table 7-1 Command (1)**

| Command | Register No./ bit No. | Contents |
|---|---|---|
| ACILMT4-0 | 03H,bit7-3 | AC input current limit |
| USB51 | 13H,bit6 | USB mode setting when ILIM_OTG is valid |
| ATPSDET | 13H,bit4 | Automatic power source detection |
| LMT_OTG1-0 | 13H,bit3-2 | Input current limit setting |
| ILIMLVL1-0 | 13H,bit1-0 | Input current limit setting when $I^2C$ is valid. |
| ATILMT | 13H,bit5 | Current limit function by DCIN voltage |
| INTATIL | 20H,bit5 | Generated the interrupt factor of input current limit |

(1) Forced setting (13H,bit4="1")

| Input current limit | Input current limit setting ILIM_OTG pin / $I^2C$ | Source detection DP / DM detection |
|---|---|---|
| USB500 | USB500 | * |
| USB100 | USB100 | * |
| AC | AC | * |

(2) USB automatic detection setting (13H,bit4="0")

| Input current limit | Input current limit setting ILIM_OTG pin / $I^2C$ | Source detection DP / DM detection |
|---|---|---|
| USB500 | USB500 | Unconnected |
| | USB500 | DCP |
| USB100 | USB100 | Unconnected |
| | * | SDP |
| | * | CDP |
| AC | AC | * |

Cautions: USB automatic detection setting

- In case input current limit setting is AC, source detection result is ignored.
- In case input current limit setting is USB500 and source detection is SDP or CDP, input current is limited 100mA.
- In case input current limit setting is USB100 and source detection is DCP, input current is limited 100mA.

DCP: Dedicated Charging Port
SDP: Standard Downstream Port
CDP: Charging Downstream Port

## 7.2 DCIN input voltage protection

When input voltage from DCIN pin exceeds specified voltage (Typ. 6.5V), input is shutdown. Charge is valid when input voltage is higher than the UVLO and lower than the OVLO. As soon as DCIN input supply is removed, charge is invalid automatically. Under the condition that charge is invalid, UVLO / OVLO detection for DCIN pin and OVLO detection for battery voltage are invalid.

## 7.3 Preliminary charge state

When DCIN input supply is connected, the TC7710AWBG check the following items for charge start-up. After starting charge, charge is suspended when one of the following items is outside the limits

(1) DCIN input voltage ≥ UVLO voltage, DCIN input voltage ≤ OVLO voltage

(2) DCIN voltage > Battery voltage + 100mV

(3) Charge is enabled. (Set by I²C or EN pin. Refer to the command: ENSEL(11H,bit2), ENCMD(11H,bit1), ENPINPOL(11H,bit0).)

(4) Battery temperature is between high limit and low limit (Refer to the command: TEMPDET(12H,bit7), BIASCRT1-0(1EH,bit7-6), COLDVTH1-0(1EH,bit3-2), HOTVTH1-0(1EH,bit1-0).).

**Table 7-2 Command (2)**

| Command | Register No./ bit No. | Contents |
|---|---|---|
| ENSEL | 11H,bit2 | EN control |
| ENCMD | 11H,bit1 | EN control by $I^2C$ |
| ENPINPOL | 11H,bit0 | Polarity of EN pin |
| TEMPDET | 12H,bit7 | Battery temperature detection |

## 7.4 Trickle charge

Preliminary charge state is OK, the TC7710AWBG starts trickle charge with 50mA (Typ.) if battery voltage is lower than 2.1V.

## 7.5 Pre-charge

When battery voltage exceeds 2.1V, the TC7710AWBG starts pre-charge with the charge current set by the register. Pre-charge continues until the battery voltage reaches the fast charge threshold voltage set by the register (Refer to the command: CCVTH2-0(01H,bit2-0).). If the battery voltage is not exceed the fast charge threshold voltage before the pre-charge timer expires, charge is suspended and an interrupt signal is indicated (Refer to the command: INTCHGER(20H,bit1), ST_TMER1-0(23H,bit1-0).). If battery voltage is lower to the trickle charge level during pre-charge, the TC7710AWBG becomes trickle charge mode and indicates an interrupt signal (Refer to the command: INTVBAT(20H,bit6).).In this case, if trickle charge is invalid (12H,bit0= ”1”), the TC7710AWBG doesn’t become trickle charge and doesn’t indicate an interrupt signal.

**Table 7-3 Command (3)**

| Command | Register No./ bit No. | Contents |
|---|---|---|
| PCI1-0 | 00H,bit1-0 | Pre-charge current |
| CCVTH2-0 | 01H,bit2-0 | Threshold voltage for fast charge |

## 7.6 Fast charge (Constant Current charge mode)

When fast charge mode is valid, the TC7710AWBG starts constant current charge mode if battery voltage exceeds the fast charge threshold voltage set by the register. The TC7710AWBG limits charge current to below input current limit value (Refer to the command: CCISET(12H,bit2), PRCCTH(12H,bit1), CCVTH2-0 (01H,bit2-0).). If battery voltage is lower to the pre charge level during fast charge, the TC7710AWBG becomes pre-charge mode and indicates an interrupt signal (Refer to the command: INTVBAT(20H,bit6).).

**Table 7-4 Command (4)**

| Command | Register No./ bit No. | Contents |
|---|---|---|
| CCI4-0 | 01H,bit7-3 | Fast charge current |
| CCISET | 12H,bit2 | Fast charge mode setting |

## 7.7 Fast charge (Constant Voltage charge mode)

The TC7710AWBG starts constant voltage charge mode if battery voltage becomes the float voltage set by the register during constant current charge mode (Refer to the command: FLTV6-0(02H,bit6-0).).

**Table 7-5 Command (5)**

| Command | Register No./ bit No. | Contents |
|---|---|---|
| FLTV6-0 | 02H,bit6-0 | Float voltage |

## 7.8 Charge completion

When charge completion is valid (Refer to the command: CT(12H,bit3).), charging is completed if charge current is lower than the charge termination current set by the register (Refer to the command: CEI1-0(00H,bit5-4).). If charge timer has expired until charge is completed, the TC7710AWBG terminates the charge and indicates an interrupt signal (Refer to the command: INTCHGER(20H,bit1), ST_TMER1-0(23H,bit1-0).). If charge completion is invalid (CT(12H,bit3)=1), the TC7710AWBG continues CV charge and doesn't indicate an interrupt signal. In this case, the TC7710AWBG is controlled by $I^2C$ to terminate the charge. The status ST_CGED0 (24H,bit4) can be checked if charge current is lower than the current set by the register during CV charge mode.

**Table 7-6 Command (6)**

| Command | Register No./ bit No. | Contents |
|---|---|---|
| CT | 12H,bit3 | Charge completion |
| CEI1-0 | 00H,bit5-4 | Charge termination current |
| ST_CGED0 | 24H,bit4 | Charge current is lower than the charge termination current (only CV mode). |

## 7.9 Re-charge

The TC7710AWBG recharges the battery when the battery voltage falls by a value set by the register below the float voltage (Refer to the command: FLTV6-0(02H,bit6-0), ATRCHGTH(00H,bit6) is fixed to 140mV. ).
The TC7710AWBG can recharge only when DCIN input supply is connected, charge is enabled and the charge start-up condition is satisfied before charge. In this case, the TC7710AWBG is controlled by command to recharge the battery automatically (Refer to the command: ATRCHG(12H,bit4).).

**Table 7-7 Command (7)**

| Command | Register No./ bit No. | Contents |
|---|---|---|
| ATRCHGTH | 00H,bit6 | Threshold voltage for automatic recharge. *140mV only. |
| ATRCHG | 12H,bit4 | Automatic recharge |

## 7.10 Automatic charge

The TC7710AWBG can start charge automatically regardless of enable control (Refer to the command: DBATVDET(00H,bit7), ATCHG(11H,bit3).) when battery voltage is lower than dead battery threshold. In case the battery voltage is higher than dead battery threshold, charge is controlled by EN pin / I²C, and in case the battery voltage is lower than dead battery threshold, the TC7710AWBG starts charge when DCIN input supply is connected, charge is enabled and the charge start-up condition is satisfied before charge. A charge enable shall be set after 3ms since the float voltage is set. The TC7710AWBG continues charge until charge is completed or pre-charge safety timer of 36minutes is expired.

**Table 7-8 Command (8)**

| Command | Register No./ bit No. | Contents |
|---|---|---|
| DBATVDET | 00H,bit7 | Threshold for dead battery |
| ATCHG | 11H,bit3 | Automatic charge |

## 7.11 USB OTG

The TC7710AWBG can supply a regulated 5V output at the DCIN pin for powering peripherals compliant with the USB OTG specification (Refer to the command: OTGVCTL1-0(04H,bit5-4).). When only a battery is connected (AC adaptor or USB isn't connected) and battery voltage is higher than battery UVLO voltage, OTG control can be enabled by ILIM_OTG pin or I²C (Refer to the command: OTGUVTH1-0(04H,bit1-0), OTGMD(13H,bit7), LMT_OTG1-0(13H,bit3-2).). If battery UVLO, battery current limit and DCIN UVLO are occurred during OTG mode, OTG operation is suspended. OTG operation resumes by ILIM_OTG pin or I²C. During OTG operation, output current is controlled by a value set by the register (Refer to the command: CCI4-0(01H,bit7-3).).When output current exceeds the preset value, the TC7710AWBG shuts off the OTG voltage and indicates an interrupt signal (Refer to the command: INTOTGER(20H,bit3), ST_OTGLM(22H,bit1).). When the chip temperature exceeds 135°C during OTG operation, the TC7710AWBG shuts off the OTG voltage and indicates an interrupt signal (Refer to the command: INTOTGER(20H,bit3), ST_OTGJCT(22H,bit3).). During OTG operation, a watchdog timer should be valid for system safety. When a watchdog timer is expired, the TC7710AWBG shuts off the OTG voltage and indicates an interrupt signal (Refer to the command: OTGWDTM(10H,bit4), INTOTGER(20H,bit3), ST_OTWDT(22H,bit2).).

**Table 7-9 Command (9)**

| Command | Register No./ bit No. | Contents |
|---|---|---|
| CCI4-0 | 01H,bit7-3 | OTG battery current limit |
| OTGVCTL1-0 | 04H,bit5-4 | OTG output voltage |
| OTGUVTH1-0 | 04H,bit1-0 | Battery UVLO setting in OTG |
| OTGWDTM | 10H,bit4 | OTG watchdog timer |
| OTGMD | 13H,bit7 | OTG control by $I^2C$ |
| LMT_OTG1-0 | 13H,bit3-2 | OTG control setting |

## 7.12 Watchdog timer

A watchdog timer is reset with every I²C ACK signal transmitted from a system. If watchdog timer is expired during the charging / OTG operation, the TC7710AWBG suspends the charging / OTG operation, indicates an interrupt signal and reset the following registers: 00H-13H, 1EH, and 1FH (e-Fuse data is reloaded.). During OTG operation, a watchdog timer should be valid for system safety. And standby watchdog timer should be valid when the TC7710AWBG doesn't charge or supply OTG power (Refer to the command: STBWDTM(10H,bit5), OTGWDTM(10H,bit4), CHGWDTM(10H,bit3).). However both watchdog timers are not valid from a fully charged state to an automatic recharge starts, since the TC7710AWBG isn't in a charge mode or a standby mode. To set a charge disable, standby watchdog timer is valid for this time.

**Table 7-10 Command (10)**

| Command | Register No./ bit No. | Contents |
|---|---|---|
| OTGWDTM | 10H,bit4 | OTG watchdog timer |
| CHGWDTM | 10H,bit3 | Charge watchdog timer |
| STBWDTM | 10H,bit5 | Standby watchdog timer |

## 7.13 Safety timer

The TC7710AWBG has a pre-charge timer of 36 minutes and a charge timer of 240 minutes (Refer to the command: PRCHGTM(10H,bit2), CHGSTM(10H,bit1).). A pre-charge timer of 36 minutes is started after preliminary charge state is OK, the TC7710AWBG starts trickle charge. And this timer is reset when the mode is changed from pre-charge to fast charge. A charge timer of 240 minutes is also started after preliminary charge state is OK, the TC7710AWBG suspends the charging if charge current isn't lower than the charge termination current within a timer. It is possible not to include trickle charge time in the charge timers (Refer to the command: TCSTON(10H,bit0).). Both timers can be cleared by I²C in case charge timers are monitored by system (Refer to the command: CHGTMCLR(10H,bit6).). When the TC7710AWBG starts recharge in case an auto recharge is valid, these safety timers aren't valid. Therefore it is recommended that an external timer is applied by system for charge protection.

**Table 7-11 Command (11)**

| Command | Register No./ bit No. | Contents |
|---|---|---|
| PRCHGTM | 10H,bit2 | Pre-charge timer |
| CHGSTM | 10H,bit1 | Charge timer |
| TCSTON | 10H,bit0 | Include or not include trickle charge time in the timers |
| CHGTMCLR | 10H,bit6 | Timer clear |

## 7.14 Operating state

STAT pin is output that indicates operating state. When battery is charging or DCIN voltage is lower than UVLO / higher than OVLO, this pin is asserted low level. A type of state from STAT pin is controlled by command, and the output is invalided controlled by command (Refer to the command: STATMD(14H,bit2), STATOUT(14H,bit1).). STAT pin is open-drain output, a pull-up resistor should be connected to this pin.

**Table 7-12 Command (12)**

| Command | Register No./ bit No. | Contents |
|---|---|---|
| STATMD | 14H,bit2 | Select a type of state from STAT pin |
| STATOUT | 14H,bit1 | STAT output ON/OFF |

## 7.15 Interrupt / Abnormal detection

STAT pin is output that indicates seven interrupt signals. Interrupt signal and interrupt mask are set by I²C. The TC7710AWBG outputs a pulse signal from STAT pin for 0.8ms every 350ms and indicates an interrupt signal to system. The system checks an interrupt factor, clears the factor and executes the interrupt process according to the factor.

Standby WDT error
OTG error
Re-charge
Charge error
Charge completion
Occurrence of automatic input current limit
Occurrence of charge state back to previous mode

The following tables describe the error recovery.

**Table 7-13 Interrupt process**

Standby WDT error

| Interrupt factor | TC7710AWBG process | Recovery process |
|---|---|---|
| Timer expired | Registers of 00H-13H, 1EH, and 1FH are initialized.<br>Standby mode transition | Set registers of 00H-13H, 1EH, and 1FH. |

OTG error

| Interrupt factor | TC7710AWBG process | Recovery process |
|---|---|---|
| WD Timer expired | Shut off OTG supply.<br>Registers of 00H-13H, 1EH, and 1FH are initialized.<br>Standby mode transition | Set registers of 00H-13H, 1EH, and 1FH. |
| Exceed current limit | Shut off OTG supply. | Control OTG function disable to enable manually. |
| Battery UVLO occur | Shut off OTG supply. | Control OTG function disable to enable manually. |
| Exceed chip temperature | Shut off OTG supply. | Control OTG function disable to enable manually. |
| Output (DCIN) voltage drop under UVLO | Shut off OTG supply. | Control OTG function disable to enable manually. |

Re-charge

| Interrupt factor | TC7710AWBG process | Recovery process |
|---|---|---|
| Vbat < Vfloat - 140mV | Restart charging<br>(ATRCHG=0) | - |

Charge error

| Interrupt factor | TC7710AWBG process | Recovery process |
|---|---|---|
| Input OVLO occur | Stop charging. | After charge start-up condition is satisfied, the TC7710AWBG restarts charging from standby mode. |
| Input UVLO occur | Stop charging. | After charge start-up condition is satisfied, the TC7710AWBG restarts charging from standby mode.<br>* The TC7710AWBG doesn't output an interrupt signal since all registers are initialized for POR. |
| DCIN < Vbat + 105mV | Stop charging. | After charge start-up condition is satisfied, the TC7710AWBG restarts charging from standby mode. |
| Out of battery temperature limit | Continue charging.<br>(TEMPDET="0") | EN should be turned off manually. |
| | Suspend charging.<br>(TEMPDET="1") | After charge start-up condition is satisfied, the TC7710AWBG resumes charging automatically. |
| Exceed chip temperature | Continue charging.<br>(OVTLMT="0") | EN should be turned off manually.<br>* It is recommended charging is suspended in this case (OVTLMT(12h,bit6)=1). |
| | Suspend charging.<br>(OVTLMT="1") | After charge start-up condition is satisfied, the TC7710AWBG resumes charging automatically. |
| Battery OVLO occur | Stop charging.<br>(BATOV="1") | After charge start-up condition is satisfied, EN should be turned on manually. |
| Unconnected battery | Stop charging. | After charge start-up condition is satisfied, EN should be turned on manually. |
| Charge WDT expired | Continue charging.<br>Registers of 00H-13H, 1EH, and 1FH are initialized. | Set registers of 00H-13H, 1EH, and 1FH.<br>* Charge timers are running on. |
| Charge timer expired | Stop charging. | EN should be turned on manually. |
| Input voltage drop | Continue charging.<br>The TC7710AWBG limits current to the 100mA.<br>(ATILMT="0") | To resume the current limit to the former level, the interrupt signal must be cleared. |

Charge completion

| Interrupt factor | TC7710AWBG process | Recovery process |
|---|---|---|
| Ichg < Iterm | Charge completion<br>(CT="0") | - |

Occurrence of automatic input current limit

| Interrupt factor | TC7710AWBG process | Recovery process |
|---|---|---|
| Exceed input current | Continue charging.<br>The TC7710AWBG limits current to the 100mA. | To resume the current limit to the former level, the interrupt signal must be cleared. |

Occurrence of charge state back to previous mode

| Interrupt factor | TC7710AWBG process | Recovery process |
|---|---|---|
| Charge state is back to previous mode by battery voltage drop. | - | - |

**Table 7-14 Command (13)**

| Command | Register No./ bit No. | Contents |
|---|---|---|
| INTOUT | 14H,bit3 | Select an information from STAT pin. |
| STATOUT | 14H,bit1 | Control an output from STAT pin. |
| INT*** | 20H,bit6-0 | Interrupt factor |
| ST_*** | 21H, 22H, 23H | Status information |

## 7.16 Chip temperature monitoring

Chip temperature is monitored during charge/OTG. When chip temperature exceeds 135°C, chip temperature monitoring bit is set high. And when chip temperature falls 115°C, it is set low (Refer to the command: ST_JCTON(21H,bit2).). Charge stops when chip temperature monitoring bit is set high. And charge re-starts automatically when it is set low. (It depends on the set conditions. Refer to the command: OVTLMT(12H,bit6).)) OTG stops when chip temperature monitoring bit is set high (Refer to the command: ST_OTGJCT(22H,bit3).).

**Table 7-15 Command (14)**

| Command | Register No./ bit No. | Contents |
|---|---|---|
| ST_JCTON | 21H,bit2 | Chip temperature state (Charging mode) |
| ST_OTGJCT | 22H,bit3 | Chip temperature state (OTG mode) |
| OVTLMT | 12H,bit6 | Charge stop in high temperature |

## 7.17 Battery temperature monitoring

Battery temperature is monitored before charging and in charging through THERM pin. When battery temperature exceeds the programmed temperature limit, charge can be suspended (Refer to the command: TEMPDET(12H,bit7).). While battery temperature is out of the limit range, the TC7710AWBG stops charge timer indicates charge error interrupt signal (Refer to the command: INTCHGER(20H,bit1), ST_BATHT(21H,bit1), ST_BATCL(21H,bit0).). And when the temperature becomes within the limit range, the TC7710AWBG resumes charge and charge timer. As detection range is different depending on a characteristic of NTC thermistor, external resistance which is the same value of R25 is connected in parallel typically. And the intended range of temperature is set (Refer to the command: COLDVTH1-0(1EH,bit3-2), HOTVTH1-0(1EH,bit1-0).). The TC7710AWBG supports thermistors which value of R25 is 10kΩ, 25kΩ, 50kΩ, and 100kΩ. A current source of 200μA, 80μA, 40μA, and 20μA is selected depending on the resister (Refer to the command: BIASCRT1-0(1EH,bit7-6).).

**Table 7-16 Temperature limit**

| Vtherm [V] | β | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | 3000 | 3250 | 3500 | 3750 | 4000 | 4250 | 4500 | 4750 | 5000 |
| 0.509 | 61 | 58 | 55 | 53 | 51 | 50 | 48 | 47 | 46 |
| 0.574 | 55 | 53 | 50 | 49 | 47 | 46 | 45 | 44 | 43 |
| 0.647 | 49 | 47 | 45 | 44 | 43 | 42 | 41 | 40 | 39 |
| 0.726 | 43 | 42 | 40 | 39 | 39 | 38 | 37 | 36 | 36 |
| 1.000 | 25 | 25 | 25 | 25 | 25 | 25 | 25 | 25 | 25 |
| 1.399 | 1 | 3 | 5 | 6 | 7 | 8 | 9 | 9 | 10 |
| 1.491 | -4 | -2 | 0 | 1 | 2 | 4 | 5 | 6 | 7 |
| 1.577 | -10 | -8 | -5 | -4 | -2 | -1 | 1 | 2 | 3 |
| 1.654 | -16 | -13 | -10 | -8 | -7 | -5 | -3 | -2 | -1 |

**Table 7-17 Command (15)**

| Command | Register No./ bit No. | Contents |
|---|---|---|
| TEMPDET | 12H,bit7 | Charge control with battery temperature monitoring |
| BIASCRT1-0 | 1EH,bit7-6 | Current source value for temperature monitoring |
| COLDVTH1-0 | 1EH,bit3-2 | Threshold voltage for low temperature detection |
| HOTVTH1-0 | 1EH,bit1-0 | Threshold voltage for high temperature detection |
| INTCHGER | 20H,bit1 | Charge error interrupt |
| ST_BATHT | 21H,bit1 | Battery high temperature detection status |
| ST_BATCL | 21H,bit0 | Battery low temperature detection status |

## 7.18 Power source detection

The TC7710AWBG corresponds to Battery Charging Specification Rev1.2. Automatic power source detection can be set by the register (Refer to the command: ATPSDET(13H,bit4).). Source detection starts as soon as DCIN is connected. There are four kinds of detection results as follows; non-connection, SDP (Standard Downstream Port), CDP (Charging Downstream Port), and DCP (Dedicated Charging Port) (Refer to the command: ST_STYP1-0 (25H,bit1-0).). Input current limit can be set depending on the detection state (Refer to 7.1 Input current limit.).

**Table 7-18 Command (16)**

| Command | Register No./ bit No. | Contents |
|---|---|---|
| ATPSDET | 13H,bit4 | Automatic power source detection |
| ST_STYP1-0 | 25H,bit1-0 | Source detection result |

## 7.19 Unconnected battery detection

The TC7710AWBG executes battery detection through VBATT pin (Refer to the command: BATMSDET(11H,bit4).). When battery voltage is lower than 2.1V, the TC7710AWBG starts trickle charge. And when battery voltage exceeds 2.1V, the TC7710AWBG starts pre-charge. If battery voltage exceeds 3.3V within 85ms after starting pre-charge, the TC7710AWBG detects as unconnected battery (Refer to the command: INTCHGER(20H,bit1), ST_BATMS(21H,bit7).).

**Table 7-19 Command (17)**

| Command | Register No./ bit No. | Contents |
|---|---|---|
| BATMSDET | 11H,bit4 | Execute battery detection |
| INTCHGER | 20H,bit1 | Charge error interrupt |
| ST_BATMS | 21H,bit7 | Unconnected battery detection |

## 7.20 VMONI output

The TC7710AWBG outputs the signal which monitored DCIN input voltage.

**Table 7-20 Command (18)**

| Command | Register No./ bit No. | Contents |
|---|---|---|
| VMONICNT | 14H,bit4 | Output VMONI signal |

## 7.21 Battery save mode

The TC7710AWBG becomes battery save mode when DCIN is in UVLO and standby WDT is invalid, or when OTG is disable. If there are I²C signals among the battery save mode, the TC7710AWBG changes the mode to the standby mode. Wait time 1ms is necessary to write next I²C signal successively. If there is a DCIN input among the battery save mode, the TC7710AWBG enables POR and becomes standby mode.

## 7.22 I²C Bus

A communication between the TC7710AWBG and the host is operated using I²C format. Both the clock line (SCL) and the data line (SDA) provide a communication between the TC7710AWBG and the host. There are Start Condition and Stop Condition, when they send and receive the data. The commands are sent between Start Condition and Stop Condition. Refer to the following figure.

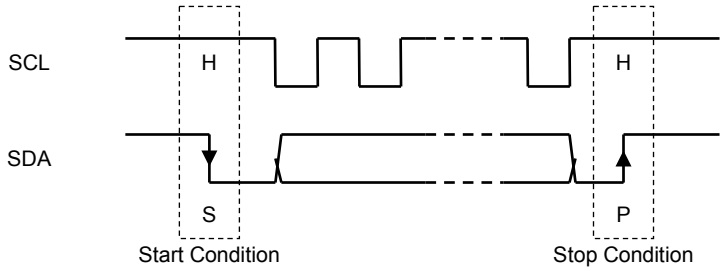



**Figure 7-1 Relation between Start Condition and Stop Condition**

**Table 7-21 List of the protocol symbols**

| Symbols | Descriptions |
|---|---|
| S | Start Condition |
| SR | Repeat Start Condition |
| P | Stop Condition |
| Slave Address | Slave Address(high 7 bits) |
| R | Read mode(TC7710AWBG -> HOST) |
| W | Write mode(HOST -> TC7710AWBG) |
| X | Undefined (1 or 0) |
| A / A | ACK (HOST -> TC7710AWBG). This symbol in gray shows that the TC7710AWBG output “Low” level when it receives ACK (TC7710AWBG -> HOST) |
| NA / NA | NACK (HOST -> TC7710AWBG). This symbol in gray shows that the TC7710AWBG output Hi-Z when it receives NACK(TC7710AWBG -> HOST) |
| COMMAND CODE | Command register for the TC7710AWBG |
| Data Byte<br>Data Byte | This symbol shows 1 byte. This symbol in gray shows data flow from the TC7710AWBG to HOST in read. |
| ・・・ | This symbol shows that the block (bit or byte, Packet) is continued. |

### 7.22.1 Detailed bits

The TC7710AWBG supports the following I²C bus bit sequence.

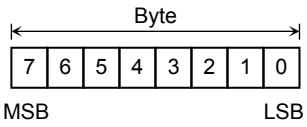



**Figure 7-2 bit sequence**

### 7.22.2 Start Condition / Stop Condition

The TC7710AWBG is communicated on I²C format. So, the packets divided by Start Condition / Stop Condition are transmitted and received. The communication consists of SCL (clock line) and SDA (data line). If they don't communicate, both clock line and data line are fixed to High level. It goes through Start Condition that data line goes down earlier than clock line. And it goes through Stop Condition that clock line goes down earlier than data line. It is prohibited changing condition of the data line, while the clock line is High level in normal communication.
It regards as the end of the communication, if the receiver doesn't operate that data line with low level in the timing which it receives ACK bit. And, after the end of the communication, it is possible to restart from Start Condition without Stop Condition.

### 7.22.3 ACK data

The receiver notifies the transceiver of ACK data by receiving 1 byte (8 bits) to indicate its condition. If it is no problems, it operates data line with low level after the clock of byte 8 (LSB) goes down. If the data communication error has occurred by any problems, the TC7710AWBG reports NACK.

### 7.22.4 Slave Address

The TC7710AWBG can choose the Slave Address that has 8 types by the fixed e-fuse data.

**Table 7-22 Slave Address**

| | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Address | 0 | 0 | 0 | 1 | 0 | 0 | 1 | R / $\overline{W}$ |
| | 0 | 0 | 0 | 1 | 0 | 0 | 0 | R / $\overline{W}$ |
| | 0 | 0 | 0 | 1 | 0 | 1 | 1 | R / $\overline{W}$ |
| | 0 | 0 | 0 | 1 | 1 | 0 | 1 | R / $\overline{W}$ |
| | 0 | 0 | 1 | 1 | 0 | 0 | 1 | R / $\overline{W}$ |
| | 0 | 1 | 0 | 1 | 0 | 0 | 1 | R / $\overline{W}$ |
| | 1 | 0 | 0 | 1 | 0 | 0 | 1 | R / $\overline{W}$ |

### 7.22.5 Write bytes

It transmits in order of an Slave Address, COMMAND CODE and Data Byte.


**Figure 7-3 Write bytes**

### 7.22.6 Read bytes

If the following bit of Slave Address is set to "1", the TC7710AWBG is selected in Read mode. The TC7710AWBG sends the data that is issued by COMMAND CODE to the host, just before selected in Read mode.

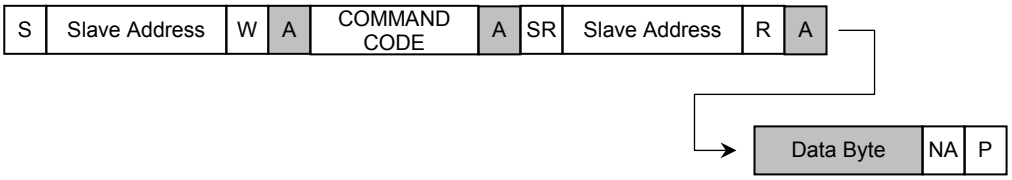



**Figure 7-4 Read bytes**

## 7.23 Cautions in writing $I^2C$ register

To avoid a transitional response of operating parameter by $I^2C$ register rewriting, the TC7710AWBG stops an internal operation change for about 250μs after $I^2C$ register writing. So if $I^2C$ register is written successively in 250μs, internal operation remains stopping in the meantime. And register is written normally.

If programmed parameters are rewritten continuously after writing the charge EN control register and the OTG control register, charge and OTG operation do not start while $I^2C$ register is under writing. So rewrite parameter first, then rewrite of the EN control register and the OTG control register.

As for reading of $I^2C$ register, internal operation does not stop.

## 8. Register Map

**Address=00H**

<table>
<tr><th>bit</th><th>Command</th><th>R/W</th><th>Initial value</th><th>Contents</th></tr>
<tr><td>7</td><td>DBATVDET</td><td>R/W</td><td>1</td><td>Dead battery voltage threshold<br><table><tr><td>0</td><td>VBATT < 3.47V</td></tr><tr><td>1</td><td>VBATT < 3.54V</td></tr></table></td></tr>
<tr><td>6</td><td>ATRCHGTH</td><td>R/W</td><td>0</td><td>Automatic re-charge voltage threshold<br><table><tr><td>0</td><td>140mV</td></tr><tr><td>1</td><td>140mV</td></tr></table></td></tr>
<tr><td>5</td><td>CEI1</td><td>R/W</td><td>0</td><td rowspan="2">Charge completion current<br><table><tr><td>00</td><td>50mA *Unavailable</td></tr><tr><td>01</td><td>100mA</td></tr><tr><td>10</td><td>150mA</td></tr><tr><td>11</td><td>200mA</td></tr></table>Initial state: ”01”=100mA</td></tr>
<tr><td>4</td><td>CEI0</td><td>R/W</td><td>1</td></tr>
<tr><td>3</td><td>-</td><td>R</td><td>0</td><td>-</td></tr>
<tr><td>2</td><td>-</td><td>R</td><td>0</td><td>-</td></tr>
<tr><td>1</td><td>PCI1</td><td>R/W</td><td>1</td><td rowspan="2">Pre-charge current<br><table><tr><td>00</td><td>50mA</td></tr><tr><td>01</td><td>100mA</td></tr><tr><td>10</td><td>150mA</td></tr><tr><td>11</td><td>200mA</td></tr></table></td></tr>
<tr><td>0</td><td>PCI0</td><td>R/W</td><td>1</td></tr>
</table>

**Address=01H**

<table>
<tr><th>bit</th><th>Command</th><th>R/W</th><th>Initial value</th><th>Contents</th></tr>
<tr><td>7</td><td>CCI4</td><td>R/W</td><td>0</td><td rowspan="4">Fast charge current<br><table><tr><td>00000</td><td>300mA</td><td>01001</td><td>1,200mA</td></tr><tr><td>00001</td><td>400mA</td><td>01010</td><td>1,300mA</td></tr><tr><td>00010</td><td>500mA</td><td>01011</td><td>1,400mA</td></tr><tr><td>00011</td><td>600mA</td><td>01100</td><td>1,500mA</td></tr><tr><td>00100</td><td>700mA</td><td>01101</td><td>1,600mA</td></tr><tr><td>00101</td><td>800mA</td><td>01110</td><td>1,700mA</td></tr><tr><td>00110</td><td>900mA</td><td>01111</td><td>1,800mA</td></tr><tr><td>00111</td><td>1,000mA</td><td>10000</td><td>1,900mA</td></tr><tr><td>01000</td><td>1,100mA</td><td>10001</td><td>2,000mA</td></tr></table>Initial value: ”00010”=500mA</td></tr>
<tr><td>6</td><td>CCI3</td><td>R/W</td><td>0</td></tr>
<tr><td>5</td><td>CCI2</td><td>R/W</td><td>0</td></tr>
<tr><td>4</td><td>CCI1</td><td>R/W</td><td>1</td></tr>
<tr><td>3</td><td>CCI0</td><td>R/W</td><td>0</td><td>OTG current limit *only OTG is enabled<br><table><tr><td>00010</td><td>500mA</td><td>01100</td><td>1,500mA</td></tr><tr><td>00111</td><td>1000mA</td><td>01111</td><td>1,800mA</td></tr></table>Initial value: ”00010”=500mA</td></tr>
<tr><td>2</td><td>CCVTH2</td><td>R/W</td><td>1</td><td rowspan="3">Threshold voltage from pre-charge to fast charge<br><table><tr><td>000</td><td>2.6V</td><td>100</td><td>3.0V</td></tr><tr><td>001</td><td>2.7V</td><td>101</td><td>3.1V</td></tr><tr><td>010</td><td>2.8V</td><td>110</td><td>3.2V</td></tr><tr><td>011</td><td>2.9V</td><td>111</td><td>3.3V</td></tr></table>Initial value is 3.0V.</td></tr>
<tr><td>1</td><td>CCVTH1</td><td>R/W</td><td>0</td></tr>
<tr><td>0</td><td>CCVTH0</td><td>R/W</td><td>0</td></tr>
</table>

**Address=02H**

<table>
<tr><th>bit</th><th>Command</th><th>R/W</th><th>Initial value</th><th>Contents</th></tr>
<tr><td>7</td><td>-</td><td>R</td><td>0</td><td>-</td></tr>
<tr><td>6</td><td>FLTV6</td><td>R/W</td><td>0</td><td rowspan="7">Float voltage<br><table><tr><td>0000000</td><td>3.46V</td></tr><tr><td>0000001</td><td>3.47V</td></tr><tr><td>0000010</td><td>3.48V</td></tr><tr><td>:</td><td>:</td></tr><tr><td>1111101</td><td>4.71V</td></tr><tr><td>1111110</td><td>4.72V</td></tr><tr><td>1111111</td><td>4.73V</td></tr></table>Initial value: ”0000100”=3.50V</td></tr>
<tr><td>5</td><td>FLTV5</td><td>R/W</td><td>0</td></tr>
<tr><td>4</td><td>FLTV4</td><td>R/W</td><td>0</td></tr>
<tr><td>3</td><td>FLTV3</td><td>R/W</td><td>0</td></tr>
<tr><td>2</td><td>FLTV2</td><td>R/W</td><td>1</td></tr>
<tr><td>1</td><td>FLTV1</td><td>R/W</td><td>0</td></tr>
<tr><td>0</td><td>FLTV0</td><td>R/W</td><td>0</td></tr>
</table>

**Address=03H**

<table>
<tr><th>bit</th><th>Command</th><th>R/W</th><th>Initial value</th><th>Contents</th></tr>
<tr><td>7</td><td>ACILMT4</td><td>R/W</td><td>0</td><td rowspan="4">AC input current limit<br><table><tr><td>00000</td><td>300mA</td><td>01001</td><td>1,200mA</td></tr><tr><td>00001</td><td>400mA</td><td>01010</td><td>1,300mA</td></tr><tr><td>00010</td><td>500mA</td><td>01011</td><td>1,400mA</td></tr><tr><td>00011</td><td>600mA</td><td>01100</td><td>1,500mA</td></tr><tr><td>00100</td><td>700mA</td><td>01101</td><td>1,600mA</td></tr><tr><td>00101</td><td>800mA</td><td>01110</td><td>1,700mA</td></tr><tr><td>00110</td><td>900mA</td><td>01111</td><td>1,800mA</td></tr><tr><td>00111</td><td>1,000mA</td><td>10000</td><td>1,900mA</td></tr><tr><td>01000</td><td>1,100mA</td><td>10001</td><td>2,000mA</td></tr></table>Current values in above table are maximum limit current. Initial value is 500mA.</td></tr>
<tr><td>6</td><td>ACILMT3</td><td>R/W</td><td>0</td></tr>
<tr><td>5</td><td>ACILMT2</td><td>R/W</td><td>0</td></tr>
<tr><td>4</td><td>ACILMT1</td><td>R/W</td><td>1</td></tr>
<tr><td>3</td><td>ACILMT0</td><td>R/W</td><td>0</td></tr>
<tr><td>2</td><td>-</td><td>R</td><td>0</td><td>-</td></tr>
<tr><td>1</td><td>ATLMTTH1</td><td>R/W</td><td>0</td><td rowspan="2">Automatic input current limit threshold<br><table><tr><td>00</td><td>4.25V</td></tr><tr><td>01</td><td>4.50V</td></tr><tr><td>10</td><td>4.75V</td></tr><tr><td>11</td><td>5.00V</td></tr></table>Initial value: ”01”=4.5V</td></tr>
<tr><td>0</td><td>ATLMTTH0</td><td>R/W</td><td>1</td></tr>
</table>

**Address=04H**

<table>
<tr><th>bit</th><th>Command</th><th>R/W</th><th>Initial value</th><th>Contents</th></tr>
<tr><td>7</td><td>-</td><td>R</td><td>0</td><td>-</td></tr>
<tr><td>6</td><td>-</td><td>R</td><td>0</td><td>-</td></tr>
<tr><td>5</td><td>OTGVCTL1</td><td>R/W</td><td>0</td><td rowspan="2">OTG output voltage<br><table><tr><td>00</td><td>5.0V</td></tr><tr><td>01</td><td>5.1V</td></tr><tr><td>10</td><td>5.2V</td></tr><tr><td>11</td><td>5.3V</td></tr></table>Initial value: ”00”=5.0V</td></tr>
<tr><td>4</td><td>OTGVCTL0</td><td>R/W</td><td>0</td></tr>
<tr><td>3</td><td>-</td><td>R</td><td>0</td><td>-</td></tr>
<tr><td>2</td><td>-</td><td>R</td><td>0</td><td>-</td></tr>
<tr><td>1</td><td>OTGUVTH1</td><td>R/W</td><td>0</td><td rowspan="2">UVLO threshold in OTG mode<br><table><tr><td>00</td><td>2.75V</td></tr><tr><td>01</td><td>3.00V</td></tr><tr><td>10</td><td>3.25V</td></tr><tr><td>11</td><td>3.50V</td></tr></table>Initial value: ”00”=2.75V</td></tr>
<tr><td>0</td><td>OTGUVTH0</td><td>R/W</td><td>0</td></tr>
</table>

**Address=05H**

<table>
<tr><th>bit</th><th>Command</th><th>R/W</th><th>Initial value</th><th>Contents</th></tr>
<tr><td>7</td><td>-</td><td>R</td><td>0</td><td>-</td></tr>
<tr><td>6</td><td>-</td><td>R</td><td>0</td><td>-</td></tr>
<tr><td>5</td><td>-</td><td>R</td><td>0</td><td>-</td></tr>
<tr><td>4</td><td>-</td><td>R</td><td>0</td><td>-</td></tr>
<tr><td>3</td><td>-</td><td>R</td><td>0</td><td>-</td></tr>
<tr><td>2</td><td>-</td><td>R</td><td>0</td><td>-</td></tr>
<tr><td>1</td><td>OVTHL1</td><td>R/W</td><td>1</td><td rowspan="2">Over charge threshold voltage<br><table><tr><td>00</td><td>200mV</td></tr><tr><td>01</td><td>150mV</td></tr><tr><td>10</td><td>100mV * Not recommended</td></tr><tr><td>11</td><td>50mV * Not recommended</td></tr></table>Initial value: ”10”=100mV<br>Notice: Please use 150mV or 200mV setting instead of initial value.<br>Over charge threshold voltage: Float voltage + α (setting voltage of this register) corresponds to over-charge voltage threshold.</td></tr>
<tr><td>0</td><td>OVTHL0</td><td>R/W</td><td>0</td></tr>
</table>

**Address=10H**

| bit | Command | R/W | Initial value | Contents |
|---|---|---|---|---|
| 7 | - | R | 0 | - |
| 6 | CHGTMCLR | R/W | 0 | Pre-charge safety timer / Charge safety timer clear<br>0: Timer operation<br>1: Both of charge timers are cleared. (Pulse command) In this time, status information of pre-charge and charge timer is cleared. |
| 5 | STBWDTM | R/W | 0 | Standby WD timer<br>0: 42sec WDT: Invalid<br>1: 42sec WDT: Valid<br>If the TC7710AWBG is controlled by $I^2C$ before DCIN is inputted, standby WD timer should be valid. |
| 4 | OTGWDTM | R/W | 0 | OTG WD timer<br>0: 42sec WDT: Invalid<br>1: 42sec WDT: Valid<br>OTG WD timer should be valid in OTG mode. |
| 3 | CHGWDTM | R/W | 0 | Charge WD timer<br>0: 42sec WDT: Invalid<br>1: 42sec WDT: Valid |
| 2 | PRCHGTM | R/W | 0 | Pre-charge safety timer<br>0: 36min timer: Valid<br>1: 36min timer: Invalid |
| 1 | CHGSTM | R/W | 0 | Charge safety timer<br>0: 240min timer: Valid<br>1: 240min timer: Invalid |
| 0 | TCSTON | R/W | 1 | Trickle charge safety timer<br>0: Pre-charge timer and charge timer do not operate in trickle charging.<br>1: Pre-charge timer and charge timer operate in trickle charging. |

**Address=11H**

| bit | Command | R/W | Initial value | Contents |
|---|---|---|---|---|
| 7 | - | R | 0 | - |
| 6 | - | R | 0 | - |
| 5 | - | R | 0 | - |
| 4 | BATMSDET | R/W | 1 | Unconnected battery detection<br>0: Invalid<br>1: Valid |
| 3 | ATCHG | R/W | 1 | Automatic charge control<br>0: Invalid (OFF in charge disable)<br>1: Valid (In charge disable, it is charged only when the battery voltage is lower than threshold.)<br>(In charge enable, it is charged regardless of the battery voltage.) It is charged automatically when the battery voltage is lower than dead battery threshold. |
| 2 | ENSEL | R/W | 0 | EN is controlled by $I^2C$ or EN pin.<br>0: Controlled by EN pin. (Polarity is selected by ENPINPOL)<br>1: Controlled by $I^2C$. (Selected by ENCMD.) |
| 1 | ENCMD | R/W | 1 | EN is controlled by $I^2C$.<br>0: Enable (charger is tuned on.)<br>1: Disable (charger is turned off.) |
| 0 | ENPINPOL | R/W | 1 | Polarity of EN control is selected by EN pin.<br>0: "L" is active. ("L"=Enable, "H"=Disable)<br>1: "H" is active. ("L"=Disable, "H"=Enable) |

**Address=12H**

| bit | Command | R/W | Initial value | Contents |
|---|---|---|---|---|
| 7 | TEMPDET | R/W | 0 | Battery thermal detection<br>0: Valid (Charging stops when the temperature exceeds the limit value. And charging re-starts automatically when the temperature falls within the range.)<br>1: Invalid (Charging does not stop though the temperature exceeds limit value.) |
| 6 | OVTLMT | R/W | 1 | IC temperature limit<br>0: Only status bit: Valid<br>1: Status bit: Valid. Permission of suspending charge. |
| 5 | BATOV | R/W | 1 | Battery OV<br>0: Charging cycle does not terminate when battery voltage is OV.<br>1: Charging cycle terminates when battery voltage is OV. |
| 4 | ATRCHG | R/W | 0 | Auto re-charge<br>0: Valid<br>1: Invalid |
| 3 | CT | R/W | 0 | Terminating<br>0: Permitting termination of charging cycle.<br>1: Not permitting termination of charging cycle.<br>Charging is completed when charge current is lower than the value set by CEI1-0. |
| 2 | CCISET | R/W | 1 | Fast charge setting (PRCCTH = "1": Valid)<br>0: Setting forced pre-charge current<br>1: Permission of setting fast charge current |
| 1 | PRCCTH | R/W | 0 | Threshold voltage from pre-charge to fast charge<br>0: Valid<br>1: Invalid |
| 0 | TRCHG | R/W | 0 | Trickle charge<br>0: Valid<br>1: Invalid |

**Address=13H**

<table>
<tr><th>bit</th><th>Command</th><th>R/W</th><th>Initial value</th><th>Contents</th></tr>
<tr><td>7</td><td>OTGMD</td><td>R/W</td><td>0</td><td>OTG mode<br><table><tr><td>0</td><td>Invalid</td></tr><tr><td>1</td><td>Valid</td></tr></table></td></tr>
<tr><td>6</td><td>USB51</td><td>R/W</td><td>0</td><td>Input current limit level set by ILIM_OTG pin in USB ("L" level).<br><table><tr><td>0</td><td>USB500 mode</td></tr><tr><td>1</td><td>USB100 mode</td></tr></table>This setting is valid under the following condition.<br>LMT_OTG1-0 = "01", ILIM_OTG pin="L".</td></tr>
<tr><td>5</td><td>ATILMT</td><td>R/W</td><td>0</td><td>Automatic input current limit<br><table><tr><td>0</td><td>Valid</td></tr><tr><td>1</td><td>Invalid</td></tr></table>Input current limit is set USB100 when DCIN falls to the level set by ATLMTTH1-0. When an interrupt is cleared, it is set to previous limit level.</td></tr>
<tr><td>4</td><td>ATPSDET</td><td>R/W</td><td>0</td><td>Automatic power source detection<br><table><tr><td>0</td><td>Valid</td></tr><tr><td>1</td><td>Invalid (Set level = Limit level)</td></tr></table></td></tr>
<tr><td>3</td><td>LMT_OTG1</td><td>R/W</td><td>0</td><td rowspan="2">Input current limit and OTG control are set by pin or $I^2C$.<br><table><tr><td>00</td><td>Input current limit is set by $I^2C$ (ILIMLVL1-0). OTG mode is set by $I^2C$ (OTGMD).</td></tr><tr><td>01</td><td>Input current limit is set by ILIM_OTG pin.<br>"L"= USB mode, USB51="L" -> USB500 mode<br>"L"= USB mode, USB51="H" -> USB100 mode<br>"H"=AC mode (set by ACILMT4-0)<br>OTG mode is set by $I^2C$ (OTGMD).</td></tr><tr><td>10</td><td>Input current limit is set by $I^2C$ (ILIMLVL1-0). OTG mode is set by ILIM OTG pin ("H" active).<br>"L": Invalid, "H": Valid</td></tr><tr><td>11</td><td>Input current limit is set by $I^2C$ (ILIMLVL1-0). OTG mode is set by ILIM_OTG pin ("L" active).<br>"L": Valid, "H": Invalid</td></tr></table></td></tr>
<tr><td>2</td><td>LMT_OTG0</td><td>R/W</td><td>1</td></tr>
<tr><td>1</td><td>ILIMLVL1</td><td>R/W</td><td>1</td><td rowspan="2">Input current limit level in $I^2C$ control.<br><table><tr><td>00</td><td>USB500 mode (Typ. = 475mA, Max = 500mA)</td></tr><tr><td>01</td><td>USB100 mode (Typ. = 90mA, Max = 100mA)</td></tr><tr><td>10</td><td>AC mode (Set by ACILMT4-0.)</td></tr><tr><td>11</td><td>AC mode (Set by ACILMT4-0.)</td></tr></table>Initial value: ”10” = AC mode.</td></tr>
<tr><td>0</td><td>ILIMLVL0</td><td>R/W</td><td>0</td></tr>
</table>

**Address=14H**

| bit | Command | R/W | Initial value | Contents |
|---|---|---|---|---|
| 7 | - | R | 0 | - |
| 6 | - | R | 0 | - |
| 5 | - | R | 0 | - |
| 4 | VMONICNT | R/W | 0 | VMONI control<br>0: Valid<br>1: Invalid |
| 3 | INTOUT | R/W | 0 | Information from STAT pin is selected.<br>0: Status information is outputted. (Information is set by STATMD. STATOUT = "0": Output is valid.)<br>1: Interrupt output (STATOUT = "1": Interrupt information is valid.) |
| 2 | STATMD | R/W | 0 | Information from STAT pin is selected.<br>0: Charging state is indicated.<br>1: State of input UV/OV is indicated. |
| 1 | STATOUT | R/W | 0 | Output of STAT pin: ON/OFF<br>0: ON<br>1: OFF |
| 0 | SFTRST | R/W | 0 | Soft reset command<br>0: OFF<br>1: Internal reset (Pulse command)<br>Register is cleared and default value is reloaded. |

**Address=15H**

| bit | Command | R/W | Initial value | Contents |
|---|---|---|---|---|
| 7 | INTCLR7 | R | 0 | Interrupt factor is cleared.<br>Interrupt factor for each bit of 20h is cleared. (Pulse command) |
| 6 | INTCLR6 | R/W | 0 | |
| 5 | INTCLR5 | R/W | 0 | |
| 4 | INTCLR4 | R/W | 0 | |
| 3 | INTCLR3 | R/W | 0 | |
| 2 | INTCLR2 | R/W | 0 | |
| 1 | INTCLR1 | R/W | 0 | |
| 0 | INTCLR0 | R/W | 0 | |

**Address=16H**

| bit | Command | R/W | Initial value | Contents |
|---|---|---|---|---|
| 7 | INTMSK7 | R | 0 | Interrupt output from STAT pin is masked. (Interrupt information is active regardless of state of this bit.)<br>0: Interrupt factor is not masked.<br>1: Interrupt factor is masked. |
| 6 | INTMSK6 | R/W | 1 | |
| 5 | INTMSK5 | R/W | 1 | |
| 4 | INTMSK4 | R/W | 1 | |
| 3 | INTMSK3 | R/W | 1 | |
| 2 | INTMSK2 | R/W | 1 | |
| 1 | INTMSK1 | R/W | 1 | |
| 0 | INTMSK0 | R/W | 1 | |

**Address=1EH**

| bit | Command | R/W | Initial value | Contents |
|---|---|---|---|---|
| 7 | BIASCRT1 | R/W | 0 | Current source for temperature monitoring<br>00: 200μA<br>01: 80μA<br>10: 40μA<br>11: 20μA |
| 6 | BIASCRT0 | R/W | 0 | |
| 5 | - | R | 0 | - |
| 4 | - | R | 0 | - |
| 3 | COLDVTH1 | R/W | 0 | Threshold level for low temperature judge<br>00: 1.399V<br>01: 1.491V<br>10: 1.577V<br>11: 1.654V |
| 2 | COLDVTH0 | R/W | 0 | |
| 1 | HOTVTH1 | R/W | 0 | Threshold level for high temperature judge<br>00: 0.509V<br>01: 0.574V<br>10: 0.647V<br>11: 0.726V |
| 0 | HOTVTH0 | R/W | 1 | |

**Address=1FH**

| bit | Command | R/W | Initial value | Contents |
|---|---|---|---|---|
| 7 | - | R | 0 | - |
| 6 | - | R | 0 | - |
| 5 | - | R | 0 | - |
| 4 | - | R | 0 | - |
| 3 | - | R | 0 | - |
| 2 | I2CSVAD2 | R/W | 0 | $I^2C$ slave address |
| 1 | I2CSVAD1 | R/W | 0 | |
| 0 | I2CSVAD0 | R/W | 0 | |

| | |
|---|---|
| 000 | No conversion -> 0001001 |
| 001 | Convert bit0 -> 0001000 |
| 010 | Convert bit1 -> 0001011 |
| 011 | Convert bit2 -> 0001101 |
| 100 | Convert bit3 -> 0000001<br>*Reserved: CBUS address |
| 101 | Convert bit4 -> 0011001 |
| 110 | Convert bit5 -> 0101001 |
| 111 | Convert bit6 -> 1001001 |

**Address=20H**

| bit | Command | R/W | Initial value | Contents |
|---|---|---|---|---|
| 7 | - | R | 0 | - |
| 6 | INTVBAT | R | 0 | 1: Charge state is back to previous mode by battery voltage drop. |
| 5 | INTATIL | R | 0 | 1: Automatic input current limit is occurred. |
| 4 | INTSTBER | R | 0 | Interrupt of standby WDT error<br>1: WDT error is occurred. Register of 00H - 13H, 1EH and 1FH are initialized. |
| 3 | INTOTGER | R | 0 | Interrupt of OTG error (Interrupt factor should be confirmed 22H)<br>1: OTG error is occurred. |
| 2 | INTRCHG | R | 0 | Interrupt of re-charge<br>1: Re-charge |
| 1 | INTCHGER | R | 0 | Interrupt of charge error (Interrupt factor should be confirmed 21H and 23H.)<br>1: Charge error is occurred. |
| 0 | INTTERMN | R | 0 | Interrupt of charge complete. However, it is valid only when CT (12H, bit3) is "0".<br>1: Charge completion |

**Address=21H**

| bit | Command | R/W | Initial value | Contents |
|---|---|---|---|---|
| 7 | ST_BATMS | R | 0 | Status<br>1: Unconnected battery detected. |
| 6 | ST_VBATN | R | - | Status: Initial value depends on DCIN voltage and battery voltage.<br>1: DCIN < VBATT |
| 5 | ST_BATOV | R | - | Status: Initial value depends on battery voltage.<br>1: Battery OVLO |
| 4 | ST_DCOVL | R | - | Status: Initial value depends on DCIN input voltage.<br>1: Input OVLO |
| 3 | ST_DCUVL | R | - | Status: Initial value depends on DCIN input voltage.<br>1: Input UVLO |
| 2 | ST_JCTON | R | - | Status: Initial value depends on chip temperature.<br>It operates though in charging or OTG mode.<br>Chip temperature ≥ 135°C: 1, Chip temperature ≤ 115°C: 0<br>1: Internal temperature is limited. |
| 1 | ST_BATHT | R | - | Status: Initial value depends on battery temperature.<br>1: High temperature detected |
| 0 | ST_BATCL | R | - | Status: Initial value depends on battery temperature.<br>1: Low temperature detected |

**Address=22H**

| bit | Command | R/W | Initial value | Contents |
|---|---|---|---|---|
| 7 | - | R | 0 | - |
| 6 | - | R | 0 | - |
| 5 | - | R | 0 | - |
| 4 | ST_OTGVOL | R | 0 | Status: It shows “0” for 250ms after starting OTG.<br>1: Output voltage drops under DCIN UVLO. |
| 3 | ST_OTGJCT | R | - | Status: Initial value depends on chip temperature.<br>It operates though in charging or OTG mode.<br>Chip temperature ≥ 135°C: 1, Chip temperature ≤ 115°C: 0.<br>1: Internal temperature limited. |
| 2 | ST_OTWDT | R | 0 | Status<br>1: WDT error occurred.<br>OTG supply is shut off. Registers of 00H-13H, 1EH and 1FH are initialized. |
| 1 | ST_OTGLM | R | - | Status: Initial value depends on OTG current.<br>1: OTG current limit reached |
| 0 | ST_ OTUVL | R | - | Status: Initial value depends on battery voltage.<br>1: OTG battery UVLO |

**Address=23H**

| bit | Command | R/W | Initial value | Contents |
|---|---|---|---|---|
| 7 | - | R | 0 | - |
| 6 | - | R | 0 | - |
| 5 | - | R | 0 | - |
| 4 | - | R | 0 | - |
| 3 | - | R | 0 | - |
| 2 | ST_CHWDT | R | 0 | Status<br>1: WDT error occurred.<br>Charging stops. Register of 00H-13H, 1EH and 1FH are initialized. However, only charging timer operates continuously. |
| 1 | ST_TMER1 | R | 1 | Status: Safety timer<br>00: No timeout occurred.<br>01: Pre-charge timer expired.<br>10: Charge timer expired.<br>11: Waiting to start charge |
| 0 | ST_TMER0 | R | 1 | |

**Address=24H**

| bit | Command | R/W | Initial value | Contents |
|---|---|---|---|---|
| 7 | ST_OTGMD | R | 0 | Status<br>1: OTG in progress |
| 6 | - | R | 0 | - |
| 5 | ST_CGED1 | R | 0 | Status: Charge completion<br>1: At least, one charge cycle starts and completes. |
| 4 | ST_CGED0 | R | - | Status: Charge completion<br>Initial value depends on charge current.<br>1: Charge current is lower than charge completion current (Valid only in CV charge mode.). |
| 3 | ST_TRCHG | R | 0 | Status<br>1: Trickle charge mode (VBATT < 2.1V) |
| 2 | ST_CGMD1 | R | 0 | Status: Charging<br>00: No charge<br>01: Pre-charge<br>10: Constant current charge (CC mode)<br>11: Constant voltage charge (CV mode) |
| 1 | ST_CGMD0 | R | 0 | |
| 0 | ST_CHGEN | R | 0 | Status: Charge valid / invalid<br>0: Charge invalid<br>1: Charge valid |

**Address=25H**

| bit | Command | R/W | Initial value | Contents |
|---|---|---|---|---|
| 7 | - | R | 0 | - |
| 6 | - | R | 0 | - |
| 5 | ST_USB51 | R | * | Status: USB5/1 mode<br>Initial value is determined by 13h, 6.<br>0: USB 100mA mode<br>1: USB 500mA mode |
| 4 | ST_USBAC | R | 0 | Status: USB / AC mode<br>0: USB mode<br>1: AC mode |
| 3 | ST_DTBSY | R | 0 | Status: Power source detection function<br>0: Not busy<br>1: Busy |
| 2 | ST_PSDST | R | 1 | Status: Power source detection<br>0: Detecting<br>1: Finished (after source detected) |
| 1 | ST_STYP1 | R | 0 | Status: Power source type<br>00: Non connection<br>01: SDP (Standard Downstream Port)<br>10: CDP (Charging Downstream Port)<br>11: DCP (Dedicated Charging Port) |
| 0 | ST_STYP0 | R | 0 | |

**Address=26H**

| bit | Command | R/W | Initial value | Contents |
|---|---|---|---|---|
| 7 | - | R | 0 | - |
| 6 | REVCODE2 | R | 0 | Device revision code<br>000: #1.0 |
| 5 | REVCODE1 | R | 0 | |
| 4 | REVCODE0 | R | 0 | |
| 3 | - | R | 0 | - |
| 2 | - | R | 0 | - |
| 1 | - | R | 0 | - |
| 0 | - | R | 0 | - |

## 9. Mode Transition Diagram

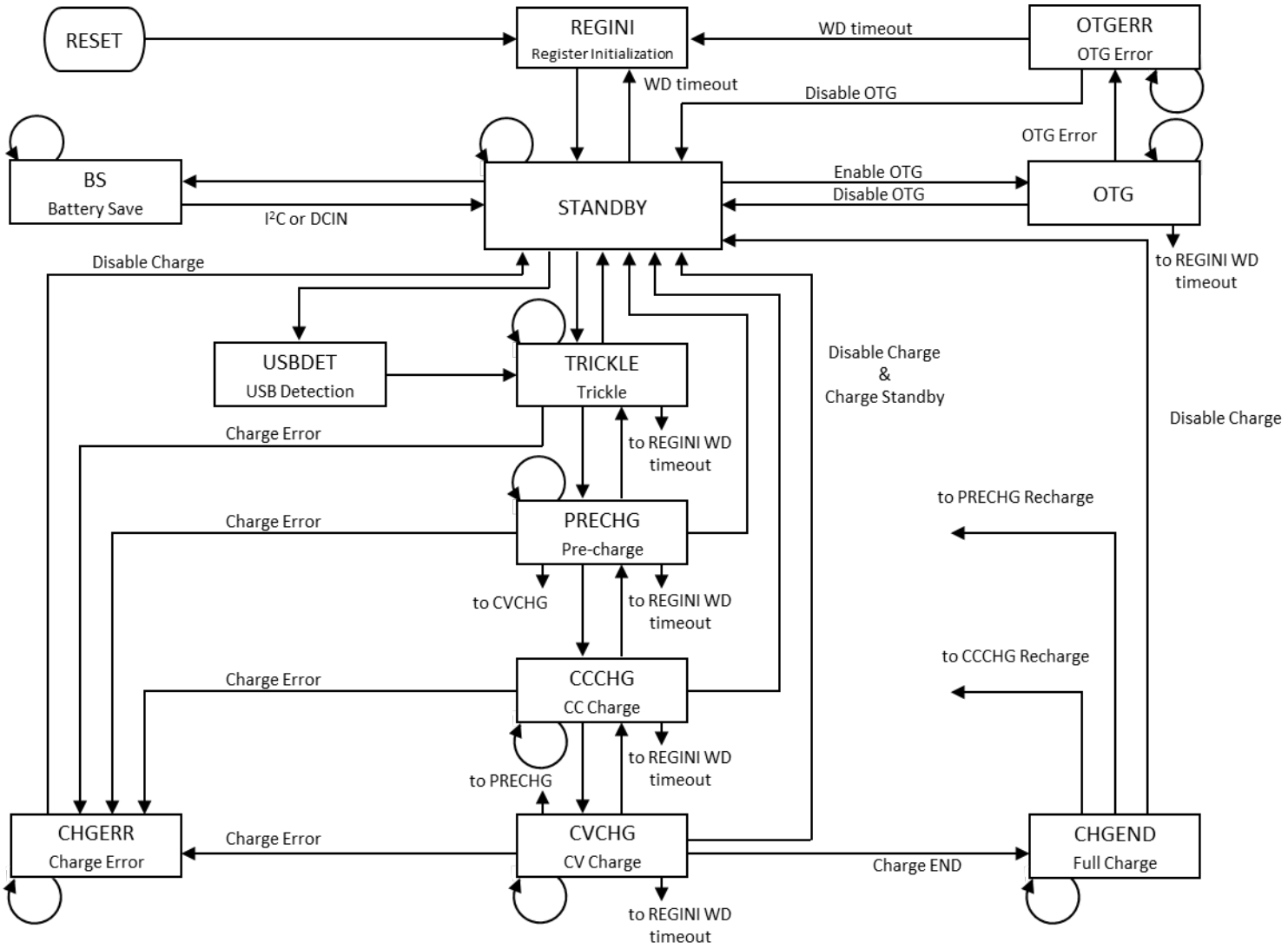



**Figure 9-1 Mode transition diagram**

## 10. Flow chart of function

**<Before charge>**

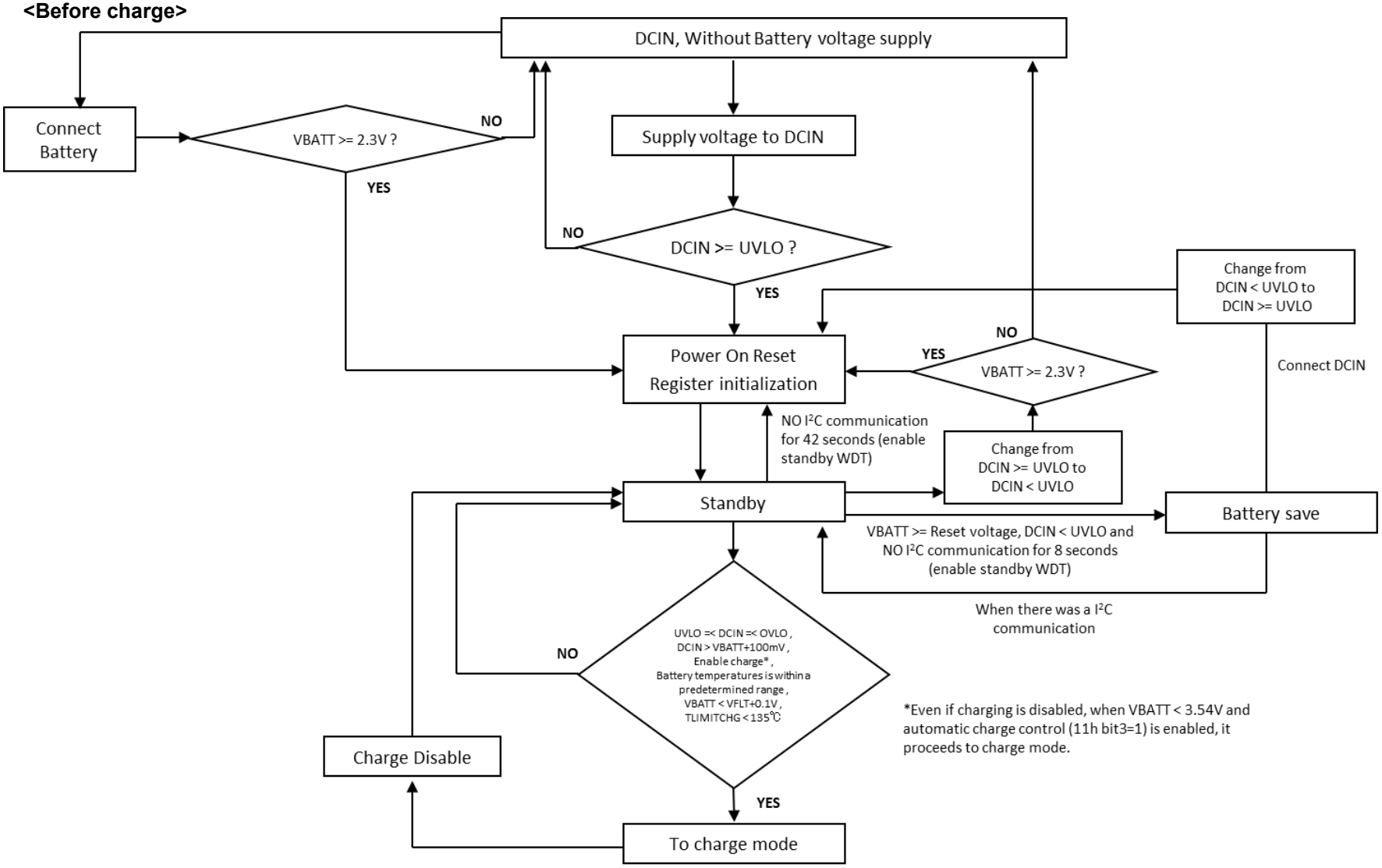



**Figure 10-1 Flow chart: Before charge**

**<After start charging>**

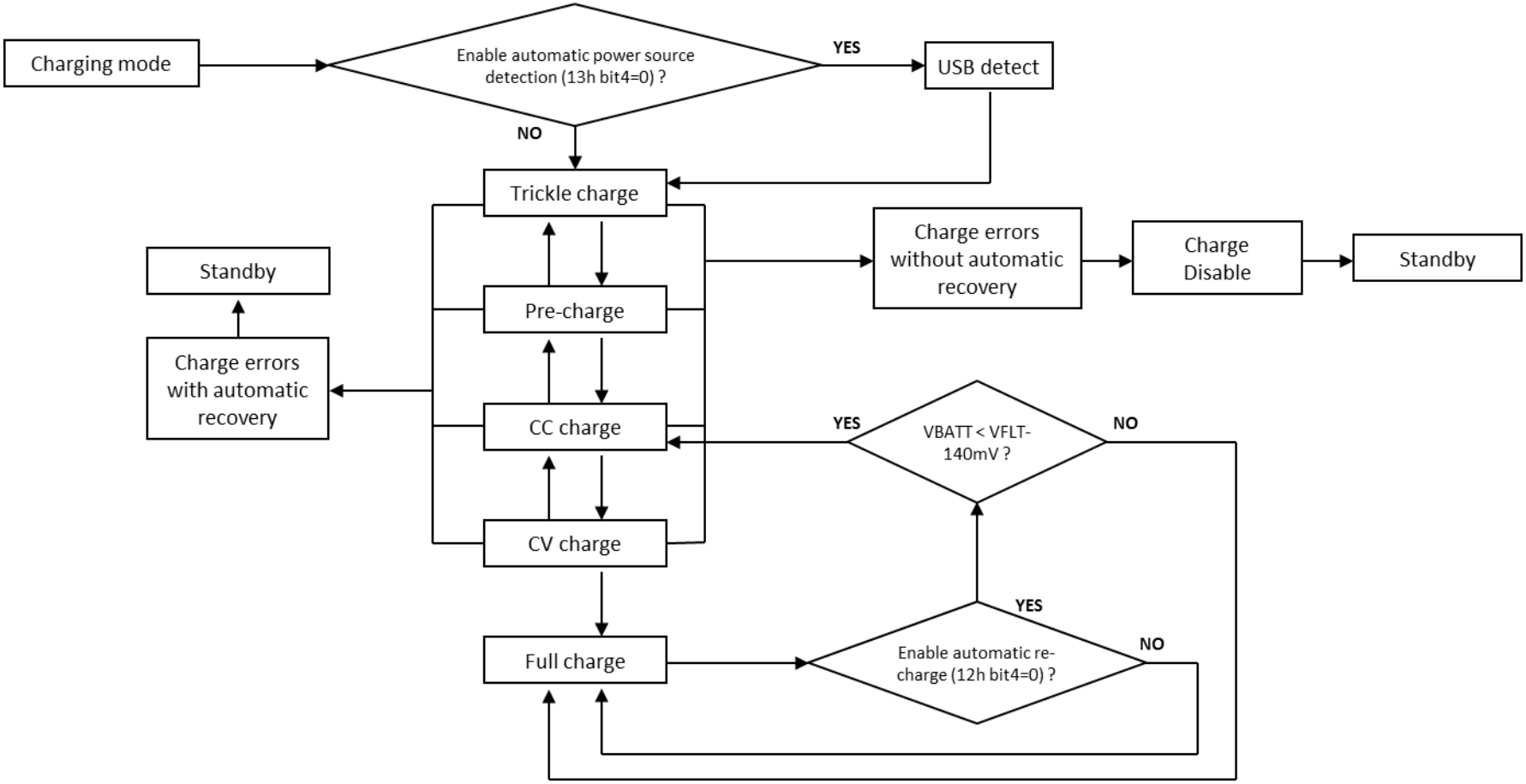



**Figure 10-2 Flow chart: After start charging**

**<Trickle charge>**

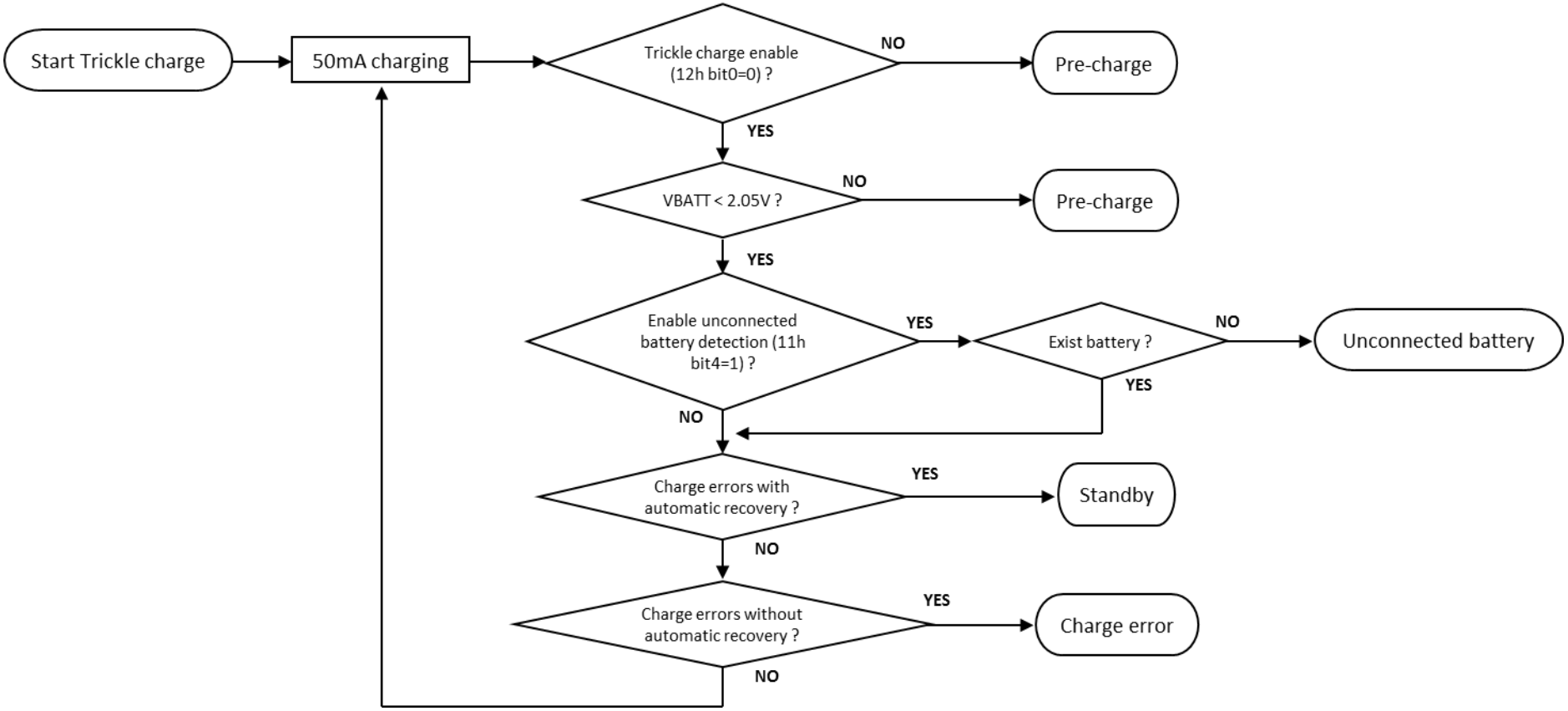



**Figure 10-3 Flow chart: Trickle charge**

**<Pre charge>**

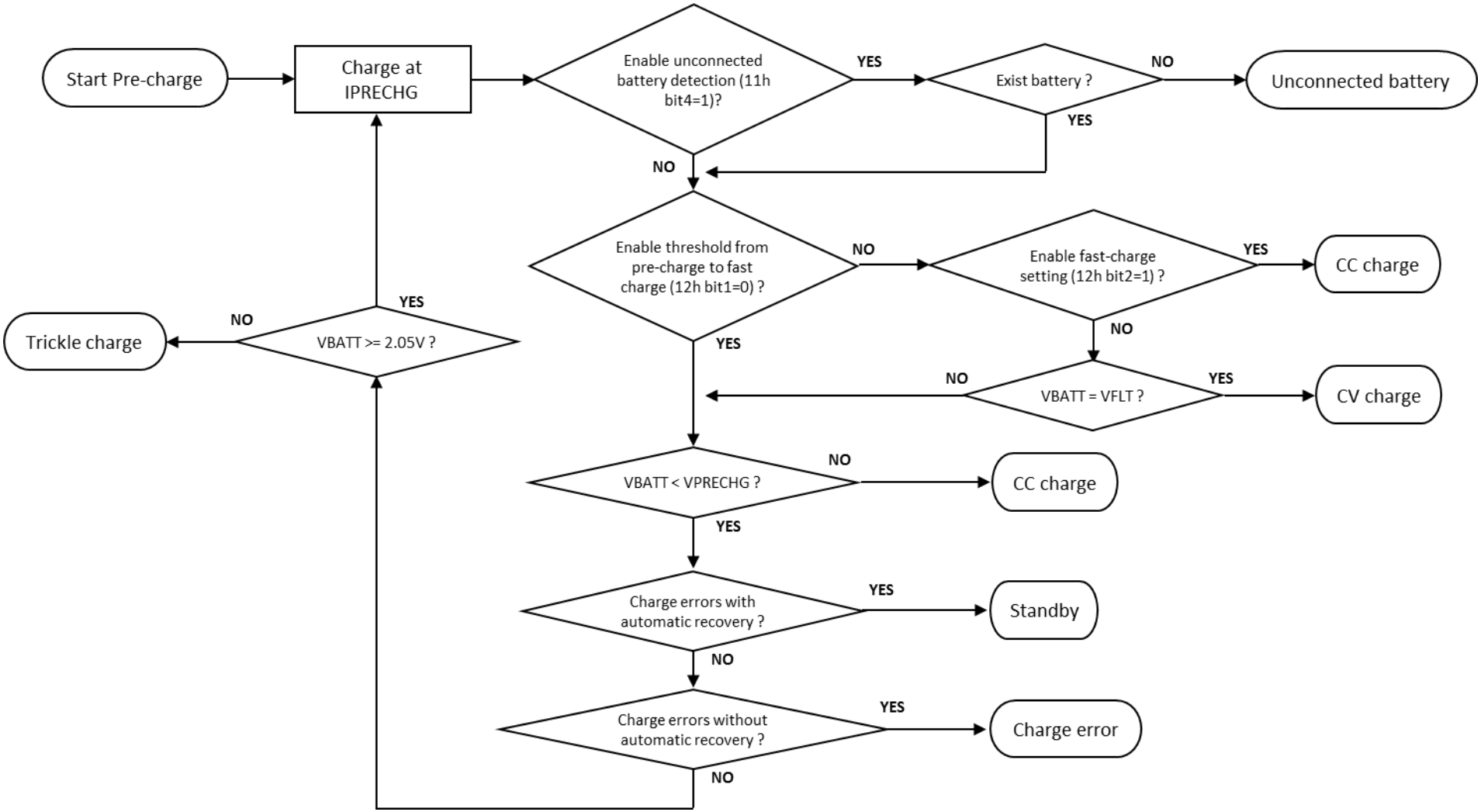



**Figure 10-4 Flow chart: Pre-charge**

**<CC charge>**

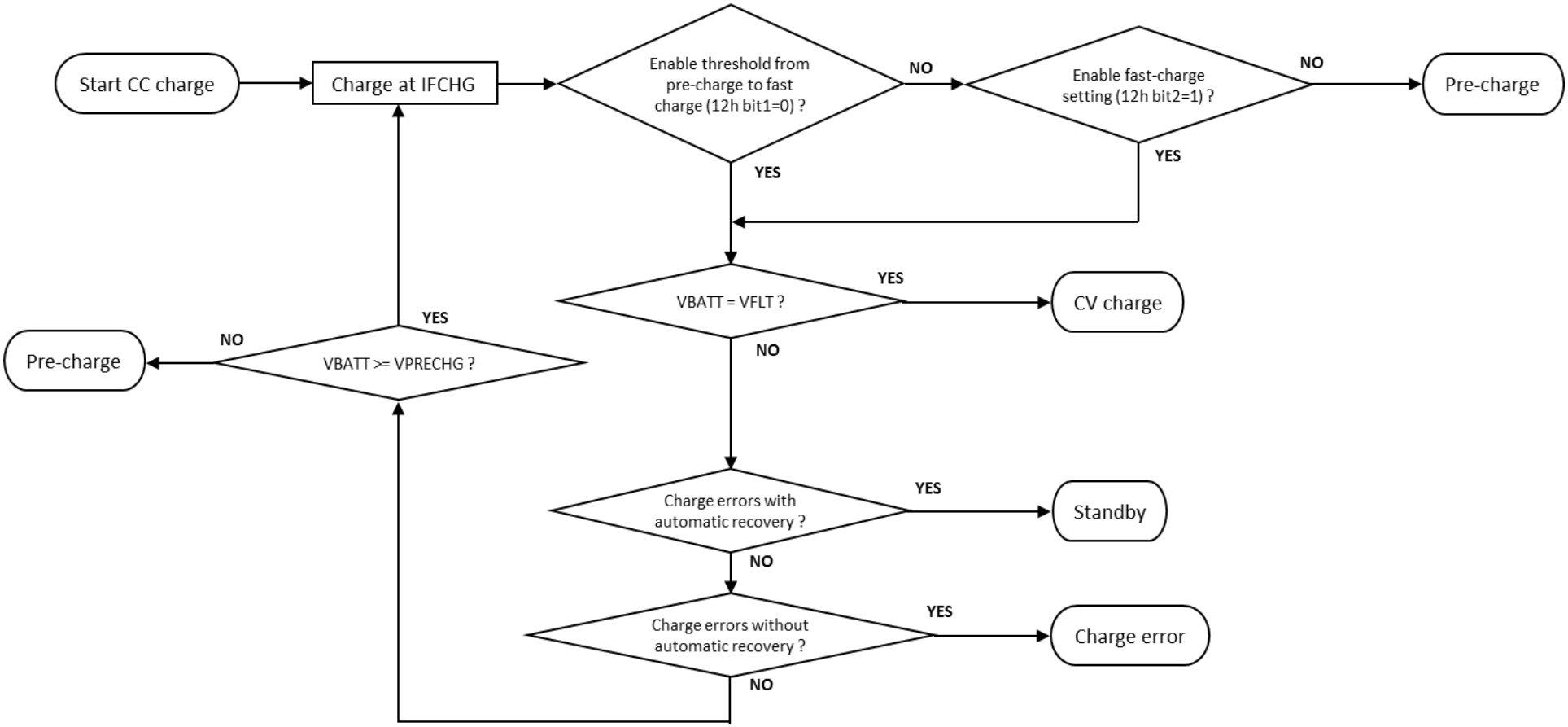



**Figure 10-5 Flow chart: CC charge**

**<CV charge>**

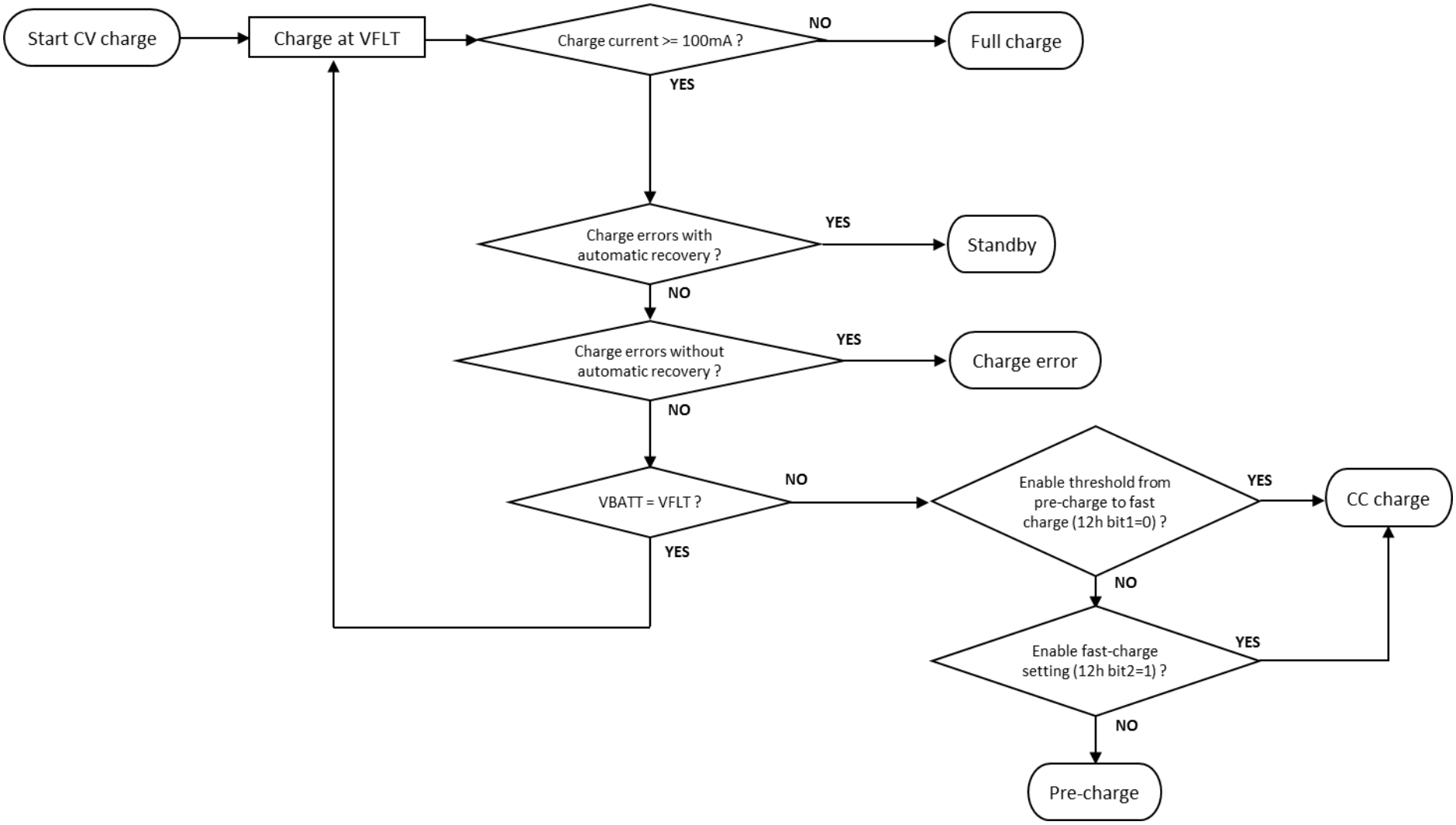



**Figure 10-6 Flow chart: CV charge**

**<Full charge>**

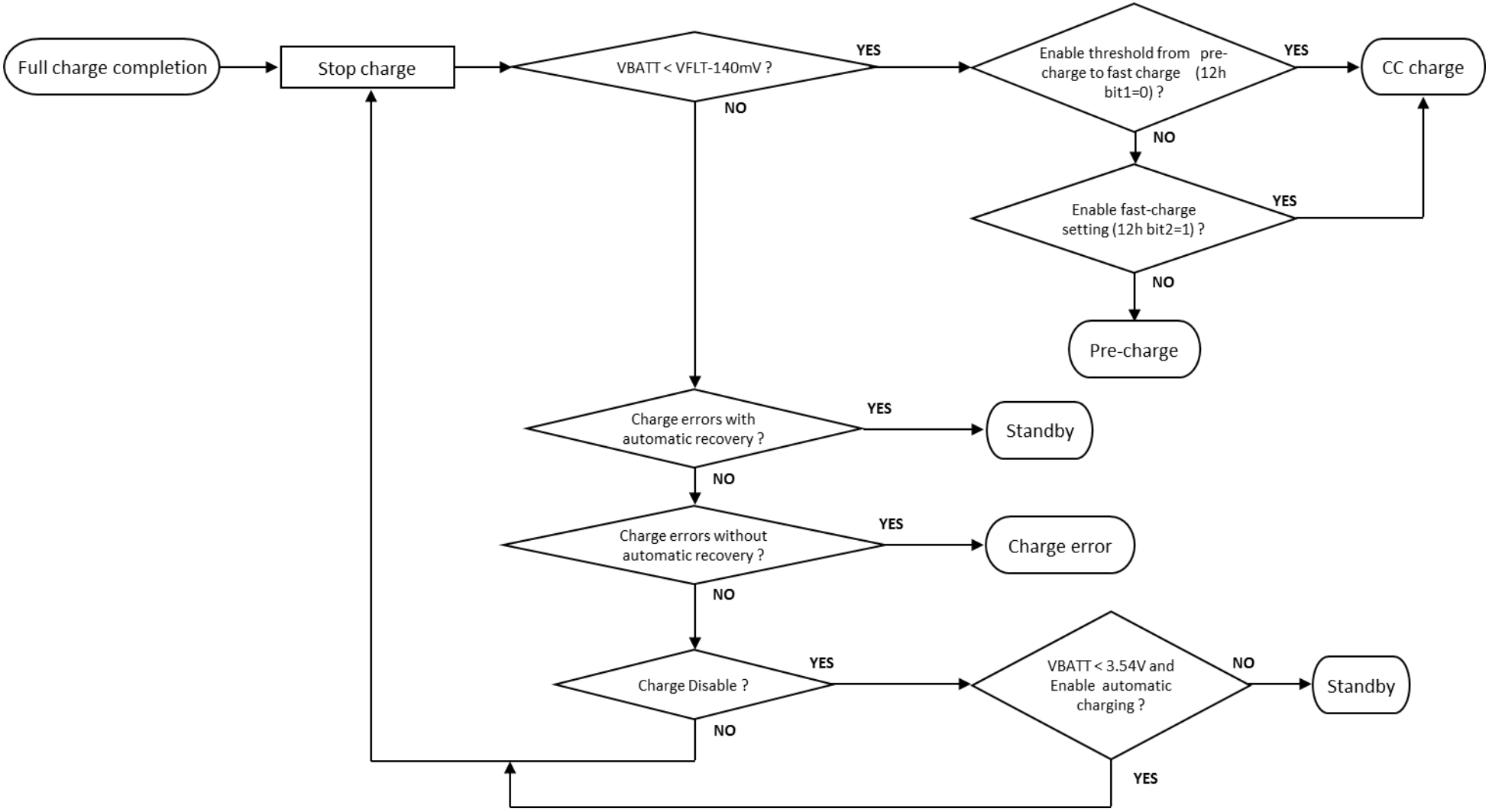



**Figure 10-7 Flow chart: Full charge**

**<Unconnected battery detection>**

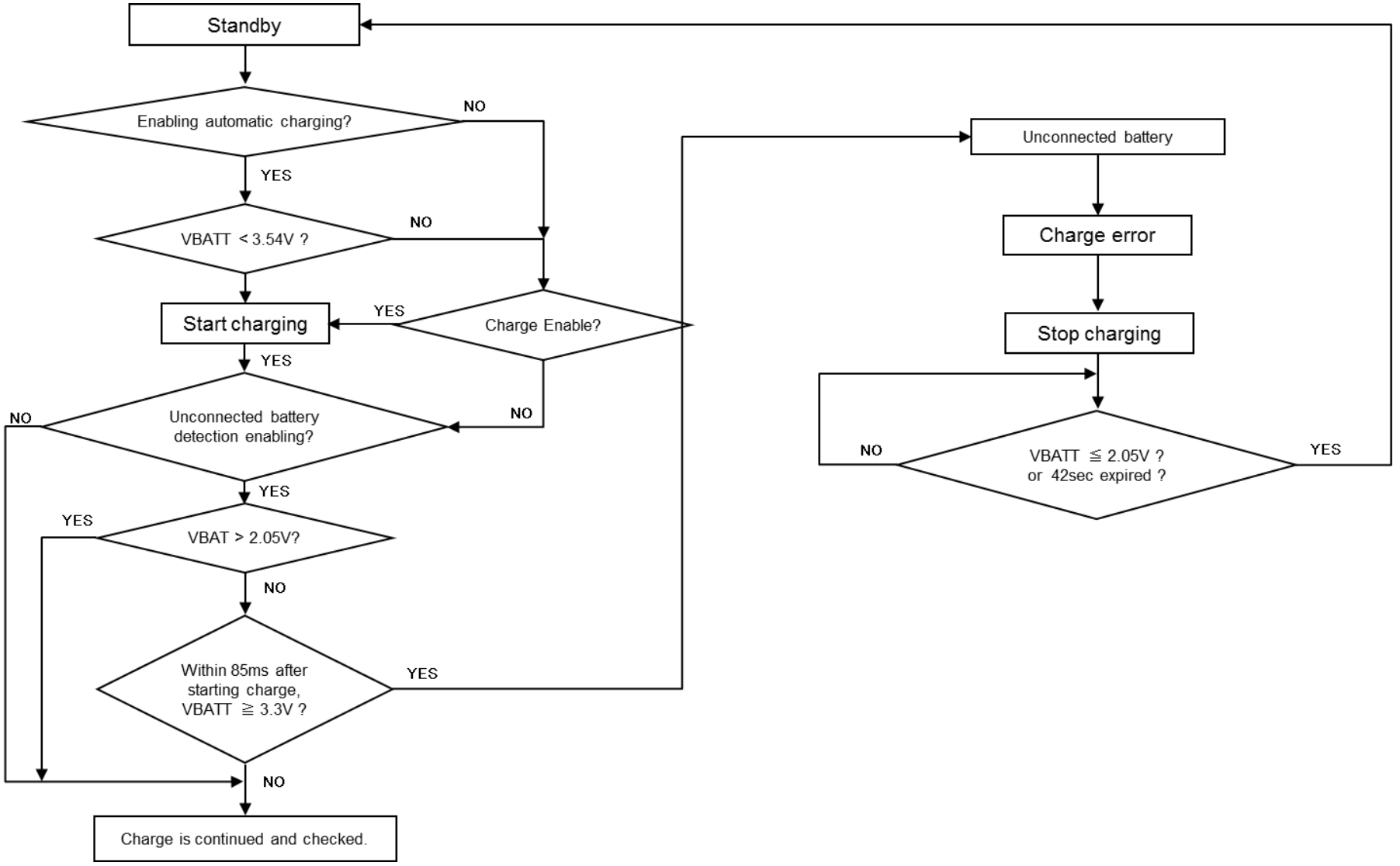



**Figure 10-8 Flow chart: Unconnected battery detection**

**<OTG>**

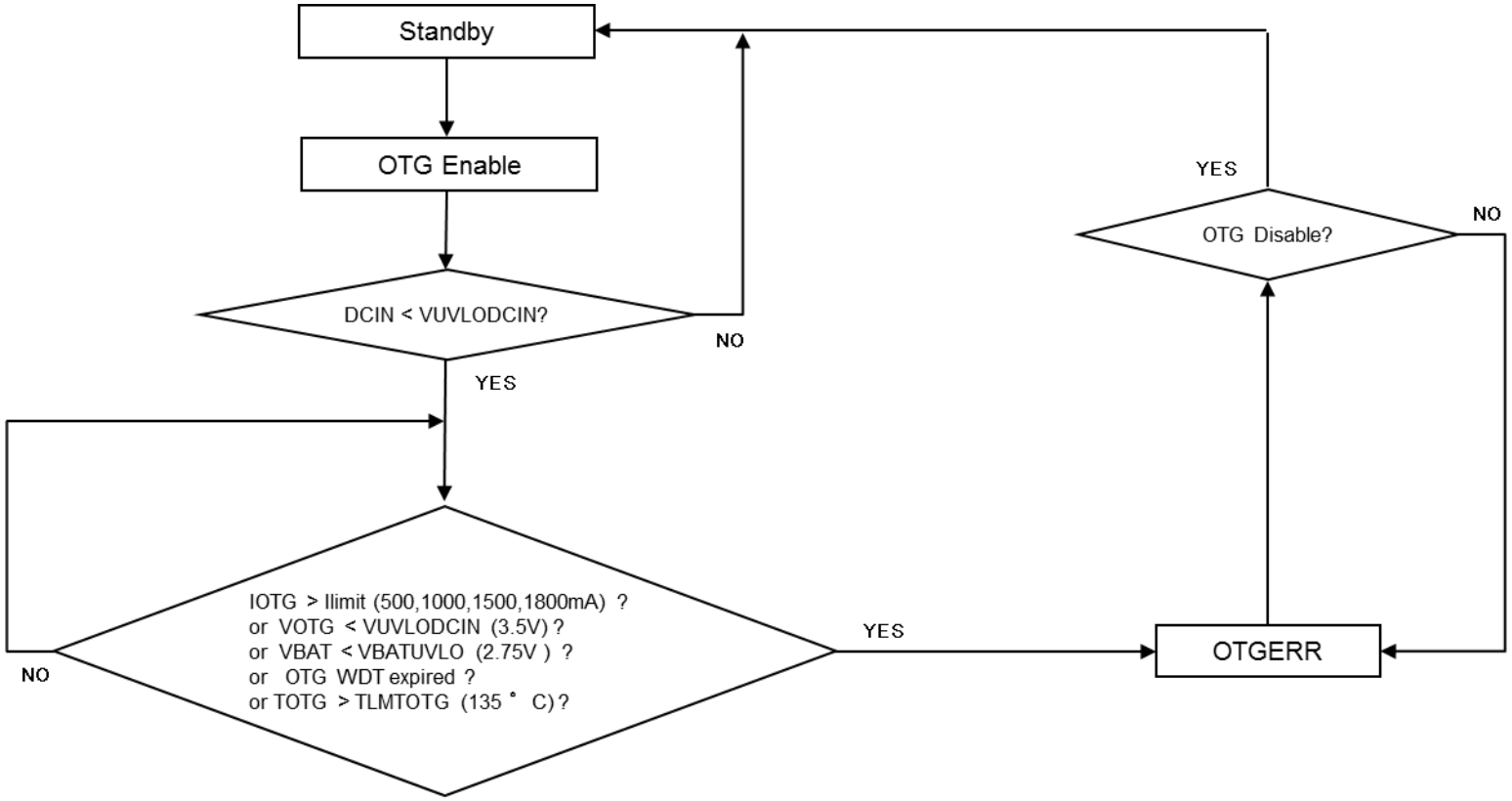
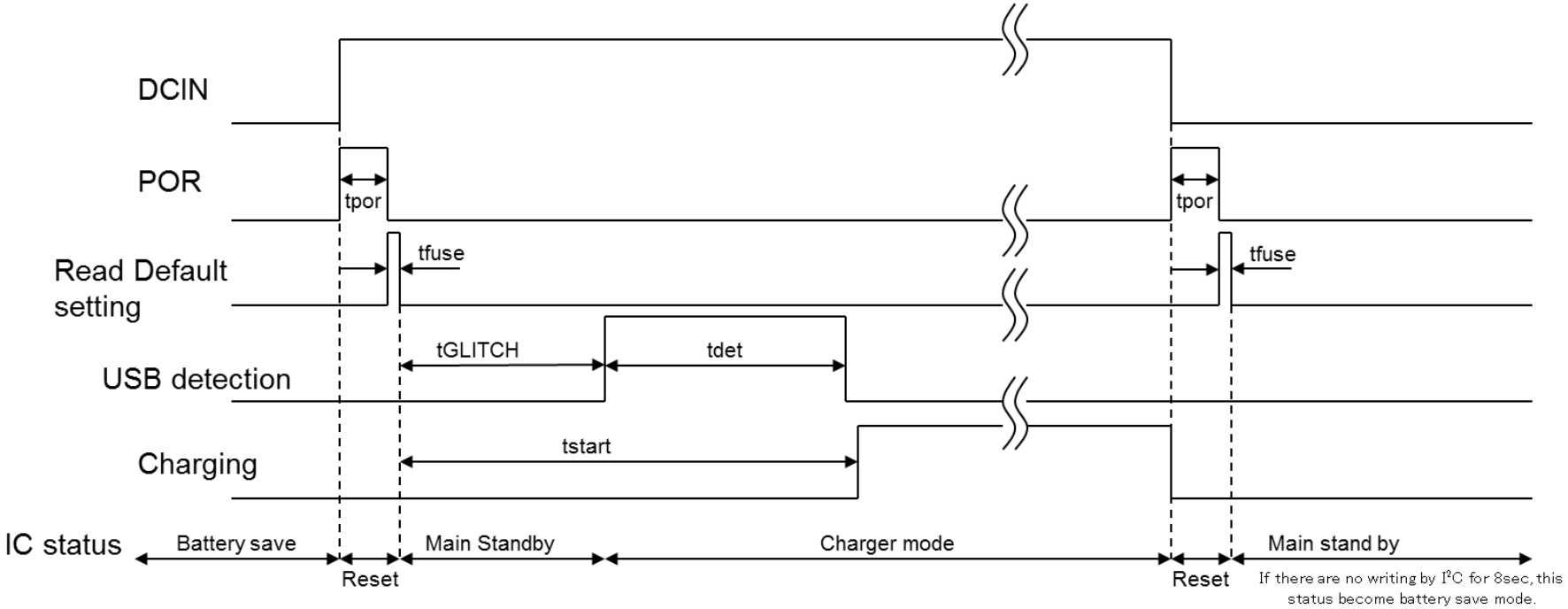



**Figure 10-9 Flow chart: OTG**

## 11. Timing chart

**<DCIN ON / OFF>**




| Symbol | Contents | Time |
|---|---|---|
| tpor | DCIN～POR time | 20ms (Max) |
| tfuse | Read default setting | 5μs (Max) |
| tGLITCH | Removal Chattering | 168ms (Max210ms) |
| tdet | USB detection time: No connect case | 470ms (Max) |
| | USB detection time: SDP | 95ms (Max) |
| | USB detection time : CDP/DCP | 164ms (Max) |
| tstart | DCIN～start charging | tdchat+tdet+1μs |

**Figure 11-1 Timing chart: DCIN ON / OFF**

**<Forced charge termination>**

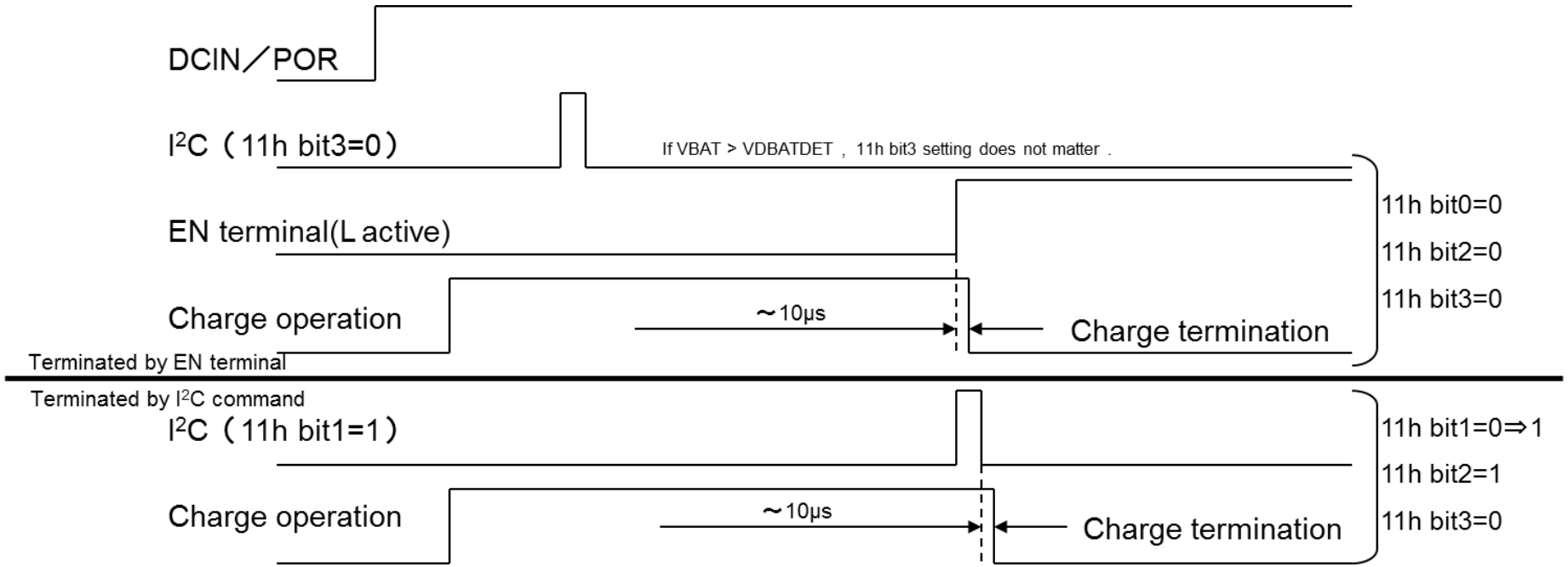



**Figure 11-2 Timing chart: Forced charge termination**

| | | |
|---|---|---|
| Auto charge control | 11H,bit3=”0” | Set charge disable, forced charge termination. |
| | 11H,bit3=”1” | Set charge disable, charge operates if VBAT < VDBATDET(00H,bit7). [Initial value] |
| EN control polarity | 11H,bit2=”0” | Controlled by EN pin. [Initial value] |
| | 11H,bit2=”1” | Controlled by $I^2C$ command. |
| EN controlled by $I^2C$ | 11H,bit1=”0” | Charge enable |
| | 11H,bit1=”1” | Charge disable |
| EN pin polarity select | 11H,bit0=”0” | L active (EN=L: Enable, H: Disable) |
| | 11H,bit0=”1” | H active (EN=H: Enable, L: Disable) |

**<I²C>**

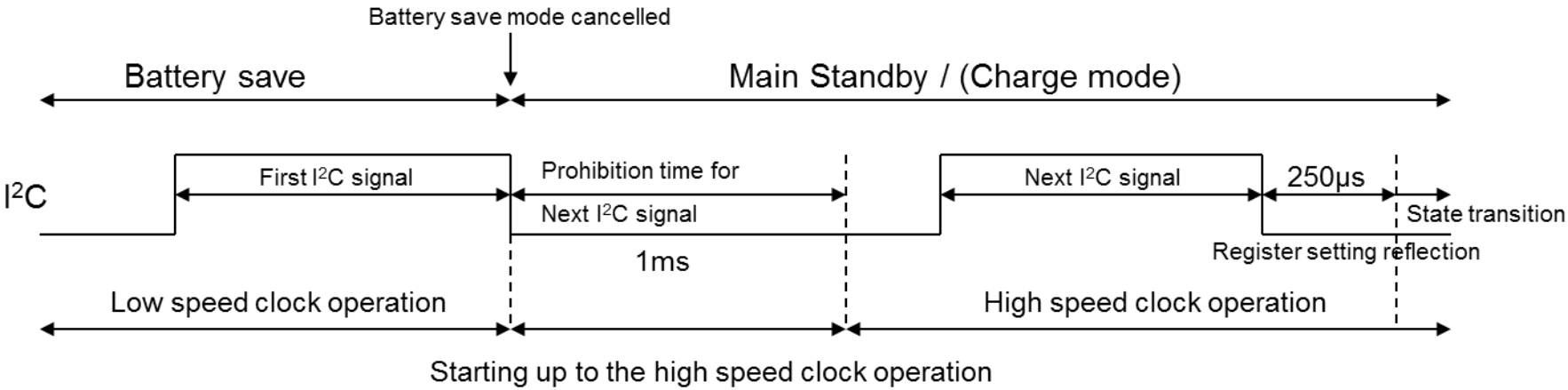



**Figure 11-3 Timing chart: I²C**

- When DCIN = UVLO and standby WDT is invalid, or OTG = Disable, the TC7710AWBG becomes the battery save mode.
- If there is an I²C signal among the battery save mode, the TC7710AWBG changes the mode to the standby mode.
  Wait time 1ms is necessary to write next I²C signal successively.
- If standby WDT is valid by command in the battery save mode, the TC7710AWBG cannot resume the battery save mode.
- When the TC7710AWBG is communicated by I²C in standby mode or charge mode, register setting is reflect soon, but state transition is occurred 250µs after that.
  If I²C command is set successively in 250µs, state transition is occurred 250µs after last communication.

## 12. Absolute Maximum Ratings

**Table 12-1 Absolute maximum ratings**

(Unless otherwise specified, Ta = 25°C)

| Characteristics | Symbol | Rating | Unit | Remarks |
|---|---|---|---|---|
| Applied voltage of SW pin | Vin1 | -0.3 to 6.5 | V | |
| Applied voltage of DCIN pin, MID pin | Vin2 | -1.5 to 10.0 | V | |
| Applied voltage of STAT pin | Vin3 | -0.3 to 6.5 | V | |
| Applied voltage of other pins | Vin4 | -0.3 to 6.5 | V | |
| Power dissipation 1 (*Note1) | PDmax | 1080 | mW | |
| Operating temperature (*Note2) | Topr | -40 to 85 | °C | |
| Junction temperature | Tj | 150 | °C | |
| Storage temperature | Tstg | -55 to 150 | °C | |

Note1: When Ta is 25°C or more, 16.67mW decreases per 1°C rise.

Note2: The operation range of actual use without any problems.

Note3: The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings. Exceeding the rating (s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion. Please use the IC within the specified operating ranges.

## 13. Electrical Characteristics

### DC characteristics (1)

**Table 13-1 DC characteristics**

(Unless otherwise specified, $V_{DCIN}$ = 5.0V, $V_{FLT}$ = 4.2V, $V_{BATT}$ = 3.7V, Ta = -30 to 85°C, all voltages are relative to GND.)

| Characteristics | Symbol | Test condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| **Input voltage** | $V_{DCIN}$ | | +4.35 | - | +6.5 | V |
| **Input UVLO voltage** | $V_{UVLODCIN}$ | $V_{DCIN}$ rising | 3.40 | 3.60 | 3.80 | V |
| | | $V_{DCIN}$ falling | 3.20 | 3.50 | 3.70 | V |
| **Input OVLO voltage** | $V_{OVLODCIN}$ | $V_{DCIN}$ rising (no glitch filter) | 6.20 | 6.50 | 6.90 | V |
| | | $V_{DCIN}$ falling | 6.10 | 6.30 | 6.60 | V |
| **VMONI output voltage** | $V_{VMONIRNG}$ | $V_{UVLODCIN}$ < $V_{DCIN}$ < $V_{OVLODCIN}$, | - | $V_{DCIN}$-1.0 | - | V |
| **VMONI output On-resistance** | $R_{VMONI}$ | | - | 1.7 | - | kΩ |
| **Current limit threshold accuracy** | $V_{CLACC}$ | AC mode, $V_{CL}$ = 4.5V | -4 | - | +4 | % |
| **Battery OVLO voltage** | $V_{BOV}$ | Δ =150mV or 200mV | - | $V_{FLT}$+Δ | - | V |
| **Automatic shutdown threshold** | $V_{ASHDN}$ | $V_{DCIN}$ - $V_{BATT}$, $V_{DCIN}$ rising | 60 | 130 | 200 | mV |
| | | $V_{DCIN}$ - $V_{BATT}$, $V_{DCIN}$ falling | 0 | 60 | 130 | mV |
| **DCIN current (Active)** | $I_{DCIN-ACTIVE}$ | Charging, not including ICHG, Linear | - | 1.6 | - | mA |
| | | Charging, not including ICHG, PWM | - | 14 | - | mA |
| **Shutdown current** | $I_{SHDN}$ | Charge invalid, $V_{DCIN}$ = 5V, $V_{BATT}$ = 3.7V, no load, DCIN ≥ UVLO, standby mode | - | 1.3 | 2.5 | mA |
| **Battery shutdown current** | $I_{AUXSHDN}$ | Current from battery DCIN = OPEN, VBATT = 3.7V | - | 38 | 67 | μA |
| **Leakage current** | $I_{DCINLK}$ | DCIN current when charge is invalid, $V_{DCIN}$ = 1V, $V_{BATT}$ = 4.2V | - | - | 2 | μA |
| **OTG current** | $I_{DDMOTG}$ | OTG valid, $V_{BATT}$ = 3.7V, no load | - | 4 | - | mA |
| **Over temperature threshold, charge mode** | $T_{LIMITCHG}$ | | - | 135 | - | °C |
| **Over temperature threshold hysteresis, charge mode** | $T_{HYSTCHG}$ | | - | 20 | - | °C |
| **Over temperature threshold, OTG mode** | $T_{LIMITOTG}$ | | - | 135 | - | °C |
| **Over temperature threshold hysteresis, OTG mode** | $T_{HYSTOTG}$ | | - | 20 | - | °C |

### DC characteristics (2) SW mode controller

**Table 13-2 DC characteristic (continued)**

(Unless otherwise specified, $V_{DCIN}$ = 5.0V, $V_{FLT}$ = 4.2V, $V_{BATT}$ = 3.7V, Ta = -30 to 85°C, all voltages are relative to GND.)

| Characteristics | Symbol | Test condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| **FET on-resistance** | $R_{RDSON}$ | High-side (DCIN to SW), Note 3 | - | 233 | 367 | mΩ |
| | | Low-side (SW to GND), Note 3 | - | 125 | 200 | mΩ |
| **Current limit** | $I_{LIMIT}$ | $V_{BATT}$ = 3.0V | - | 3 | - | A |
| **Duty cycle** | D.C. | Maximum | - | 100 | - | % |
| | | Minimum | - | 0 | - | % |

### DC characteristics (3) Battery charger

**Table 13-3 DC characteristics (continued)**

(Unless otherwise specified, $V_{DCIN}$ = 5.0V, $V_{FLT}$ = 4.2V, $V_{BATT}$ = 3.7V, Ta = -30 to 85°C, all voltages are relative to GND.)

| Characteristics | Symbol | Test condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| **Trickle charge to Pre-charge voltage threshold** | $V_{TRICKLECHG}$ | | 1.9 | 2.05 | 2.2 | V |
| **Unconnected battery voltage threshold** | $V_{BATMIS}$ | | 3.15 | 3.3 | 3.45 | V |
| **Trickle charge current** | $I_{TRICKLECHG}$ | $V_{BATT}$ = 1.7V | 30 | 50 | 80 | mA |
| **Dead battery voltage threshold accuracy** | $V_{BATDEAD}$ | Programmable (2 settings): 3.47V, 3.54V | -4 | - | 4 | % |
| **Pre-charge to Fast charge voltage threshold accuracy** | $V_{PRECHG}$ | Programmable $V_{PRECHG}$ = 2.6 to 3.3 V (8steps) | -3.5 | - | 3.5 | % |
| **USB1 input current limit** | $I_{USB1LMT}$ | Ta = 0 to 70°C, $I_{USB1LMT}$ = 90mA, Note 2, VMONI off | 60 | 80 | 100 | mA |
| **USB5 input current limit** | $I_{USB5LMT}$ | Ta = 0 to 70°C, $I_{USB5LMT}$ = 475mA, | 400 | 460 | 500 | mA |
| **AC input current limit (programmable 300mA to 2000mA, 18steps)** | $I_{ACLMT}$ | Ta = 0 to 70°C, $I_{ACLMT}$ = 500mA | -100 | - | 55 | mA |
| **Constant current sense voltage** | $V_{SENSE}$ | $I_{FCHG}$ = 1000mA | | 68 | | mV |
| **Pre-charge current (programmable 50mA to 200mA, 50mA/step)** | $I_{PRECHG}$ | Ta = 0 to 70°C, $I_{PRECHG}$ = 100mA, Note 1 | -30 | - | 30 | mA |
| **Fast charge current (programmable 300mA to 2000mA, 18steps)** | $I_{FCHG}$ | Ta = 0 to 70°C, $R_{SENSE}$ = 68mΩ, $I_{FCHG}$ = 500mA, Note 1 | -50 | - | 50 | mA |
| **Charge termination current (Programmable 100mA to 200mA, 50mA/step)** | $I_{TERM}$ | Ta = 0 to 70°C, $R_{SENSE}$ = 68mΩ, $I_{TERM}$ = 100mA | -30 | - | 30 | mA |
| **Charge termination current accuracy (Programmable 100mA to 200mA, 50mA/step)** | $I_{TERM}$ | Ta = 0 to 70°C, $R_{SENSE}$ = 68mΩ, $I_{TERM}$ = 150mA, 200mA | -30 | - | 30 | % |
| **Float voltage accuracy (Programmable 3.46V to 4.73V, 10mV/step)** | $V_{FLT}$ | Ta = 0 to 70°C, $V_{FLT}$ = 4.0V to 4.42V | -1 | - | 1 | % |
| **Automatic re-charge threshold voltage** | $V_{RECH}$ | | 70 | 140 | 190 | mV |

### DC characteristics (4) Thermal monitor (Factory programmable option)

**Table 13-4 DC characteristics (continued)**

(Unless otherwise specified, $V_{DCIN}$ = 5.0V, $V_{FLT}$ = 4.2V, $V_{BATT}$ = 3.7V, Ta = -30 to 85°C, all voltages are relative to GND.)

| Characteristics | Symbol | Test condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| **High temperature trip point (Programmable 509mV to 726mV, 4steps)** | $V_{HOT}$ | $V_{THERM}$ falling, $V_{HOT}$ = 0.726V, Ta = 0 to 70°C | 675 | 726 | 776 | mV |
| **Low temperature trip point (Programmable 1.399V to 1.654V, 4steps)** | $V_{COLD}$ | $V_{THERM}$ rising, $V_{COLD}$ = 1.491V, Ta = 0 to 70°C | 1.437 | 1.491 | 1.543 | V |
| **Current source for NTC thermistor** | $I_{NTC}$ | 10kΩ NTC, Ta = 0 to 70°C | 180 | 200 | 220 | μA |
| | | 25kΩ NTC | 72 | 80 | 88 | μA |
| | | 50kΩ NTC | 36 | 40 | 44 | μA |
| | | 100kΩ NTC | 18 | 20 | 22 | μA |
| **Current source hysteresis for NTC thermistor** | $I_{NTCHYS}$ | High temperature hysteresis, $I_{NTC}$ = 200μA | 160 | 180 | 198 | μA |
| | | Low temperature hysteresis, $I_{NTC}$ = 200μA | 198 | 220 | 242 | μA |

### DC characteristics (5) Logic inputs / outputs

**Table 13-5 DC characteristics (continued)**

(Unless otherwise specified, $V_{DCIN}$ = 5.0V, $V_{FLT}$ = 4.2V, $V_{BATT}$ = 3.7V, Ta = -30 to 85°C, all voltages are relative to GND.)

| Characteristics | Symbol | Test condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| **Input "L" level** | $V_{IL}$ | | - | - | 600 | mV |
| **Input "H" level** | $V_{IH}$ | | 1.4 | - | - | V |
| **SDA / STAT output "L" level** | $V_{OL}$ | $I_{SINK}$ = 3mA | - | - | 300 | mV |
| **STAT leakage current** | $I_{STATLK}$ | | - | - | 1 | μA |
| **EN input bias current** | $I_{ENBIAS}$ | | - | - | 1 | μA |
| **ILIM_OTG logic level voltage threshold** | $V_{ILIMOTG}$ | Input logic low-to-high state | - | 0.9 | - | V |
| **ILIM_OTG input bias current** | $I_{ILIMOTGBS}$ | Input logic low | - | 10 | - | nA |
| | | Input logic high, pull-up voltage 3.3V | - | +5.5 | +8 | μA |

### DC characteristics (6) USB OTG power

**Table 13-6 DC characteristics (continued)**

(Unless otherwise specified, $V_{DCIN}$ = 5.0V, $V_{FLT}$ = 4.2V, $V_{BATT}$ = 3.7V, Ta = -30 to 85°C, all voltages are relative to GND.)

| Characteristics | Symbol | Test condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| **Output voltage (DCIN pin)** | VOTG | VBATT = 3.6V,programmable 4steps, 5.0V output setting | 4.75 | 5.0 | 5.25 | V |
| **UVLO battery voltage** | VBATUVLO | OTG operation (refer to register 04H), 2.75Vsetting | 2.63 | 2.75 | 2.87 | V |
| **UVLO hysteresis** | VBATUVLOHY | OTG operation | 110 | 170 | 230 | mV |
| **OTG battery current range** | IOTG | VBATT = 3.6V, current from battery, programmable 4steps, CCI4-0=500mA, Note 4 | 400 | 500 | 600 | mA |
| | | CCI4-0=1000mA | 800 | 1000 | 1200 | |
| | | CCI4-0=1500mA, Ta = -20 to 85°C | 1200 | 1500 | 1800 | |
| | | CCI4-0=1800mA, Ta = -20 to 85°C | 1440 | 1800 | 2160 | |

### DC characteristics (7) Automatic power source detection (DP / DM) Note 5

**Table 13-7 DC characteristics (continued)**

(Unless otherwise specified, $V_{DCIN}$ = 5.0V, $V_{FLT}$ = 4.2V, $V_{BATT}$ = 3.7V, Ta = -30 to 85°C, all voltages are relative to GND.)

| Characteristics | Symbol | Test condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| **Data line leakage voltage** | VDAT_LKG | | 0 | | 3.6 | V |
| **Data detection voltage** | VDAT_REF | | 0.25 | 0.33 | 0.40 | V |
| **D+ source voltage** | VDP_SRC | | 0.50 | 0.60 | 0.70 | V |
| **D- source voltage** | VDM_SRC | | 0.50 | 0.60 | 0.70 | V |
| **D+ pull-up voltage** | VDP_UP | | 3.0 | 3.3 | 3.6 | V |
| **Logic threshold** | VLGC | | 0.8 | 1.2 | 2.0 | V |
| **D+ sink current** | IDP_SINK | | 25 | 100 | 175 | μA |
| **D- sink current** | IDM_SINK | | 25 | 100 | 175 | μA |
| **Current source for data connected detection** | IDP_SRC | | 7 | 10 | 13 | μA |
| **Data line leakage resistance** | RDAT_LKG | | 300 | - | - | kΩ |
| **D- pull-down resistance** | RDM_DOWN | | 14.25 | 20.0 | 24.80 | kΩ |
| **D+ pull-up resistance** | RDP_UP | | 900 | 1200 | 1575 | Ω |

### AC characteristics (1) Oscillator

**Table 13-8 AC characteristics**

(Unless otherwise specified, $V_{DCIN}$ = 5.0V, $V_{FLT}$ = 4.2V, $V_{BATT}$ = 3.7V, Ta = -30 to 85°C, all voltages are relative to GND.)

| Characteristics | Symbol | Test condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| **Oscillator frequency 1, Timer frequency** | fOSC | Ta = 0 to 70°C | 2.40 | 3.0 | 3.60 | MHz |
| **Start-up time** | tSTART | | - | - | 20 | ms |
| **Oscillator frequency 2, Start-up timer frequency** | fTM | Ta = 0 to 70°C | - | 85 | - | kHz |
| **Pre-charge time out** | tPCTOFC | Safety timer | 29 | 36 | 43 | min |
| **Charge completion time out** | tCTOFC | Safety timer | 204 | 240 | 276 | min |
| **Charge watchdog timer** | tCWD | | 33.6 | 42 | 50.4 | sec |
| **OTG power watchdog timer** | tOTGWD | | 33.6 | 42 | 50.4 | sec |
| **Standby watchdog timer** | tSTBYWD | No charging, no OTG power | 21 | 42 | 63 | sec |
| **Unconnected battery timer** | tBATMIS | | 65 | 86 | 105 | ms |
| **Device glitch filter** | tGLITCH | Enabled | 130 | 168 | 210 | ms |

### AC characteristics (2) Power source detection

**Table 13-9 AC characteristics (continued)**

(Unless otherwise specified, $V_{DCIN}$ = 5.0V, $V_{FLT}$ = 4.2V, $V_{BATT}$ = 3.7V, Ta = -30 to 85°C, all voltages are relative to GND.)

| Characteristics | Symbol | Test condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| **Data connected detection debounce** | tDCD_DBNC | Note 3, 5 | 10 | - | - | ms |
| **Data connected detection time out** | tDCD_TIMEOUT | Note 3, 5 | 300 | - | - | ms |
| **DP source on time** | tVDPSRC_ON | Note 3, 5 | 40 | - | - | ms |
| **DM source on time** | tVDMSRC_ON | Note 3, 5 | 40 | - | - | ms |

### AC characteristics (3) I²C interface @ 400kHz

**Table 13-10 AC characteristics (continued)**

(Unless otherwise specified, $V_{DCIN}$ = 5.0V, $V_{FLT}$ = 4.2V, $V_{BATT}$ = 3.7V, Ta = -30 to 85°C, all voltages are relative to GND.)

| Characteristics | Symbol | Test condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| **SCL clock frequency** | fSCL | | 0 | - | 400 | kHz |
| **SCL clock low period** | tLOW | | 1.3 | - | - | μs |
| **SCL clock high period** | tHIGH | | 0.6 | - | - | μs |
| **Bus free time (Stop condition to Start condition)** | tBUF | Note 6 | 1.3 | - | - | μs |
| **START condition setup time** | tSU:STA | | 0.6 | - | - | μs |
| **START condition hold time** | tHD:STA | | 0.6 | - | - | μs |
| **STOP condition setup time** | tSU:STO | | 0.6 | - | - | μs |
| **SCL / SDA rising time** | tR | Note 6 | 20+0.1Cb | - | 300 | ns |
| **SCL / SDA falling time** | tF | Note 6 | 20+0.1Cb | - | 300 | ns |
| **Data in setup time** | tSU:DAT | | 100 | - | - | ns |
| **Data in hold time** | tHD:DAT | | 0 | - | 0.9 | μs |
| **Noise filter** | TI | Noise suppression | - | 80 | - | ns |

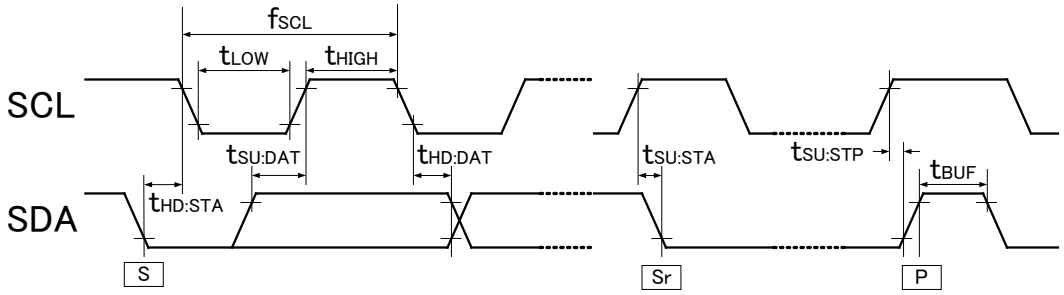



**Figure 13-1 I²C interface**

Note 1 : Input current limit $I_{LIM}$ is prior to $I_{PRECHG}$ ,$I_{FCHG}$.

Note 2 : IC is not used as a battery protection.

Note 3 : Design and characteristics are guaranteed. Not 100% test.

Note 4 : OTG power path is shut off after 168ms (glitch filter period) since the selected OTG current limit is reached.
To re-start OTG power path, set OTG mode invalid, and then set it valid.

Note 5 : Refer to Battery Charging Specification Rev1.2.

Note 6 : Guaranteed by design.

## 14. Application Circuit

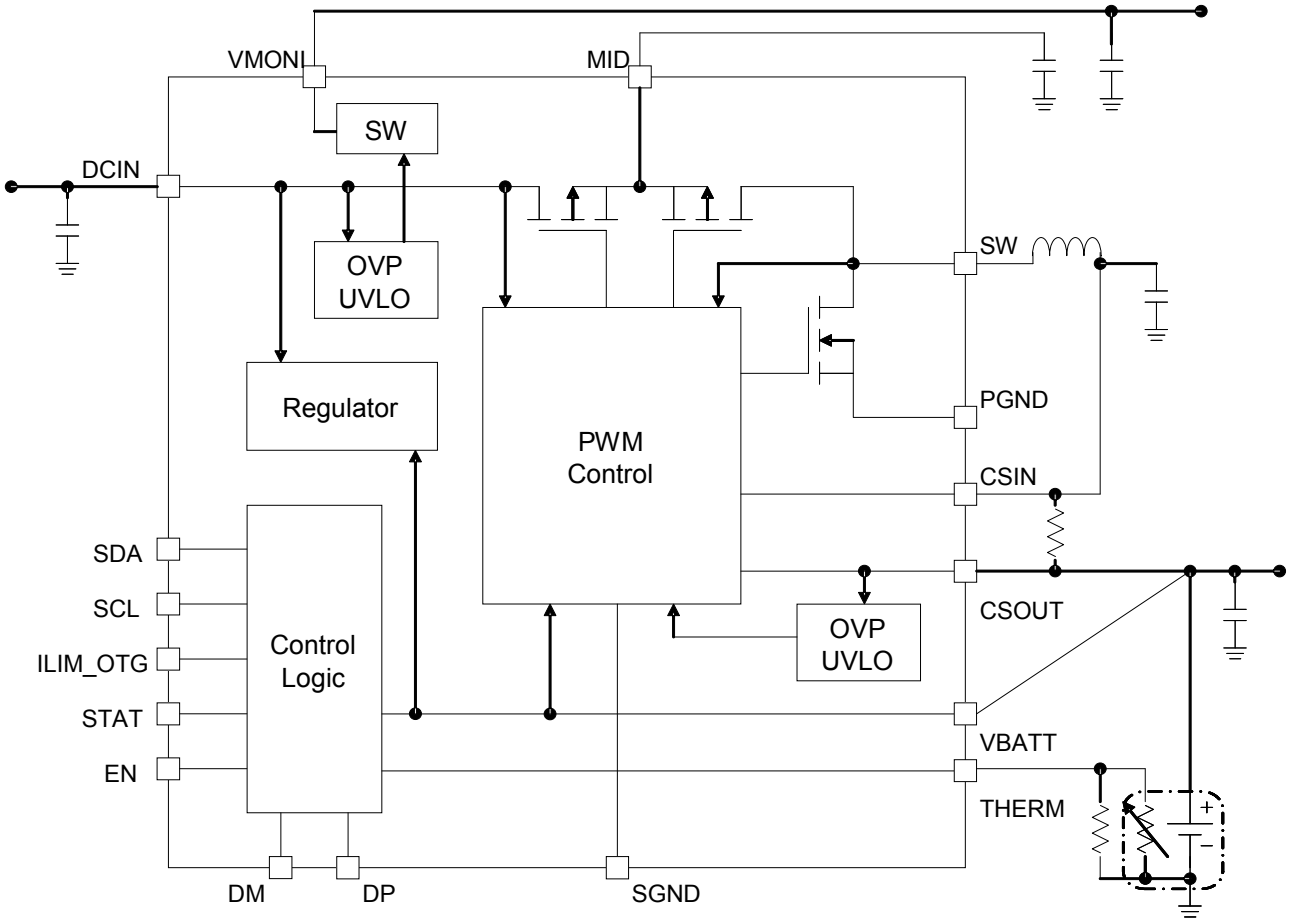
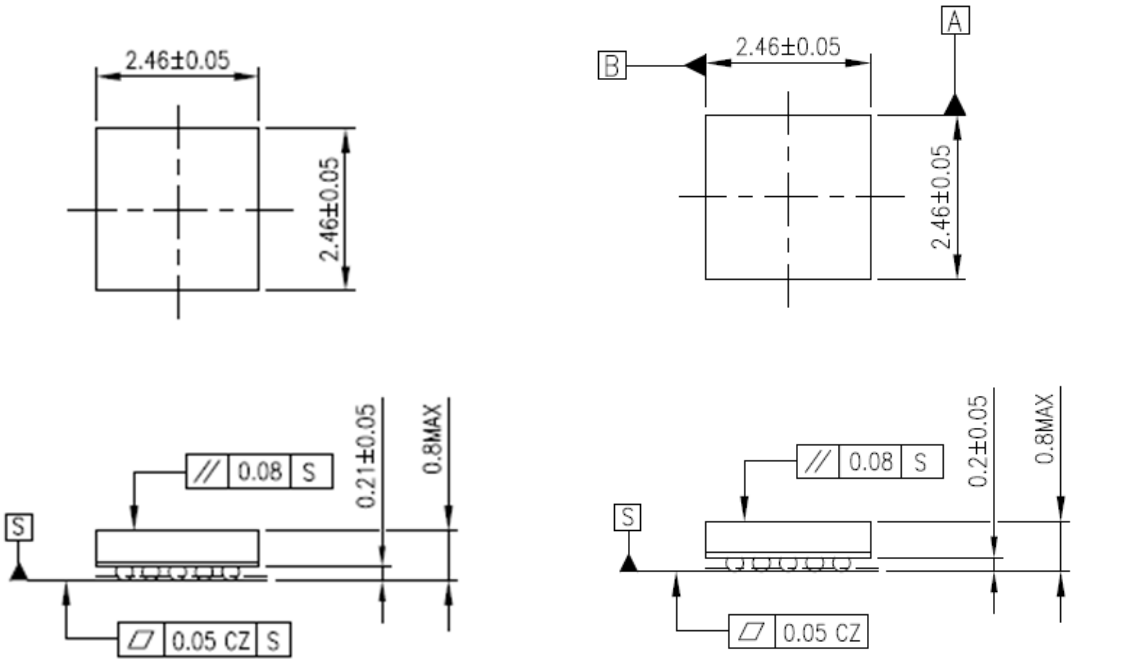


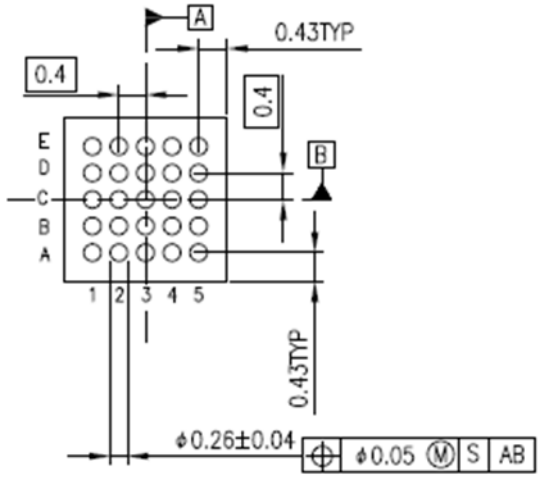

**Figure 14-1 Application circuit**

## 15. Outline drawing

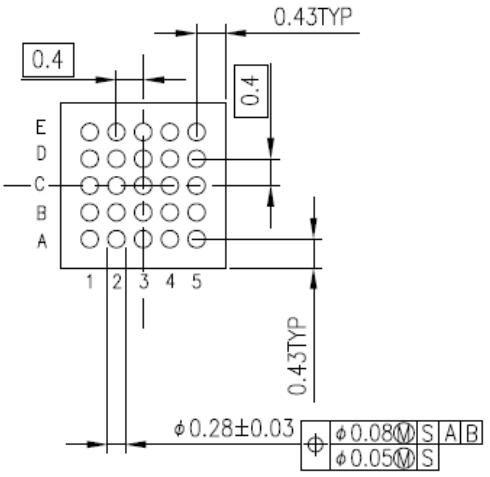
### 15.1 Package Dimensions

Unit: mm




S-WFBGA25-0303-0.40-001
TC7710AWBG(O*)

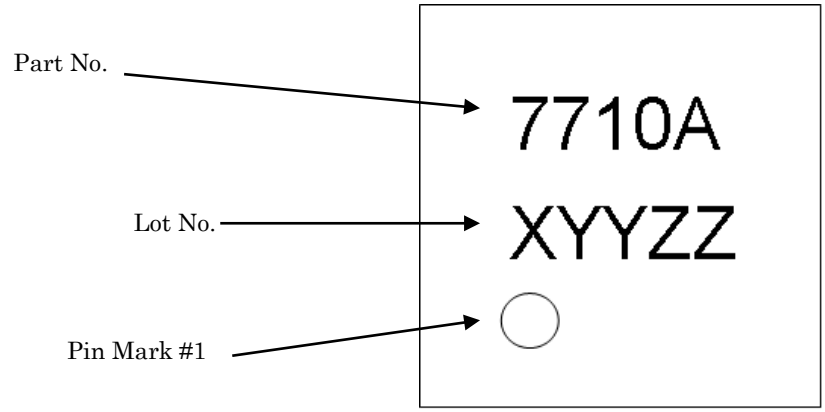



S-WFBGA25-0303-0.40-002
TC7710AWBG(Z*)

Weight: 0.009 g (Typ.)

## 15.2 Marking

TC7710AWBG(O*) Marking




TC7710AWBG(O*) Lot No.:

| X | YY | ZZ |
|---|---|---|
| (1) | (2) | (3) |

(1) Manufactured year code Annual code expressed as the last digit of year

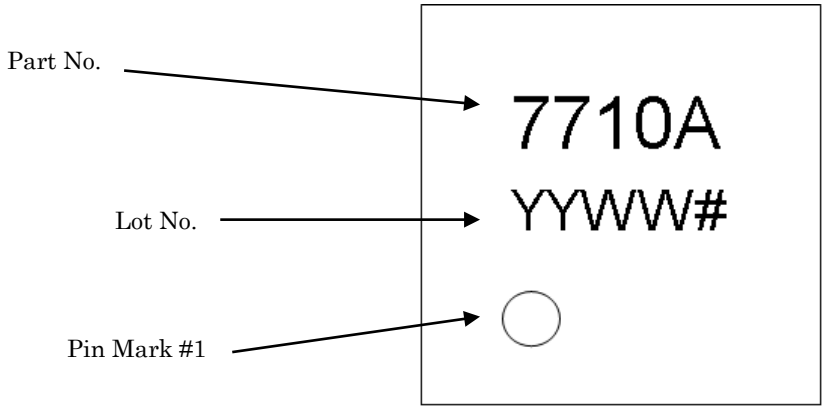
Example

| Year | 2009 | 2010 | 2011 | 2012 | 2013 |
|---|---|---|---|---|---|
| Code | 9 | 0 | 1 | 2 | 3 |

(2) Manufactured week code Weekly code as the first Thursday of January being determined the first week and accordingly reaches 52nd or 53th week in a year.

(3) Our control number

TC7710AWBG(Z*) Marking




TC7710AWBG(Z*) Lot No.:

| YY | WW | # |
|---|---|---|
| (1) | (2) | (3) |

(1) Manufactured year code Annual code expressed as the last digit of year

Example

| Year | 2009 | 2010 | 2011 | 2012 | 2013 |
|---|---|---|---|---|---|
| Code | 09 | 10 | 11 | 12 | 13 |

(2) Manufactured week code Weekly code as the first week of January being determined 01 and accordingly reaches 52nd or 53th week in a year.

(3) Our control number

## RESTRICTIONS ON PRODUCT USE

- Toshiba Corporation, and its subsidiaries and affiliates (collectively "TOSHIBA"), reserve the right to make changes to the information in this document, and related hardware, software and systems (collectively "Product") without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, devices related to electric power, and equipment used in finance-related fields. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**