Surface Mount Small Signal Transistor (BJT) Precautions for use

Outline:

This document describes the maximum ratings (definition of maximum ratings, voltage ratings, current ratings, temperature ratings, and power ratings) listed in the datasheet.

Small-signal transistors (Bipolar junction transistor, BJT) mainly refer to transistors with a power dissipation (P_C) of 1W or less.

This is for reference only. Do not design the final equipment in this document.

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1. Maximum rating

1.1. Definition of maximum rating

For semiconductor devices, applied voltage, current, temperature, power dissipation, and other factors are major factors limiting the operation function.

The maximum rating is the maximum allowable value that must not be exceeded in order to operate the semiconductor element effectively and ensure sufficient reliability, and is specified as the absolute maximum rating.

The absolute maximum rating (hereinafter referred to as the maximum rating) is defined as "the limit value that must not be exceeded either instantaneously or simultaneously, and that must not be reached for any two items at the same time." Operation exceeding the maximum rating may cause breakage, damage or deterioration, and may cause explosion or burn-in hazards.

1.2. Voltage ratings

Transistors are composed of input and output circuit using any one of the emitter, base, and collector terminals as a common terminal. Therefore, the voltage rating is also specified for the collector-base voltage V_{CB}, collector-emitter voltage V_{CE}, and emitter-base voltage V_{EB}.

The voltage breakdown that determines the voltage rating is divided into transistor specific characteristics (such as $V_{(BR)CBO}$, $V_{(BR)CEO}$) and input circuit condition dependent characteristics (such as $V_{(BR)CER}$, $V_{(BR)CEX}$), which are generally related to both circuitry and transistor specific characteristics.

1.3. Current ratings

The maximum current that can flow forward in the emitter junction $I_{E\ max}$, the maximum current that can flow backwards in the collector junction $I_{C\ max}$ is available for transistors. However, in many cases, the maximum current that can flow backwards in transistors is $I_{C\ max} = I_{E\ max}$ and is determined primarily by the following considerations.

(1)The presence of a finite collector saturation voltage prevents the internal power loss from exceeding the rated value and hence the junction temperature from exceeding the rated value Current that does not exceed.

(2)Current at which DC amplification factor h_{FE} is lowerd to 1/2 to 1/3 or less of peak value.

Namely for switching purposes, $h_{FE} \cong 10$ for medium-power transistors of $h_{FE} \cong 3$ for large-power transistors.

(3)Current at which the internal lead wire are blown off.

The maximum base current $I_{B\ max}$ is generally $I_{B\ max} \cong \frac{1}{2}\ to\ \frac{1}{6} \times I_{C\ max.}$

1.4. Temperature ratings

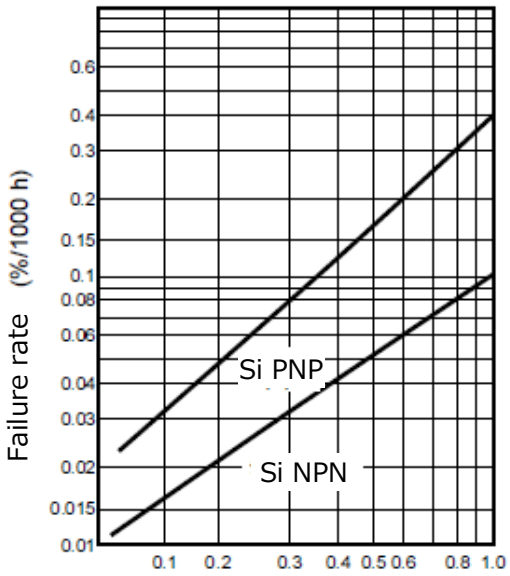
The maximum-junction-temperature T_{jmax} is defined by the material and reliability of the transistor, and operates simply. It must also be considered in terms of reliability, such as degradation and life.

Generally, the degradation of transistors is accelerated as the junction temperature increases, and the following relations are recognized between the average service life Lm(hours) and junction temperature T_j(K) with A and B as constants inherent to transistor.

$$\log \ Lm \cong A + \frac{B}{T_j}$$

Therefore, for transistors requiring long-term life assurance, the upper limit of the allowable junction temperature is determined to match the defect rate and reliability, and values of 100 to 150°C for Si transistors and 150 to 200°C for surface-stabilized Si planar transistors.

The storage temperature T_{stg} is a temperature range that can be stored without operating the transistor, which is also specified by the nature and reliability of the component material. Figure 1.1 shows an example of the relationship between transistor life and junction temperature.



Junction temperature Ta regulated
by standard temperature To

$$Ta = \frac{Tj - To}{T_{jmax} - To}$$

Figure 1.1 Relationship between failure rate and
junction temperature of transistors
(Based on MIL-HDBK-217A)

1.5. Power ratings

Power loss inside the transistor is converted to thermal energy, which increases the internal temperature.

The internal power loss of a transistor operating at an operating point is the sum of collector loss = $I_C V_{CB}$ and emitter loss = $I_E V_{BE}$, but normally the emitter junction is forward biased and is VCB>VBE and IC ≃ IE and therefore determined by the collector loss $P_C = I_C V_{CB} \simeq I_C V_{CE}$.

It is well known that the parameters limiting the maximum allowable loss P_{Cmax} of the transistors are the maximum junction temperature T_{jmax} and the reference temperature T_o (ambient temperature T_a or case temperature T_c) described above, which are related by the thermal resistance θ (or R_{th}) as follows.

$$P_{Cmax} = \frac{(\mathrm{Tjmax} - \mathrm{To})}{\theta} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (1)$$

Thermal resistance is a physical quantity that indicates the rate at which the junction temperature rises relative to the unit power loss, i.e. the difficulty of heat dissipation. Therefore, a transistor with a large P_{Cmax} must be selected to achieve a large power loss. In particular, heat dissipation designs are crucial for power transistors.

Normally, the rated value of P_{Cmax} is Ta=25°C, and when the use of a radiator is expected, the value is indicated when T_c=25°C. Therefore, the thermal resistance between the junction and outside air of the transistor or the thermal resistance between the junction and case can be known using Equation (1) respectively.

The power dissipation should be derated according to the temperature. Figure 1.2 shows the power dissipation for each temperature package.

Power dissipation varies greatly depending on how the surface-mount component is mounted. The following table shows examples of power dissipation changes for each package.

(1) Super mini (S-Mini) type

The super mini-type has a smaller $P_{C(max)}$ of = 150 mW for the device itself because of the smaller packages. However, when mounted on a board, the heat dissipation from the lead to the board increases, and the power dissipation in the mounted state becomes considerably large. Figures 1.2 to 1.4 show the power dissipation when mounted on a board. Note that the power dissipation at the time of board mounting is slightly different depending on the product type, and the larger the pellet, the greater the power dissipation in the mounted state tends to be.

●Substrate material and multiple mounting

The relation between $P_{C(max)}$-T_a characteristic and the board size and $P_{C\ (max)}$ when mounting the board in Figures 1.2 to 1.4 is the value when one transistor is mounted, but in actual cases, multiple transistors will be installed.

In this case, heat is generated from the individual transistors and the heat dissipation to the board interferes with each other. Therefore, the power dissipation is smaller than that of a single transistor.

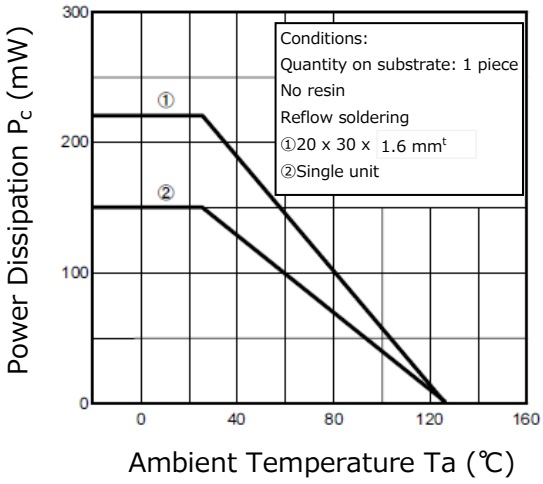


Figure 1.2 P_C–T_a Properties for Epoxy Glass Board Installation

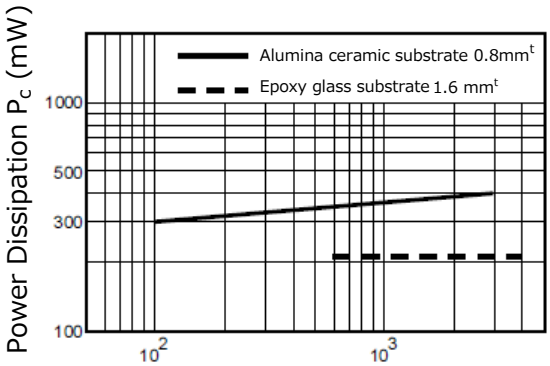


Figure 1.3 Power Dissipation P_C – Substrate Area S

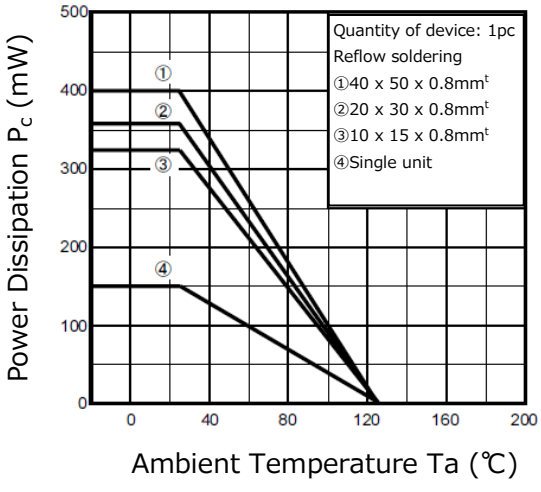


Figure 1.4 P_C–T_a Properties for Mounting Alumina-Ceramic Board

(2) Small Super Mini (SSM) Type, Ultra Super Mini (USM) Type

The power dissipation $P_{C\ (max)}$ of the SSM type and USM type are reduced to 100 mW because the package is even smaller than the super mini type package. However, when mounted on a board, the power dissipation will be increased in the same way as the super mini type described above due to heat dissipation from leads, etc.

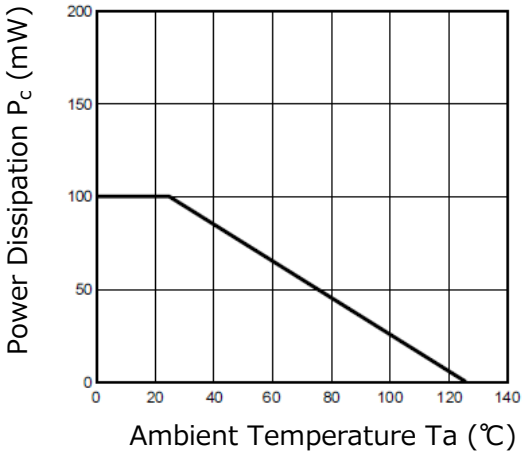
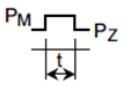
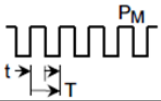


Figure 1.5 SSM, USM package Power Loss P_C-Ambient Temperature Ta

The power dissipation when pulsed rather than continuous power is applied to the transistor is determined by the transient thermal resistivity r_{th} and the following tables. Fig. 1.6 shows the transient thermal resistance r_{th}-t of the enclosures.

Table 1.1 Formula for calculating allowable power when pulsed power is applied

Load type	Power waveform	Permissible power (peak value)
Single pulse load		$P_M = \frac{T_j - Ta}{r_{th}}$
A load in which a single pulse load is superimposed on a continuous DC load		$P_M = \frac{T_j - Ta - P_Z \cdot R_{th}}{r_{th}} + P_Z$
Continuously repeated pulse load		$P_M = \frac{T_j - Ta}{\frac{t}{T} R_{th} + (1 - \frac{t}{T}) r_{(t+T)h} - r_{Th} + r_{th}}$

However, (R_{Th}: Constant thermal resistance, r_{th}: Transient thermal resistance at time t

r_{Th}: Transient thermal resistance at time T, $r_{(t+T)h}$: Transient thermal resistance at time t + T)

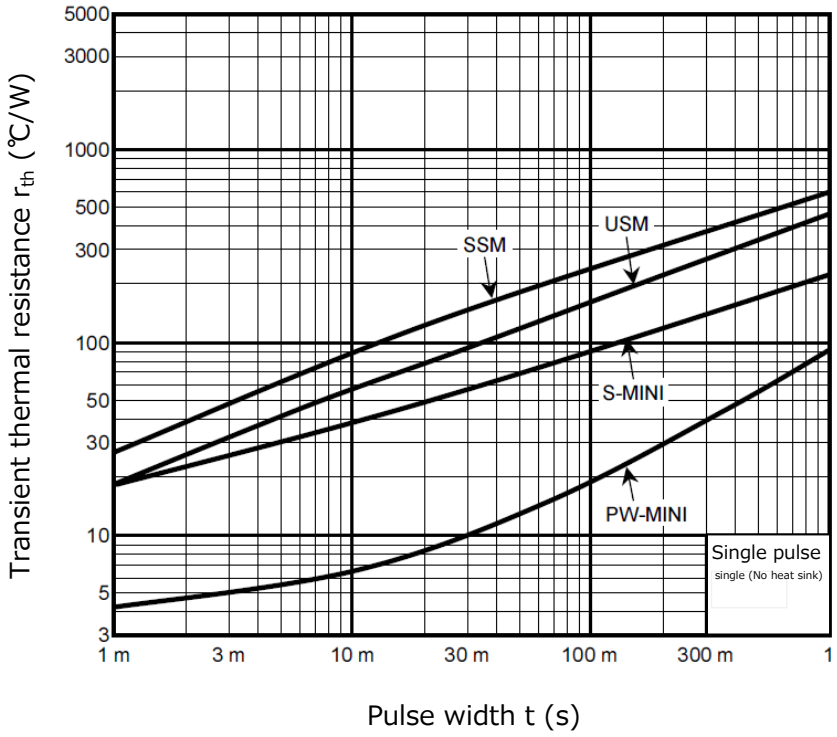


Figure 1.6 r_{th} by Package-Pulse width

2. Related Links

- ■ Bipolar Transistors Lineup — Click
- ■ Bipolar Transistors (Parametric Search) — Click
- ■ Bias Resistor Built-in Transistors (Digital Transistors) (Parametric Search) — Click
- ■ RF Bipolar Transistors （Parametric Search) — Click
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