

TLP5705H

1. Applications

- Photovoltaic (PV) Power Conditioning Systems
- Industrial Inverters
- Induction Cooktop and Home Appliances
- Air Conditioner Inverters
- MOSFET Gate Drivers
- IGBT Gate Drivers

2. General

The TLP5705H is a photocoupler in a 6-pin SO6L package that consists of an infrared LED optically coupled to an integrated high-gain, high-speed photodetector IC chip. It provides guaranteed performance and specifications at temperature up to 125 °C.

The TLP5705H is physically smaller / thinner than the one in an 8-pin DIP package and compliant with international safety standards for reinforced insulation. It thus provides a smaller footprint solution for applications that require safety standard certification. An internal noise shield provides a guaranteed common-mode transient immunity of ± 50 kV/ μ s.

The TLP5705H is ideal for small to medium class IGBT and power MOSFET gate drive.

3. Features

- (1) Buffer logic type (totem pole output)
- (2) Output peak current: ± 5.0 A (max)
- (3) Operating temperature: -40 to 125 °C
- (4) Supply current: 3.0 mA (max)
- (5) Supply voltage: 15 to 30 V
- (6) Threshold input current: 5 mA (max)
- (7) Propagation delay time: $t_{pHL}/t_{pLH} = 200$ ns (max)
- (8) Common-mode transient immunity: ± 50 kV/ μ s (min)
- (9) Isolation voltage: 5000 Vrms (min)
- (10) Safety standards

UL-recognized: UL 1577, File No.E67349

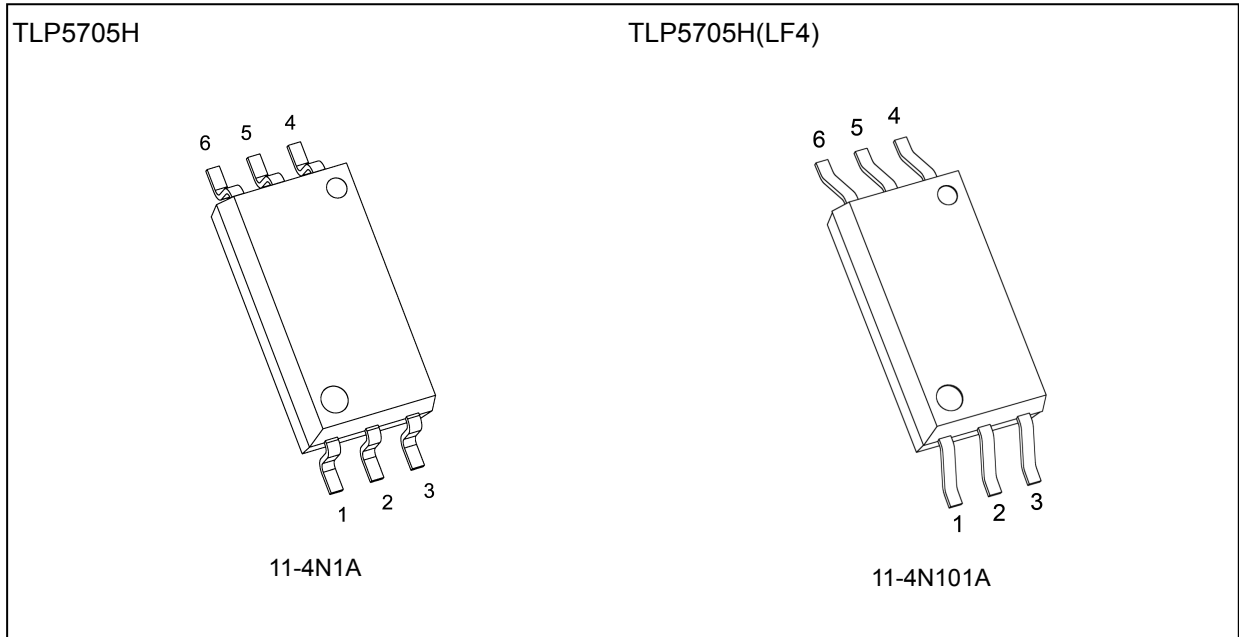
cUL-recognized: CSA Component Acceptance Service No.5A File No.E67349

VDE-approved: EN 60747-5-5, EN 62368-1 (**Note 1**)

CQC-approved: GB4943.1, GB8898 Japan Factory

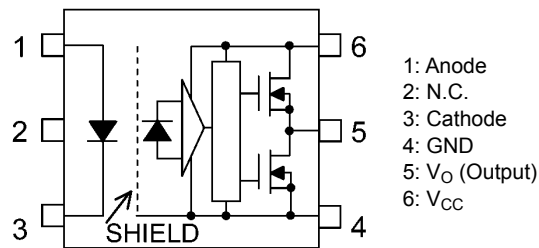
Note 1: When a VDE approved type is needed, please designate the **Option (D4)**.

4. Packaging (Note)

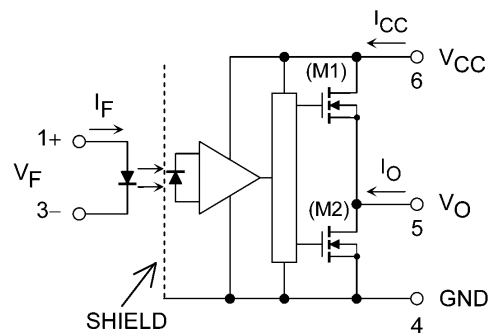


Note: Lead-formed product: (LF4)

5. Pin Assignment



6. Internal Circuit (Note)



Note: A 1.0- μ F bypass capacitor must be connected between pin 6 and pin 4.

7. Principle of Operation

7.1. Truth Table

| Input | LED | M1 | M2 | Output |
|-------|-----|-----|-----|--------|
| H | ON | ON | OFF | H |
| L | OFF | OFF | ON | L |

7.2. Mechanical Parameters

| Characteristics | Size | Unit |
|------------------------------|-----------|------|
| Height | 2.3 (max) | mm |
| Creepage distances | 8.0 (min) | |
| Clearance distances | 8.0 (min) | |
| Internal isolation thickness | 0.4 (min) | |

8. Absolute Maximum Ratings (Note) (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$)

| | Characteristics | Symbol | Note | Rating | Unit |
|----------|--|-----------------------------|----------|------------|----------------------|
| LED | Input forward current | I_F | | 20 | mA |
| | Input forward current derating ($T_a \geq 100\text{ }^\circ\text{C}$) | $\Delta I_F/\Delta T_a$ | | -0.4 | mA/ $^\circ\text{C}$ |
| | Peak transient input forward current | I_{FPT} | (Note 1) | 1 | A |
| | Peak transient input forward current derating ($T_a \geq 100\text{ }^\circ\text{C}$) | $\Delta I_{FPT}/\Delta T_a$ | | -20 | mA/ $^\circ\text{C}$ |
| | Input reverse voltage | V_R | | 5 | V |
| | Input power dissipation | P_D | | 40 | mW |
| | Input power dissipation derating ($T_a \geq 100\text{ }^\circ\text{C}$) | $\Delta P_D/\Delta T_a$ | | -0.8 | mW/ $^\circ\text{C}$ |
| | Junction temperature | T_j | | 150 | $^\circ\text{C}$ |
| Detector | Peak low-level output current ($T_a = -40\text{ to }125\text{ }^\circ\text{C}$) | I_{OPL} | (Note 2) | +5.0 | A |
| | Peak high-level output current ($T_a = -40\text{ to }125\text{ }^\circ\text{C}$) | I_{OPH} | | -5.0 | |
| | Output voltage | V_O | | 35 | V |
| | Supply voltage | V_{CC} | | 35 | |
| | Output power dissipation | P_O | | 500 | mW |
| | Output power dissipation derating ($T_a \geq 100\text{ }^\circ\text{C}$) | $\Delta P_O/\Delta T_a$ | | -10 | mW/ $^\circ\text{C}$ |
| | Junction temperature | T_j | | 150 | $^\circ\text{C}$ |
| Common | Operating temperature | T_{opr} | | -40 to 125 | |
| | Storage temperature | T_{stg} | | -55 to 150 | |
| | Lead soldering temperature (10 s) | T_{sol} | (Note 3) | 260 | |
| | Isolation voltage AC, 60 s, R.H. $\leq 60\%$ | BV_S | (Note 4) | 5000 | Vrms |

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Pulse width (PW) $\leq 1\text{ }\mu\text{s}$, 300 pps

Note 2: Exponential waveform. Pulse width $\leq 130\text{ ns}$, $f \leq 10\text{ kHz}$, JEDEC compliant board (JESD51-7)

Note 3: $\geq 2\text{ mm}$ below seating plane.

Note 4: This device is considered as a two-terminal device: Pins 1, 2 and 3 are shorted together, and pins 4, 5 and 6 are shorted together.

9. Recommended Operating Conditions (Note)

| Characteristics | Symbol | Note | Min | Typ. | Max | Unit |
|--------------------------------|--------------|----------|-----|------|------|------|
| Input on-state current | $I_{F(ON)}$ | (Note 1) | 6.5 | — | 10 | mA |
| Input off-state voltage | $V_{F(OFF)}$ | | 0 | — | 0.8 | V |
| Supply voltage | V_{CC} | (Note 2) | 15 | — | 30 | |
| Peak high-level output current | I_{OPH} | (Note 2) | — | — | -5.0 | A |
| Peak low-level output current | I_{OPL} | (Note 2) | — | — | +5.0 | |
| Operating frequency | f | (Note 3) | — | — | 50 | kHz |

Note: The recommended operating conditions are given as a design guide necessary to obtain the intended performance of the device. Each parameter is an independent value. When creating a system design using this device, the electrical characteristics specified in this datasheet should also be considered.

Note: A ceramic capacitor (1.0 μ F) should be connected between pin 6 (V_{CC}) and pin 4 (GND) to stabilize the operation of a high-gain linear amplifier. Otherwise, this photocoupler may not switch properly. The bypass capacitor should be placed within 1 cm of each pin.

Note 1: The rise and fall times of the input on-current should be less than 0.5 μ s.

Note 2: Denotes the operating range, not the recommended operating condition.

Note 3: Exponential waveform. $I_{OPH} \geq -3.0$ A (≤ 60 ns), $I_{OPL} \leq 3.0$ A (≤ 60 ns), $V_{CC} = 30$ V, $T_a = 125$ °C, JEDEC compliant board (JESD51-7)

10. Electrical Characteristics (Note) (Unless otherwise specified, $T_a = -40$ to 125 °C)

| Characteristics | Symbol | Note | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|---|---------------------------|----------|--------------|--|------|-------|-------|---------|
| Input forward voltage | V_F | | — | $I_F = 10$ mA, $T_a = 25$ °C | 1.45 | 1.55 | 1.70 | V |
| Input forward voltage temperature coefficient | $\Delta V_F / \Delta T_a$ | | — | $I_F = 10$ mA | — | -2.0 | — | mV/°C |
| Input reverse current | I_R | | — | $V_R = 5$ V, $T_a = 25$ °C | — | — | 10 | μ A |
| Input capacitance | C_t | | — | $V = 0$ V, $f = 1$ MHz, $T_a = 25$ °C | — | 60 | — | pF |
| Peak high-level output current | I_{OPH} | (Note 1) | Fig. 13.1.1 | $I_F = 5$ mA, $V_{CC} = 15$ V, $V_{6-5} = -3.5$ V | — | -2.0 | -1.0 | A |
| | | | | $I_F = 5$ mA, $V_{CC} = 15$ V, $V_{6-5} = -7$ V | — | — | -2.0 | |
| Peak low-level output current | I_{OPL} | (Note 1) | Fig. 13.1.2 | $I_F = 0$ mA, $V_{CC} = 15$ V, $V_{5-4} = 2.5$ V | 1.0 | 2.9 | — | |
| | | | | $I_F = 0$ mA, $V_{CC} = 15$ V, $V_{5-4} = 7$ V | 2.0 | — | — | |
| Peak high-level output current (L/H) | I_{OLH} | (Note 2) | Fig. 13.1.7 | $I_F = 0 \rightarrow 10$ mA, $V_{CC} = 15$ V, $C_g = 0.18$ μ F, $C_{VDD} = 10$ μ F | — | — | -3.5 | |
| Peak low-level output current (H/L) | I_{OHL} | | | $I_F = 10 \rightarrow 0$ mA, $V_{CC} = 15$ V, $C_g = 0.18$ μ F, $C_{VDD} = 10$ μ F | 3.0 | — | — | |
| High-level output voltage | V_{OH} | | Fig. 13.1.3 | $I_F = 5$ mA, $R_L = 200$ Ω , $V_{CC1} = +15$ V, $V_{EE1} = -15$ V | 11.0 | 13.7 | — | V |
| Low-level output voltage | V_{OL} | | Fig. 13.1.4 | $V_F = 0.8$ V, $R_L = 200$ Ω , $V_{CC1} = +15$ V, $V_{EE1} = -15$ V | — | -14.9 | -12.5 | |
| High-level supply current | I_{CCH} | | Fig. 13.1.5 | $I_F = 10$ mA, $V_{CC} = 30$ V, $V_O =$ Open | — | 1.5 | 3.0 | mA |
| Low-level supply current | I_{CCL} | | Fig. 13.1.6 | $I_F = 0$ mA, $V_{CC} = 30$ V, $V_O =$ Open | — | 1.5 | 3.0 | |
| Threshold input current (L/H) | I_{FLH} | | — | $V_{CC} = 15$ V, $V_O > 1$ V | — | 1.5 | 5 | V |
| Threshold input voltage (H/L) | V_{FHL} | | — | $V_{CC} = 15$ V, $V_O < 1$ V | 0.8 | — | — | |
| Supply voltage | V_{CC} | | — | — | 15 | — | 30 | |
| UVLO threshold voltage | V_{UVLO+} | | — | $I_F = 5$ mA, $V_O > 2.5$ V | 11.0 | 12.5 | 13.5 | |
| | V_{UVLO-} | | — | $I_F = 5$ mA, $V_O < 2.5$ V | 9.5 | 11.0 | 12.0 | |
| UVLO hysteresis | $UVLO_{HYS}$ | | — | — | — | 1.5 | — | |

Note: All typical values are at $T_a = 25$ °C.

Note: This device is designed for low power consumption, making it more sensitive to ESD than its predecessors. Extra care should be taken in the design of circuitry and pc board implementation to avoid ESD problems.

Note 1: I_O application time ≤ 50 μ s; single pulse. (Nonrepeatable)

Note 2: I_O application time ≤ 10 μ s; single pulse. (Nonrepeatable)

11. Isolation Characteristics (Unless otherwise specified, $T_a = 25$ °C)

| Characteristics | Symbol | Note | Test Conditions | Min | Typ. | Max | Unit |
|-------------------------------------|--------|----------|---------------------------------|-----------|-----------|-----|----------|
| Total capacitance (input to output) | C_S | (Note 1) | $V_S = 0$ V, $f = 1$ MHz | — | 1.0 | — | pF |
| Isolation resistance | R_S | (Note 1) | $V_S = 500$ V, R.H. ≤ 60 % | 10^{12} | 10^{14} | — | Ω |
| Isolation voltage | BV_S | (Note 1) | AC, 60 s | 5000 | — | — | Vrms |

Note 1: This device is considered as a two-terminal device: Pins 1, 2 and 3 are shorted together, and pins 4, 5 and 6 are shorted together.

12. Switching Characteristics (Note) (Unless otherwise specified, $T_a = -40$ to 125 °C)

| Characteristics | Symbol | Note | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|---|-----------------------|--------------------|--------------|---|----------|-----------|-----|-------------|
| Propagation delay time (L/H) | t_{pLH} | (Note 1) | Fig. 13.1.8 | $I_F = 0 \rightarrow 5$ mA, $V_{CC} = 30$ V, $R_g = 20$ Ω , $C_g = 10$ nF | 50 | — | 200 | ns |
| Propagation delay time (H/L) | t_{pHL} | | | | 50 | — | 200 | |
| Rise time | t_r | (Note 1) | | | — | 37 | — | |
| Fall time | t_f | (Note 1) | | | — | 50 | — | |
| Pulse width distortion | $ t_{pHL} - t_{pLH} $ | (Note 1) | | | — | — | 50 | |
| Propagation delay skew (device to device) | t_{psk} | (Note 1), (Note 2) | | | -80 | — | 80 | |
| High-level common-mode transient immunity | CM_H | (Note 3) | Fig. 13.1.9 | $V_{CM} = 1000$ V_{p-p} , $I_F = 5$ mA, $V_{CC} = 30$ V, $T_a = 25$ °C, $V_{O(min)} = 26$ V | ± 50 | ± 100 | — | kV/ μ s |
| Low-level common-mode transient immunity | CM_L | (Note 4) | | | ± 50 | ± 100 | — | |

Note: All typical values are at $T_a = 25$ °C.

Note 1: Input signal ($f = 25$ kHz, duty = 50 %, $t_r = t_f = 5$ ns or less).

C_L is less than 15 pF which includes probe and stray wiring capacitance.

Note 2: The propagation delay skew, t_{psk} , is equal to the magnitude of the worst-case difference in t_{pHL} and/or t_{pLH} that will be seen between units at the same given conditions (supply voltage, input current, temperature, etc).

Note 3: CM_H is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic high state ($V_O > 26$ V).

Note 4: CM_L is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic low state ($V_O < 1$ V).

13. Test Circuits and Characteristics Curves

13.1. Test Circuits

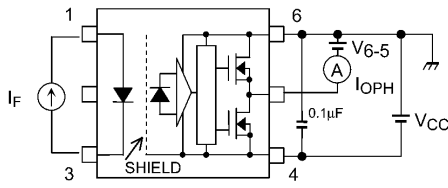


Fig. 13.1.1 I_{OPH} Test Circuit

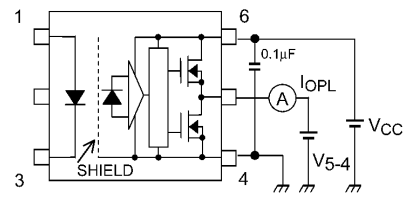


Fig. 13.1.2 I_{OPL} Test Circuit

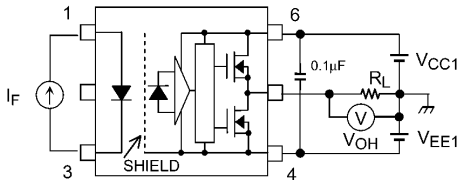


Fig. 13.1.3 V_{OH} Test Circuit

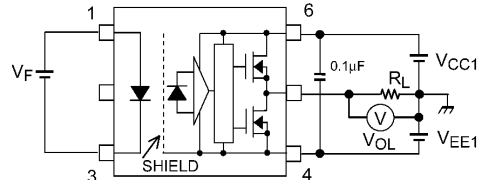


Fig. 13.1.4 V_{OL} Test Circuit

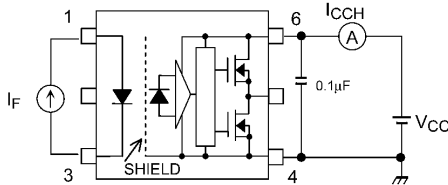


Fig. 13.1.5 I_{CCH} Test Circuit

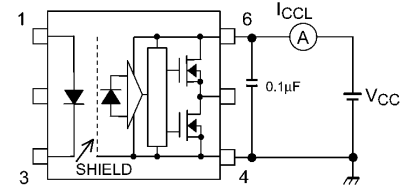


Fig. 13.1.6 I_{CCL} Test Circuit

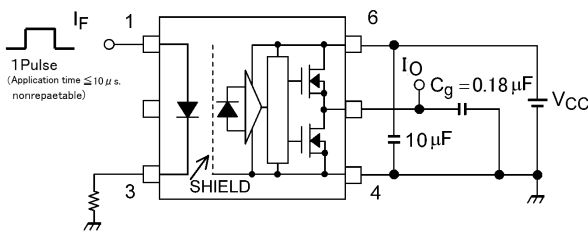
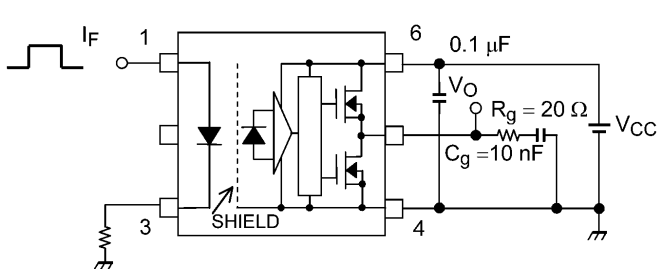


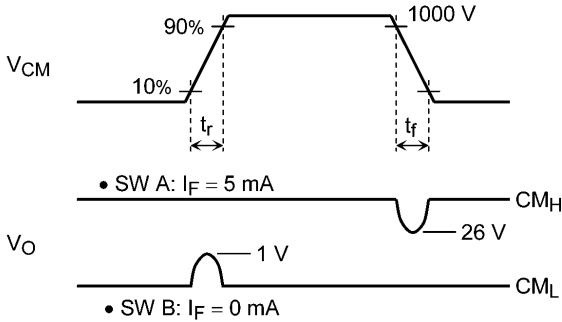
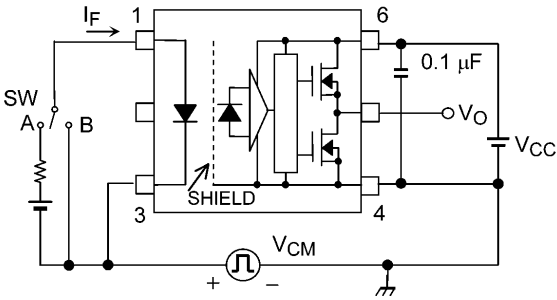
Fig. 13.1.7 I_{OLH} / I_{OHL} Test Circuit

$I_F = 5 \text{ mA (P.G.)}$
 ($f = 25 \text{ kHz, duty} = 50\%, t_r = t_f = 5 \text{ ns or less}$)



P.G.: Pulse Generator

Fig. 13.1.8 Switching Time Test Circuit and Waveform



$$CM_H = - \frac{800 \text{ V}}{t_r (\mu\text{s})} \quad CM_L = \frac{800 \text{ V}}{t_r (\mu\text{s})}$$

Fig. 13.1.9 Common-Mode Transient Immunity Test Circuit and Waveform

13.2. Characteristics Curves (Note)

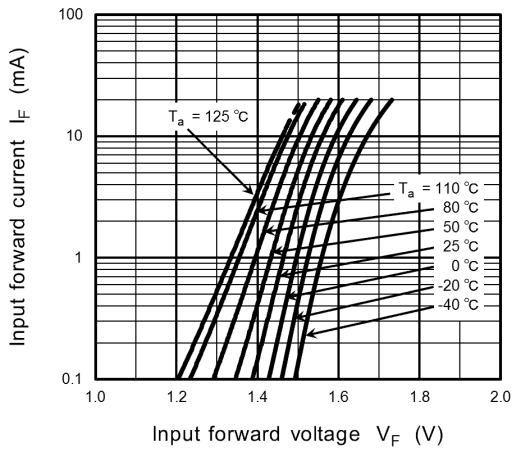


Fig. 13.2.1 $I_F - V_F$

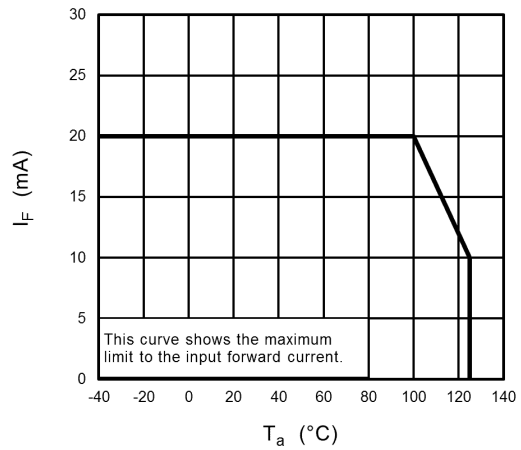


Fig. 13.2.2 $I_F - T_a$

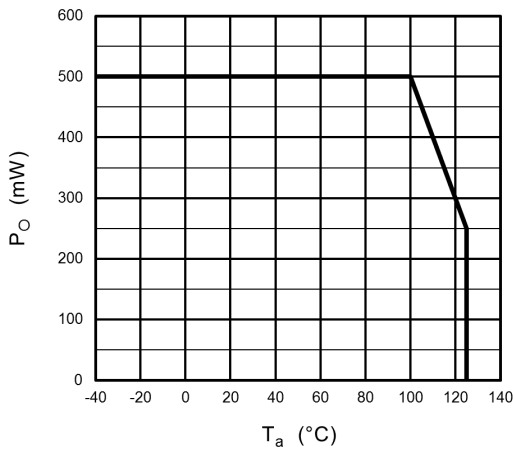


Fig. 13.2.3 $P_O - T_a$

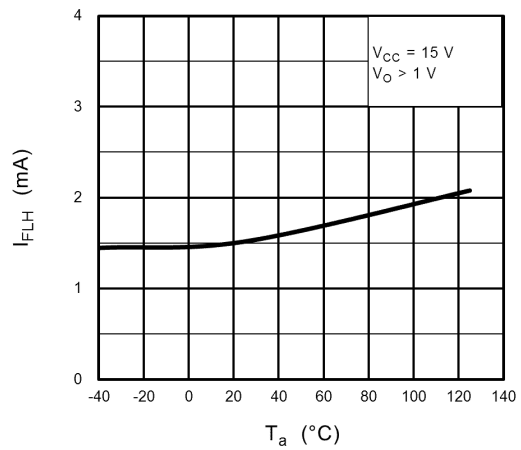


Fig. 13.2.4 $I_{FLH} - T_a$

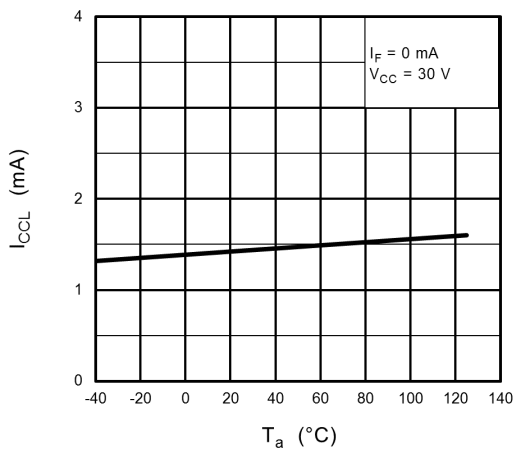


Fig. 13.2.5 $I_{CCL} - T_a$

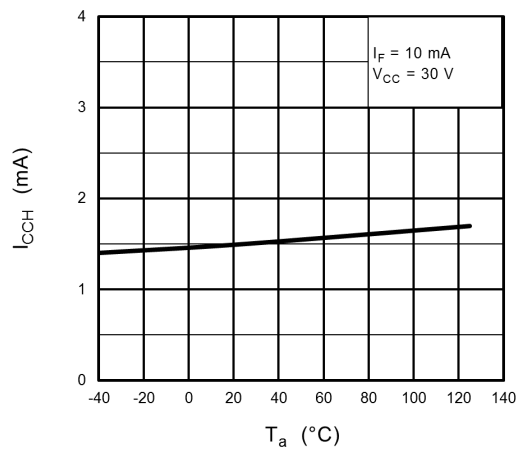


Fig. 13.2.6 $I_{CCH} - T_a$

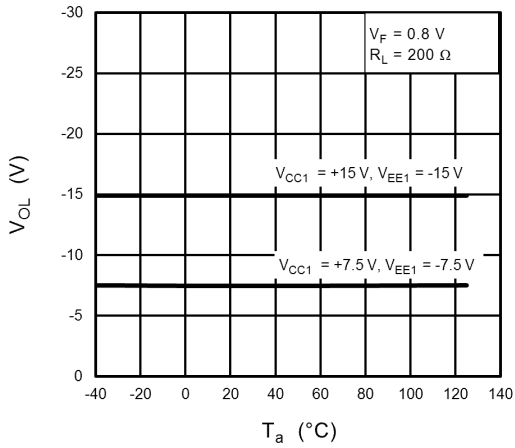


Fig. 13.2.7 $V_{OL} - T_a$

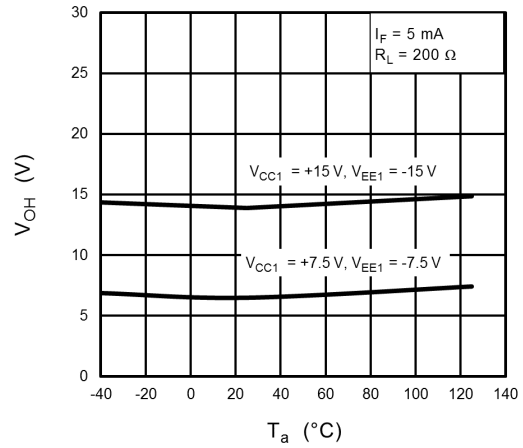


Fig. 13.2.8 $V_{OH} - T_a$

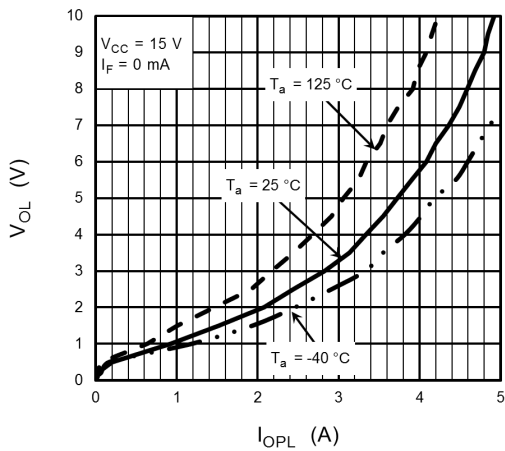


Fig. 13.2.9 $V_{OL} - I_{OPL}$

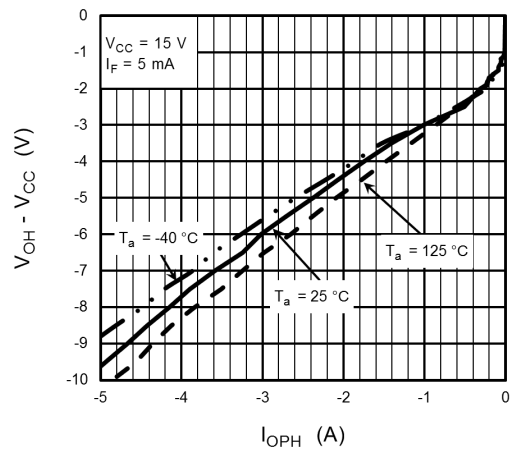


Fig. 13.2.10 $(V_{OH} - V_{CC}) - I_{OPH}$

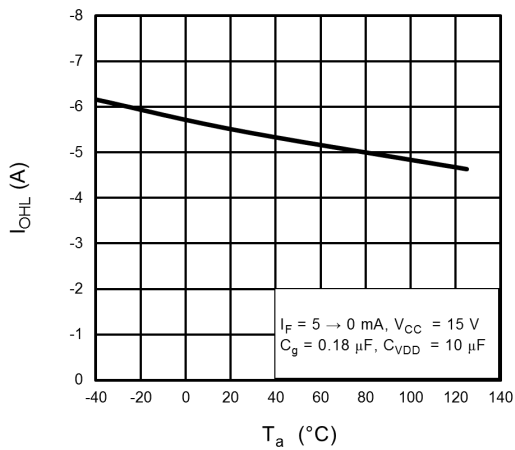


Fig. 13.2.11 $I_{OHL} - T_a$

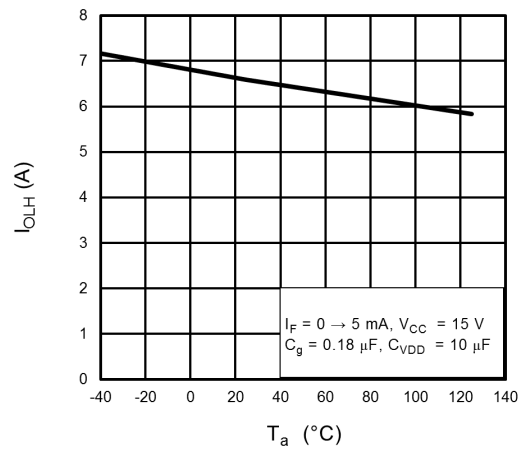


Fig. 13.2.12 $I_{OLH} - T_a$

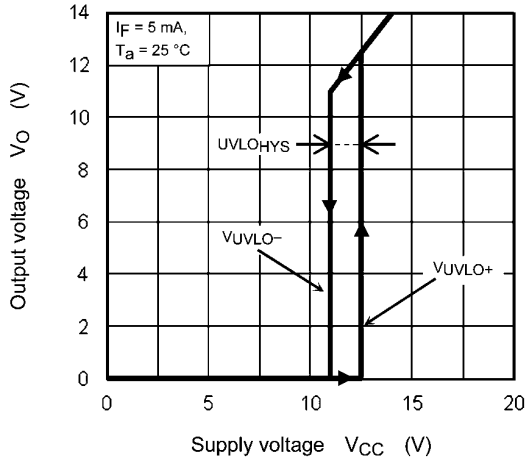


Fig. 13.2.13 $V_O(V_{UVLO}) - V_{CC}$

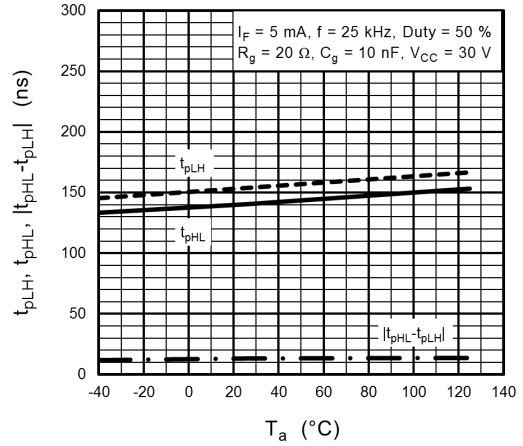


Fig. 13.2.14 $t_{pLH}, t_{pHL}, |t_{pHL} - t_{pLH}| - T_a$

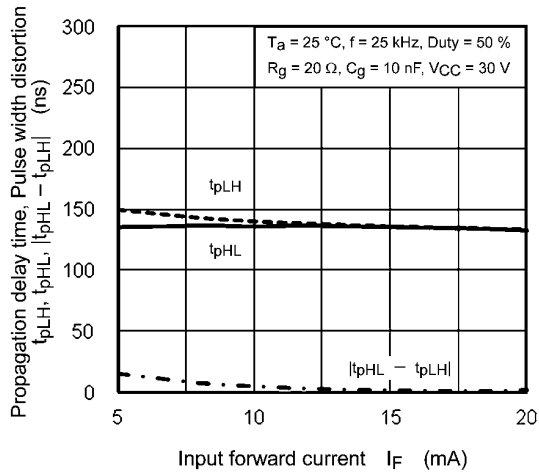


Fig. 13.2.15 $t_{pLH}, t_{pHL}, |t_{pHL} - t_{pLH}| - I_F$

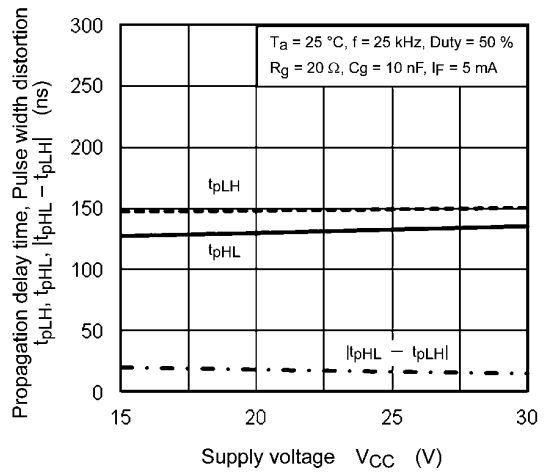


Fig. 13.2.16 $t_{pLH}, t_{pHL}, |t_{pHL} - t_{pLH}| - V_{CC}$

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

14. Soldering and Storage

14.1. Precautions for Soldering

The soldering temperature should be controlled as closely as possible to the conditions shown below, irrespective of whether a soldering iron or a reflow soldering method is used.

- When using soldering reflow.

The soldering temperature profile is based on the package surface temperature.

(See the figure shown below, which is based on the package surface temperature.)

Reflow soldering must be performed once or twice.

The mounting should be completed with the interval from the first to the last mountings being 2 weeks.

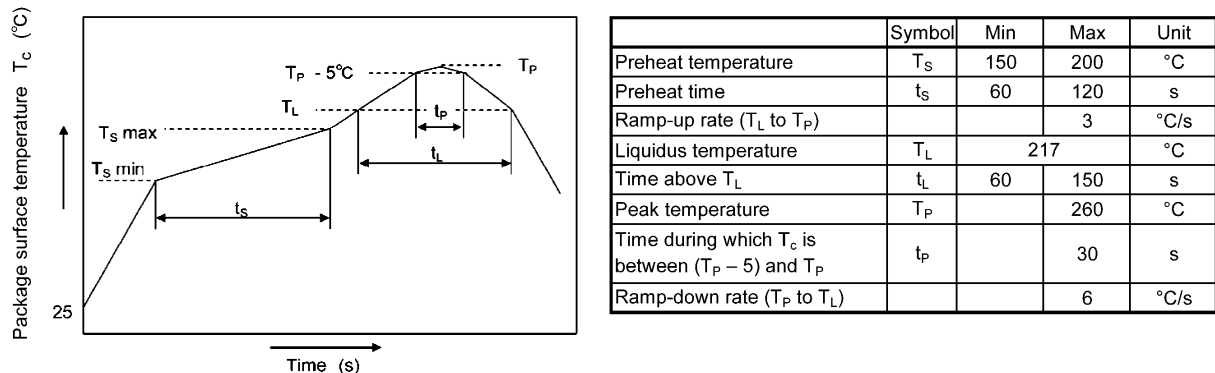


Fig. 14.1.1 An example of a temperature profile when lead(Pb)-free solder is used

- When using soldering flow
Preheat the device at a temperature of 150 °C (package surface temperature) for 60 to 120 seconds.
Mounting condition of 260 °C within 10 seconds is recommended.
Flow soldering must be performed once.
- When using soldering Iron
Complete soldering within 10 seconds for lead temperature not exceeding 260 °C or within 3 seconds not exceeding 350 °C
Heating by soldering iron must be done only once per lead.

14.2. Precautions for General Storage

- Avoid storage locations where devices may be exposed to moisture or direct sunlight.
- Follow the precautions printed on the packing label of the device for transportation and storage.
- Keep the storage location temperature and humidity within a range of 5 °C to 35 °C and 45 % to 75 %, respectively.
- Do not store the products in locations with poisonous gases (especially corrosive gases) or in dusty conditions.
- Store the products in locations with minimal temperature fluctuations. Rapid temperature changes during storage can cause condensation, resulting in lead oxidation or corrosion, which will deteriorate the solderability of the leads.
- When restoring devices after removal from their packing, use anti-static containers.
- Do not allow loads to be applied directly to devices while they are in storage.
- If devices have been stored for more than two years under normal storage conditions, it is recommended that you check the leads for ease of soldering prior to use.

15. Land Pattern Dimensions (for reference only)

Unit: mm

TLP5705H

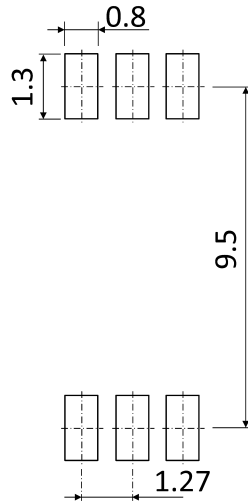


Fig. 15.1 Lead Forming Option (standard)

TLP5705H(LF4)

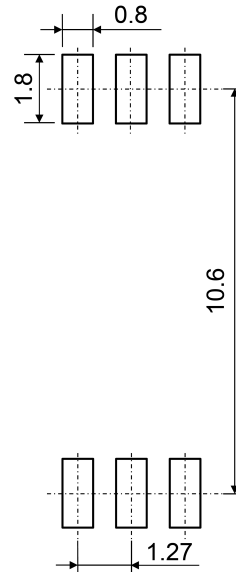
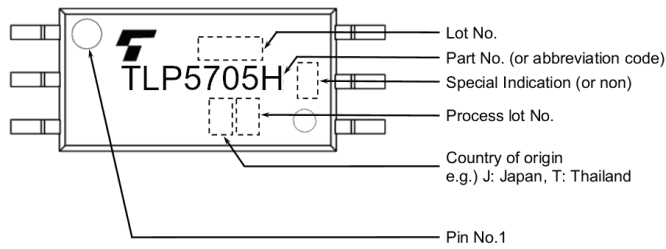


Fig. 15.2 Lead Forming Option (LF4)

16. Marking



17. EN 60747-5-5 Option (D4) Specification

- Part number: TLP5705H (Note 1)
- The following part naming conventions are used for the devices that have been qualified according to option (D4) of EN 60747.

Example: TLP5705H(D4-TP,E)

D4: EN 60747 option

TP: Tape type

E: [[G]]/RoHS COMPATIBLE (Note 2)

Note 1: Use TOSHIBA standard type number for safety standard application.

e.g., TLP5705H(D4-TP,E → TLP5705H

Note 2: Please contact your Toshiba sales representative for details on environmental information such as the product's RoHS compatibility.

RoHS is the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

| Description | Symbol | Rating | Unit |
|---|--|---|-------------------|
| Application classification for rated mains voltage ≤ 600 Vrms for rated mains voltage ≤ 1000 Vrms | | I-IV I-III | — |
| Climatic classification | | 40 / 125 / 21 | — |
| Pollution degree | | 2 | — |
| Maximum operating insulation voltage | V _{IORM} | 1414 | V _{peak} |
| Input to output test voltage, Method A V _{pr} = 1.6 × V _{IORM} , type and sample test t _p = 10 s, partial discharge < 5 pC | V _{pr} | 2262 | V _{peak} |
| Input to output test voltage, Method B V _{pr} = 1.875 × V _{IORM} , 100 % production test t _p = 1 s, partial discharge < 5 pC | V _{pr} | 2652 | V _{peak} |
| Highest permissible overvoltage (transient overvoltage, t _{pr} = 60 s) | V _{TR} | 8000 | V _{peak} |
| Safety limiting values (max. permissible ratings in case of fault, also refer to thermal derating curve) current (input current I _F , P _{SO} = 0) power (output or total power dissipation) temperature | I _{si} P _{so} T _s | 300 700 150 | mA mW °C |
| Insulation resistance V _{IO} = 500 V, T _a = 25 °C V _{IO} = 500 V, T _a = 100 °C V _{IO} = 500 V, T _a = T _s | R _{si} | $\geq 10^{12}$ $\geq 10^{11}$ $\geq 10^9$ | Ω |

Fig. 17.1 EN 60747 Insulation Characteristics

| | | |
|------------------------------|-----|--------|
| Minimum creepage distance | Cr | 8.0 mm |
| Minimum clearance | Cl | 8.0 mm |
| Minimum insulation thickness | ti | 0.4 mm |
| Comparative tracking index | CTI | 500 |

Fig. 17.2 Insulation Related Specifications (Note)

Note: This photocoupler is suitable for safe electrical isolation only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits.



Fig. 17.3 Marking on Packing

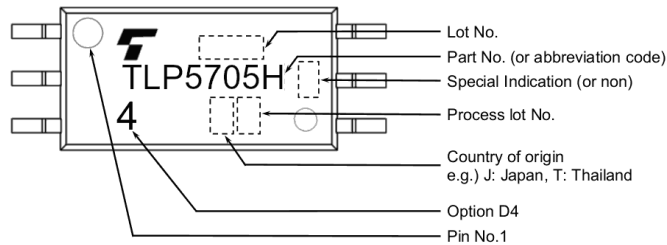


Fig. 17.4 Marking Example (Note)

Note: The above marking is applied to the photocouplers that have been qualified according to option (D4) of EN 60747.

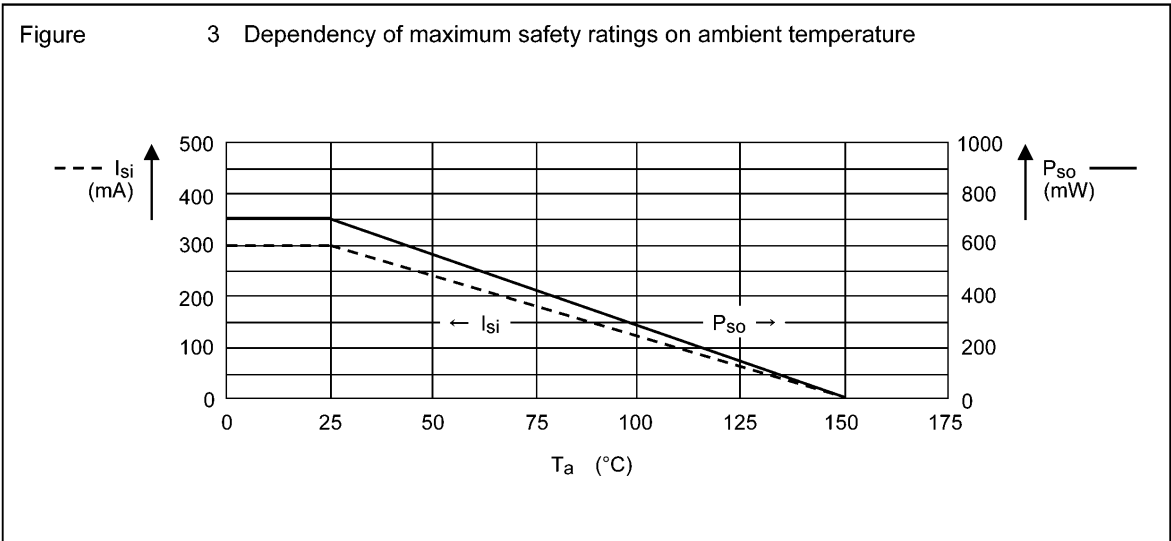
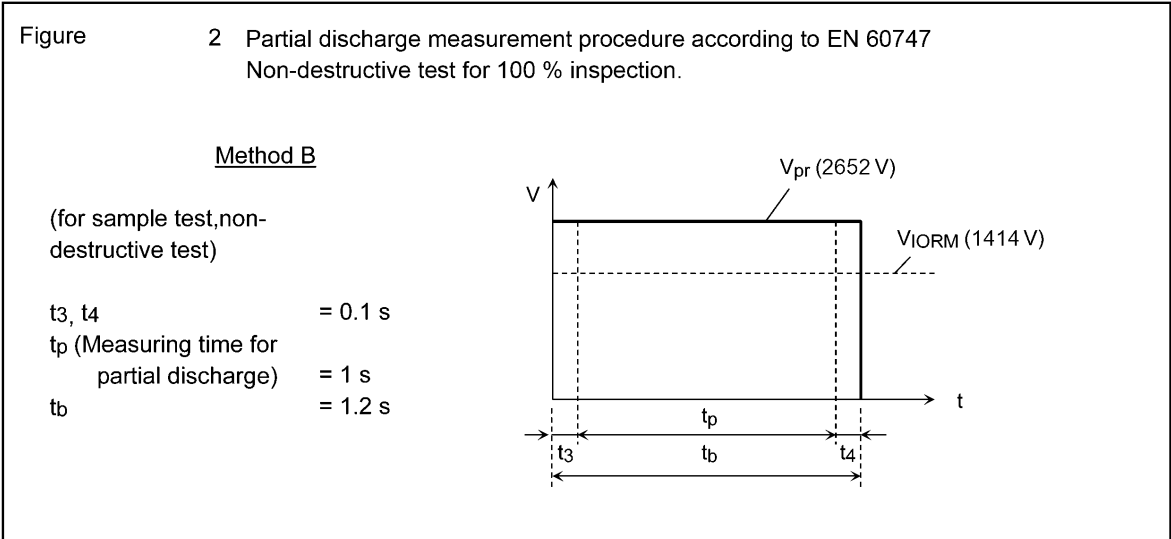
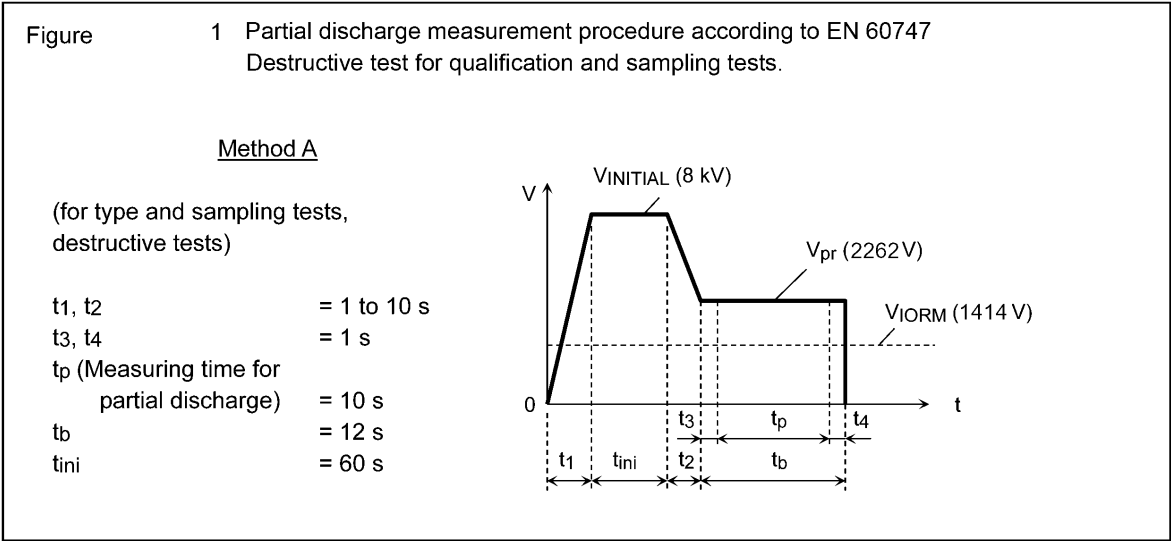


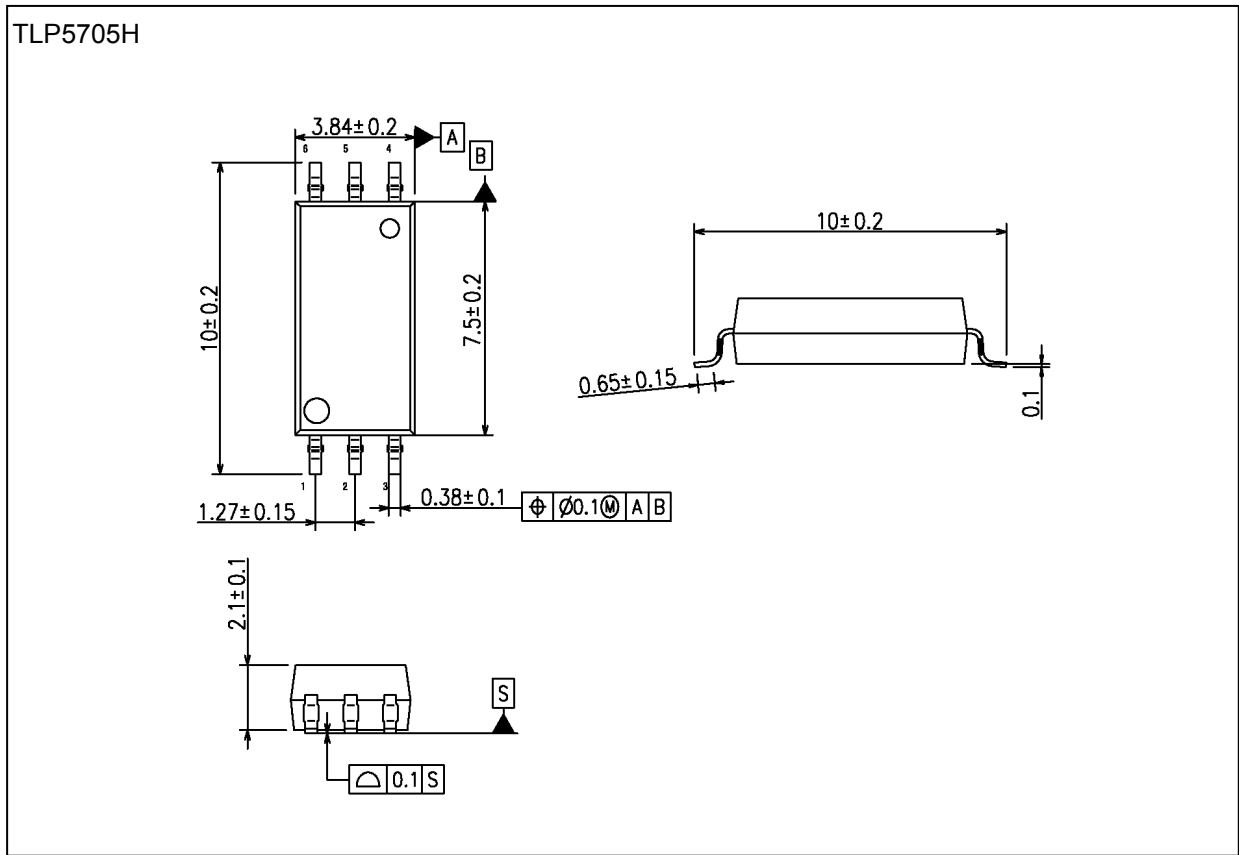
Fig. 17.5 Measurement Procedure

18. Ordering Information (Example of Item Name)

| Item Name | Packaging | VDE Option | Packing (MOQ) |
|-------------------|-------------------|--------------|--------------------------|
| TLP5705H(E) | | | Magazine (125 pcs) |
| TLP5705H(TP,E) | | | Tape and reel (1500 pcs) |
| TLP5705H(D4,E) | | EN 60747-5-5 | Magazine (125 pcs) |
| TLP5705H(D4-TP,E) | | EN 60747-5-5 | Tape and reel (1500 pcs) |
| TLP5705H(LF4,E) | LF4, Wide forming | | Magazine (125 pcs) |
| TLP5705H(TP4,E) | LF4, Wide forming | | Tape and reel (1500 pcs) |
| TLP5705H(D4LF4,E) | LF4, Wide forming | EN 60747-5-5 | Magazine (125 pcs) |
| TLP5705H(D4TP4,E) | LF4, Wide forming | EN 60747-5-5 | Tape and reel (1500 pcs) |

Package Dimensions

Unit: mm

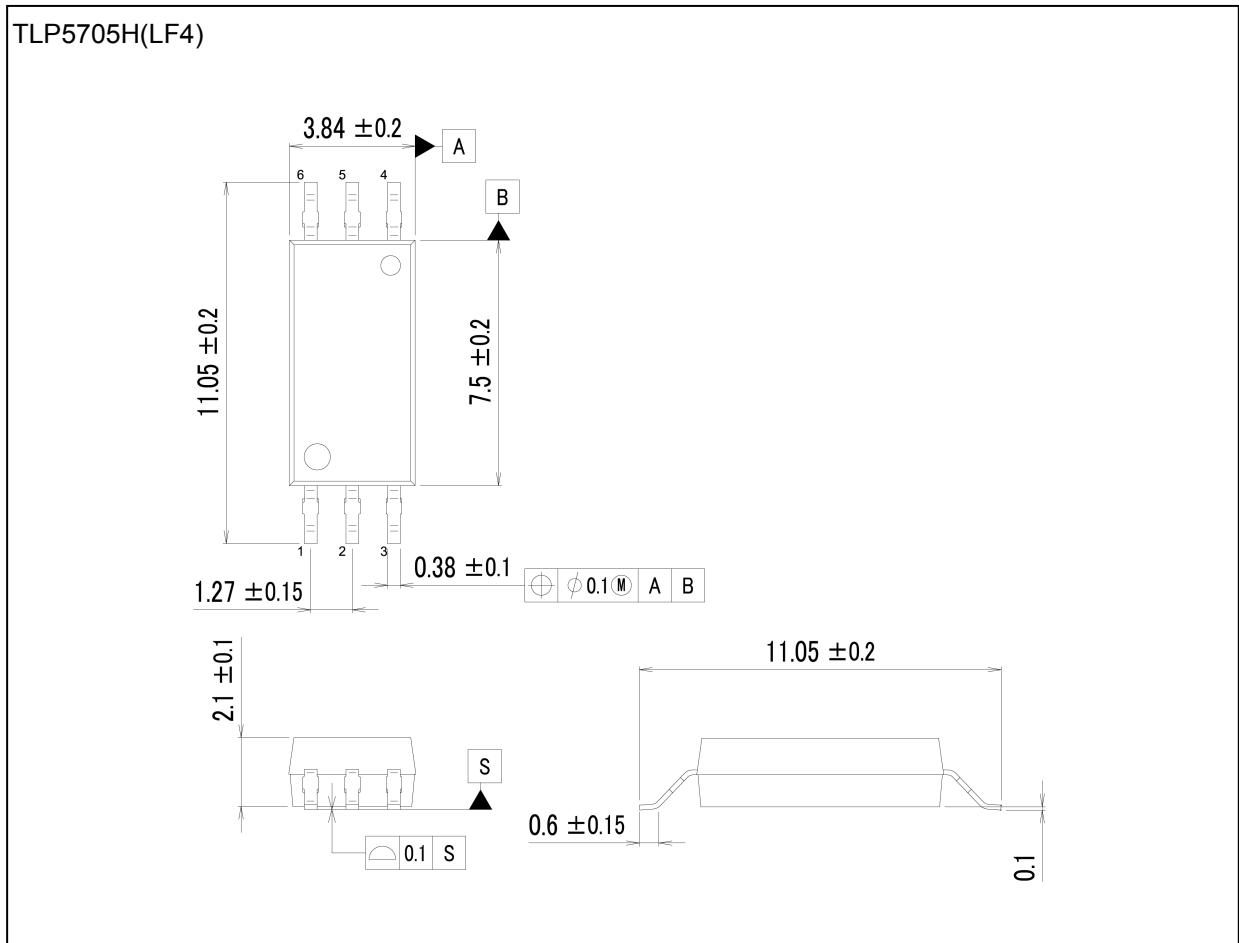


Weight: 0.126 g (typ.)

| Package Name(s) |
|------------------|
| TOSHIBA: 11-4N1A |

Package Dimensions

Unit: mm



Weight: 0.126 g (typ.)

| Package Name(s) |
|--------------------|
| TOSHIBA: 11-4N101A |

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