# TOLL package

# Application Note

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# 1. Introduction to TOLL package

TOLL package is surface mount package developed for applications that require high-efficiency, such as servers, telecoms, and data centers, as represented by industrial power supplies.

Until now, through hole package with long terminal leads, such as TO-247 and TO-220, have been mainly used as high voltage MOSFET package for industrial power supplies, but there have been problems with the MOSFET performance that was limited due to the parasitic inductance of the terminal leads. In addition, various SMD (Surface Mount Device) packages have been released increasing further power density and to reduce the cost, but these package adoption has been limited due to heat dissipation and on-board reliability problem.

Our TOLL package is surface mount package that solves these challenges for high-efficiency, high-current applications. By incorporating our newest-generation Super Junction MOSFET process DTMOSVI Series, it will contribute to improve the power density, performance, and cost reduction of our customer's products.

## 1.1. TOLL Package Lineup

Five products equipped with the high performance DTMOSVI series. Table 1.1 shows the lineup of TOLL packages.

Table 1.1 TOLL Package Lineup

| Product Number | Package | Absolute maximum rating | | Drain-source on-resistance $R_{DS(ON)}$ max @$V_{GS}$=10 V (Ω) | Total gate charge $Q_g$ Typ. (nC) | Gate-drain charge $Q_{gd}$ Typ. (nC) | Input capacitance $C_{iss}$ Typ. (pF) @$V_{DS}$=300V | Conventional series (DTMOSIV D2PAK) Product Number |
|---|---|---|---|---|---|---|---|---|
| | | Drain-source voltage $V_{DSS}$ (V) | Drain current (DC) $I_D$ (A) | | | | | |
| TK065U65Z | TOLL | 650 | 38 | 0.065 | 62 | 17 | 3650 | |
| TK090U65Z | TOLL | 650 | 30 | 0.090 | 47 | 12 | 2780 | |
| TK110U65Z | TOLL | 650 | 24 | 0.110 | 40 | 11 | 2250 | |
| TK155U65Z | TOLL | 650 | 18 | 0.155 | 29 | 8 | 1635 | TK20G60W |
| TK190U65Z | TOLL | 650 | 15 | 0.190 | 25 | 7.1 | 1370 | TK16G60W |

# 2. Product performance improvement

## 2.1. DTMOSVI device performance

Our newest generation super junction MOSFET process DTMOSVI(Deep Trench MOSFET, the sixth generation) achieves best in class $R_{DS(ON)}$xQgd performance. As shown in Fig.2-1, we have reduced $R_{DS(ON)}$xQgd by about 40% compared to our previous-generation product DTMOSIV-H. Also, we confirmed the parts have superior characteristic compared to competitors' high-performance series products (Company A Part1 and Part2).

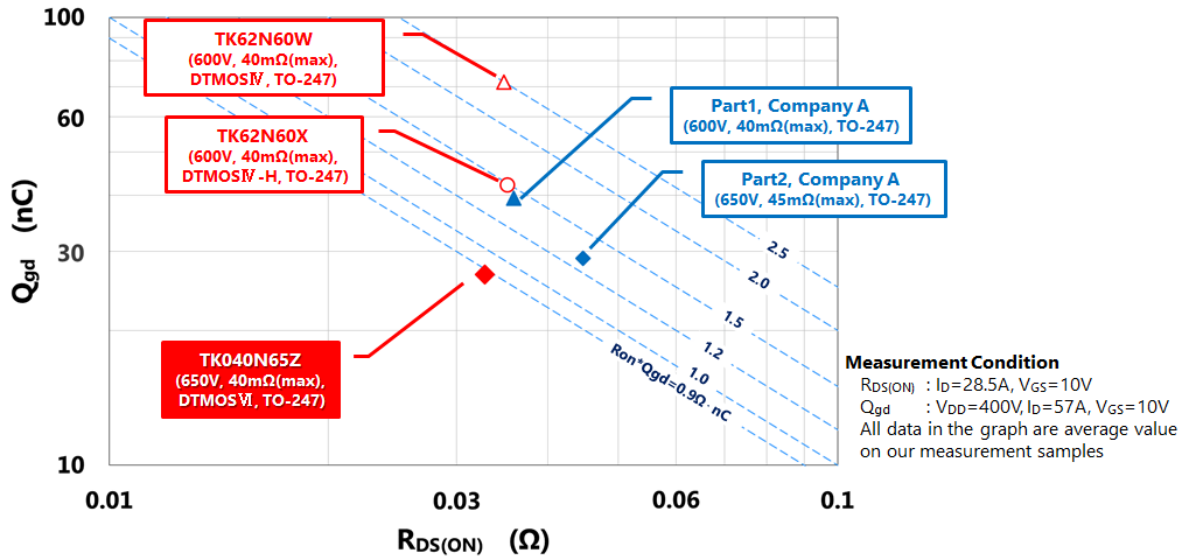



Fig.2-1 Qgd-$R_{DS(ON)}$ characteristics comparison

Because of best in class $R_{DS(ON)}$xQgd characteristic, we realize more efficient power supply compared to our previous-generation products and competitors' high-performance series products (Company A Part3), as shown in Fig. 2-2.

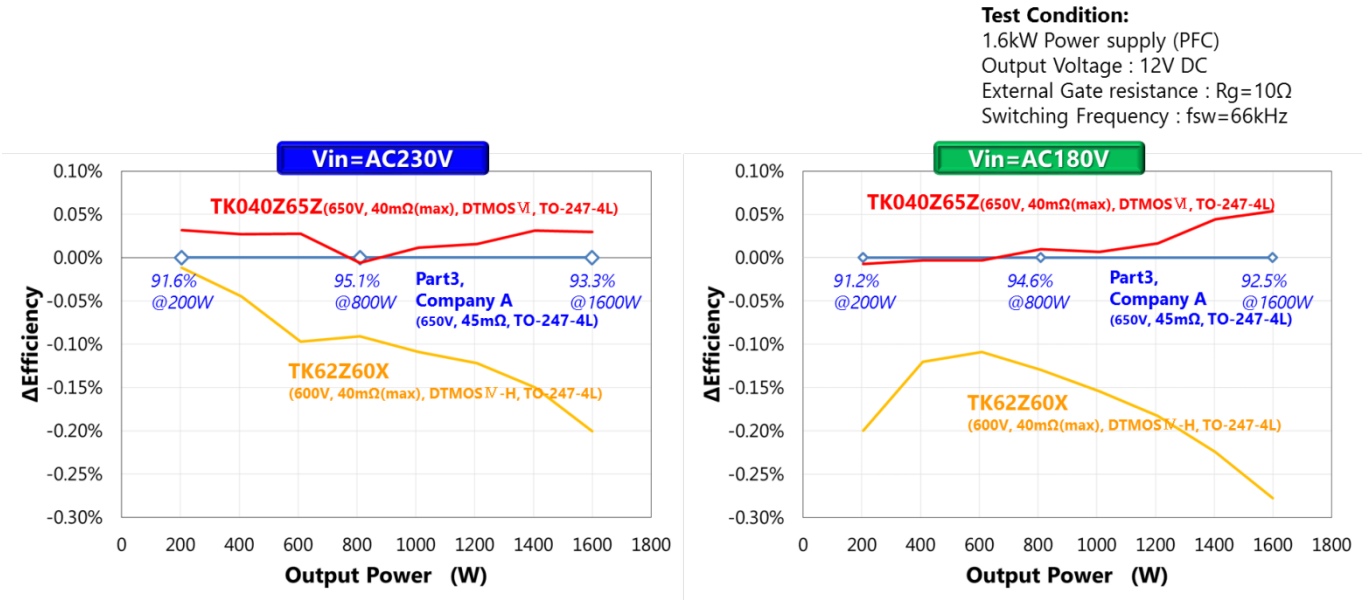



Fig.2-2 Efficiency Comparison Data 1.6kW Power Supply

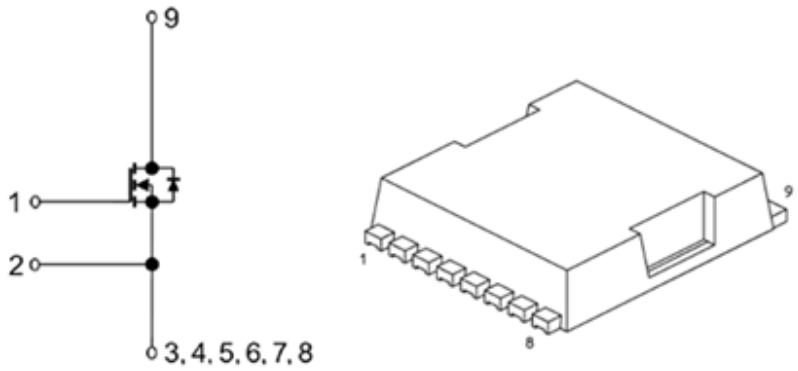
## 2.2. Effect of 4-Terminal Package

### 2.2.1. 4-Terminal Package Structure, Drive Mechanism

Fig.2.3 shows the internal circuit configuration and the external view of TOLL package. TOLL package is a 4-terminal type with the source terminal separated into source 1 and source 2, and the 2-pin Source 2 terminal can be used for the return of the gate signal, and you can connect the 3 to 8-pin Source 1 terminal, which are used the drain-source current path.

Fig2-4 shows driving outline for a 4-terminal type TOLL package comparing to a 3-terminal type package when these are switching.

In 3-terminal package, steep-slope drain currents and source wire inductance create a voltage drop ($V_{LS}$) that reduces MOSFET gate drive voltage ($V_{GS}$). Therefore, the gate voltage $V_{GS}$ applied to the actual MOSFET chip is a $V_{DRV}$-$V_{LS}$ obtained by subtracting $V_{LS}$ from the gate voltage $V_{DRV}$ applied between the gate terminal and the source terminal of the package. On the other hand, in TOLL package, by separating the source pins for the drive circuitry, the effects of voltage drop ($V_{LS}$) due to the source inductance can be reduced, and you can maximize the high-speed switching performance of MOSFET chip.




1: Gate
2: Source 2
3, 4, 5, 6, 7, 8: Source 1
9: Drain (heatsink)

Fig.2-3 TOLL Package Pinout, External View

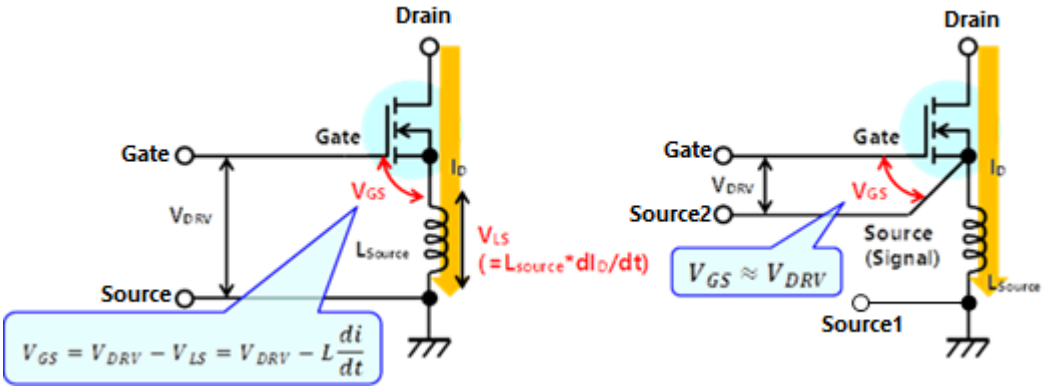


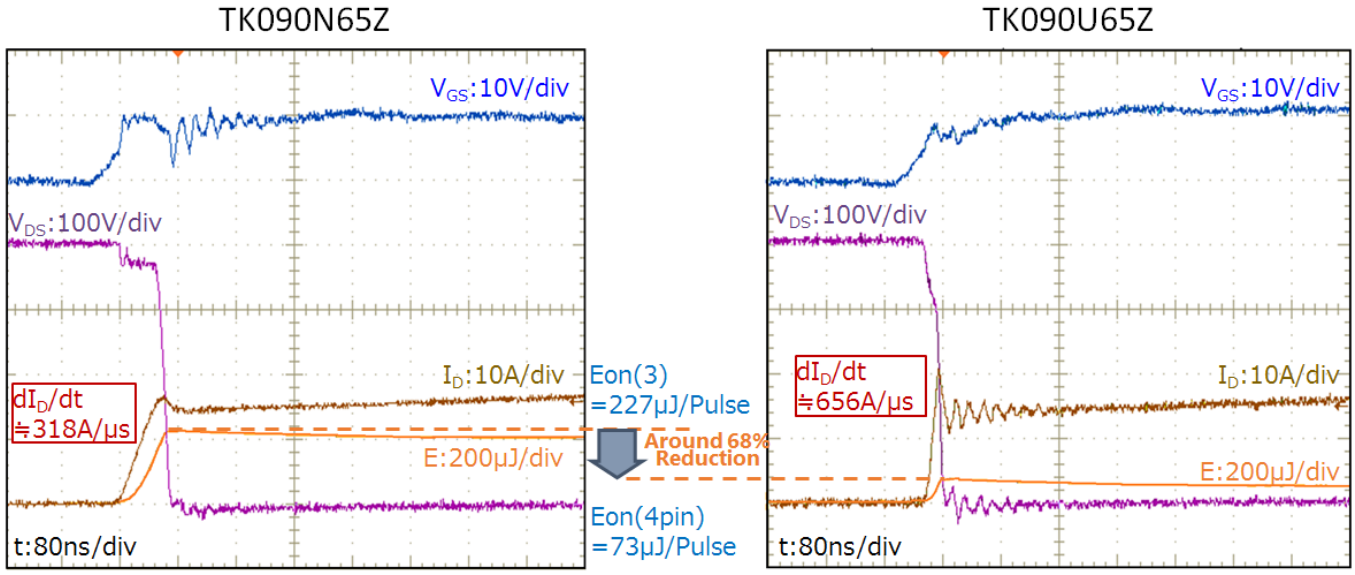

Fig.2-4 Driving outline of 4-terminal package

### 2.2.2. 4-Terminal Package Switching Loss Reduction Effect

Fig. 2-5 and 2-6 compare the Inductive-load switching waveforms between four-terminal-type TOLL package (TK090U65Z) and three-terminal-type TO-247 package (TK090N65Z) which is not divided source line into a gate signal line and a power line. The mounted chips are same.

From the turn-on waveform shown in Fig. 2-5, we have confirmed that the turn-on loss Eon improves by 68% by reducing the effect of the back electromotive force ($V_{LS}$) caused by the source inductance as described earlier. Similarly, the turn-off loss Eoff on turn-off waveform shown in Fig. 2-6 has been improved by 56%.

We have confirmed that the amplitude of the gate voltage oscillation is reduced significantly on a turn-off waveform. This oscillation waveform is due to the back electromotive force caused by the source inductance, which can be reduced by dividing the source line into the gate signal line and the power line. Since this gate-voltage oscillation affects the electromagnetic noise of the power supply, by using TOLL package also contributes to reduce their noise in customer's




products.

Fig.2-5 Inductive Load Turn-on Waveform Comparison (TO-247 TK090N65Z vs TOLL TK090U65Z)

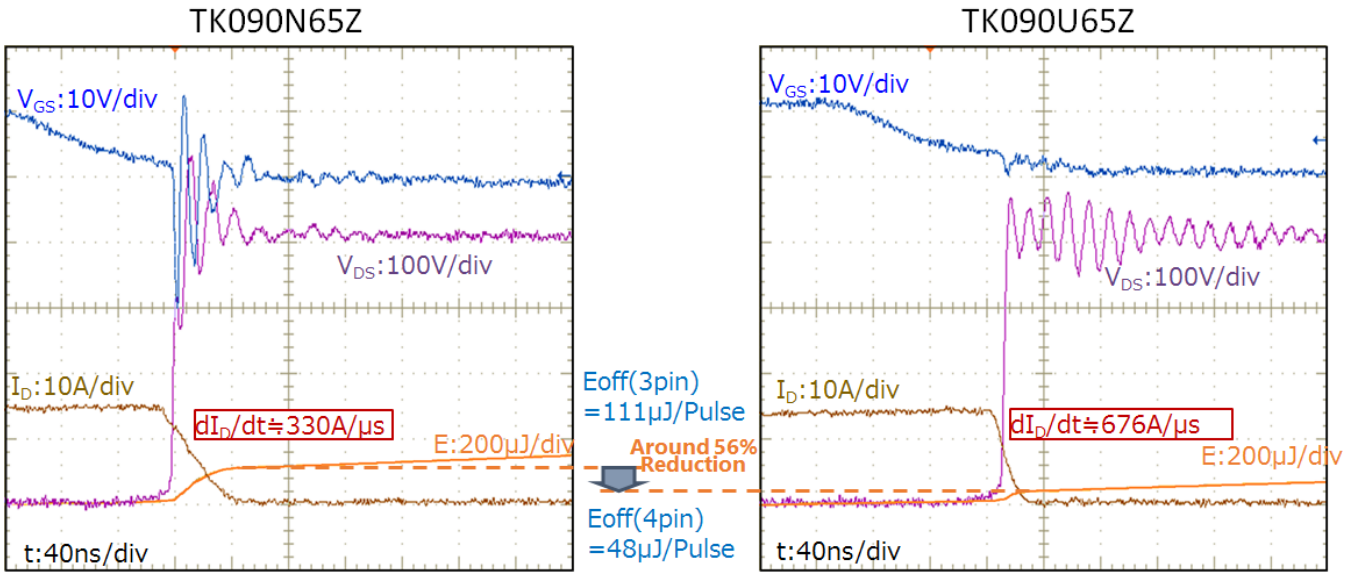



Fig.2-6 Inductive-Load Turn-off Waveform Comparison (TO-247 TK090N65Z vs TOLL TK090U65Z)

# 3. TOLL package mounting

## 3.1. Package Dimensions and Reference Pad Dimensions

Fig.3-1 shows the package dimensions and Fig.3-2 shows the reference pad dimensions. This reference pad dimension is used as a board pattern for our on-board reliability test which will be described later (3-3). By placing thermal via in the drain pad, heat can be dispersed to each layer and back surface of the board to improve heat dissipation (refer to Section 4 for details). In addition, our TOLL package is compatible with other manufacturer's TOLL package, and it can utilize on same pad dimensions as shown in Figs. 3-3 and 3-4. (When you actually use the package, please thoroughly evaluate and verify in advance on your board and your operating conditions.)

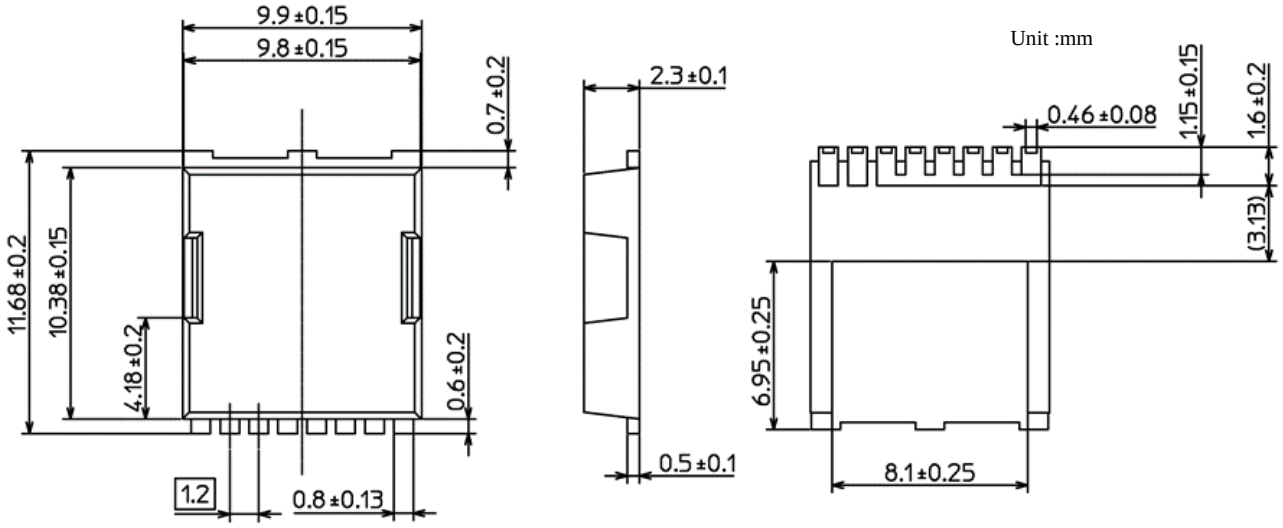



Fig. 3-1 TOLL Packaging Dimensions

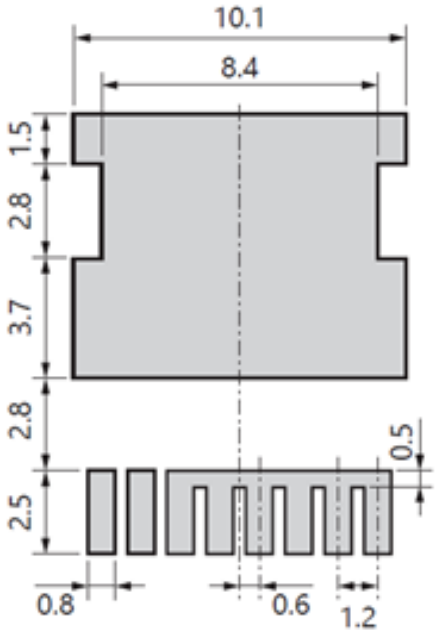



Figure 3-2 Reference Pad Dimensions

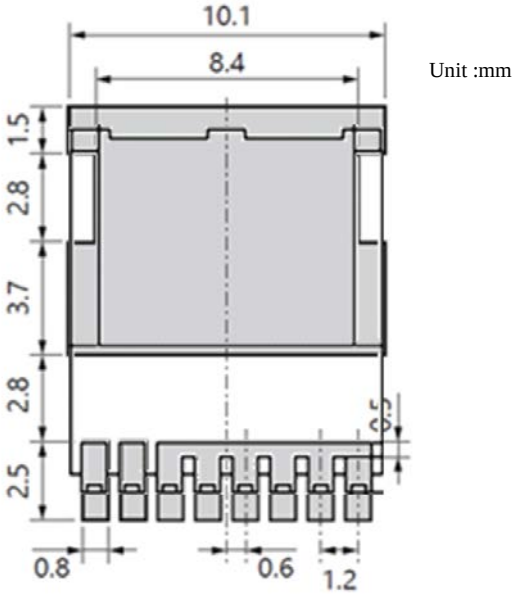



Fig. 3-3 Reference Pad Dimensions + Our TOLL
(When back side and reference pad dimensions are overlapped)

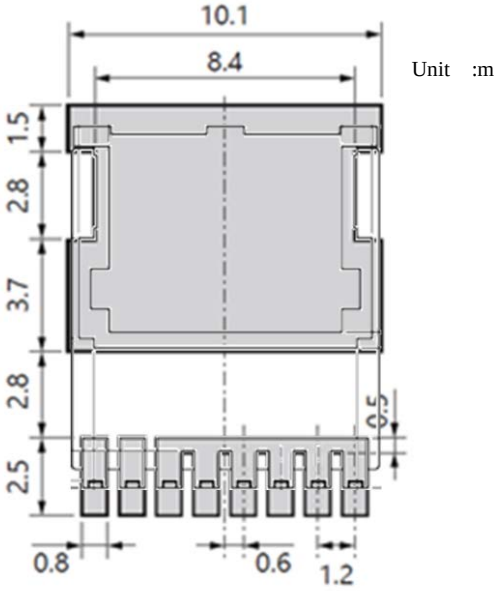



Fig. 3-4 Reference Pad Dimensions + Company A TOLL
(When back side and reference pad dimensions are overlapped)

## 3.2. Distance between terminals

Our TOLL package has a 3.13mm terminal distance between the drain and source pin. This is wider than the 2.795mm of the through hole TO-247, and it can ensure adequate terminal distance (see Fig. 3-5). From the terminal distance stand point, TOLL package is ideal as a replacement from he through hole TO-247 package.

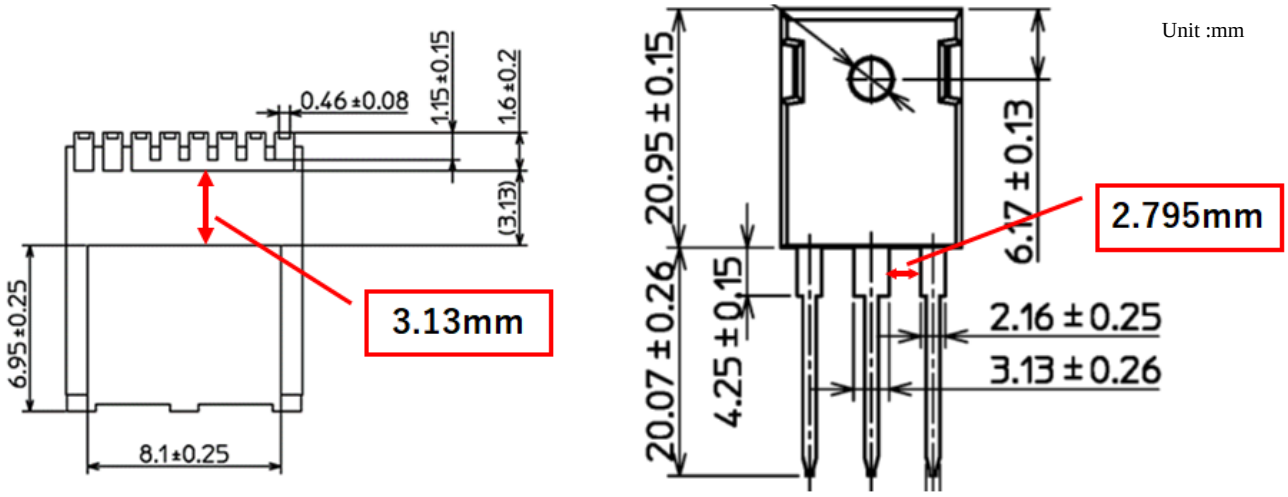



Fig. 3-5 Drain-Source Terminal distance comparison (TOLL vs TO-247)

## 3.3. TOLL package reliability

In order to clarify the board level reliability of TOLL package, we conducted the board level reliability test on the following boards, mounting conditions, and test conditions. For reference, we compared the results of the board level reliability test with the other TOLL package manufactured by the other company (Company B) on same board and mounting/testing conditions.

### 3.3.1. Test conditions, cross-sectional observation method

Table 3-1 shows the board level reliability test conditions, mounting board composition, size, mounting solder materials, etc. of our TOLL package.

Table 3-1: Pretreatment and test conditions of the board level reliability test

| | Conditions |
|---|---|
| Pretreatment | Leave MOSFET alone at 105°C for 100% for 8 hours prior to mounting on a board. |
| Mounting conditions | Solder paste 150±50μm (finished 70 to 100μm) SAC305<br>Heating treatment temperature peak temperature: 230 to 235°C, preheating condition: 160 to 180°C (60 to 120s) |
| Temperature cycle | -55°C ⇔ 125°C 1 cycle/1 hour |
| Number of cycles | ～1000 cycles |
| Mounting board | Board material: FR-4<br>Glass-transition temperature Tg : 140°C<br>Number of layers: 4 layers (Cu 2oz)<br>Board size :25.4 mm×25.4 mm×1.6 mm<br>Solder stencil thickness: 100 μm<br>Mounting solder material: SAC305 |

Fig.3-6 shows the cross-sectional view direction and cross-sectional view location of the package. The gate terminal 1pin was cut to observe the degradation of the lead mount solder, the presence or absence of cracks, and the degree. In addition, we cut the vicinity of 5 pins and observed the degradation of the mount solder between the chip and the lead frame in the center of the package, the presence or absence of cracks, and the degree of such degradation.

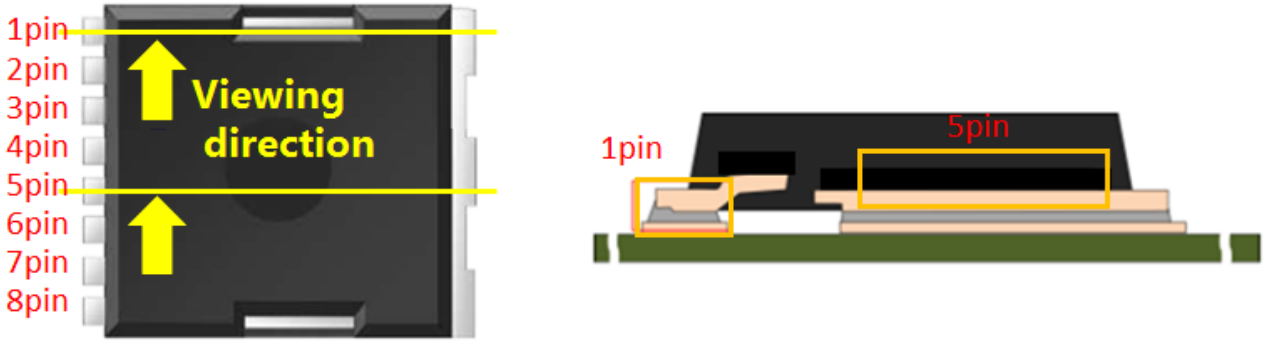
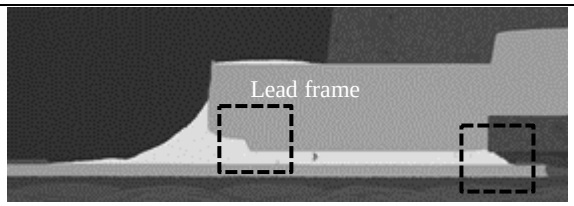
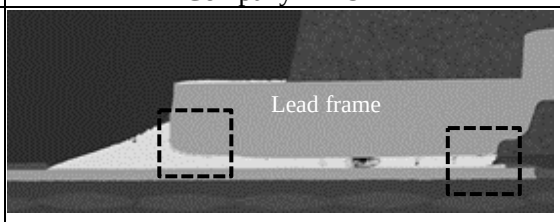
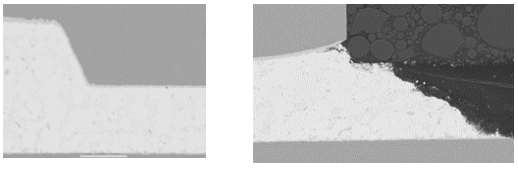
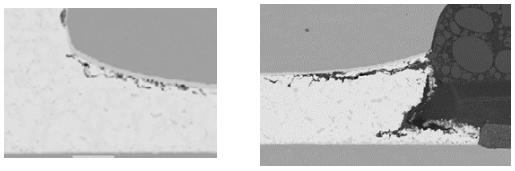
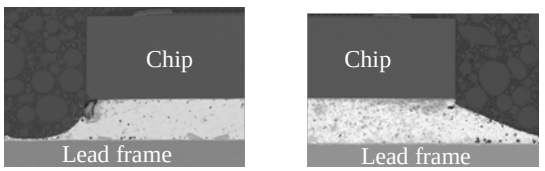
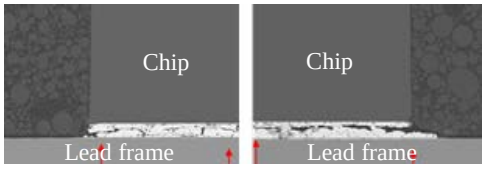



Fig. 3-6: Cross-sectional view direction and cross-sectional view location

### 3.3.2. Results of the board level reliability test

Table 3-2 shows the board level reliability test result conducted by both our TOLL package and the other company (Company B) under our mount and test conditions. In our test and board conditions, our TOLL package did not exhibit any property variations or large mounting solder cracks after 1000 cycles @-55 to 125°C testing. On the other hand, on same 1000 cycles, the Company B showed the cracks in the mounting solder at multiple locations, and confirmed wide range of mounting solder cracks too. We have also confirmed that solder cracks, which occurred in the mounting solder between the chip and Cu frames inside Company B's TOLL package. We have confirmed that our TOLL package is more reliable than the Company B on the board level reliability stand point in the same environment. (However, this result is based on our own reliability test and board condition. When you adopt our part, please sufficiently evaluate and confirm our part on your own board and your own test condition in advance.)

Table 3-2 TOLL Package board level reliability test results@1000 Cycles (Compared with Company B)

| | | Our TOLL | Company B TOLL |
|---|---|---|---|
| 1000 Cycle | 1pin |   |   |
| | 1pin Scale up |  |  |
| | 5pin Inside |   |   |

# 4. TOLL package heat dissipation designs

## 4.1. Heat dissipation method

For surface-mounted products such as TOLL packages, as shown in Fig. 4-1, a package is mounted on PCB such as a FR-4, and external heatsink is connected to the back surface of the board through a heat dissipation (insulation) sheet. In such cases, TOLL package need to handle large amounts of power, and it is required high efficiency on high power condition. Therefore, board pad designs, such as the size of the Cu-pad on the mounting board and the number of thermal via, greatly affect heat dissipation.

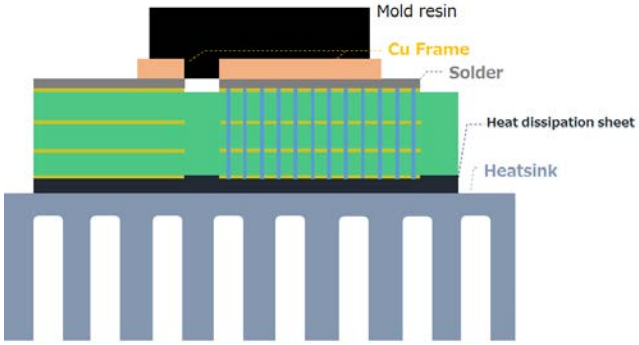



Fig. 4-1: TOLL Package Recommended Board Mounting Image

## 4.2. Optimal Design of Board Pads and Thermal Via

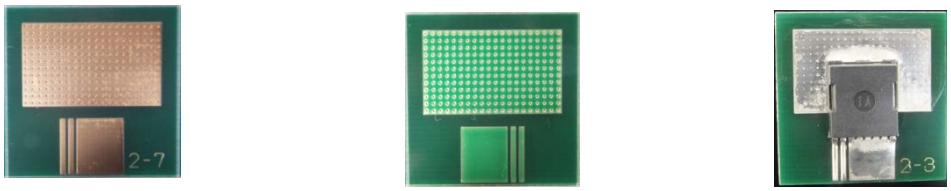
In order to clarify the design guideline for the pad size and thermal via on the TOLL package board, we measured the surface temperature (Tc) for the applied power by changing the number of thermal via, the size of the Cu pad, and other parameters using our own heat dissipation evaluation boards. We also showed quantitatively the heat dissipation effect by the board design.

### 4.2.1. Specifications of PCB for evaluation of heat dissipation

Table 4-1 shows the 1-inch PCB specifications for which heat dissipation was evaluated for TOLL package. Fig. 4-2 shows the mounting surface, back surface, and mounting picture, and Fig.4-3 shows the cross-sectional image and dimensions of the PCB. As for boards, a total of five patterns (Table 4-2) were created and prepared by changing the drain pad size, the presence or absence of thermal via, the number of thermal via, etc. In addition, the via diameter is now uniform at 0.3mm.

Table 4-1: Specifications of PCB for evaluation of heat dissipation

| Land pattern | Five conditions |
|---|---|
| PCB size | 25.4mm×25.4mm×1.6mm |
| Number of PCB layers | 4 layers |
| PCB material | FR-4, Tg=140℃ |
| Layer material/thickness | Cu 2oz |




Mounting surface　　Back surface　　Mounting photo

Fig.4-2: Mounting Surface, Back Surface, and Mounting Photos

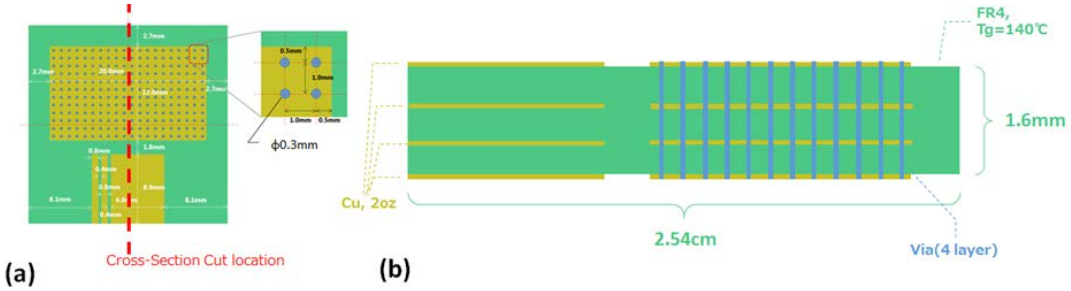
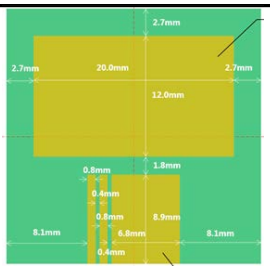
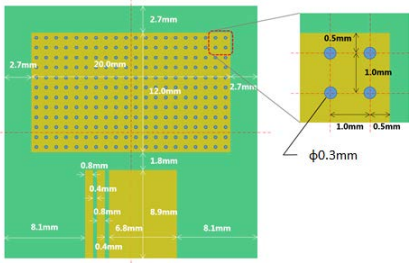
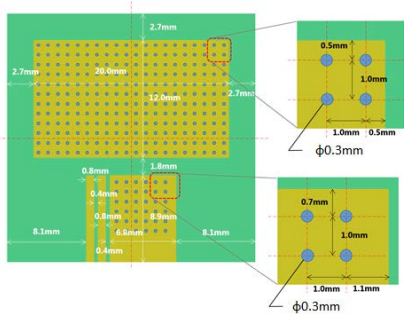
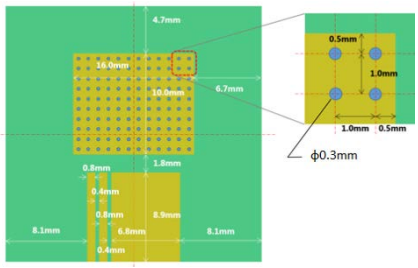
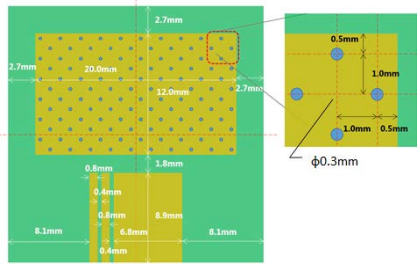



Figure 4-3 Cross-sectional view and dimensions of the board

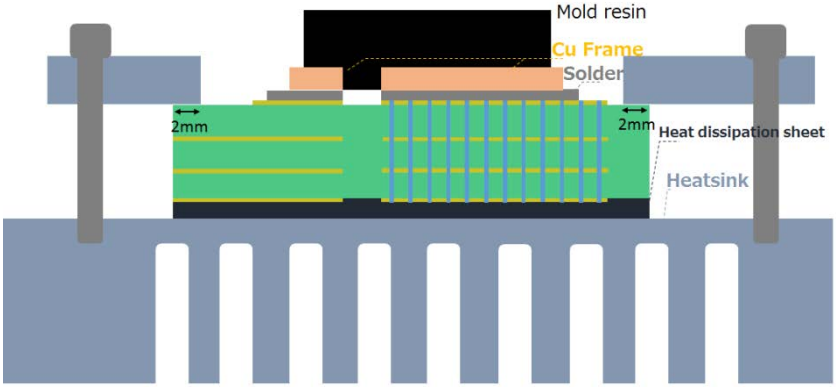
Table 4-2 Cu Pattern Drain Pad Size, Thermal via Design, and Number

| Pattern | Dimensions | Drain pad size | Drain via | Drain Number of via | Remarks |
|---|---|---|---|---|---|
| 1 |  | Large | None | 0 | |
| 2 |  | Large | Entire surface | 240pcs | |
| 3 |  | Large | Entire surface | 240pcs | Source via addition (Number: 36pcs) |
| 4 |  | Small | Entire surface | 120pcs | |
| 5 |  | Large | Entire surface | 120pcs | Drain via Spacing expansion |

### 4.2.2. Heat dissipation evaluation environment

On evaluating heat dissipation, we used a DC power supply to apply power to TOLL package.We set the power supply to 300 sec in this time in order to rise device temperature satulated. Thermography was used to measure the device surface temperature (Tc) after 300 sec. The external heatsink were cooled by an air-cooled fan and the PCB was fixed to the heatsink by holding the board end (2mm) with an aluminum plate (see Fig.4-4).

Fig. 4-4 Heat dissipation sheet and external heatsink installation method




A heat dissipation sheet (1 inch, MAC EIGHT, CW-200, thickness 3mm (typ), material: Sarcon TR (UL84V-0)) is sandwiched between the external heatsink and the board to ensure insulation and heat dissipation.
To minimize the influence of Heat dissipation from the wires, the wires for the gate, drain, and source are soldered to the ends of each terminal pad as shown in Fig.4-5 below to secure a distance from the device. As shown in the figure, the temperature was observed at the point where the temperature became the highest at the mold resin surface near the drain terminal (directly above the chip).

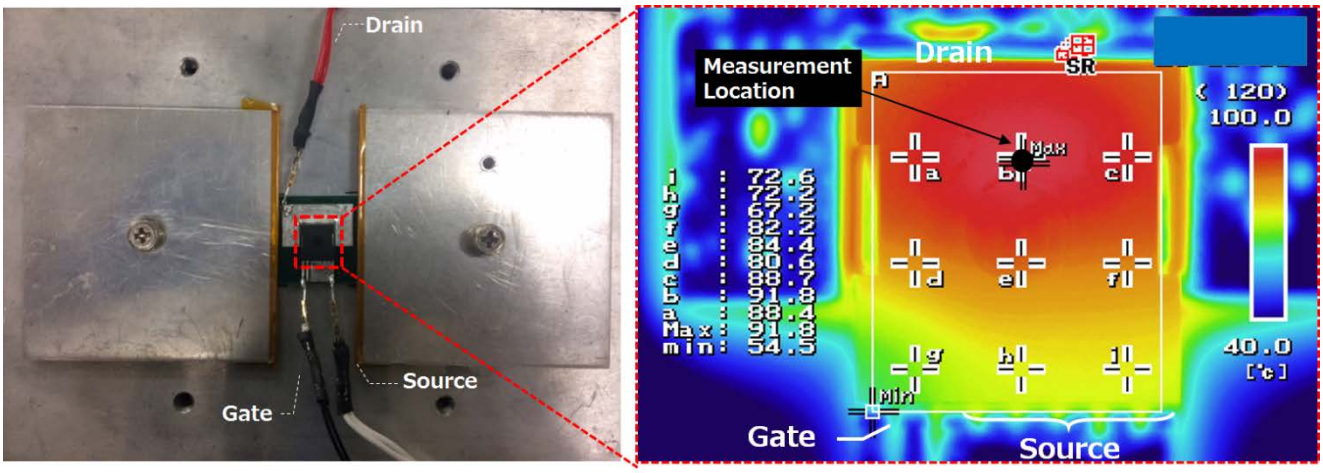



Fig.4-5 Tc (Case Temp.) Measurement method/point

### 4.2.3. Evaluation results of heat dissipation

Fig.4-6 shows the measured case temperature ($T_c$ (Max)) at the maximum surface temperature point (measurement point) for the applied power (Pin) using the board of each pattern. To prevent damage to the device, the upper limit of $T_c$ was set to about 100°C.

Pattern 1 and Pattern 2 are the difference between the presence and absence of thermal via. In the case of device loss: 10W, the calculated value is equivalent to Tc=131°C in Pattern 1, and the measured value is Tc=66°C in Pattern 2, which results in a large difference in heat dissipation with and without thermal via.

Pattern 3 also has a board with thermal vias on the source pads of Pattern 2, and its heat dissipation is improved from Pattern 2. We confirmed that $T_c$ was reduced around 3°C at a device loss: 18W (100.1°C⇒97.1°C).

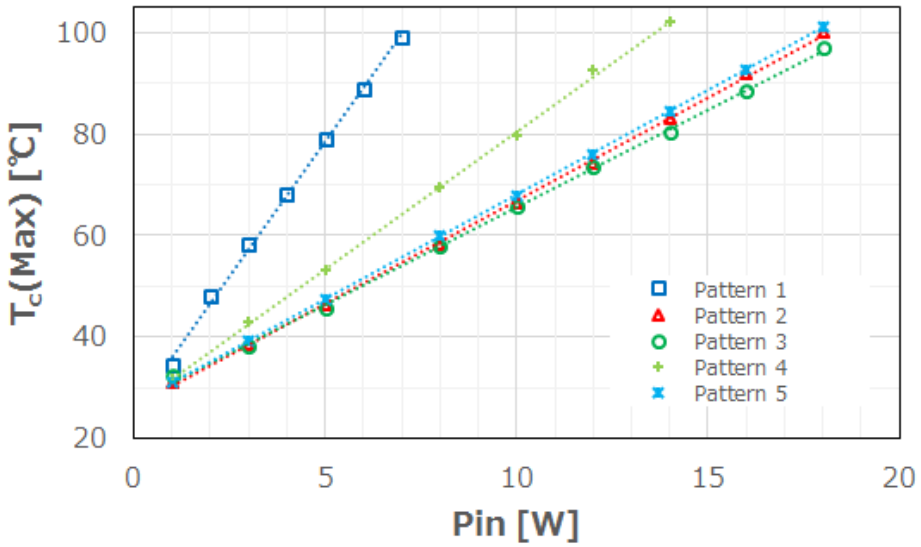



Fig.4-6: $T_c$ (Max)-Pin Characteristics

Fig.4-7 shows the Drain Pad via number-$T_c$(Max) at Pin=14W.

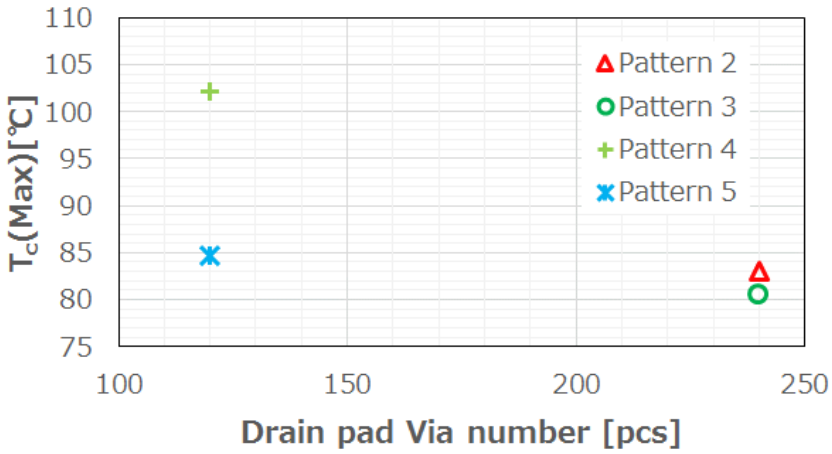



Fig. 4-7: $T_c$(Max) @Pin= 14W-Drain Pad Via number

The number of drain pad via in Pattern 2 is 240 pcs. The number of drain pad via in Pattern 5 is 120 pcs. Even the number of drain pad via doubles, Tc reduction is only 1.6°C@Pin=14W, which means the heat dissipation by increasing the number of thermal via is saturated.

Patterns 4 and 5 are large and small patterns of drain pad size at the same number of drain via (120pcs), we found that Pattern 5 with larger drain pad has 17.5°C @ Pin = 14 W lower Tc than Pattern 4.

On the other hand, in order to expand the drain pad size for practical use, it is necessary to consider securing the creepage distance with other components and patterns in the board, and you need to design the pattern considering heat dissipation and space.

### 4.2.4. Design Guideline for PCB for TOLL package

As a guideline for designing pads and thermal via for TOLL package PCB board based on the evaluation of heat dissipation in 4.2.3

- Ensure large drain pads within the space and creepage distances allowed
- It is better to increase the number of thermal via. However, it is necessary to determine the minimum number of thermal vias required because the heat dissipation effect is saturated.
- The arrangement of the source pad thermal via is also effective in improving heat dissipation.

And so on.

Please understand that our evaluation results of heat dissipation in this time only show the tendency of heat dissipation, and that the absolute value changes depending on the composition of the board, conditions, size of the heat sink, etc.

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