High-power device
Press Pack IEGT(PPI)
Application note

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1. Structure and Features of IEGT

1.1. Press Pack IEGT (PPI)

Press pack IEGT is a pressure contact type high power device with built-in IEGT (Injection Enhanced Gate Transistor (electron-injection-enhanced insulated gate transistor). Figure 1.1 is the structural drawing of the press pack IEGT. All electrical connections use press pack. Since wire bonding connections are not used, high reliability against thermal fatigue can be expected. Using several series connections of PPIs ensures uninterrupted operation of the equipment even when the product fails due to electrical damage. This is because the collector and the emitter electrodes will be short-circuited. Using a double-sided heat dissipation structure can cool down both the collector and the emitter sides. The device has high moisture resistance due to its hermetic sealing structure in a ceramic and metal enclosure, so it can be directly immersed in cooling liquid for efficient cooling. The following are the features of the press pack IEGT.

- Electrical connections using press pack
  IEGT chips are arranged on the same plane and are then uniformly pressed from both sides using a molybdenum plate. Each of collector and emitter electrodes of the chip comes into contact with the copper electrode via the molybdenum plate when mechanical pressure is applied. This makes electrical connections and allows heat dissipation.

- High reliability due to a hermetic sealing structure
  Inert gas is hermetically sealed inside the device to prevent degradation of the electrode surface due to oxidation, ensuring high thermal reliability for PPIs.

- Outstanding parallel operation technology
  The wiring inside the gate terminal plate is designed to operate a number of parallel-connected IEGT chips consistently so that they do not interfere with each other and oscillate during switching.

- Rupture-resistant package structure
  The resin-frame structure that guides the IEGT chip makes the package less prone to rupture even if a chip is melted and destroyed during a switching operation.
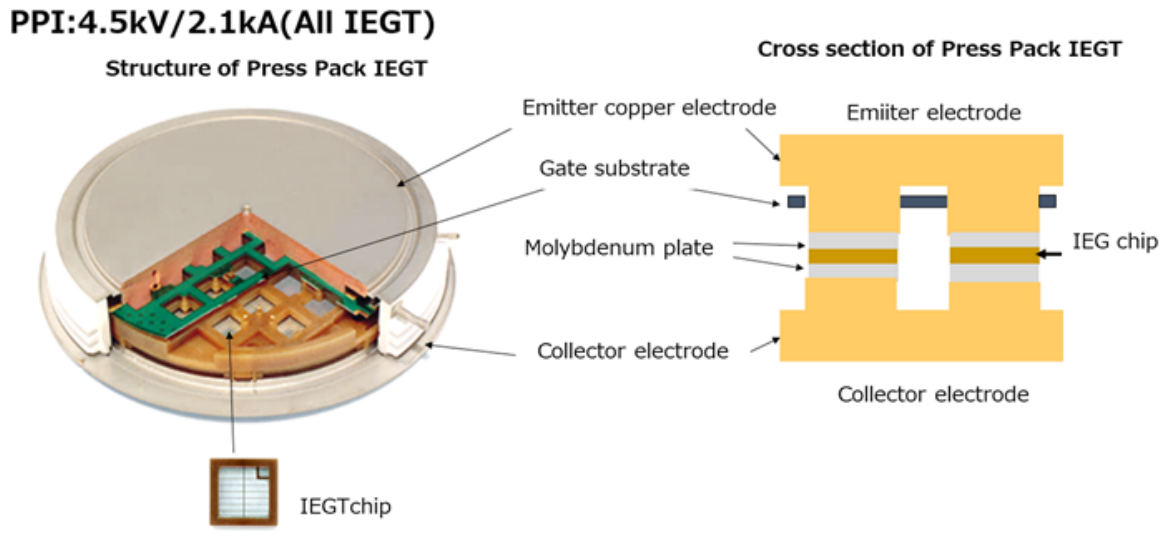
PPI:4.5kV/2.1kA(All IEGT)

Structure of Press Pack IEGT

Cross section of Press Pack IEGT

Figure 1.1 Construction of Press Pack IEGT

1.2. Structure and Features of IEGT

IEGT is a voltage-driven power device for switching high current. To enhance the withstand voltage of an IGBT, the on-state voltage will sharply increase. In IEGT, devising the device structure on the emitter side has solved the problem, thereby achieving low on-state voltage characteristics. The basic structure and equivalent circuit of an n channel IGBT that is a base of IEGT are shown in Figure 1.2. The structure is similar to MOSFET. The basic difference is that it adopts a p^+-n^+- n^- substrate whereas MOSFET uses an n^+-n^- substrate. Therefore, its manufacturing processes after the substrate process are basically the same as for MOSFET.

On the equivalent circuit, a thyristor is formed by PNP-NPN transistor coupling. However, as shown in the structure diagram, the base and emitter of the NPN transistor are short-circuited with Al wiring and are designed to operate as little as possible. The thyristor does not normally affect IGBT's basic operation. Hence, the equivalent circuit and operating mechanism of the n-channel IGBT can be considered as the same as the MOS input inverted Darlington with the n-channel enhancement-type MOSFET at the input stage and the PNP transistor at the output stage.

However, the IGBT features are not just limited to the behaviors described for the equivalent circuit. Another important feature is the conductivity modulation of the n^- edge region due to the monolithic configuration of the MOSFET and the PNP transistor. Conductivity modulation (decrease in MOSFET drain resistance) is induced in the n^- layer by holes (minority carriers) injected from the p^+ - n^+ layer into the n^- layer. With this conductivity modulation mechanism, the IGBT can obtain low saturation voltage characteristics, which were difficult to obtain from the high withstand voltage MOSFET.

IGBT's saturation voltage Vce(sat) from the equivalent circuit can be expressed as follows:

$$V_{ce(sat)} = V_{BE} + I_{MOS}[R_{N-(MOD)} + R_{ch}]$$

In addition, the relationship of the current between the MOSFET and the PNP transistor can be expressed as

$$I_{MOS} = I_{IGBT} / (hFE+1)$$

The PNP transistor's hFE strongly affects the trade-off relationship between the saturation voltage and the switching characteristics of the IGBT.
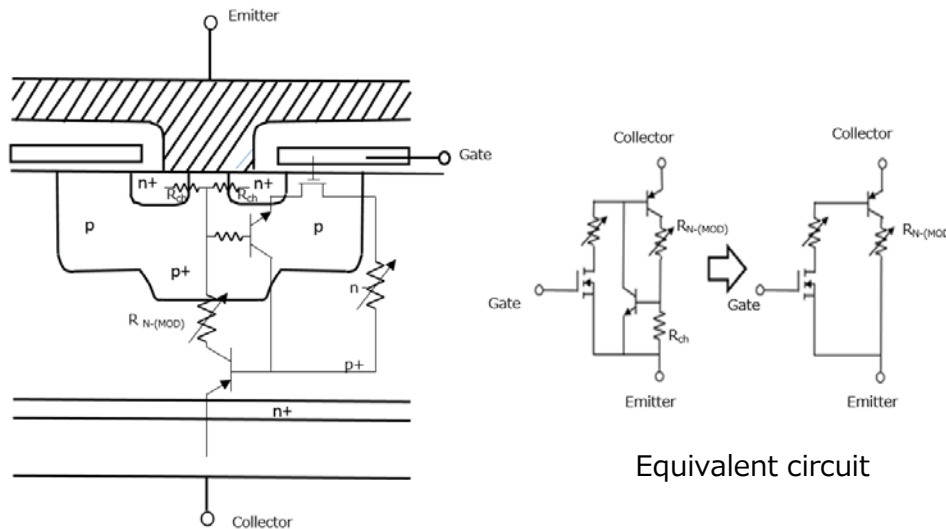

Equivalent circuit

Figure. 1.2 Basic structure of IGBT and equivalent circuit

The features of IEGT are as follows. In addition to high withstand voltage and low on-resistance, it also has excellent cutoff current capability and high breakdown tolerance, so it contributes to energy saving and miniaturization and efficiency of equipment.
It demonstrates its performance in industrial fields that support social infrastructure such as motor drive equipment and power converters. Press Pack IEGTs are available and can be selected according to the power capacity and load characteristics of the application.

- High withstand voltage, low on-resistance
- Wide safe operating area equivalent to IGBT (high di/dt, dv/dt tolerance)
- Simplification and miniaturization of drive circuit by voltage drive
- High-speed switching operation

1.3. Cross-section structure of IGBT and Problems with high voltage resistance

Figure. 1.3 shows the cross-section structure of a conventional IGBT and its carrier distribution in the n⁻ base. The carrier distribution decreases monotonically from the collector electrode side to the emitter electrode side. To enhance voltage resistance, it is necessary to widen the n⁻ base region between the collector and the emitter, so the region of minority carriers becomes thick and increases resistance, thus increasing the voltage drop. There was a

problem that the on-state voltage was higher.

1.4. Features of the Gating Structure of IEGT and IE-Effect

Figure 1.4 shows the cross-section structure and carrier distribution of an IEGT. Compared to IGBTs, the IEGT has deep and wide trench gate electrodes, which increase the carrier density inside the device and prevent carriers from passing to the emitter electrode. Consequently, carrier accumulation occurs and n⁻ base carrier distribution increases on the emitter electrode side. Since this has the same effect as carrier injection and accumulation, it is called the Injection Enhancement (IE) effect. With this gate structure adopted, it is now possible to suppress an increase in voltage drop even while enhancing voltage resistance.

　* Another structure which can produce a similar effect is currently being developed and adopted.
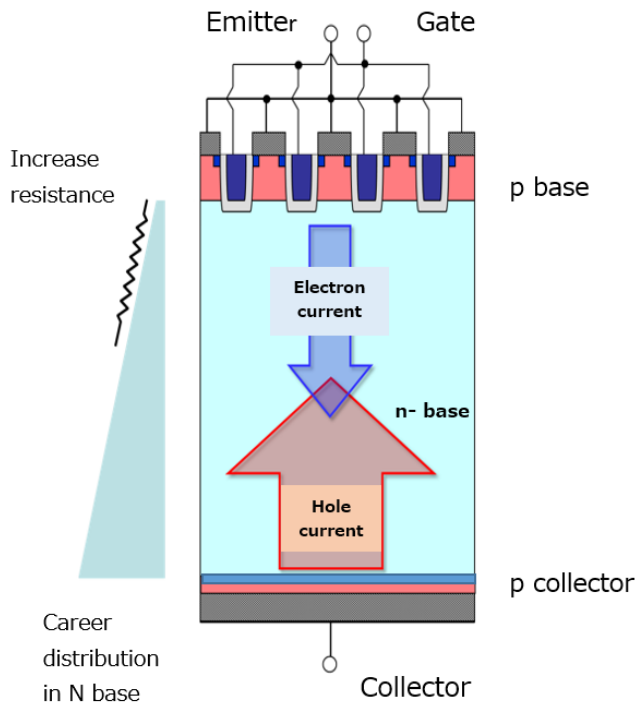

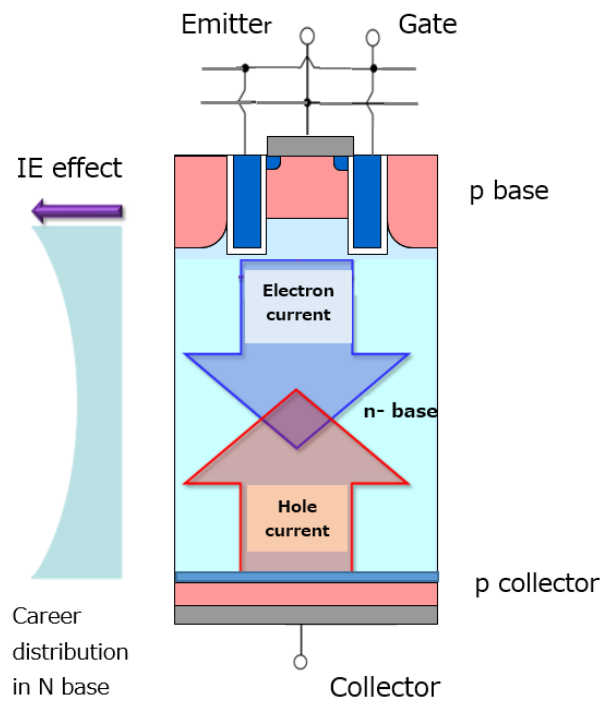**Figure. 1.3 IGBT Chip cross-section and carrier profile**

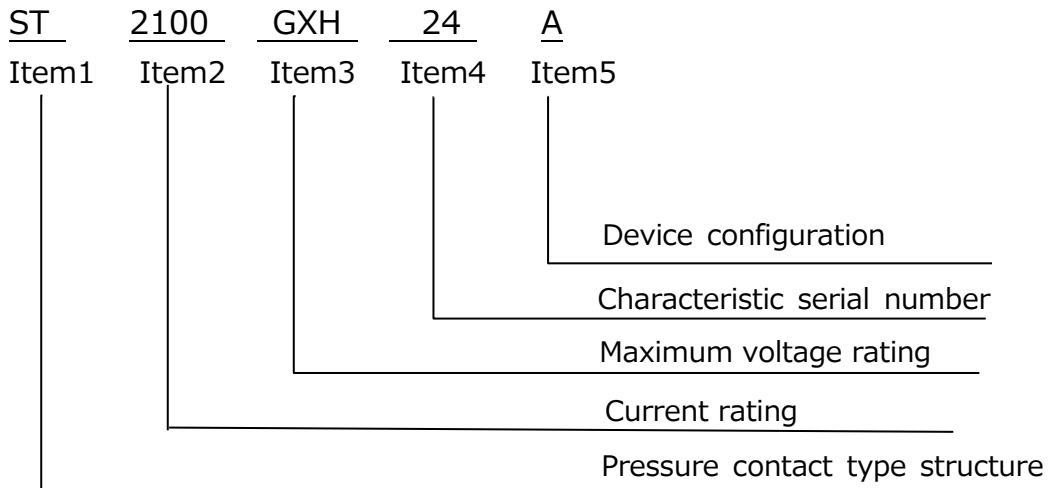**Figure. 1.4 IEGT Chip cross-section and carrier profile**

2. Terms and Characteristics

The properties of the Press Pack IEGT are shown in ST2100GXH24A and 1500GXHH24, and the data given in the technical data are described below.

Type

The Press Pack IEGTs (PPIs) are constructed as follows:

Product containing IEGT

ST	2100	GXH	24	A
Item1	Item2	Item3	Item4	Item5

Device configuration

Characteristic serial number

Maximum voltage rating

Current rating

Pressure contact type structure

Diode product

1500	GXH	H	24
Item1	Item2	Item3	Item4

Characteristic serial number

H: Diode

Maximum voltage rating

Current rating
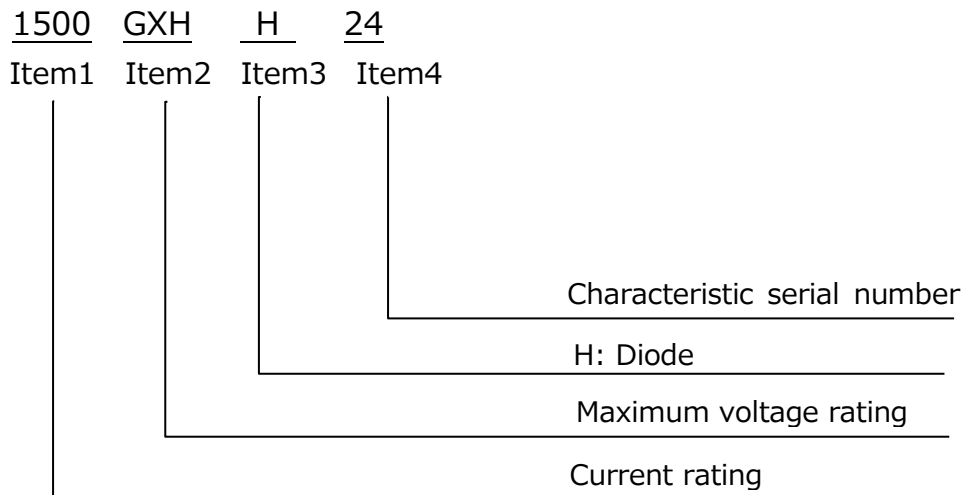
The meanings of the Item 2 or 3 is as follows.

Characters of Item2 or 3	Maximum Voltage(V)
FXF	3300
GXH	4500
JX	6000
JXH	6500

The explanation of the Item5 of the device including IEGT is as follows.

A: It is equipped with IEGT chips. Freewheeling diode with
anti-parallel connection not mounted

R: It is equipped with a RC-IEGT chips.

Without symbol: A freewheeling diode connected in anti-parallel
with IEGT is installed inside.

2.1. Meaning of Characteristic Data

Press Pack IEGTs are all built-in IEGT type, type with built-in IEGT and freewheeling diode (FWD), and type with all built-in freewheeling diode. The loss when the devices are in the ON state of IEGT and of FWD respectively is called the conduction loss, and the loss that occurs at the moment when the device change from ON to OFF or from OFF to ON state is called the switching loss.

The data related to conduction loss are I_C-V_{CE}, and I_F-V_F.

The data related to switching loss is E_{on}-I_C, E_{off}-I_C, E_{rr}-I_F, E_{on}-$R_{G(on)}$, E_{off}-$R_{G(off)}$, E_{rr}-$R_{G(on)}$.

The data required to design the capacitance of IEGT drive circuit are C_{ies}, C_{oes}, C_{res}-V_{CE}, V_{GE}-Qg, and the data related to the timing of the ON signal input to the drive circuit are $t_{d(on)}$, t_{on}, t_r t_{rr}.

The data related to heat dissipation design is $R_{th(j-f)-t}$.
The data related to the mode which is destroyed by the loss by surge voltage generated at the moment when IEGT turns OFF is RBSOA, and the data related to the breakdown strength in the reverse-recovery operation of FWD is called RRSOA.

2.2. How to Read Data

(1) I_C-V_{CE}

Figure.2.1 shows the relationship between the C-E current (I_C) and the voltage drop between the collector and emitter (V_{CE}) when +15 V is applied between the gate and emitter and the device is turned ON. The on-state power loss (P_{sat}) when the device is ON can be calculated by multiplying the supplied current I_C and the voltage drop (V_{CE}) for operating time. Since the device temperature rises during operation, use the curve for T_j= 125°C or 150°C to calculate the power.

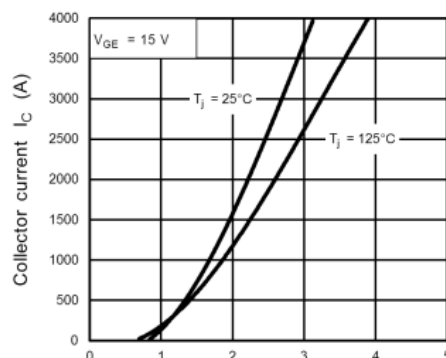**Figure 2.1 I_C vs. V_{CE} Characteristics**

(2) Output characteristics

As I_C-V_{CE} characteristics, collector-emitter voltage is measured by holding T_j=150°C or T_j=125°C and varying I_C by sweeping the gate-emitter voltage (V_{GE}) as Figure2.2. This data is used to determine the V_{GE} voltage necessary to lower the conduction loss under an I_C condition.
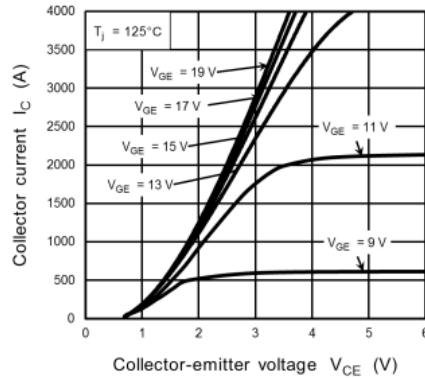
Figure 2.2 Output Characteristics

(3) IF-VF

Figure. 2.3 shows the voltage drop between the anode and cathode when forward current (I_F) is applied to the FWD. As with I_C-V_{CE} property, the FWD conduction loss (P_F) can be calculated.

Figure. 2.3 I_F-V_F Characteristics

(4) E_{on}-I_C

Figure 2.4 shows a simplified circuit when IEGT is switched, and Figure 2.5 shows a simplified waveform of each part.

Figure 2.4 Inductive load switching measurement circuit diagram

Figure 2.5 Timing Chart (IEGT Section)

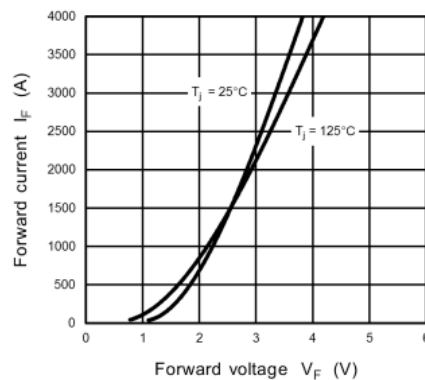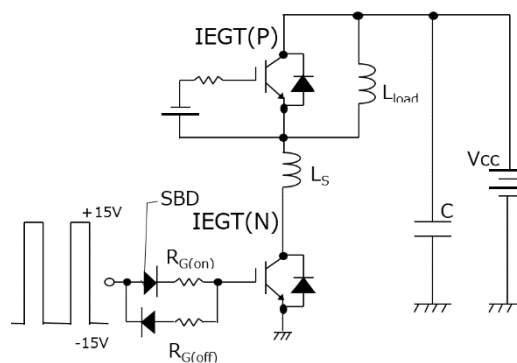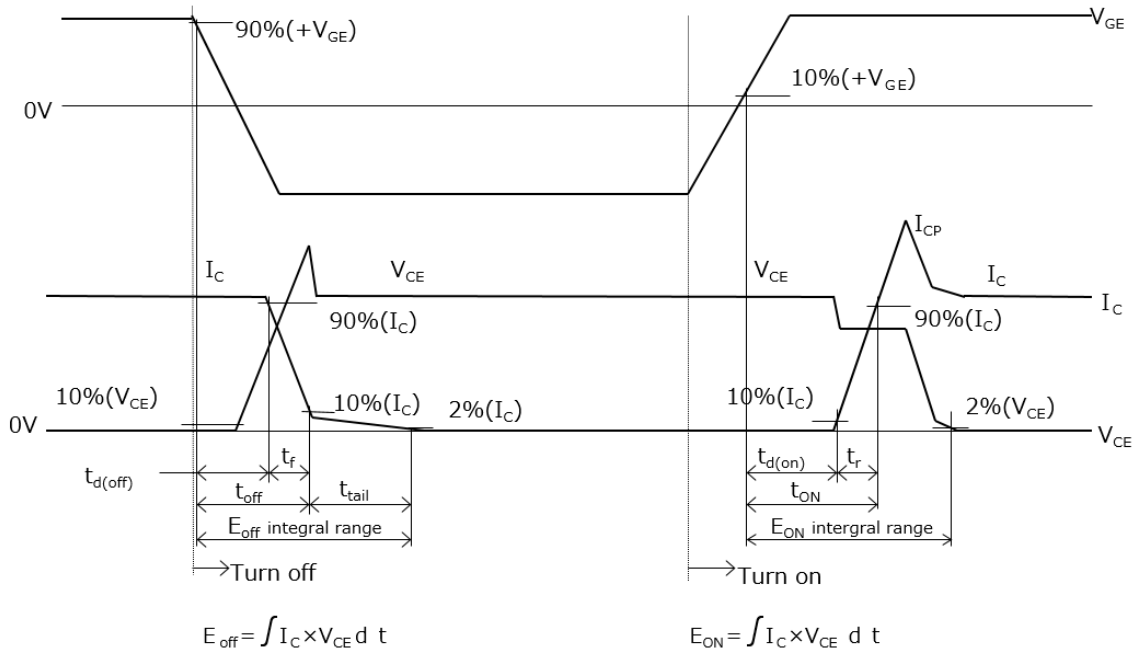E_{ON} shows the power loss generated when the elements in Fig. 2.4 are turned ON. The integrated energy is obtained by the period in which the product of the current waveform (I_C) and voltage waveform (V_{CE}) in Fig. 2.5 is described as E_{ON} integral range.

Figure 2.6 shows the data obtained by varying I_C. Turn-on power loss (P_{ON}) can be calculated by obtaining the E_{ON} for an I_C and then multiplying this value by the operating frequency.

Figure 2. 6 E_{ON}-I_C Characteristics

E_{off} shows the power loss generated when the elements in Fig. 2.4 are turned OFF. The integrated energy is obtained by the period in which the product of the current waveform (I_C) and voltage waveform (V_{CE}) in Fig. 2.5 is described as E_{off} integral range.

Figure 2.7 shows the data obtained by varying I_C. Turn-on power loss (P_{off}) can be calculated by obtaining the Eon for an I_C and then multiplying this value by the operating frequency.
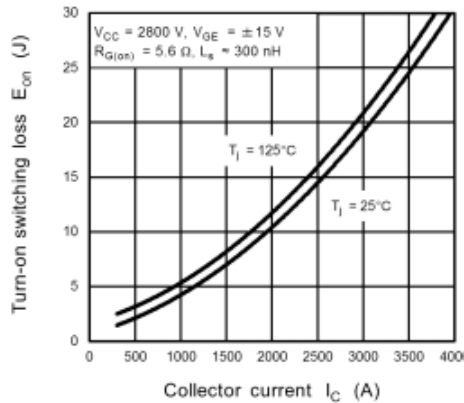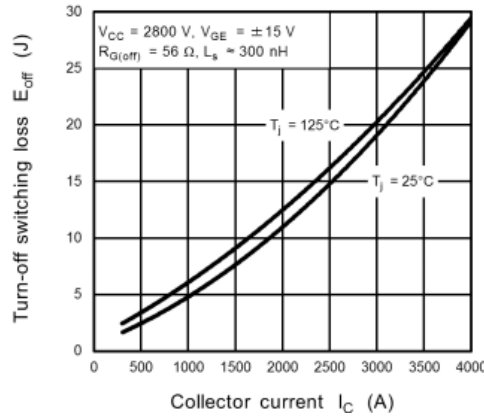
Figure 2. 7 E_off-I_C Characteristics

(5) $E_{rr(E_{dsw})}$-I_F

Figure 2.8 shows a simplified waveform for each part when using an FWD while it is switching. E_{rr} is the energy integrating the product of the current waveform (I_F) and the voltage waveform (V_r) during the period specified as E_{rr} integral range in Figure 2.3. E_{rr} data is provided for various I_F as Figure2.9. The FWD switching loss (P_{rr}) can be calculated by obtaining E_{rr} under the IF condition and then multiplying this value by the operating frequency.
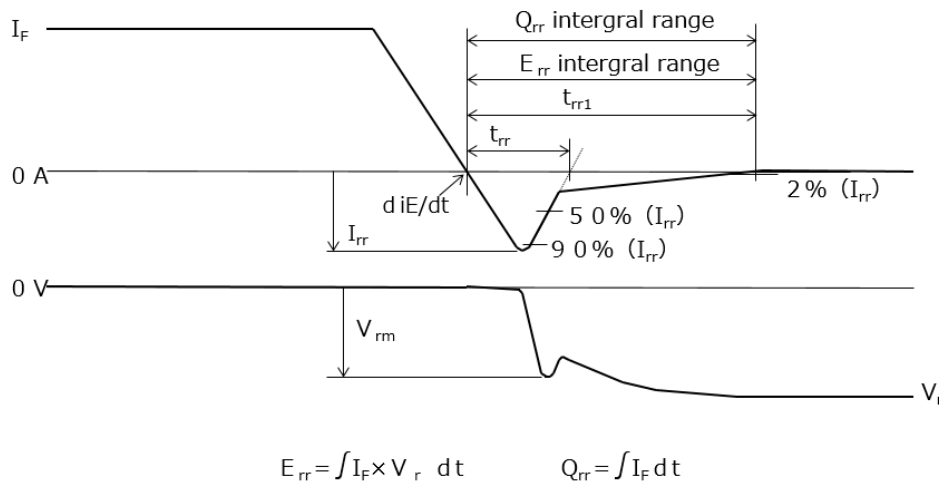

$$E_{rr} = \int I_F \times V_r \; dt \qquad Q_{rr} = \int I_F dt$$

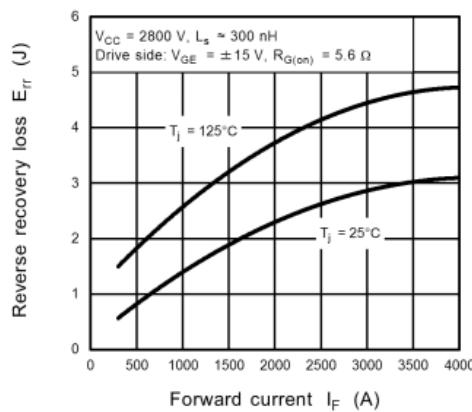**Figure 2.8 Timing Chart (FWD)**

Figure 2.9 E_rr-I_F Characteristics

(6) E_{on}-$R_{G(on)}$, E_{off}-$R_{G(off)}$, E_{rr}-$R_{G(on)}$

E_{on}, E_{off}, E_{rr} can be varied by $R_{G(on)}$ or $R_{G(off)}$ shown in Figure 2.4 and the values are shown in Figure 2.10, Figure 2.11 and Figure 2.12.

In IEGT, varying the drive circuit R_G changes switching time, switching loss, and surge voltage generated at switching time. However, the switching time and the switching loss are in conflict with the surge voltage. Therefore, consider this point to determine the optimum R_G value.
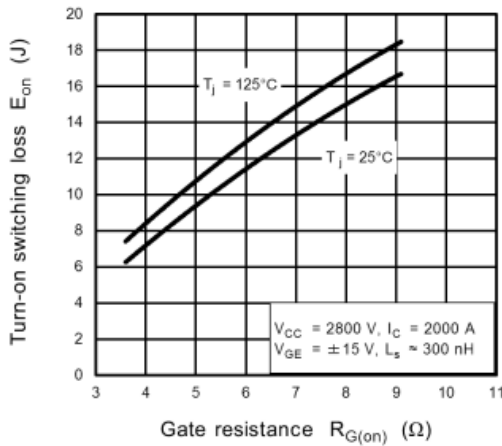
Figure 2.10 Characteristics of E_{on}-$R_{G(on)}$
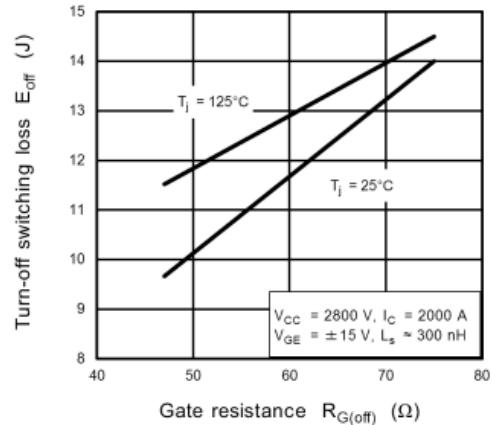
Figure 2.11 Characteristics of E_{off}-$R_{G(off)}$
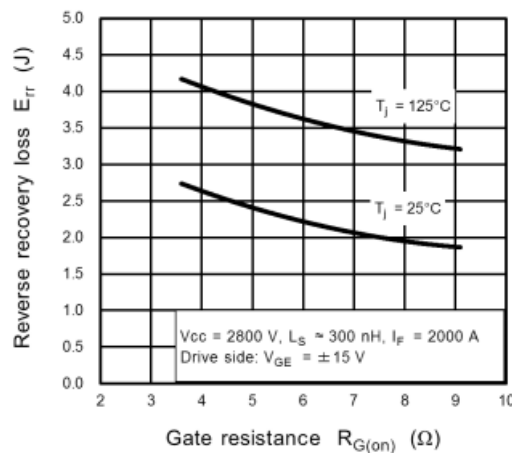
Figure 2.12 of E_{rr}-$R_{G(on)}$ Characteristics

(7) V_{GE}-Q_g

Figure 2.13 shows the amount of input charge required to design an IEGT gate drive circuit. The characteristics show the change of gate-emitter voltage (V_{GE}) relative to the gate input charge value (Q_g). This indicates the charge amount of gate capacitance needed to turn on the IEGT. To calculate the current supply capability required for the drive circuit, obtain from this figure the charge amount Q_g until V_{GE} obtained in (2), and then multiply it by the switching frequency.
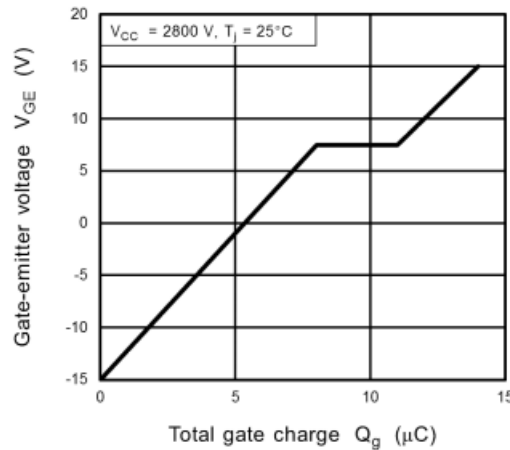
Figure 2.13 V$_{GE}$-Q$_g$ Characteristics

(8) C$_{ies}$, C$_{oss}$, C$_{res}$ - V$_{CE}$

IEGT has a junction capacitance between the gate and emitter, between the collector and emitter, and between the collector and gate. Specifically, C$_{ies}$ is the input capacitance between the gate and emitter, C$_{oes}$ is the output capacitance between the collector and emitter, and C$_{res}$ is the feedback capacitance between the collector and gate. Figure 2.14 shows the capacitance when the voltage V$_{CE}$ between the collector and emitter is changed. It should be used in conjunction with V$_{GE}$-Q$_g$ features for designing the drive-circuit.
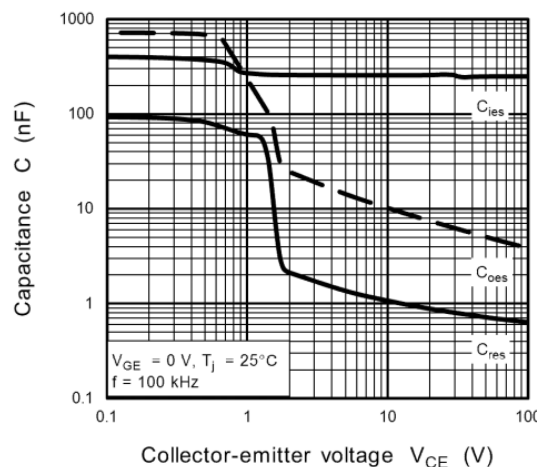
Figure 2.14 C$_{ies}$, C$_{oss}$, C$_{res}$-V$_{CE}$ Characteristics

(9) t$_{d(on)}$, t$_r$, t$_{d(off)}$, t$_f$-I$_c$, and t$_{rr}$, I$_{rr}$-I$_F$

Figure 2.15 and Figure 2.16 show the current dependences of the items defined in Figure 2.5 and Figure 2.8. When IEGTs connected in series are turned on and off, if they are turned on at the same time, excessive through current flows from the main power supply to the device. This may result in heat generation due to an increase in dissipation or the possibility of a breakdown in the worst case. Therefore, it is necessary to provide a pause period in which neither element is turned on. This data is used to design the timing of the input signal to each element.
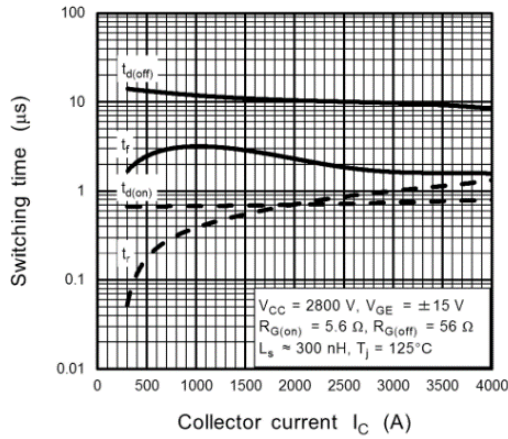
Figure 2.15 $t_{d(on)}$, t_r, $t_{d(off)}$, t_f-I_c Characteristics
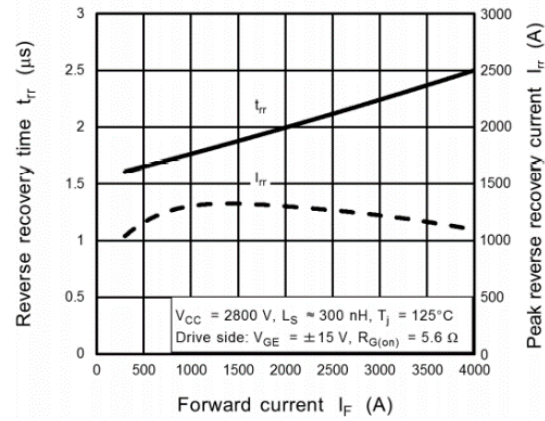
Figure 2.16 t_{rr}-I_{rr}-I_F Characteristics

(10) $R_{th(j-f)-t}$

Figure 2.17 shows the data which is used for thermal design. In general, when power (P_C) is applied during application time (t), rise in chip temperature is $R_{th(j-c)(t)}$ x P_C. However, since the waveform of the actual power applied is complicated, a detailed explanation will be discussed later. $R_{th(j-f)}$ is the thermal resistance between the junction and the cooling-fin of the press pack IEGT and includes the thermal resistance of the conductive thermal compound.
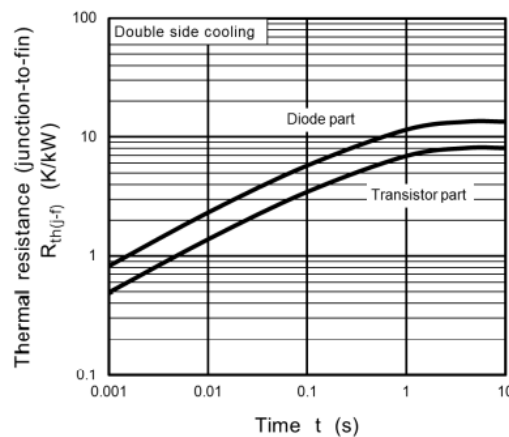
Figure 2.17 $R_{th(j-f)-t}$ Characteristics

(11) RBSOA

A surge voltage is generated in the device due to stray inductance of the circuit at the moment the IEGT changes from an ON to an OFF state. Here, the cutoff current in OFF state and the surge voltage generated at that time are expressed as Locus. Figure 2.8 shows the area where the device does not break. It is necessary to design so that Locus of the turn-off waveform stay within the acceptable area (by lowering circuit stray inductance, adding a surge absorption circuit, or relaxing turn-off speed).
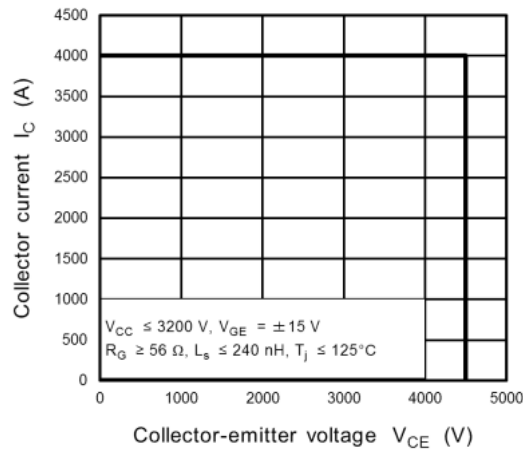
Figure 2.18 RBSOA Characteristics

(12) RRSOA

Figure 2.19 shows the safe operating area for the reverse recovery current at FWD reverse recovery operation (see Figure 2.8) and the device's collector-emitter voltage generated at that time. It is necessary to design so that the FWD's waveform in use during the reverse recovery operation stay within this area (by reducing circuit stray inductance, relaxing di/dt by relaxation of turn-on time, and so on).

Figure 2.19 RRSOA Characteristics

2.3. Absolute Maximum Rating

Do not exceed the absolute maximum rating value in any case. In addition, using the product under marginal conditions may affect reliability (device life) although each value is below the absolute maximum rating. Therefore, read TOSHIBA Semiconductor Reliability Handbook and derate the device accordingly.

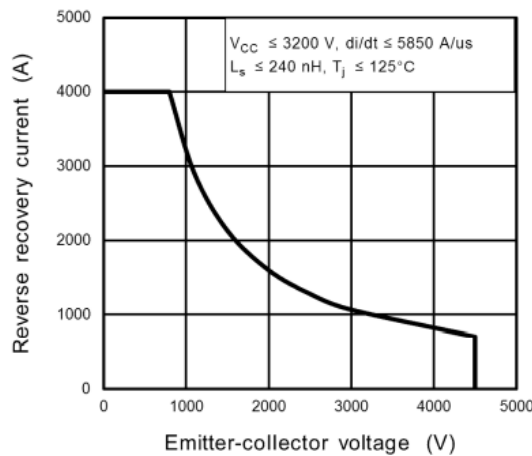| Item	Symbol	Definitions and Contents (Refer to the individual datasheet of each product for guaranteed values.)
Collector-emitter voltage	V_{CES}	This is the maximum voltage that can be applied between the collector and the emitter in a zero bias state between the gate and emitter (when the gate and emitter are short-circuited). It is necessary to decide the allowable value of the surge voltage so that the breakdown voltage due to the surge generated during actual use is lower than the V_{CES} value by referring to the RBSOA and RRSOA data of each device.
Gate-emitter voltage	V_{GES}	This is the maximum voltage that can be applied between the gate and the emitter in a zero bias state between the collector and emitter (when the collector and emitter are short-circuited). However, even if a voltage less than V_{GES} is applied, applying voltage for long periods may affect the lifetime of the IEGT gate oxide film. Take this point into consideration.
Collector current	I_C	This is the maximum DC current allowed for the collector current. However, the maximum may be limited due to power dissipation and heat dissipation conditions of the device. Use the device under conditions that do not exceed the maximum junction temperature Tj.
	I_{CP}	This is the maximum pulse current allowed for the collector current. However, the maximum may be limited due to power dissipation and heat dissipation conditions of the device. Use the device under conditions that do not exceed the maximum junction temperature Tj
	I_F	This is the maximum allowable DC current for freewheeling diode. However, the maximum may be limited due to power dissipation and heat dissipation conditions of the device. Use the device under conditions that do not exceed the maximum junction temperature Tj
Collector current	I_{FP}	This is the maximum pulse current allowed for freewheeling diode. However, the maximum may be limited due to power dissipation and heat dissipation conditions of the device. Use the device under conditions that do not exceed the maximum junction temperature Tj.

Item	Symbol	Definitions and Contents(Refer to the individual data sheet of each product for guaranteed values)
Collector power dissipation	P_C	This is the maximum power dissipation allowed for a single device. However, the guaranteed value is the ideal theoretical value when the case temperature of the device is fixed at 25°C. Derating is needed under limited heat dissipation conditions for practical use. (For more details, refer to the explanation on thermal design.)
Junction temperature	T_j	This is the maximum value of chip junction temperature that can operate normally. Since junction temperature affects reliability, it should be taken into consideration in design. For more details, refer to the Reliability Handbook
Operating junction temperature	$T_{j(opr)}$	This is the maximum value of chip junction temperature that can operate normally with continued operation. Since junction temperature affects reliability, it should be taken into consideration in design. For more details, refer to the Reliability Handbook
Storage temperature	T_{stg}	This is the guaranteed temperature range when storing or shipping a device without subjecting it to electrical load.

2.4. Electrical Characteristics

Item		Symbol	Definitions and Contents(Refer to the individual data sheet of each product for guaranteed values)
Static characteristic	Collector-emitter cut-off current	I_{CES}	This is the collector current value that flows when the gate and emitter electrodes are short-circuited and the specified voltage is applied between the collector and the emitter. Since it increases with temperature, it should be considered as loss if necessary.
	Gate leakage current	I_{GES}	This is the gate current that flows when the collector and the emitter electrodes are short-circuited and a specified voltage is applied between the gate and the emitter. Since this is a leakage current through the gate oxide, the increase due to temperature increase is small.
	Gate-emitter cutoff voltage	$V_{GE(off)}$	This is the gate-emitter applied voltage value for a specified collector current to flow when applying a specified collector-emitter voltage. When surge voltage exceeding this value occurs between the gate and emitter, the device may be erroneously turned ON. Therefore, the surge voltage should be checked in design.

Item		Symbol	Definitions and Contents (Refer to the individual data sheet of each product for guaranteed values)
Static characteristic	Collector-emitter saturation voltage	$V_{CE(sat)}$	This is the voltage value between the collector and the emitter when a specified voltage is applied between the gate and the emitter while a specified current flows through the collector. Since it is an important characteristic affecting the static loss of the device, the voltage should be applied below V_{GES} to keep this value sufficiently low and stable.
	Input capacitance	C_{ies}	This is the capacitance between the gate and emitter when specified voltages are applied between the collector and the emitter and between the gate and the emitter with the collector-emitter short-circuited in an AC manner.
	Output capacitance	C_{oes}	This is the capacitance between the collector and the emitter when a specified voltage is applied between the collector and the emitter and between the gate and the emitter with the gate-emitter short-circuited in an AC manner.
	Feedback capacitance	C_{res}	This is the capacitance between the collector and the gate when a specified voltage is applied between the gate and the emitter while the emitter is grounded.
	Diode forward voltage	V_F	This is the voltage between the anode and the cathode when a specified forward biased current is applied to the freewheeling diode connected in reverse-parallel between the IEGT collector and the emitter. It is an important characteristic affecting the conduction loss of a device.
Dynamic characteristic	Turn-on delay time	$t_{d(on)}$	When the IEGT is turned on, this is the time interval from the time when the gate voltage is at 10% of its setting to the time when the collector current reaches 10% of its setting.
	Rise time	t_r	When the IEGT is turned on, this is the time interval during which the collector current changes from 10% to 90% of its setting.
	Turn-on time	t_{on}	When the IEGT is turned on, this is the time interval from the time when the gate voltage is at 10% of its setting to the time when the collector current reaches 90% of its setting.
	Turn-off delay time	$t_{d(off)}$	When the IEGT is turned off, this is the time interval from the time when the gate voltage is at 90% of the maximum setting to the time when the collector current reaches 90% of the setting.
	Fall time	t_f	When the IEGT is turned off, this is the time interval during which the collector current changes from 90% to 10% of its setting.

	Item	Symbol	Definitions and Contents (Refer to the individual data sheet of each product for guaranteed values)
Dynamic characteristic	Turn-off time	t_{off}	When the IEGT is turned off, this is the time interval from the time when the gate voltage is 90% of its maximum setting to the time when the collector current reaches 10% of its maximum setting on the tangent of the falling current.
	Reverse recovery current	I_{rr}	This is the minimum value of the reverse recovery current of the FWD connected in reverse-parallel between the IEGT collector and the emitter.
	Reverse recovery time	t_{rr}	This is the time interval from the time when reverse recovery current of the FWD, connected in reverse-parallel between the IEGT collector and emitter, is 0 A to the time when reverse recovery current reaches the minimum current value Irr and then the tangent of 90% to 50% of Irr, which is again returning toward 0 A, becomes 0 A.
	Reverse recovery charge	Q_{rr}	This is the FWD charge amount (the time-integral value of the reverse recovery current) for the period when the reverse recovery current of the freewheeling diode, which is connected in reverse-parallel between the collector and the emitter of the IEGT, reaches the minimum current value (I_{rr}) from 0 A, and then the reverse recovery current, again returning toward 0 A, becomes 2%.
	Turn-on switching loss	E_{on}	When the IEGT is turned on, this is the integral value of the product of the collector current and the collector voltage for the period from the time when the gate voltage is at 10% of its setting to the time when the collector voltage reaches 2% of its setting value.
	Turn-off switching loss	E_{off}	When the IEGT is turned off, this is the integral value of the product of the collector current and the collector voltage for the period from the time when the gate voltage is at 90% of the maximum setting to the time when the collector current reaches 2% of its setting.
	Reverse recovery loss	Err (E_{dsw})	This is the integral value of the product of the reverse recovery current and the voltage applied to FWD for the period from the time when the reverse recovery current of the FWD, which is connected in reverse-parallel between the collector and the emitter of the IEGT, is 0 A to the time when the reverse recovery current reaches the minimum current value (Irr) and then the reverse recovery current, which is again returning toward 0 A, becomes 2% of Irr.

Item	Symbol	Definitions and Contents (Refer to the individual data sheet of each product for guaranteed values)
Gate charge	Q_g	This is the amount of electronic charge that needs to be supplied to the gate in order to turn the IEGT on. (When turning the IEGT off, the same amount of discharge is required.)
Thermal resistance (junction-to-fin)	$R_{th(j-f)}$	This is the saturated thermal resistance between the junction and cooling fin in one device of the IEGT or FWD equivalent circuit.

3. When Using Semiconductor Products

3.1. IEGT Device Selection

(1) Voltage rating

The voltage rating of IEGT elements must take into account the incoming power source of the applied device and its stability, as well as the circuit constants used. Select an element according to the purpose. Generally, at steady state,

- Peak voltage: 80% or less of the device rating (V_{CES})
- DC voltage: 50 to 60% of device rating (V_{CES})

It is recommended to use it at 90% or less of the element rating (V_{CES}) even in non-stationary conditions. The relationship between the device voltage rating and the power supply voltage (input AC line voltage) when an inverter is applied is summarized in the following equation.

Device rated voltage (V_{CES}) = [Input voltage] + [Surge voltage] + [Voltage variation] + [Margin]

- Input voltage: multiply by $\sqrt{2}$ for alternating current
- Surge voltage: Maximum value of spikes due to circuit inductance, etc.
- Voltage fluctuation: Voltage rise caused by power regeneration, etc.
- Margin: Safety factor

(2) Current rating

When the collector current of IEGT device increases, $V_{CE(sat)}$ increases and the generated conduction loss increases. At the same time, the switching loss also increases, which increases the heat generation of the device.

When using the IEGT device, the junction temperature (T_j) of IEGT and FWD should be less than the maximum junction temperature T_j(max). Improper selection may cause device damage or deterioration of the device's long-term reliability.

The overload value is often set for inverter applications. Therefore, the following settings are considered safe:

- Steady state: 50 to 60% or less of the device rated current
- Unsteady state (maximum): Within the rated current of the device (the junction temperature should also be less than the maximum junction temperature)

Note that the 1ms rated current (Icp) in the device specification is the peak value, which includes the recovery current at the time of the reverse recovery of the freewheeling diode, and the value when an accident causes various protection operation. (It cannot be used repeatedly, exceeding the maximum junction temperature as described above.)

The following equation can be used to select the current for general inverter applications.

Peak current (Ip) =[inverter capacity] × [overload ratio]/[AC voltage]/$\sqrt{3}$ × $\sqrt{2}$
$\qquad\qquad\qquad$ × [current ripple ratio]
Element rated current (Ic) = Ip/derating rate

- Inverter capacity: Output load (W) / Efficiency
- AC Voltage: RMS

However, the selection of the rated current depends on the operating and heat dissipation conditions of the equipment. Select the current rating after checking the loss and temperature rise caused by the equipment.

3.2. Electrostatic Discharge and Gate Protection

The V_{GE} guaranteed value of the IEGT device is generally ± 20 V maximum (refer to the guaranteed value in the technical datasheet). The IEGT gate may malfunction if a voltage exceeding the V_{GES} guaranteed value is applied between G-E of IEGT. Make sure that the voltage does not exceed the guaranteed value between G-E.

Also, since the IEGT gate requires handling even against static electricity and other charges, use the product with caution by complying with the following handling precautions:

(1) When handling IEGT, discharge static electricity from the human body and clothing by using anti-static straps, etc. and work on grounded conductive mats.
(2) Handle an IEGT device with its package body. Do not touch the collector and emitter electrodes directly without gloves.
(3) When connecting and fixing wiring parts and materials (bus bars, wires, etc.) to the

IEGT terminal, make sure that the material used is not charged to avoid static electricity being applied to the IEGT as in item (1).

(4) The IEGT device is shipped with electrostatic countermeasures between G-E with conductive materials like copper wire, copper tape, IC foam, etc. Remove this conductive material immediately before electrically wiring the product.

In addition, the IEGT may be damaged if voltage is applied between the collector and the emitter while the gate-emitter is in the OPEN state. This is caused by the events that the collector potential changes, the gate potential rises after current (i) flows as shown in Figure 3.1, then the IEGT turns on, and the collector current flows. Consequently, when a product is incorporated into the equipment, the IEGT may be damaged if voltage is applied to the main circuit with a failed gate circuit or if a gate circuit is not operating normally (gate is in the open state). To prevent this damage, it is recommended to add a protection circuit. For example, when the gate circuit power supply is not turned on, the protection circuit short-circuits between the gate and the emitter. Or it prevents the main circuit from being charged without making sure that the gate circuit power supply is ON (the gate and the emitter are negatively biased).
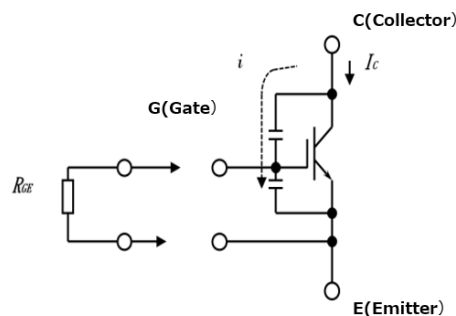
Figure 3.1 Behavior of IEGT when G-E is open

3.3. Protection Circuit Design

IEGT devices may be damaged by abnormal phenomena like overcurrent and overvoltage. To protect the devices from damage, a protection circuit such as a snubber circuit may be added. The design of the protection circuit should match the device characteristics. The characteristics and circuit operation of the device should be carefully considered. If the match is inadequate, the effect of the added protection circuit will be ineffective and the desired result may not be obtained. An example is when applying overcurrent protection: the interruption time may take too long to deviate from the SOA and may cause a breakdown. Another example is that when the capacitor capacitance of the snubber circuit is too small, an excessive spike voltage is generated. For more details on overcurrent and overvoltage protection methods, refer to "Protection Circuit Design Method" in Chapter 4.

3.4. Thermal Design

The maximum allowable junction temperature Tj(max) of an IEGT device is predefined.

Therefore, thermal design should be below this temperature. When determining thermal design, the application operation to which the IEGT device will be applied should be thoroughly considered. Inadequate thermal design may cause problems such as breakdowns when the device's temperature exceeds its allowable limit during hardware operation. To determine the thermal design, calculate the device power loss and then select thermal fins that keep the device below the allowable temperature based on that loss. For more details regarding this topic, refer to "Heat Dissipation Principle" in Section 4.4.

3.5. Drive Circuit Design

Designing the drive circuit is important to fully maximize the device's performance. It is also closely related to the design of protection circuits. The drive circuit consists of a forward-biased circuit for turning the device on and a reverse-biased circuit for keeping the device off steady-state and for accurately turning it off. The device characteristics change according to each of these condition settings. In addition, depending on the position of the drive circuit and the wiring method, problems such as device malfunctions may occur. The design of an optimal drive circuit is very important. Therefore, refer to "Gate Driver Circuit Design" in Chapter 5 for more details.

3.6. Mounting Precautions

Pay special attention to the following when mounting the Press Pack IEGT device.

(1) The press-contact state (evenly flat contact pressure) is important since the press pack type device applies pressure to all contacts between the main electrodes. A specified contact pressure is also used after applying a conductive thermal compound between the device electrode surface and the heat sink.

(2) There is a possibility that the device itself expands and the contact pressure rises due to temperature change from the load applied to the device. Even in such conditions, apply contact pressure evenly by using it together with a Belleville washer or similar hardware. For more details about this topic, refer to Subsection 4.4.4.

3.7. Storage and Transportation Precautions

Storage

(1) Keep the storage temperature of the semiconductor devices at 5°C to 35°C and the humidity at 45% to 75%.

(2) Avoid locations that generate corrosive gases, and dusty locations. The packaging box used for delivering the devices is made of corrugated cardboard and is thus not suitable for long-term storage. Consider other packaging for long-term storage.

(3) Rapid temperature changes can cause condensation on the semiconductor device. Avoid such environments and store the devices in locations with minimal temperature

fluctuations.

(4) Do not allow external force or load to be applied to semiconductor devices while they are in storage. Unexpected load may be applied especially when devices are stacked on top of or under other items.

(5) Use containers that are less susceptible to static electricity when temporarily storing semiconductor devices.

Transportation

(1) Some devices are heavy due to their ratings and structure. Be cautious of falling devices that may cause physical injury.

(2) Do not drop or apply physical shocks to products during transportation.

(3) When transporting large quantities of semiconductor devices in a container, insert soft spacers between the devices to avoid damaging the contact electrode surfaces and other components.

3.8. Reliability Precautions (Lifetime Design)

In general, when operating an inverter or other electric power converter, the incorporated IEGT device's temperature repeatedly rises and falls. Due to the temperature changes, the IEGT device undergoes thermal stress. Consequently, its lifetime depends on its operating conditions. Therefore, consider making the design lifetime longer than the required lifetime of the equipment. To achieve an optimal lifetime design in general, check the temperature change of the IEGT device and then make a lifetime design from the thermal fatigue endurance. If the lifetime design is not sufficiently considered, problems may arise such as shortened lifetime and reduced reliability. Therefore, lifetime design based on reliability is important. For more details regarding this topic, refer to "Reliability Information" in Chapter 7.

3.9. Other Notes on Handling Precaution

(1) When measuring the electrical characteristics, make sure that it is properly pressure contacted. For details, refer to the "Mounting force" characteristics in the data sheet and "Confirmation of Press Pack Condition" in Subsection 4.4.5.

(2) Make sure that the driving voltage (V_{GE}) is measured at the device gate terminal and the specified voltage is applied. (When measured at the end of the drive circuit, this voltage is not affected by the voltage drop of the transistor that is connected between the end of the gate drive circuit and the gate terminal, etc. Therefore, even if the prescribed V_{GE} is not applied to IEGT, a problem may be undetected which may lead to device damage.)

(3) Measure surge voltage and other electrical characteristics at the product's electrode when turn-on/turn-off.

(4) Use the product within the range of its absolute maximum ratings (voltage, current, temperature, etc.). The product may be damaged if used beyond its absolute maximum

ratings. In particular, when a voltage exceeding V_{CES} is applied, avalanche breakdown may occur and the device may be damaged. Make sure that the V_{CE} is used within the range of the absolute maximum ratings.

(5) In the unexpected event that the device is damaged due to an accident, prevent a secondary breakdown by providing a fuse or a fault detection circuit with appropriate capacity between the main circuit capacitor and the semiconductor device.

(6) Thoroughly understand the product's use environment. Consider whether it satisfies the product's lifetime reliability expectation before using it. If the product is used beyond its reliability lifetime, the device may be damaged before the equipment using the device can reach its target lifetime.

(7) Use this product with a thermal fatigue life or less. There are two types of thermal fatigue life: short-period power cycle endurance and TFT (Thermal Fatigue Test) endurance (or long-period power cycle endurance). The former is due to ΔTj, and the latter is due to ΔTc. However, the pressure contact type device is only TFT tolerance. These depend on the thermal design when using this product. Pay sufficient attention not only to the rise and fall of the junction temperature, but also the rise and fall of the case temperature.

(8) Avoid locations that generate acid, organic substance, or corrosive gas (such as carbon sulfide or sulfurizing gas). When used in locations that generate acid, organic substance, or corrosive. If the product is used in an environment containing acid, organic substance, corrosive gas (carbon sulfide, sulfur dioxide, etc.), the product function and appearance will not be guaranteed.

(9) Do not apply excessive stress to the pressure contact electrode when mounting the product to the equipment. Deformation of the electrode part may cause damage to the device, etc. because uniform pressure contact condition cannot be maintained. Refer to the product specifications for the recommended pressure contact force (Mounting force).

(10) When only the FWD is used and the IEGT is not used (e.g., when applying to a chopper circuit), apply a reverse bias of -5 V or more (recommended -15 V, maximum -20 V) between G-E of the unused IEGT. If the reverse bias is insufficient, the IEGT may erroneously turn on due to dv/dt at FWD reverse recovery, and this may eventually lead to damage.

(11) If turn-on dv/dt is high, the IEGT of the opposite arm may erroneously turn on. Follow optimum drive conditions (+V_{GE}, -V_{GE}, R_G, C_{GE}) to prevent erroneous turn-on.

(12) Excessive static electricity applied to the control terminal may damage the device. Take necessary countermeasure against static electricity.

(13) When attaching the device to the cooling fin, use a compound that ensures heat conduction. Also, if the coating amount is insufficient or the coating method is inappropriate, heat conductivity will decrease and thus reliability will deteriorate. When applying the compound, confirm that it spreads to the whole radiating surface of the product. (Check the spreading condition of the compound when removing the device after mounting.)

(14) The external resistor R_G stated in the specification document indicates the recommended

resistance to minimize switching loss. However, the optimum R_G varies depending on circuit configuration and the operating environment. Therefore, when determining the external resistor R_G, carefully consider characteristics such as switching loss, EMC/EMI, spike voltage, surge current, and unexpected vibration in the circuit configuration and operating environment where the IEGT device is used. Note that a proper external resistor R_G must be selected to comply with the specification.

(15) This section only explains the main practical precautions. For more details, check the notes and warnings stated in the specifications of each product.

4. Protection Circuits Design Methods

4.1. Surge voltage protection

The IEGT switching time is as short as a few μs, which works well with high-speed switching. However, such high-speed switching characteristics could cause a surge voltage to the IEGT. This is due to stray inductance Ls in the absence of circuit technology. The Vsurge size is:

$$Vsurge = -Ls \times di/dt + Vcc$$

Design the main circuit so that this value is sufficiently smaller than the maximum rated voltage between the main terminals described in the datasheet. Vsurge can be reduced by lowering the di/dt, stray inductance, etc. However, reducing the di/dt sacrifices the high-speed switching characteristics of the IEGT. Therefore, stray inductance should be reduced. For example, using a copper plate instead of a wire can greatly reduce inductance. An effective way to reduce generated surge voltage is to add a snubber circuit.

Snubber Circuit Example

Figure 4.1 shows examples of snubber circuits. Although a snubber circuit can absorb the surge voltage, the change in surge voltage would still depend on the IEGT switching characteristics and the main circuit wiring configuration. Therefore, understand the characteristics of the snubber circuit before deploying it. Next, carefully select the circuit configuration and determine the constant by experimentation.
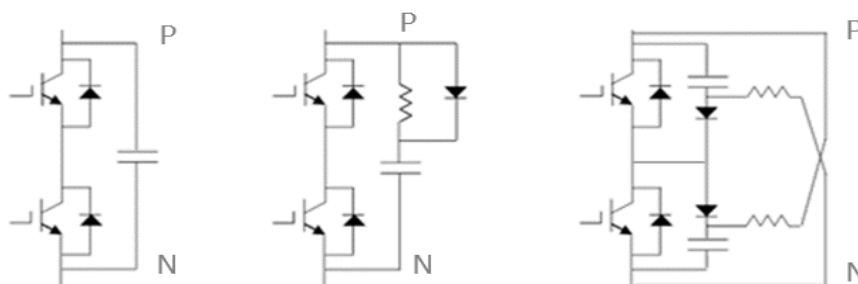
(a) Snubber between PN   (b)Non-rechargeable   (c)Rechargeable
                                RCD snubber   RCD snubber

Figure 4.1 Snubber circuit example

Next, Rechargeable RDC snubber in diagram (c) will be briefly explained. Figure 4.2 shows an example of a rechargeable RDC snubber and the turn-off waveform at that time. ΔV1 is a voltage (surge voltage) that cannot be absorbed due to inductance L2 of the snubber circuit. In other words, this is the turn-off voltage generated at di/dt × L2 at turn-off. Set Cs from the following equation

$$1/2 \times L1 \times (Ic)^2 = 1/2 \times Cs \times (\Delta V2)^2$$

Here, L1 is the main wiring inductance, L2 is the snubber circuit inductance, Rs is the snubber resistance, and Ds is the snubber diode.
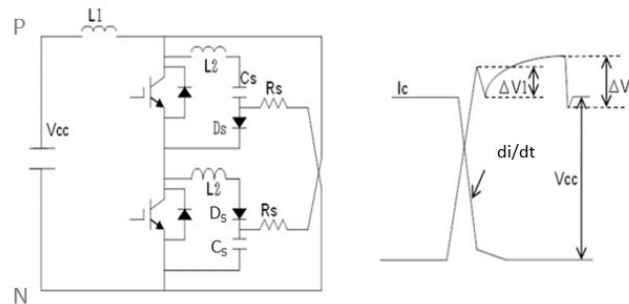
Figure 4.2 Rechargeable RDC snubber circuit and turn-off waveform example

A capacitor is needed between the P and N if excessive surge voltage is generated between them. Especially for large capacity devices, rechargeable RDC snubber circuits (c) may be used in combination with a capacitor between the P and N (a) in Figure 4.1.

4.2. Example of surge voltage generation (reverse recovery of small current of diode)

In applications such as PWM-controlled inverters using IEGT and freewheeling diodes (FWDs), when a small current flows through the FWD for a short time, IEGT on the opposite side is turned on and the FWD is reversely recovered. At this time, the depletion layer in the FWD spreads rapidly during recovery because the forward carrier accumulation is small, and a sharp peak voltage as shown in Figure 4.3 is generated. To prevent this, it is necessary to check the operation in a small current or a short time, and to devise a gate resistor and a snubber circuit so as to reduce the surge voltage. Selecting an FWD that is less prone to surge voltages is another countermeasure.
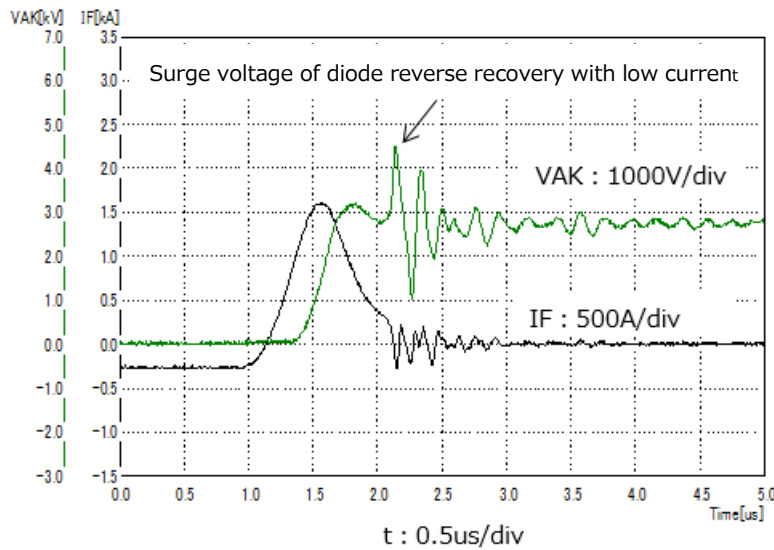
Figure 4.3 Surge voltage during reverse recovery
of FWD with small current

4.3. Short circuit protection

About short circuit capacity when an IEGT is in a short-circuit state and its collector current rapidly increases, the collector-emitter voltage rapidly increases. And the collector current at short circuit is suppressed to a certain value or less. However, this high voltage or large current state in the IEGT should be eliminated as quickly as possible. Note that the IEGT has a time limit when shutting off the current after a short circuit condition occurs. This is called short-circuit capacity and it is specified from the start time of the short-circuit current flow to the breakdown, as shown in Figure 4.4. Therefore, when a short circuit occurs, shut off it within the specified short circuit capacity. Short-circuit capacity depends on various conditions such as collector emitter voltage VCE, gate-emitter voltage VGE, and junction temperature T_j. In general, the short circuit capacity amount is smaller when power supply voltage V_{CC} or junction temperature is higher. For more details on the short-circuit capacity of each device, refer to the technical datasheet.
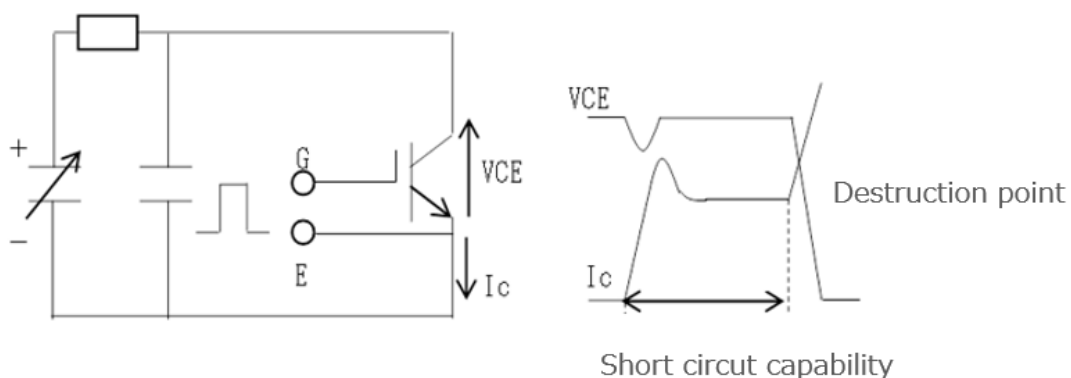
Figure 4.4 Measurement circuit diagram and waveform examples

Overcurrent detection for protection against short-circuit is performed by a CT (Current Transformer), a CE voltage, or the like. Turn the device off immediately when an overcurrent is detected. Short-circuit protection is possible only with current detection. However, depending on use conditions, there is a possibility that (1) surge current at short circuit turn-on will be large, and (2) surge voltage at short circuit turn-off may be high. It is therefore advisable to take the necessary precautions.

(1) Example of how to suppress surge current at short circuit turn-on (Figure 4.5)

When the gate-emitter voltage rises, the surge current at short circuit turn-on increases. This may cause a breakdown. To suppress the surge current, the gate voltage should be suppressed. In general, this is done by inserting a Zener diode (16 to 17 V) between the gate and the emitter. Inserting a Zener diode suppresses the gate-emitter voltage rise and the surge current. However, when the Zener diode voltage is too low, the gate voltage at the time of normal turn-on/turn-off becomes insufficient, which may increase turn-on and turn-off loss. Similarly, when Zener diode voltage is too high, the effectiveness of gate voltage suppression decreases. Therefore, select the appropriate voltage for the Zener diode while checking the waveform.
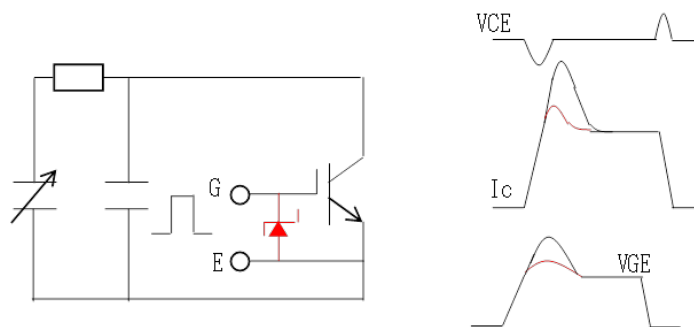
Red: Example when Zener diode is inserted
Black: Example when Zener diode is not inserted

(a) Example diagram of a circuit in which a Zener diode is inserted

(b) Example of short-circuit waveform with and without Zener diode insertion

Figure 4.5 Circuit diagram and waveform example with Zener diode inserted

(2) Surge voltage at short-circuit turn-off When the main circuit wiring is long, surge voltage at the time of short-circuit turn-off becomes high. This may lead to damage. As a common method of suppressing surge voltage, detect $V_{CE(sat)}$ abnormalities using an overcurrent detector or driver circuit and apply the soft turn-off method, which is done by increasing the gate resistance or suppressing the gate output voltage. (Figure 4.6; A separate circuit is required.) However, avoid erroneous detection by turn-on operations in every operation mode. Select the appropriate short-circuit protection circuit while checking the waveform

Black: When soft turn-off is not performed

Red: When over-current is detected and the gate resistance is increased and the device turned of softly.
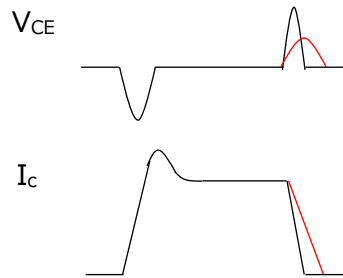
Figure 4.6 Example of short-circuit waveform when soft turn-off by gate resistor

4.4. Heat Dissipation Principle

4.4.1. Heat equivalence circuit

If the transfer of heat is replaced by an electric current, the path through which the heat is conducted to the outside can be shown by an electric circuit. Heat conduction from the junction part of the IEGT to the outside air is determined by the thermal resistance and heat capacity of this equivalent circuit. Figure 4.7 shows a heat conduction equivalent circuit in a thermally steady state.
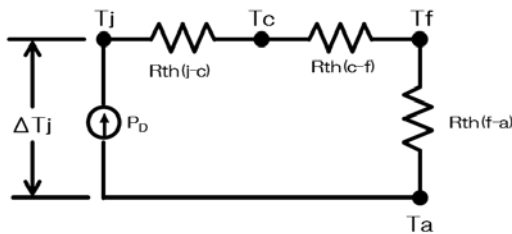
$R_{th(j-c)}$: Junction-to-Case Thermal Resistance
$R_{th(c-f)}$: Case-Fin Thermal Resistance
$R_{th(f-a)}$: Fin-Ambient Thermal Resistance

Fig. 4.7 Heat conduction   equivalent circuit

Equation (2) from the equivalent circuit in Figure 4.7 gives the whole thermal resistance Rth(j-a) from the junction part to the outside air

$$Rth(j-a) = \ Rth(j-c) + Rth(c-f) + Rth(f-a) \quad \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots(2)$$

Let PD be the power loss at the device, and the junction temperature Tj is given by equation (3).

$$Tj = \Delta Tj + Ta = P_D \times Rth(j-a) + Ta \quad \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots(3)$$

Design the heat dissipation of the fins so that Tj expressed by equation (3) never exceeds the absolute maximum rating, $T_{j(max)}$, of the data sheet.

4.4.2. Loss calculation

The loss generated by the element can be expressed by Equation (4).

$$P_D = P_{ST(IEGT)} + P_{OFF} + P_{ON} + P_{ST(FWD)} + P_{DSW} \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots(4)$$

$P_{ST(IEGT)}$: Conduction loss of the of IEGT

P_{OFF} : IEGT turn-off loss

P_{ON} : IEGT turn-on loss

$P_{ST(FWD)}$: Conduction loss of the Diode

P_{DSW} : Diode Reverse Recovery Loss

$P_{ST(IEGT)}$ can be calculated from I_c-V_{CE} curve and $P_{ST(FWD)}$ from I_F-V_F curve. For P_{ON}, P_{OFF}, P_{DSW}, measure E_{on}-I_c, E_{off}-I_c, E_{dsw}-I_F curve respectively according to the application and the driving condition, and use it for the calculation. The data sheet lists the switching loss curves for typical drive conditions. In all cases, design the thermal design so that T_j does not exceed $T_{j(max)}$ with a margin for the generation loss.

4.4.3. Pulse response of junction temperature

Generally, the thermal impedance of a power semiconductor is given by a distributed constant circuit as shown in Figure 4.8.
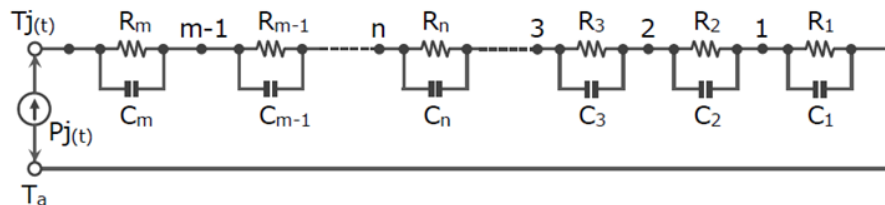
Figure 4.8 Thermal Impedance of Power Semiconductors

For ordinary power semiconductors, the actual value can be approximated by considering that m equals 4, but it is difficult to calculate the value of T_j when the values of C and R are not clear. Therefore, in general, estimate $T_{j(max)}$ using the transient thermal resistance curve. First, consider a single pulse. When a single square wave pulse (width T1, peak value P0) is applied, the transient thermal resistance $R_{th\,(T1)}$ with respect to the pulse width T1 is obtained, and $T_{j(max)}$ is given by equation (5).

$$T_{(jmax)} = R_{th(T1)} \times P0 + Ta \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots(5)$$

In the inverter operation, power loss occurs in pulses every time switching is repeated, so the junction temperature changes as shown in Figure 4.9. In this case, the peak value ($T_{j(max)}$) of the temperature can be estimated by approximating the power loss with a square-wave pulse of a fixed period and using the transient thermal resistance curve. When a continuous pulse of

period T, $T_1=T_2$ as shown in Figure 4.9 is applied, $T_{j(max)}$ is given by equation (5) in a thermally stable state. In thermal design of power semiconductors, care must be taken that $T_{j(max)}$ in equation (5) does not exceed the absolute maximum ratings of the power semiconductors.
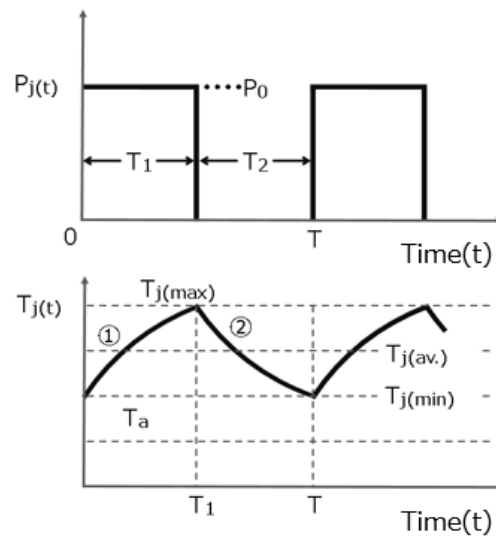
Fig. 4.9 Temperature change when pulse loss is applied

Pay attention to the following points when attaching the press pack IEGT to the thermal fin so the device can provide a sufficient heat radiation effect without applying thermal or mechanical stress to the device.

- Application of Conductive Grease
  Apply conductive grease between the device and the fins to improve the thermal resistance between them. In this case, apply a thin and uniform layer of conductive grease. Non-volatile conductive grease is suitable. (When volatile conductive grease is used, cracks may form in the grease in the long term and the heat radiation effect may decrease.)

- Mounting on the Fins
  To obtain a sufficient heat radiation effect, mount the device's electrodes directly on the fins. In this case, the fins are also used as electrodes to establish an electrical connection.

- Selecting a Cooling System
  Select a suitable cooling fin for the amount of heat the device generates. Air cooling type fins include inexpensive aluminum fins, copper laminated fins, and the like. Cover the clamp jig with an insulator tube so that it does not touch the fins. Apply contact pressure through the insulator so that the jig does not electrically connect to the frame or the ground. Use a Belleville washer as the spring. Since the Belleville washer is saturated at the specified pressure, constant pressure can be maintained even if temperature and pressure change.

A water cooling system with a significant cooling effect is suitable when handling a larger amount of power. Place the heat sink cooled by the liquid on both the sides of the press pack

type device and press the device with press equipment or a bolt until the specified contact pressure force is obtained. As shown in Figure 4.10, in addition to a water-cooling heat sink that becomes an electrode, a clamp jig, a spring (which will be a source of mechanical pressure), and a ball (to uniformly transmit pressure to the device) are required. When using a water cooling system, use high-quality water (pure water) with high electrical resistance to prevent corrosion inside the electrodes and maintain the insulation between the heat sinks. Also, contact the manufacturer of each heat sink to obtain its thermal resistance.
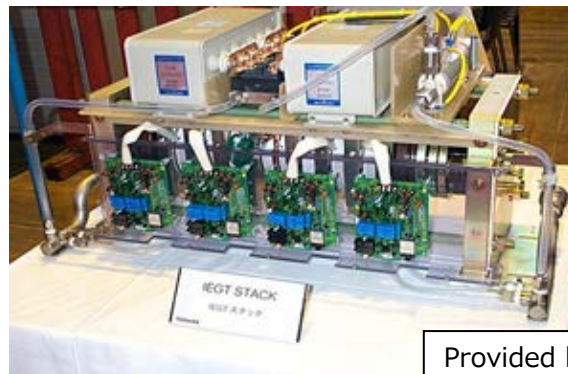
Provided by Toshiba-Mitsubishi Electric Industrial Systems Corporation

Figure 4.10 Example of Mounting a Press Pack Type Device on a Water-Cooling Fin

4.4.4. Heat Sink Design

The most important point for press pack type IEGTs is to apply pressure uniformly. Note the following when designing the heat sink.

- The heat sink should meet the specifications shown in Figure 4.11.
- Even when the operating environment (temperature, atmospheric pressure, etc.) changes, the total pressure should be within the specified value range.
- The partial pressure density difference of the device should be 20% or less of the average pressure density (total pressure/press-contact area). (see Fig. 4.12).

Item	Values on Fin's Press-Contact Surface
Flatness (entire fin)	10 μm or less
Flatness (Rz)	3 μm or less
Parallelism	100 μm or less
Hardness (Vickers hardness)	100 to 120

Figure 4.11 Recommended specifications for Cu heat dissipation fins for Press pack IEGT
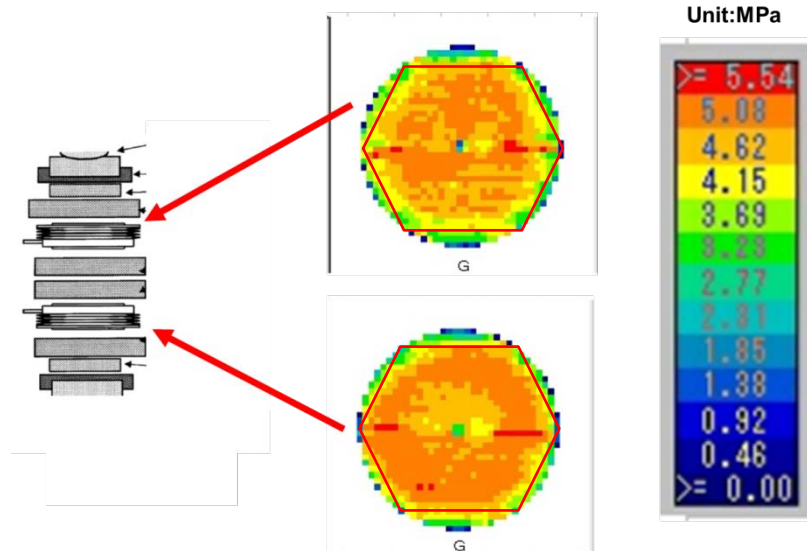
Standard: Within 20% pressure difference of average within the hexagon inscribed

Figure 4.12 Example of pressure distribution with a pressure measurement system

4.4.5. Confirmation of Pressure Contact Condition

Make sure that the individual devices being stacked are pressed uniformly. One way to check the pressure distribution on the main electrode surface of the device is to apply a load after stacking with a pressure sensor sheet or the like inserted between the press-pack device and the heat sink. Select a pressure sensor sheet with appropriate specifications according to the pressure applied to the main electrode surface of the press pack type device (see Fig. 4.13).
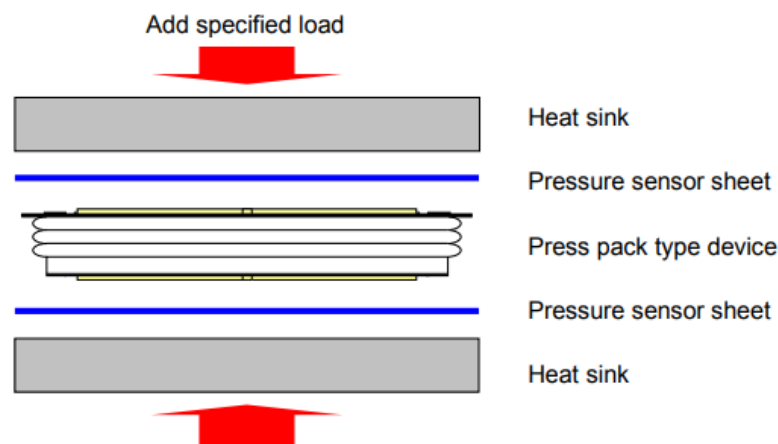
Figure 4.13 Using the Pressure Sensor Sheet

Figure 4.14 shows an example of checking with Fujifilm Corporation's presale (LW). The standard for uniform pressure density is within 20% of the average pressure within the hexagon which is inscribed. Figure 4.15 shows an example of partial pressure contact with pressure relief indicated by an arrow.
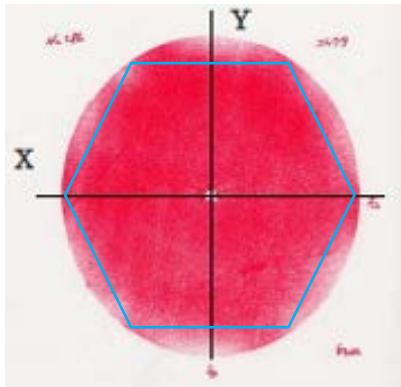
Within the standard: Within 20% of pressure density difference of the average within an inscribed hexagon

Figure 4.14 Normal pressure contact
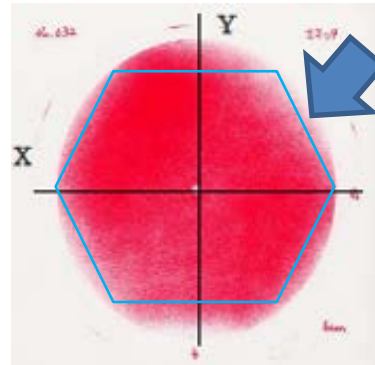
Non-standard: More than 20% of pressure density difference of the average within an inscribed hexagon (blue arrow)

Fig. 4.15 Pressure contact with pressure relief

4.4.6. Maximum allowable applied power of Press Pack IEGT

The TFT tolerance (refer to Note) determines the maximum allowable power of the press pack type IEGT. The TFT tolerance also varies depending on the applied power. The maximum allowable power can be calculated as follows, with 25°C as the maximum value of Tj. However, since the TFT tolerance, which determines lifetime by actual use, depends on the applied power, it is recommended to apply the maximum power as shown in Figure 4.16, especially for PPI.

Note: TFT (Thermal Fatigue Test), Also called long-period power cycling test, refer to "Other Notes on Handling Precaution" in Section 3.9 and "Typical reliability test" in Section 7.5

Calculation of simple maximum allowable applied power (at Tc=25°C):

$(T_{j(max)}$ value-25°C)/Thermal resistance [°C/W]

Maximum applied power (recommended value from TFT tolerance)

Product name	IEGT (W)	Diode side (W)
ST2100GXH24A /ST3000GXH31A	7000	-
ST2000GXH31/ST2000GXH32	4500	2000
ST1500GXH24	5000	1500
ST1200GXH24A	5000	-
ST750GXH24	2000	750

Figure 4.16 Recommended maximum allowable applied power

4.4.7. Maximum Allowable Power of Press Pack IEGT and TFT Tolerance

This is an example of ST1500GXH24 with an electrode diameter of Φ125 mm. As shown in Figure 4.17, the lifetime can be lengthened by derating the applied power.
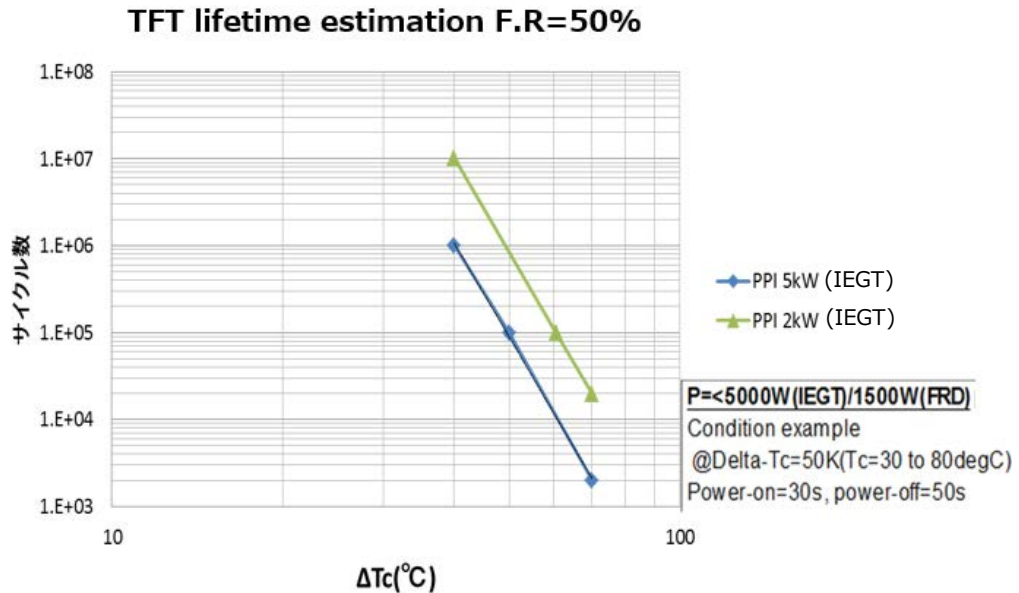
Figure 4.17 Applied power and TFT lifetime

5. Gate Driver Circuit Design

Design the gate driver for each purpose of the application by using driver IC, photocoupler, hybrid IC, etc. Design points are shown below.

Gate voltage

When designing a gate driver, the recommended value for gate forward bias is +15V and the recommended value for gate reverse bias is -15V. The fluctuation of forward and reverse bias power supply voltage should be ±10% or less.

Gate resistance

To adjust the di/dt at turn-on and to reduce the surge voltage at turn-off, verify real machine operation to optimize the gate resistance value. As gate resistance decreases, switching loss decreases, and increasing the resistance increases the switching loss, so select an appropriate gate resistance value.

Dead time

When configuring an inverter circuit with an IEGT, set dead time to prevent the upper and lower arms from short-circuiting. Dead time is the period during which the gate driver

outputs off signals to both the upper and lower arms. Set an appropriate value by verifying the dead time with an actual circuit so as not to cause erroneous turn-on.

Gate wiring

Wiring from the gate driver to the device should be as short as possible to prevent malfunctions caused by effects like electromagnetic noise. Measures such as using a coaxial cable or twisted pair for gate wiring can reduce the influence of external noise. When the gate voltage applied to the IEGT exceeds the gate absolute maximum rating (20V) described in the datasheet, protect it properly with Zener diodes, etc.
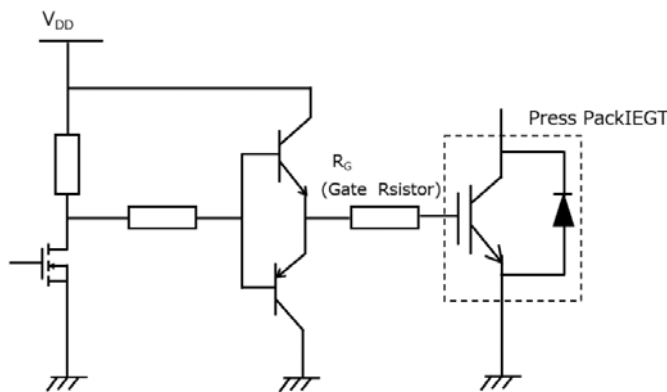
Figure 5.1 Example gate drive circuit

Manufacturers such as Power Integrations, InPower sell gate drivers for our IEGT. Figure. 5.2 shows an exemplary combination of IEGT and driver circuitry.

Driver manufacturer Product name	Power Integrations	InPower
ST1500GXH24	ISO51251-45	1IPSE1A45-105H

Figure. 5.2 Correspondence Table for IEGTs and Each Company's Drivers

6. Applying Applications

6.1. HVDC (High Voltage DC transmission)

High voltage DC transmission is used to efficient power transportation such as off-shore wind-generated power to areas of demand, by converting the generated AC power to DC power for long-distance or subsea power transmission. Press Pack IEGT are used for the high-voltage and large-capacity converter taking advantage of the characteristics of double-sided cooling and series-connection. In addition, high-voltage, large-capacity DC power transmission converters (convert alternating current to direct current) and inverters (convert direct current to alternating current) are often used in the circuitry of MMCs (Modular Multilevel Converter). The MMCs consist of a unit converter called a Sub Module (SM) composed of IEGT switches and capacitors. The MMCs convert DC-AC and AC-DC using an arm connected in series with a large number of Sub Module. Press Pack IEGT are suitable for MMCs because they are easy to connect in series and have SCFM (Short Circuit Failure Mode (Refer to Section 7.4)).
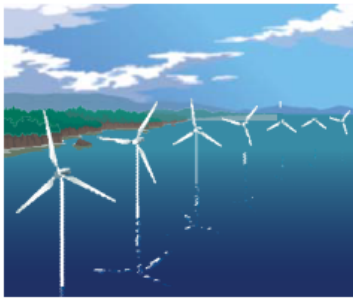
Off-shore wind power

■Submarine Power Transmission System

■MMC(Modular Multilevel Converter)

SM(Sub Module)
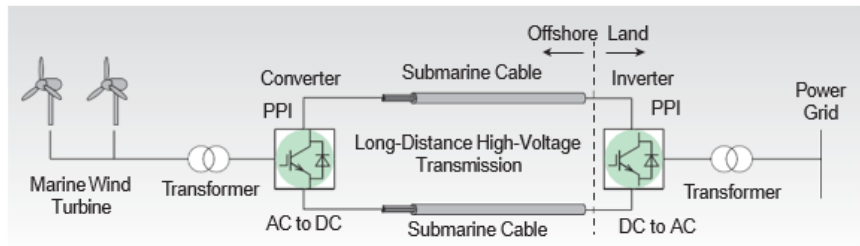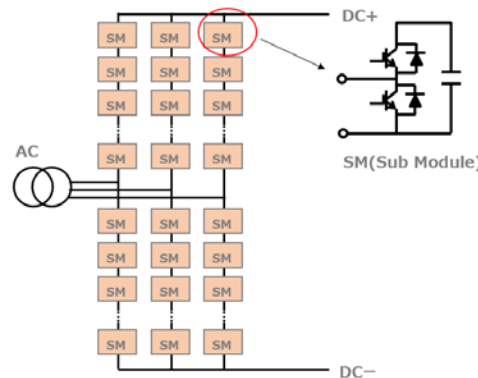
6.2. SVC: Static Var Compensator

This facility is installed in electric power systems, and is used to improve the quality of electric power, such as power factor improvement. Active SVCs include SVGs (Static Var Generator) and STATCOM(Static Synchronous Compensator), and press pack IEGTs (PPIs) are suitable as high-voltage, large-capacity conversion devices that can be connected in series and utilize the features of double-sided cooling.

■SVG Inverter Circuit

Substation
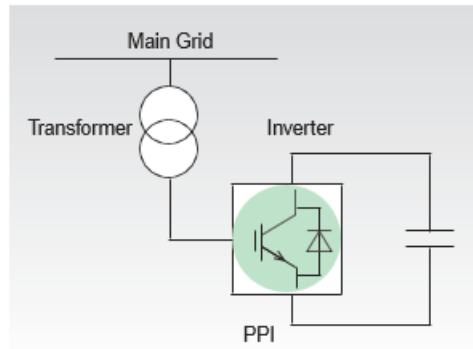
6.3. Medium Voltage Inverter

Press Pack IEGT are recommended for large-capacity inverter equipment, taking advantage of the features of series-connection and double-sided-cooling.

■ Converter Inverter Circuit

Electric propulsion ship
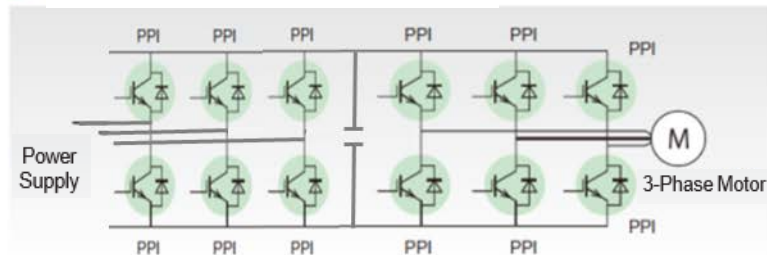
7. Reliability information

7.1. Overview

From the beginning of industrial production, makers have enhanced durability, long lifespan, safety, and serviceability as product quality features that increase the reliability of their products. However, reliability has been more systematically adopted since the 1950s. Along with the increased sophistication and complexity of devices and the progress of systemization for complex systems such as chemical plants and electric power grids, the increased social effect and damage caused by breakdowns have made reliability an important quality characteristic. For this reason, movement from the abstract concept of reliability to

developing more quantitative ways, to plan, improve, and manage the reliability of actual systems and products, has become active. JIS quantitatively defines "reliability" as "the probability that an item will perform its intended function for a specified interval under stated conditions." The following focuses on the reliability of power devices. For more information on the concept of reliability, refer to reliability information of semiconductor products on the website of Toshiba Electronic Devices & Storage Corporation.

< https://toshiba.semicon-storage.com/ap-en/semiconductor/knowledge/reliability.html>

7.2. Power Device Reliability

In general, the failure rate of a power device has a curve shape like a bathtub shown in Figure 7.1. An initial failure period at the beginning of device use is followed by a random failure period and then a wear out failure period. When choosing a power device, consider the application and the characteristics of the failure rate curve. Details of each failure period are described below.
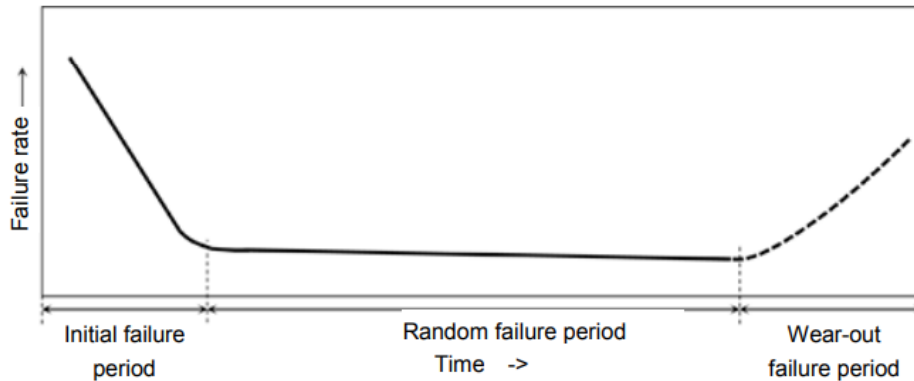
Figure 7.1   Time Course of Failure Rate of Semiconductor Products (Bathtub Curve)

Initial failure period

Initial failures are caused by errors such as minute defects in chips like IEGT and FWD, insulating board defects, or wiring defects such as a short defect. We compile past cases of quality issues and carry out continuous quality improvement activities by feeding these cases back to the design of power chips, the module structure, the assembly process, etc. In this way, we are working to reduce the number of products with initial defects. However, it is extremely difficult to completely eliminate initial defects at the design stage, so we are carrying out a shipping test to compensate for this. In the shipping test, we reduce the initial failure rate by conducting screening and aging tests.

Random failure period

In the random failure period on the failure rate curve, the failure rate of devices is almost constant because the initial failure products have been removed. In other words, the failure rate varies depending on the operating conditions of a power device application in this period. Specifically, it depends on conditions of use and the environment of the entire system composed of power devices and other parts, so it corresponds to the reliability of each system. To reduce the failure rate in this period, it is necessary to prevent various characteristics (voltage, current, temperature, etc.) from exceeding the absolute maximum ratings of the device under the worst operating conditions of the system. It is recommended to use the device with derating (in general, the voltage is 50 to 60% of the absolute maximum rating, and the junction temperature is 70 to 80% of the absolute maximum rating) with respect to the

absolute maximum ratings described in the data sheet, and to comply with conditions of the device application circuits, mounting environmental conditions, and other features specific to the system.

Wear-out failure period

The wear-out failure period of the failure rate curve is the failure period due to the life of the product. A system design that reaches the end of the product's life before this period is reached is required. Toshiba verifies the following long-term reliability tests at the design stage and confirms quality. Particularly for the thermal fatigue failure model of the Press Pack IEGT, the life of the failure mode of TFTs (Thermal Fatigue Test) is confirmed as shown in Subsection 4.4.6. For the product life design, apply the thermal fatigue fracture model and design within the thermal fatigue fracture resistance suitable for the operating mode of the application system.

7.3. Cosmic Ray Tolerance

Device destruction by cosmic rays

Power devices are influenced by terrestrial cosmic rays (Cosmic Ray) when blocking voltages are applied. And it is known to destroy with probability. Cosmic rays are high-energy particles (e.g., protons) that fly from space. They react with the earth's atmosphere and magnetic fields to produce secondary high-energy particles (e.g., neutrons) in the upper atmosphere, which fall onto the ground. When this energetic particle reaches the depletion layer at the time of device blocking, a large number of positive hole-electron pairs are generated, and eventually strong electric fields and impact ionization in the vicinity of the back collector are amplified in a positive feedback manner, leading to device destruction. Features of cosmic ray destruction are as follows.

(1) Single, unexpected fracture.
(2) Occurs while device is in the blocking state.
(3) Occurrence frequency increases in proportion to blocking voltage.
(4) The frequency of occurrence is affected by the operating environment of the device. (Frequency increases when devices are operating at higher altitudes, frequency decreases in concrete buildings, etc.)

Failure Rate for Cosmic Rays of Press Pack IEGT

Figure. 7.2 shows the cosmic ray tolerance (Fit ratio) of Press Pack IEGT. To reduce the failure rate for cosmic rays, It is effective to set the blocking voltage (DC voltage) low for use. At a high altitude use of this product requires countermeasures (concrete shielding, etc.) because the number of failures caused by cosmic ray increases.
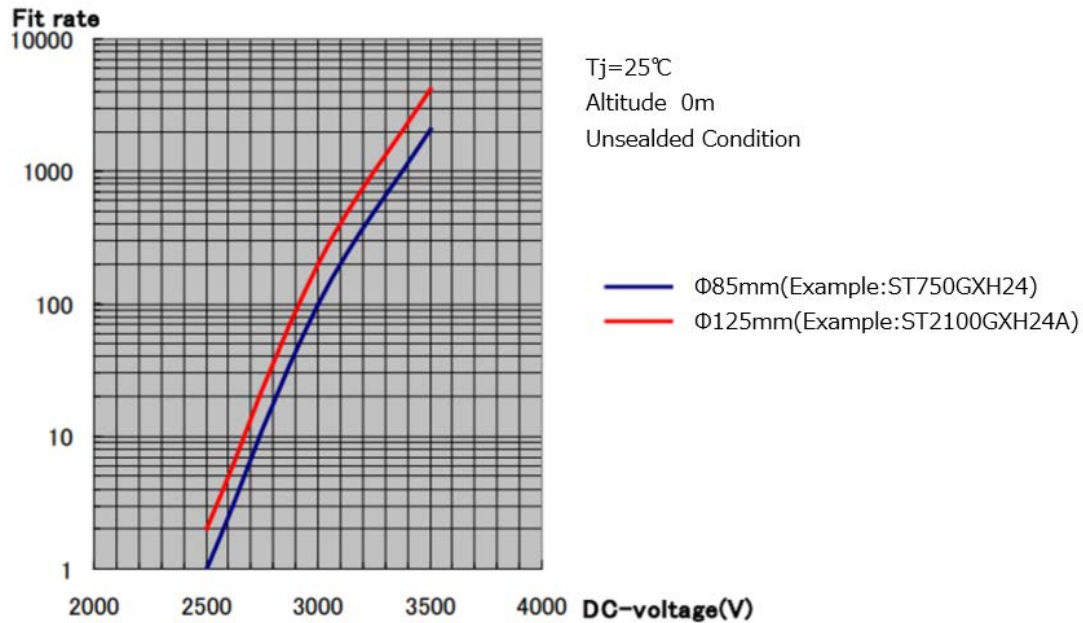
Figure. 7.2 Failure Rate for Cosmic Rays of Press Pack IEGT (Reference)

7.4. SCFM (Short Circuit Failure Mode)

Press Pack IEGT can remain in short-circuit mode even if the device is failure. This is called SCFM (Short Circuit Failure Mode) and is one of the advantages of the Press Pack IEGT. In an application system example in which SCFM is considered (used in a large number of series connections, etc.), even if a device failure occurs for some reason, the operation of the application system is maintained and not stopped by other devices because the failed device maintains a short mode.

Figure. 7.3 shows an example of VSC-HVDC using the MMC (Modular Multilevel Converter) method. In order to achieve SCFM, the system is redundantly designed (N+1 redundancy) so that the number of series-connected Press Pack IEGT has a margin and the rated operation can be performed by other devices even if some devices are damaged. The MMC typically uses about 10% of the devices for redundancy.
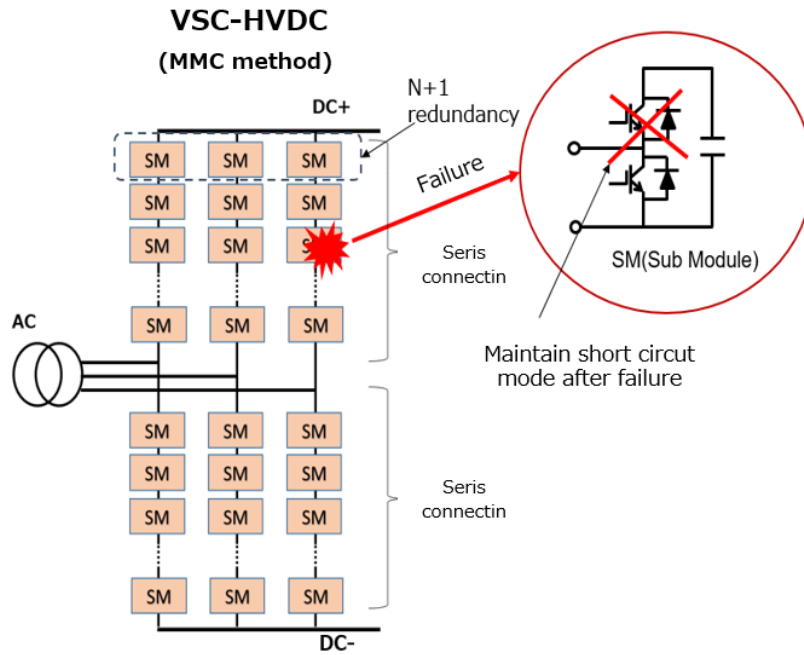
**Figure. 7.3 Applications in which Press Pack IEGTs
are connected in series (VSC-HVDC(MMC method))**

Stability of SCFM

Failed devices in the preceding paragraph will maintain SCFM, but need to be replaced according to the timing of system maintenance. In addition, the device must be kept at a stable SCFM by the time of replacement. The resistance between the collector and emitter of Press Pack IEGT is shown in Figure. 7.4 and is 1.6mΩ or less when the device is failed. It has been confirmed to maintain to short circuit mode and continue for up to 240 hours. We believe that a stable SCFM can be realized even after 240 hours if it is maintained proper pressure contact condition.
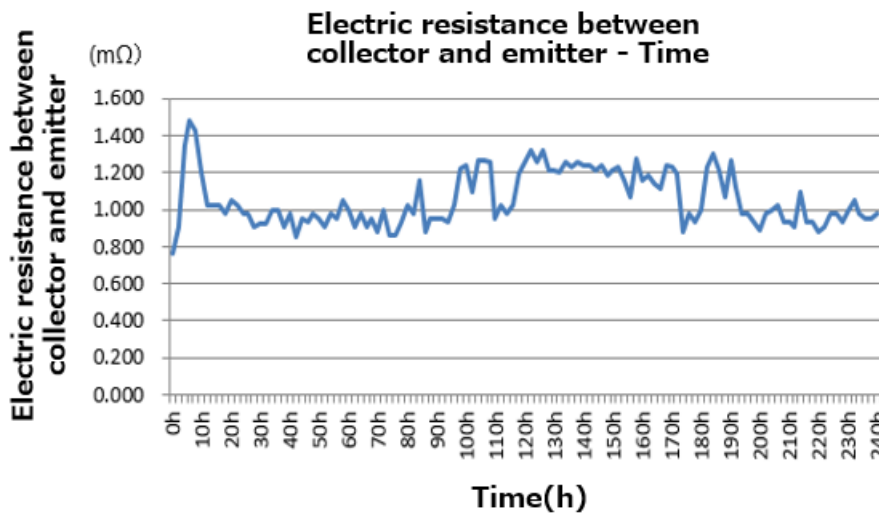
**Figure. 7.4 Maintenance of short-circuit mode
of Press Pack IEGT from device failure**

7.5. Typical Reliability Test

Figure 7.5 shows typical reliability tests.
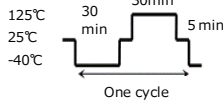
Classification	Test Item	Content and Test Conditions	Compliant Standards			
			EIAJED-4701	MIL-STD-883	IEC 60749	JESD 22
Thermal cycling Test	Temperature Cycle Test	Evaluates the tolerance when the device is left at a high temperature for a long time. Normal test conditions: Ta = -40℃/125℃ 125℃ 30min 30 min 5 min 25℃ -40℃ One cycle	105	1010.7	Part 25	A104-B
Mechanical Test	Physical Shock Test	Evaluates the tolerance to physical shock received during transport or use. Normal test conditions: Test conditions vary depending on the structure, as an example, an impact acceleration of 588 m/s^2, 1ms pulse, waveform: sine half wave, direction:X1,Y1,Y2, Z1, number of times: 3	404	2002.3	Part 10	B104-C
	Vibration Test	Evaluates tolerance to vibration experienced during transportation or use. The test has variable frequency vibration, which is normally performed, and constant frequency vibration. Variable frequency vibration: 100 to 1500 to 100Hz, 200m/s^2, three directions, four minutes up-and-down cycles each, total 48min.	403	2007.2	Part 12	B103-B
	Terminal Strength Tensile Test	Evaluates whether the strength of the terminal part(Gate lead wire of PPI) is adequate for the force applied during wiring for its mount or use. Normal test conditions: Apply a specified tensile load in a direction parallel to the lead wire and keep constant time(30s). After the test, when appearance has cutting, breakage, and slack, it is considered as a poor judging.	401	2004.5	Part 14	B105-C
Lifetime Test	High Temperature Preservation Test	Evaluates the tolerance when the device is left at a high temperature for a long time. Normal test conditions: Ta = Tstg. Max	201	1008.2	Part 6	A103-C
	TFT (Thermal Fatigue Test) or long-period power cycle test	the device and repeated. And the self-heating of a chip and cooling are repeated. In PPI, the stress which occurs according to the thermal expansion difference of each component and a semiconductor chip which constitutes the PPI element evaluates the degree which does damage to a semiconductor chip.	-	-	-	-
	Low Temperature Preservation Test	Evaluates the tolerance when the device is left at a low temperature for a long time. Normal test conditions: Ta = Tstg. Min	202	-	-	-
	High Temperature Bias Test (Gate) High Temperature Bias Test (Collector)	Applies electrical stress and thermal stress to the device for a long time and evaluate its tolerance. Normal test conditions: Ta = 85°C, Power supply voltage: Max voltage rating x 85%	102	-	Part 5	A101-B
	Room Temperature Bias Test	Stresses the device with electricity for a long time and evaluate its tolerance. Normal test conditions: Ta = 25°C, Power supply voltage: Max voltage rating x 85%	102	-	Part 5	A101-B

Figure 7.5 Typical reliability tests

7.6. Reliability Requirement of Press Pack IEGT

In the reliability of the press pack type device, it is necessary to consider the mounting method of the device, stress during operation, and stress of the use environment. These are related each other. The following explain major concepts of each for using the devices with high reliability.

- Mounting Press Pack IEGT

  The press pack type device obtains electrical and thermal contact by applying a load between the main electrodes. Note the following requirements for stack mounting.

  (1) The main electrode surface of the device uniformly applies pressure to the specified load value. To apply pressure without variations, attention must be paid to the material and surface flatness of the components (heat sink, etc.) in the stack load portion. When current is applied, the device expands due to the applied load and the pressure rises. Therefore, use items such as Belleville washers with the stack so that contact pressure can be kept uniform.

  (2) Ensure good heat conduction and perform appropriate thermal design. In order to obtain a sufficient radiation effect, bring the main electrode of the device directly to the heat sink and apply a conductive thermal compound between them. In addition, cool both the sides of the main electrode of the device.

- Operating Conditions of Press Pack IEGT

  Voltage and current added to Press Pack IEGT and environmental conditions of use for equipment are major factors affecting reliability. Set the operating point by proper device selection and circuit design according to the target circuit.

  The failure rate of Press pack IEGT is significantly affected by the temperature during operation and the difference between maximum and minimum temperatures. The failure rate increases as the temperature becomes high or the difference between the maximum and the minimum temperature increases. Press Pack IEGT are used for applications that handle relatively large current and voltage and consume large power. Power consumption generates heat to the Press Pack IEGT, which is undesirable in terms of characteristics and reliability, so efficient heat radiation is necessary.

  In circuit design, make allowance for the superposition of an extraneous surge voltage and noise as well as the deviation of the device characteristics by considering sufficient margins for circuit and protection circuits to significantly prolong the lifetime of the devices and consequently the whole system. To use the Press Pack IEGT with high reliability, it is recommended to perform derating for the specified voltage, current, power, and temperature with the absolute maximum ratings. However, it is necessary to determine the derating to use while considering reliability and economy.

- Characteristics Variation of Press Pack IEGT

Automation of the manufacturing process and progress of manufacturing technology have been remarkable. With these developments and active introduction of new technologies, quality and reliability steadily improve from year to year. Any semiconductor products including Press Pack IEGT are diverse in shape, structure, and dimensions and built by well-controlled and managed precision technologies, based on physicochemical techniques. Therefore, even a slight deviation has a large influence on characteristics, and keeping various characteristics uniform is difficult even with the latest technology. Depending on operating conditions and circuit configuration, it may be necessary to consider the circuit layout according to the characteristics of each device. Additionally, in a Press Pack IEGT, multiple semiconductor chips are arranged in parallel inside the package. We uniformize the characteristics of those semiconductor chips in the same package to improve its reliability as a single device.

● Environment Resistance of Press Pack IEGT
  The Press Pack IEGT realizes high reliability by a hermetically-sealed structure. However, direct exposure to harmful gas, saltiness, radiation, and other extrinsic devices may induce characteristics variation and degradation, as well as rusting of the seal and lead parts, so care must be taken. Also, when using the device under high voltage, care must be taken against dew condensation and surface dirt accumulation on the package. If dew condensation or the amount of dirt is severe, there may be a creeping discharge, which may destroy the equipment. For insulation, devices are sometimes immersed in a cooling medium such as oil. In this case, the cooling medium may influence the marking on actual product, and the gate and emitter leads, so consult with our company contact in advance of using this technique.

7.7. Thermal Fatigue Mode of Press Pack IEGT

The thermal fatigue lifetime of a Press Pack IEGT strongly depends on the temperature change (ΔT) and the operating conditions in which it will be used. In a Press Pack IEGT, the electrical connection and heat radiation are made possible by the press pack structure, so high thermal fatigue reliability can be expected. Due to this structural feature, unlike a wire bonding type power semiconductor device, there is no constraint on the thermal fatigue lifetime due to short-period power cycle tolerance, but there is TFT (Thermal Fatigue Test or long-period power cycle test) tolerance that strongly depends on ΔT. The degradation mode from TFT tolerance leads to damage to the semiconductor chip due to repeated occurrence of stress caused by the thermal expansion difference between the copper electrode, molybdenum plate, and semiconductor chip that make up the press pack type device.

7.8. Failure Mode of Press Pack IEGT

The types of failures are broadly classified as short-circuit, open, and degradation. The major causes of short-circuit failures are 1) overstress such as overvoltage and overcurrent, 2) short-circuit due to high deterioration, and 3) electrochemical reactions. There are other, less-likely causes. Unlike with semiconductor products with general bonding wires, open failures are less likely to happen due to the structural features of press pack type devices. In terms of electric characteristics, various cases of deterioration occur, such as reduction of breakdown voltage below standard value, abnormal increase of current, or drifting of characteristic values. Because the devices are made based on physical and chemical techniques, it is conceivable that variations occur due to thermochemical changes in the surface and inside the device depending on the voltage, current, and temperature, and these may increase gradually and exceed the specified values. The main causes are 1) manufacturing defects, 2) design problems, and 3) handling problems. In addition, when excessive current flows in a Press Pack IEGT, the package is not easily broken by the hermetic sealing structure, but the package can rupture and damage the peripheral equipment depending on the magnitude of the overcurrent.

8. Countermeasures When Problems Occur

When IEGT devices are applied to various circuits, the devices may malfunction or be damaged due to defects such as wiring mistakes, mounting errors, or control signal mismatches. If abnormal device operation or breakdown occurs, clarify the cause and take appropriate countermeasures to avoid a repetition. In investigating factors when the device breaks down, it is generally easier to get to an understanding by proceeding with FTA (Fault Tree Analysis) as shown in Figure 8.1. The breakdown mode can be determined by disassembling the broken device and observing the state of the chip. For breakdown mode details, refer to Figure 8.2.
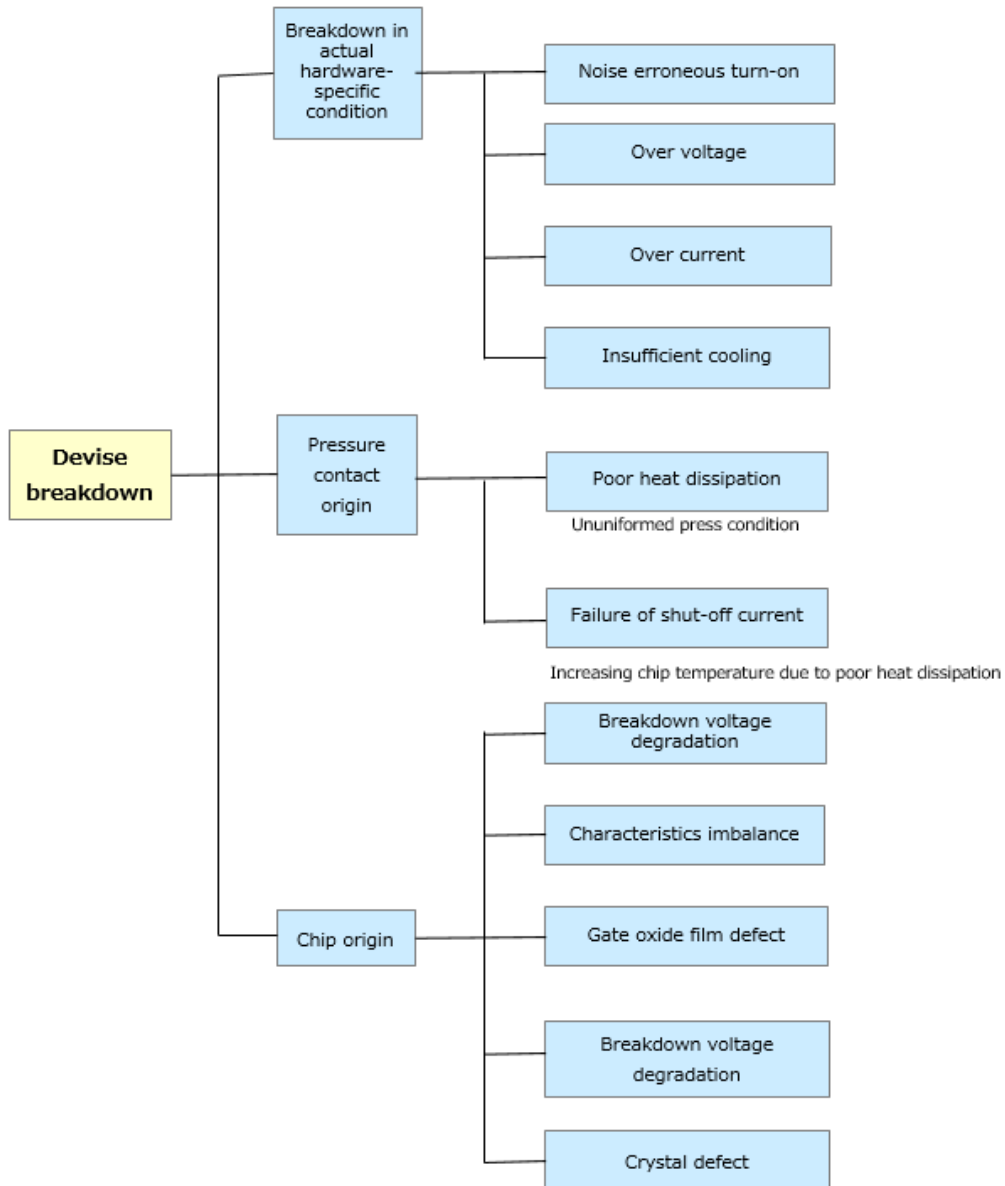
Figure 8.1 FTA (Fault Tree Analysis)

To check whether the product has broken down, measure and confirm the following (1), (2) for the IEGT device and (3) for the FWD device by characteristics measuring equipment such as a transistor curve tracer

(1) Leakage current between G and E
(2) Leakage current between C and E
(3) Leakage current between A and K(K:Cathode)

In addition, simple failure determination is possible even if using an instrument that can measure voltage and resistance, such as a tester or battery checker, instead of a curve tracer.
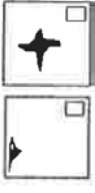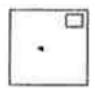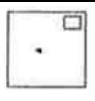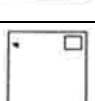
#		Time of Breakdown (Possibility = ◎: Large, O: Possible, -: Not applicable)					Pellet Breakdown Pattern Diagram	Supplementary Information (TR = IEGT, D = Diode)	Possible Electrical Factors, Others
		Turn-On	Steady On	Turn-Off	Steady Off	Others			
1	Turn-Off Breakdown	-	-	◎	-	-		One TR CE short, GE short Breakdown in the pattern's cell The size of the trace of breakdown differs depending on the power at the time of breakdown. (Includes chip sorting time) There may be degradation of other chips.	Vcc, Vcp, and Icp were applied, exceeding device tolerance. Ls is excessive. Overcurrent due to SW after FWD breakdown, etc.
2	GE Breakdown Voltage Failure 1	O	O	O	O	O		At least one TR GE or CE short circuit There may be trace amounts of melted marks (may be minor).	Applying voltage that exceeds the rating between GE (Includes VGE variation due to dv/dt) Applying voltage between CE with GE open
3	GE Breakdown Voltage Failure 2 (Mainly press pack type devices)	-	-	-	-	O	Random in the surface	One or more TR(s) Gate wiring collapse Al electrode protrudes and short circuits with other wiring	- Wiring collapsed due to excessive repeated press-contact - Foreign particle caught between devices - Wiring collapse and deformation due to excessive or uneven contact pressure
4	Overvoltage to CE/AK	-	-	-	-	-		One TR or more, or one D or more, breakdown near the end of the chip (Many at chip corners)	- At the time of IEGT shutoff, the surge voltage for FWD reverse recovery exceeding the device tolerance was applied
	IEGT	-	-	O	O	O			
	FWD			O	O	O			
5	Reverse Recovery Breakdown (FWD)	◎	-	-	-	-		Melting in one or multiple D AK short circuit	- Applying back power by excessive VR, IF, etc.
6	After short-time current application Reverse recovery breakdown (FWD)	-	-	◎	-	-		Melting in the bulk of one D AK short circuit	- Application of excessive back power for a short time (When operating as the FWD of the other arm due to IEGT turn-off breakdown, etc.)
7	Cosmic Ray Breakdown (LTDS)	-	-	O	O	O		At least one TR or D Part near the chip end or bulk melts in spots.	- Excessive Vcc/VR - High altitude and other environmental impacts
8	Surge Current Breakdown (FWD)	O	O	-	-	O	FWD example	At least one TR or D Significantly melting in bulk. In the case of FWD where reverse recovery is involved, multiple melt marks may be generated in peripheral parts.	- Applying current beyond the allowable surge current - In the case of IEGTs, current application exceeding latch tolerance

Figure. 8.2 IEGT/FWD Chip failure pattern and estimated failure mode

Note 1: When the melting area of the main breakdown chip is enormous, adjacent chips may also degrade in breakdown voltage and melt.

Note 2: Some example pattern figures double as an IEGT/diode. (For diode, there is no gate electrode at the right upper corner in the squares. In addition, although the position of the gate electrode in press pack type and module type IEGTs is generally different, it is the same here.)

RESTRICTIONS ON PRODUCT USE