TOSHIBA Field Effect Transistor Silicon P Channel MOS Type(π-MOSVI)

# SSM3J16FU

### High Speed Switching Applications

#### Analog Switch Applications

- Small package
  - Low on-resistance  $R_{DS(ON)} = 8 \Omega \pmod{(max)} (@V_{GS} = -4 V)$

 $R_{DS(ON)} = 12 \Omega (max) (@V_{GS} = -2.5 V)$ 

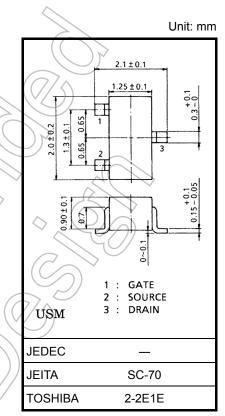
:  $R_{DS(ON)} = 45 \Omega \text{ (max)} (@V_{GS} = -1.5 \text{ V})$ 

#### Absolute Maximum Ratings (Ta = 25°C)

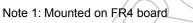
Characteristics		Symbol	Rating	Unit	
Drain-Source voltage		V <sub>DS</sub>	-20	V	
Gate-Source voltage		V <sub>GSS</sub>	±10	V	
Drain current	DC	I <sub>D</sub>	-100		
	Pulse	I <sub>DP</sub>	-200		
Power dissipation		P <sub>D</sub> (Note1)	150	mW	
Channel temperature		T <sub>ch</sub>	150	°C	
Storage temperature range		T <sub>stg</sub>	-55 to 150	°C	

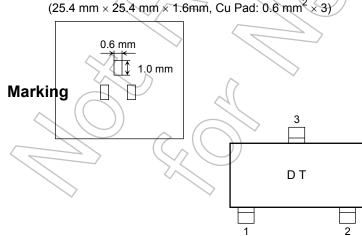
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

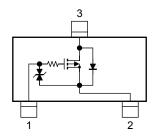


Weight: 6.0 mg (typ.)





Equivalent Circuit (top view)



### **Handling Precaution**

When handling individual devices (which are not yet mounted on a circuit board), ensure that the environment is protected against static electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

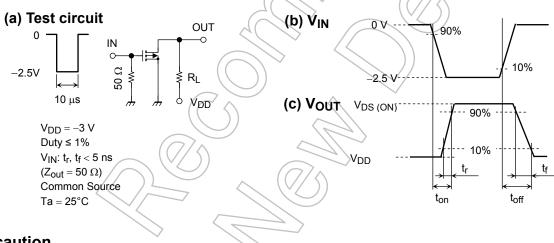
Start of commercial production 2002-01

**Electrical Characteristics (Ta = 25°C)** 

Characteristic		Symbol	Test Condition	MIN.	TYP.	MAX.	UNIT	
Gate leakage current		I <sub>GSS</sub>	$V_{GS}=\pm 10~V,~V_{DS}=0$	_	—	±1	μA	
Drain-Source breakdown voltage		V (BR) DSS	$I_D = -0.1 \text{ mA}, V_{GS} = 0$	-20	_	_	V	
Drain cut-off current		I <sub>DSS</sub>	$V_{DS} = -20 V, V_{GS} = 0$	X	_	-1	μA	
Gate threshold voltage		V <sub>th</sub>	$V_{DS} = -3 \text{ V}, \text{ I}_{D} = -0.1 \text{ mA}$	-0.6		-1.1	V	
Forward transfer admittance		Y <sub>fs</sub>	$V_{DS} = -3 V$ , $I_D = -10 mA$ (Note2)	25	-((	_	mS	
Drain-Source on-resistance		R <sub>DS (ON)</sub>	$I_D = -10$ mA, $V_{GS} = -4$ V (Note2)	2	6	8	Ω	
			I <sub>D</sub> = -10 mA, V <sub>GS</sub> = -2.5 V (Note2)	))	8	12		
			$I_D = -1 \text{ mA}, V_{GS} = -1.5 \text{ V}$ (Note2)		18	45		
Input capacitance		C <sub>iss</sub>		<u> </u>	11	_	pF	
Reverse transfer capacitance		C <sub>rss</sub>	$V_{DS} = -3 V$ , $V_{GS} = 0$ , f = 1 MHz		3.7		pF	
Output capacitance		C <sub>oss</sub>		_	(10	$\searrow$	pF	
Switching time	Turn-on time	t <sub>on</sub>	$V_{DD} = -3 V, I_D = -10 mA,$	-6	130	> -		
	Turn-off time	t <sub>off</sub>	$V_{GS} = 0$ to $-2.5$ V		190	) —	ns	

Note2: Pulse test

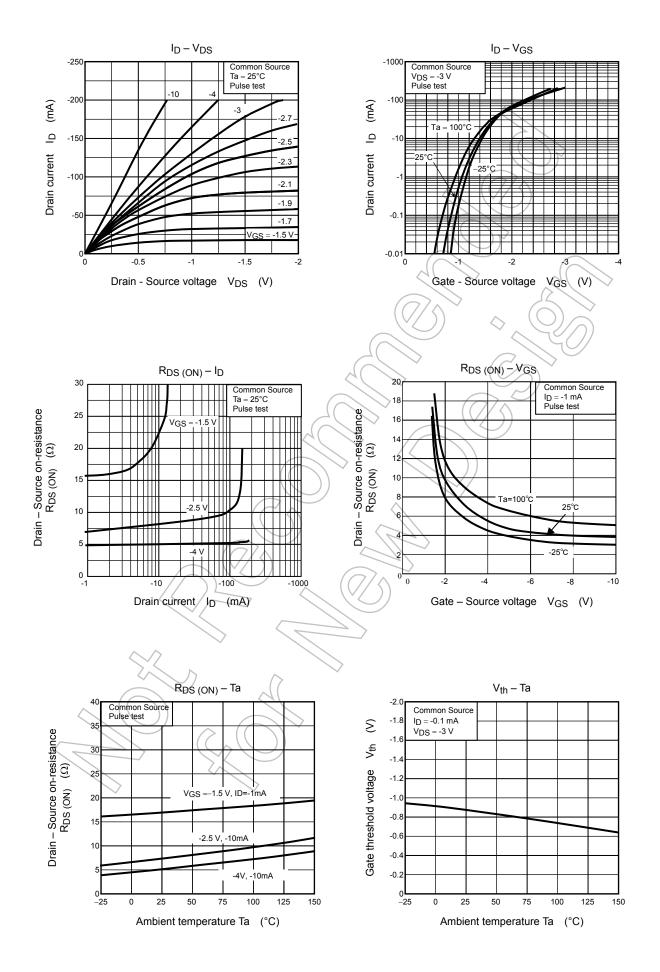
## Switching Time Test Circuit



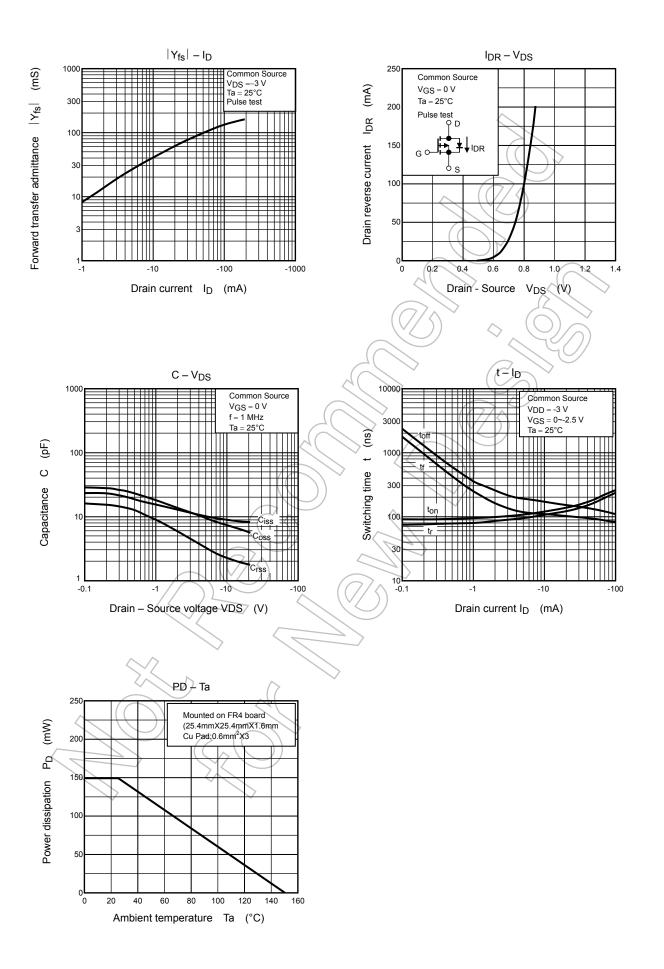
# Precaution

 $\begin{array}{l} V_{th} \mbox{ can be expressed as the voltage between the gate and source when the low operating current value is ID = $-0.1$ mA for this product. For normal switching operation, VGS (on) requires a higher voltage than V_{th} and VGS (off) requires a lower voltage than V_{th}. (The relationship can be established as follows: VGS (off) < V_{th} < V_{GS} (on).) \\ Be sure to take this into consideration when using the device. \end{array}$ 

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