Power MOSFET Electrical Characteristics

Description

This document explains electrical characteristic of power MOSFETs.

Table of Contents

1. Electrical Characteristics

(The specified characteristics differ from product to product. Ta=25°C unless otherwise specified.)

1.1. Static Characteristics

Characteristic	Symbol	Unit	Description
Gate leakage current	I_{GSS}	μA	The leakage current that occurs when the specified voltage is applied across gate and source with drain and source short-circuited
Drain cut-off current	I_{DSS}	μA	The leakage current that occurs when a voltage is applied across drain and source with gate and source short-circuited
Drain-source breakdown voltage	$V_{(BR)DSS}$ $V_{(BR)DSX}$	V	The maximum voltage that the device is guaranteed to block between drain and source $V_{(BR)DSS}$: With gate and source short-circuited $V_{(BR)DSX}$: With gate and source reverse-biased
Gate threshold voltage	V_{th}	V	V_{th} stands for "threshold voltage." V_{th} is the gate voltage that appears when the specified current flows between source and drain.
Drain-source on-resistance	$R_{DS\ (ON)}$	Ω	The resistance across drain and source when the MOSFET is in the "on" state
Forward transfer admittance	$\|Y_{fs}\|$	S	Also called g_m, $\|Y_{fs}\|$ is the ratio of the drain current variation at the output to the gate voltage variation at the input and is defined as $\|Y_{fs}\| = \Delta I_D / \Delta V_{GS}$. $\|Y_{fs}\|$ indicates the sensitivity or amplification factor of the power MOSFET. $\|Y_{fs}\|$ can be read from the I_D-V_{GS} curve.

1.2. Dynamic Characteristics

Symbol	Unit	Unit	Description
Capacitances	C_{iss} C_{rss} C_{oss}	pF	C_{iss} is the input capacitance, C_{rss} is the reverse transfer capacitance, and C_{oss} is the output capacitance. Capacitances affect the switching performance of a power MOSFET.
Effective output capacitance (energy related)	$C_{o(er)}$	pF	$C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 V to specified voltage.
Effective output capacitance (time related)	$C_{o(tr)}$	pF	$C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 V to specified voltage.
Gate resistance	r_g	Ω	The internal gate resistance of a MOSFET
Switching time	t_r t_{on} t_f t_{off}	ns	t_r is the rise time, t_{on} is the turn-on time, t_f is the fall time, and t_{off} is the turn-off time.
MOSFET dv/dt capability	dv/dt	V/ns	The maximum drain-source voltage ramp allowed at the turn-off of a MOSFET

1.2.1. Capacitance characteristics

In a power MOSFET, the gate is insulated by a thin silicon oxide. Therefore, a power MOSFET has capacitances between the gate-drain, gate-source and drain-source terminals as shown in Figure 1.1.

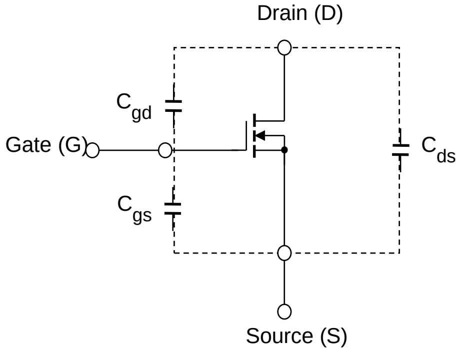
The gate-drain capacitance C_{gd} and the gate-source capacitance C_{gs} are mainly determined by the structure of the gate electrode, while the drain-source capacitance C_{ds} is determined by the capacitance of the vertical p-n junction.

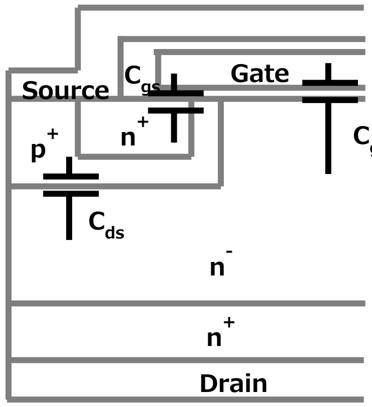
For the power MOSFET, the input capacitance ($C_{iss}=C_{gd}+C_{gs}$), the output capacitance ($C_{oss}=C_{ds}+C_{gd}$) and the reverse transfer capacitance ($C_{rss}=C_{gd}$) are important characteristics.

Figure 1.2 shows the dependency of C_{iss}, C_{rss} and C_{oss} on drain-source voltage V_{DS}.

Switching characteristics of a MOSFET manly vary with the input capacitance C_{iss} and the output impedance of the drive circuit.

Gate current flows from gate to source instantaneously to charge the input capacitance. Therefore, the lower the output impedance of the drive circuit, the faster the switching speed. Large input capacitance of a MOSFET causes a large power loss at light load. C_{iss}, C_{rss} and C_{oss} hardly vary with temperature.





Input capacitance $(C_{iss}) = C_{gd} + C_{gs}$
Output capacitance $(C_{oss}) = C_{ds} + C_{gd}$
Reverse transfer capacitance $(C_{rss}) = C_{gd}$

Figure 1.1 Capacitance Equivalent Circuit

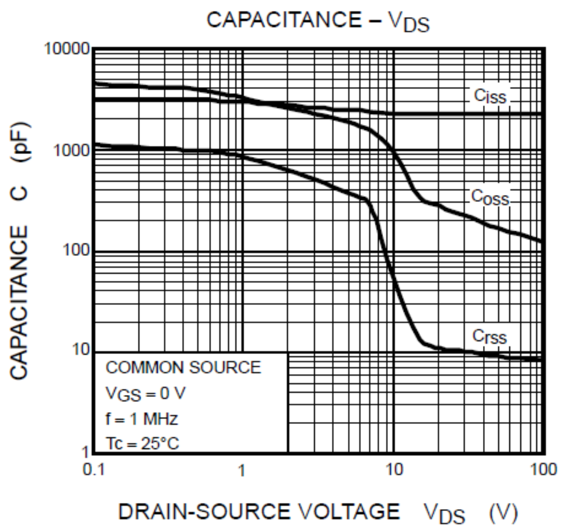


Figure 1.2 Capacitance vs V_{DS}

1.2.2. Effective output capacitance (energy related)

Effective output capacitance (energy related) $C_{o(er)}$ is the fixed capacitance calculated to give the same stored energy as C_{oss} while the drain-source voltage rises from 0V to the specified voltage.

Expressing E_{oss} in $C_{o(er)}$ is as follows.

$$E_{oss} = \frac{C_{o(er)} \times V_{DS}^2}{2}$$

In addition, E_{oss} is equal to the value obtained by integrating the amount of charge Q=C(v)×v in the capacitance characteristic curve from the drain-source voltage of 0 V to the specified V_{DS}, so the following formula holds.

$$\frac{C_{o(er)} \times {V_{DS}}^2}{2} = \int_0^{V_{DS}} v \times C(v)dv$$

Therefore, $C_{o(er)}$ is expressed as follows.

$$C_{o(er)} = \frac{2}{{V_{DS}}^2}\int_0^{V_{DS}} v \times C(v)dv$$

C(v): function of output capacitance C_{oss} dependent on V_{DS}

$C_{o(er)}$ is used when it is necessary to calculate as capacitive energy in the design of power supplies, etc.

1.2.3. Effective output capacitance (time related)

Effective capacitance (time related) $C_{o(tr)}$ is the fixed effective capacitance calculated to give the same charging time as C_{oss} while the drain-source voltage rises from 0V to the specified voltage.

Expressing the charge amount Q_{oss} in $C_{o(tr)}$ is as follows.

$$Q_{oss} = C_{o(tr)} \times V_{DS}$$

In addition, Q_{oss} is equal to the value obtained by integrating the C(v) in the capacitance characteristic curve from the drain-source voltage of 0 V to the specified V_{DS}, so the following formula holds.

If the charging (discharging) current is the same on the left and right in the following formula, the charging (discharging) time is also same.

$$C_{o(tr)} \times V_{DS} = \int_0^{V_{DS}} C(v)dv$$

Therefore, $C_{o(tr)}$ is expressed as follows.

$$C_{o(tr)} = \frac{1}{V_{DS}}\int_0^{V_{DS}} C(v)dv$$

C(v): function of output capacitance C_{oss} dependent on V_{DS}

$C_{o(tr)}$ is used for time calculation purposes in the design of power supplies, etc.

1.2.4. Switching characteristics

Since power MOSFETs are majority-carrier devices, they are faster and capable of switching at higher frequencies than bipolar transistors.

Figure 1.3 shows a switching time test circuit, and Figure 1.3 gives the input and output waveforms.

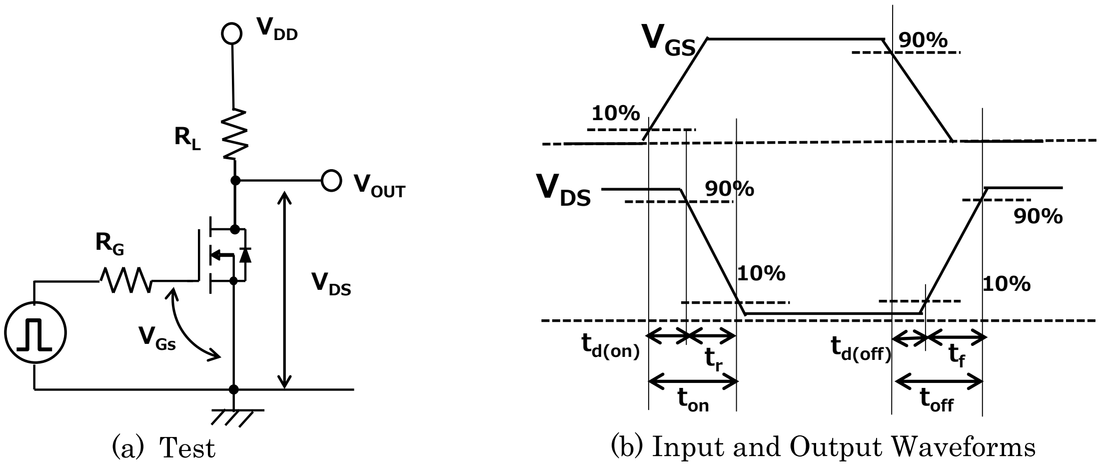


Figure 1.3 Switching Time Test Circuit and Input/Output Waveforms

The symbols used in the above input and output waveforms are briefly explained below:

(1) $t_{d\ (on)}$: Turn-on delay time

The time from when the gate-source voltage rises over 10% of V_{GS} until the drain-source voltage reaches 90% of V_{DS}

(2) t_r: Rise time

The time taken for the drain-source voltage to fall from 90% to 10% of V_{DS}

(3) t_{on}: Turn-on time

The turn-on time is equal to $t_{d\ (on)} + t_r$.

(4) $t_{d\ (off)}$: Turn-off delay time

The time from when the gate-source voltage drops below 90% of V_{GS} until the drain-source voltage reaches 10% of V_{DS}

(5) t_f: Fall time

The time taken for the drain-source voltage to rise from 10% to 90% of V_{DS}

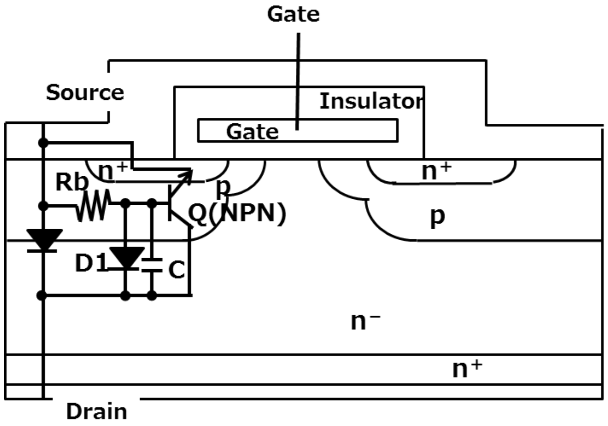
(6) t_{off}: Turn-off time

The turn-off time is equal to $t_{d\ (off)} + t_f$.

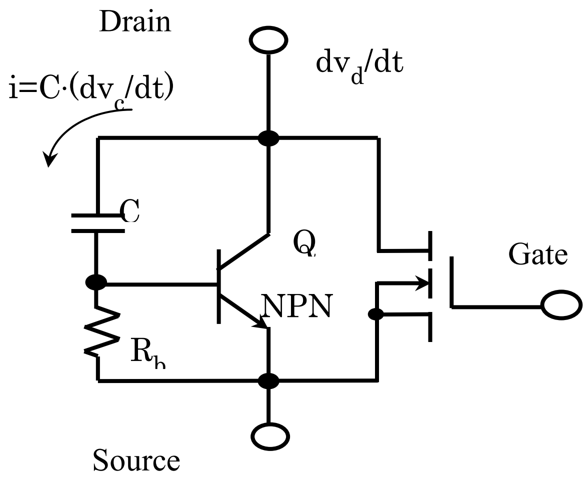
1.2.5. dv/dt capability

When the drain-source voltage is raised sharply at the turn-on of a MOSFET, a displacement current flows to the PN junction capacitance (C) between drain and source, as shown in Figure 1.4, due to the rate of voltage change dv/dt. The displacement current is calculated as $i = C \cdot (dv_c/dt)$. Current i causes a voltage drop of $i \cdot R_b$ due to the resistance R_b of this layer. If the voltage drop exceeds the base-emitter forward voltage (V_{BE}) of the parasitic NPN transistor, it is forced into conduction.

If the drain-source voltage, $V_{DS,}$ is high at this time, the parasitic NPN transistor might enter secondary breakdown, causing a catastrophic failure.



(a) Cross Section of a MOSFET
(Parasitic NPN Transistor)



(b) Equivalent Circuit of dv/dt-Induced Turn-On

Figure 1.4 Cross Section and Equivalent Circuit of a MOSFET

1.3. Charge Characteristics

Characteristic	Symbol	Unit	Description
Total gate charge	Q_g	nC	The amount of charge to apply voltage (from zero to designated voltage) to gate
Gate-source charge 1	Q_{gs1}		The amount of charge required for a MOSFET to begin to turn on (before dropping drain-source voltage)
Gate-drain charge	Q_{gd}		As the MOSFET begins to turn on, the drain-source voltage begins to fall, charging the gate-drain capacitance. The gate-source voltage stops increasing and reaches the Miller plateau. From this point to the ending point of Miller plateau is known as the gate-drain charge period.
Gate switch charge	Q_{sw}		The amount of charge stored in the gate capacitance from when the gate-source voltage has reached V_{th} until the end of the Miller plateau
Output charge	Q_{oss}		Drain-source charge

1.3.1. Gate charge

Because the Gate (G) input terminal of a MOSFET is insulated, the amounts of charge Q seen from the Gate, are important characteristics. Figure 1.5 illustrates the definitions of gate charge characteristics.

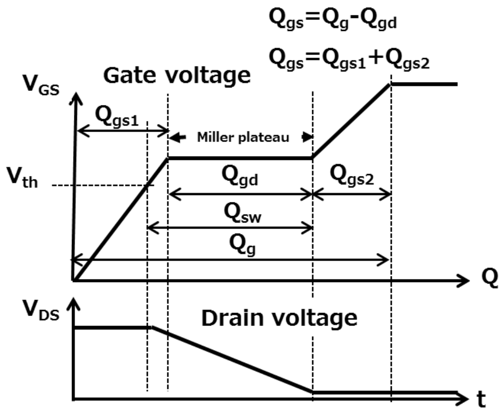
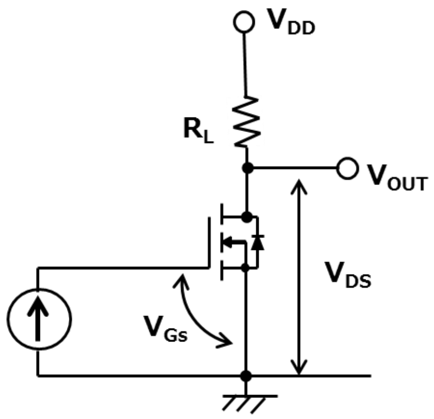


Figure 1.5 Definition of Total Gate Charge, Q_g

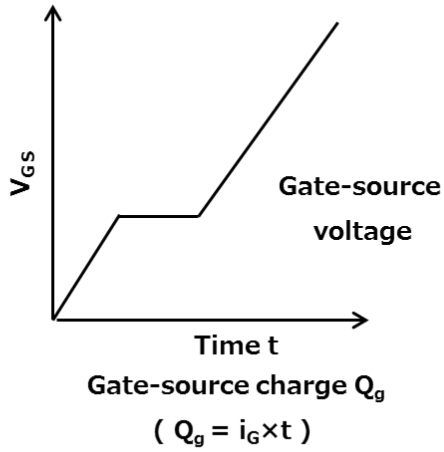
1.3.2. Calculation of Total Gate Charge

During the turn-on of a power MOSFET, a current flows to the gate, charging the gate-source and gate-drain capacitances. The amount of gate charge is measured using a test circuit shown in Figure 1.6 (a). A constant current is applied to the gate to obtain a graph like the one shown in Figure 1.6 (b) showing a change in gate-source voltage V_{GS} over time. The time axis can be expressed in terms of gate capacitance Q_g by multiplying time by constant gate current i_G. Gate charge is calculated as follows:

$$Q_g = \int_0^t i_G(t)dt$$



(a) Gate Charge Test Circuit



(b) Waveform of Gate-Source Voltage

Figure 1.6 Gate Charge

1.3.3. Output charge (Q_{oss})

Q_{oss} is the amount of charge for charging drain-source capacity.

Since the value of C_{oss} of a MOSFET varies with V_{DS} when Q = CV, Q_{oss} is calculated as follows:

$$Q_{OSS} = \int_0^{V_{DS}} C(v)dv$$

where C(v) is a function of the output capacitance C_{oss} that is dependent on V_{DS}.

Q_{oss} is equal to the integral of the C_{oss} (output capacitance) along V_{DS} shown in Figure 1.7, "Capacitance vs V_{DS}."

Q_{oss} affects efficiency in the application such as switching power supplies especially driving in light load.

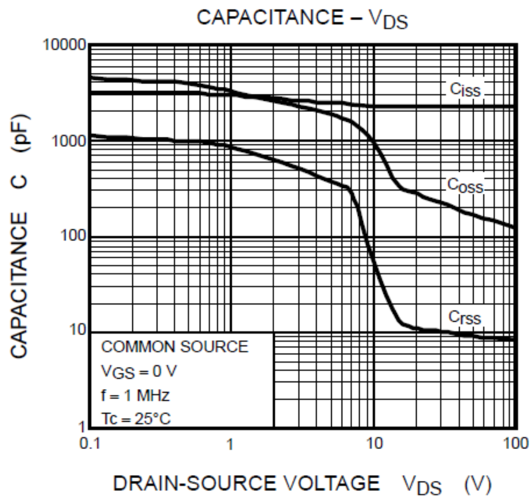


Figure 1.7 Capacitance vs V_{DS}

1.4. Source-Drain Characteristics

(The specified characteristics differ from product to product. Ta=25°C unless otherwise specified.)

Characteristic	Symbol	Unit	Description
Reverse drain current (DC)	I_{DR}	A	The maximum current that can flow to the body diode of a MOSFET in the forward direction
Reverse drain current (pulsed)	I_{DRP}		
Diode forward voltage	V_{DSF}	V	Drain-source voltage that appears when a current is applied to the body diode of a MOSFET in the forward direction
Reverse recovery time	t_{rr}	ns	The time t_{rr} and the amount of charge Q_{rr} required for the reverse recovery current to reach zero during the reverse recovery operation of the body diode under the specified test conditions. The peak current during this period is I_{rr}.
Diode reverse recovery charge	Q_{rr}	μC	
Diode peak reverse recovery current	I_{rr}	A	
Diode dv/dt capability	dv/dt	V/ns	The maximum voltage ramp allowed during the reverse recovery time of the diode

1.4.1. Body Diode Characteristics

A power MOSFET has a circuit structure between source and drain equivalent to a diode. The forward current of the body diode I_{DR} and I_{DRP} are defined on individual product datasheet. Figure 1.9 shows current characteristics of body diode. Reverse breakdown voltage is same as drain-source voltage V_{DSS}.

Regarding the reverse recovery time t_{rr} of the body diode, Figure 1.8 shows an example of a test circuit and waveform.

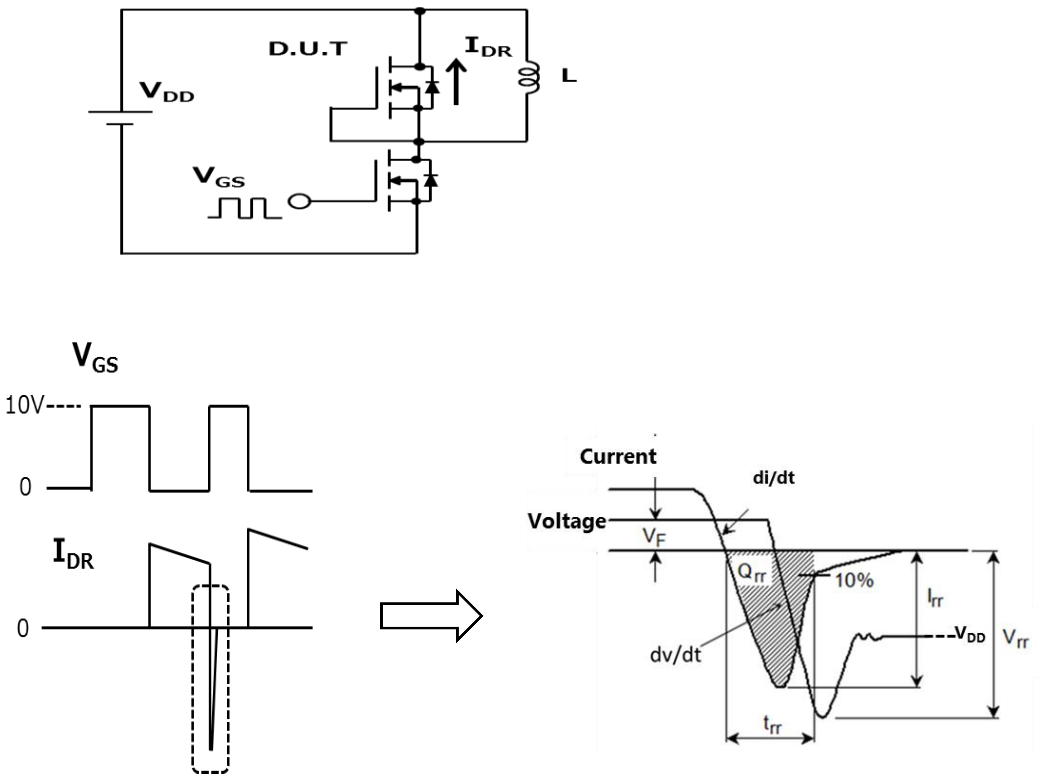


Figure 1.8 Reverse Recovery Time of the Body Diode in a Power MOSFET

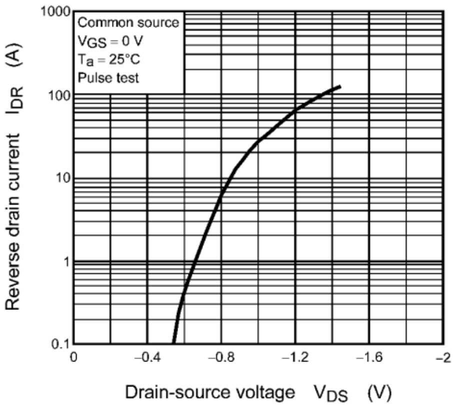
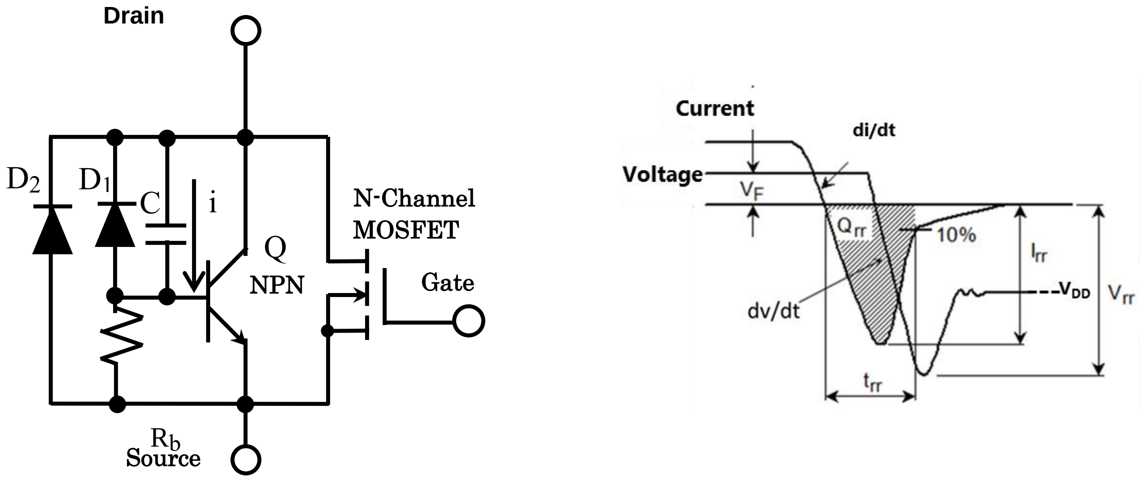


Figure 1.9 I_{DR}–V_{DS} Curve

1.4.2. dv/dt Capability of the Body Diode

When the body diode in a power MOSFET is switched from forward voltage to reverse voltage while a current is flowing, it enters the reverse recovery state. This causes the drain-source voltage to increase sharply. As shown in Figure 1.10, due to a voltage change dv/dt a displacement current, i=C·(dv/dt), flows to the capacitance C of the PN junction between drain and gate, thereby causing a voltage drop by the current i and resistance R_b. This voltage drop, in turn, causes the parasitic NPN transistor to turn on. At this time, if the drain-source voltage V_{DS} is high, the parasitic NPN transistor might enter secondary breakdown. As is the case with the MOSFET dv/dt, the diode might suffer a catastrophic failure, although the failure processes are different.



(a) dv/dt Equivalent Circuit

(b) Waveform of the Body Diode during Reverse Recovery

Figure 1.10 Equivalent Circuit and Reverse Recovery Waveform of the Body Diode

RESTRICTIONS ON PRODUCT USE

Toshiba Corporation and its subsidiaries and affiliates are collectively referred to as “TOSHIBA”.
Hardware, software and systems described in this document are collectively referred to as “Product”.

- TOSHIBA reserves the right to make changes to the information in this document and related Product without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, lifesaving and/or life supporting medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, and devices related to power plant. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT. For details, please contact your TOSHIBA sales representative or contact us via our website.**
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION
https://toshiba.semicon-storage.com/