Power MOSFET Maximum Ratings

Description

This document explains absolute maximum ratings, thermal resistance and safe operating area (SOA) of power MOSFETs.

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1. Absolute Maximum Ratings

1.1. Definition

For power MOSFETs, the maximum allowable current, voltage, power dissipation and other characteristics are specified as maximum ratings.

In circuit design, understanding maximum ratings is very important in order to obtain the best performance from power MOSFETs and maintain device reliability throughout the target operating life.

Maximum ratings must not be exceeded in order to guarantee the lifespan and reliability of devices. For power MOSFETs, maximum ratings are defined using an absolute maximum rating system.

Maximum ratings are the highest absolute values that must not be exceeded even instantaneously under any conditions.

A device may not be able to recover from stress that exceeds a specified maximum rating. None of the absolute maximum ratings may be exceeded. Care should therefore be exercised regarding bounces in supply voltage, variations in the characteristics of electronic devices, possible exposure to stress higher than maximum ratings during circuit adjustment, changes in ambient temperature, fluctuations in the input signal, and other such factors.

For example, power MOSFETs are rated in terms of drain current, pin-to-pin voltage, power dissipation, channel temperature, and storage temperature. These characteristics are interrelated and cannot be considered separately. They also depend on external circuit conditions.

1.2. Parameters Specified as Absolute Maximum Ratings

(The specified characteristics differ from product to product. Ta=25°C unless otherwise specified.)

Characteristic		Symbol	Unit	Description
Drain-source voltage		V_{DSS}	V	The maximum voltage that can be applied across drain and source, with gate and source short-circuited
Gate-source voltage		V_{GSS}	V	The maximum voltage that can be applied across gate and source, with drain and source short-circuited
Drain current	DC	I_D	A	The maximum DC current that can pass through the drain to source
	Pulse	I_{DP}		The maximum allowable peak drain current for pulsed operation
Power dissipation (Tc=25°C)		P_D	W	The maximum power that can be dissipated by a MOSFET
Avalanche current		I_{AS}	A	The maximum peak non-repetitive current that is permitted under avalanche conditions
Avalanche energy		E_{AS}	mJ	The maximum non-repetitive energy that the MOSFET can dissipate under avalanche breakdown conditions
Channel temperature		T_{ch}	°C	The maximum allowable chip temperature at which a MOSFET operates
Storage temperature range		T_{stg}	°C	The maximum temperature at which a MOSFET may be stored without voltage applying
Isolation voltage		$V_{ISO(RMS)}$	V	The maximum voltage at which a MOSFET can maintain isolation between the designated point on the case and electrode leads
Tightening torque		TOR	N·m	The maximum torque that may be applied in the axial direction when tightening a screw

1.2.1. Drain-source voltage (V_{DSS})

The drain-source breakdown voltages of a power MOSFET are defined as follows according to the gate-source bias conditions:

(1) V_{DSS}: Drain-source voltage with gate and source short-circuited. Applying a voltage higher than the rated value may cause a MOSFET to enter the breakdown region and be permanently damaged.
(2) V_{DSX}: Drain-source voltage with gate and source reverse-biased

In addition to V_{DSS} and V_{DSX}, V_{DSR} and V_{DSO} are defined for power MOSFETs. (V_{DSR} is the drain-source voltage with a resistor inserted between gate and source. V_{DSO} is drain-source voltage with gate open-circuited.) Since power MOSFETs have very high input impedance, they should not be used in V_{DSO} mode. In this mode, power MOSFETs are biased between gate and source due to electrostatic induction and enter the conduction mode. Consequently, there is a high probability that they will be permanently damaged.

1.2.2. Gate-source voltage (V_{GSS})

V_{GSS} is the maximum allowable gate-to-source voltage with drain and source short-circuited. This rating depends on the dielectric strength of the gate oxide. For MOSFETs, a permissible value is specified, taking practical voltage and reliability into consideration.

1.2.3. Drain current (I_D)

Generally, the maximum continuous (DC) current that the power MOSFET can pass in the forward direction is specified as I_D, whereas the pulsed current that the power MOSFET can pass in the forward direction is specified as I_{DP}. Likewise, the DC and pulsed currents in the reverse (diode) direction are specified as I_{DR} and I_{DRP}, respectively (under ideal heat dissipation conditions).

However, the maximum current values in the forward direction are limited by the power loss caused by drain-source on-state resistance, and those in the reverse direction are limited by the power loss due to the forward voltage across the diode. Since current ratings are affected by heat dissipation conditions, maximum allowable current values are specified so that the channel temperature will not exceed the rated T_{ch}(max) value.

$$I_D = \sqrt{\frac{T_{ch}(max) - T_c}{R_{DS(on)}(max) \times R_{th(ch-c)}}}$$

$$I_{DP} = \sqrt{\frac{T_{ch}(max) - T_c}{R_{DS(on)}(max) \times r_{th(ch-c)}(t)}}$$

T_{ch}(max): Maximum channel temperature

T_c: Case temperature (25°C)

$R_{th(ch-c)}$: Steady-state thermal resistance

$r_{th(ch-c)}(t)$: Transient thermal resistance

$R_{DS(ON)}$(max): Maximum drain-source on-state resistance at the maximum channel

temperature

The drain current I_D that the MOSFET device can carry is restricted not only by power loss but also by the current-carrying capability of a package, the maximum channel temperature, the safe operating area and other factors.

1.2.4. Power dissipation (P_D)

P_D is the maximum power that the MOSFET can dissipate continuously under the specified thermal conditions.

The allowable power dissipation varies with the conditions under which the MOSFET is used (such as ambient temperature and heat dissipation conditions).

P_D is calculated as the maximum power dissipation for a device with an infinite heat sink at 25°C ambient.

$$P_D = \frac{T_{ch}(max) - 25℃}{R_{th(ch-c)}}$$

P_{DP}, the maximum transient power dissipation, is calculated as follows using the transient thermal resistance value shown in individual MOSFET datasheets.

$$P_{DP} = \frac{T_{ch}(max) - 25℃}{r_{th(ch-c)}(t)}$$

1.2.5. Avalanche current (I_{AS}) and avalanche energy (E_{AS})

When a power MOSFET operates at high speed as a switching device, a high surge voltage is applied across drain and source at the time of turn-off due to the self-inductance of a circuit and stray inductances. This surge voltage occasionally exceeds the rated voltage of the MOSFET, causing it to enter the breakdown region. At this time, avalanche current passes through the power MOSFET. Avalanche current exceeding the current or energy limit causes permanent damage to the MOSFET. This phenomenon is called avalanche breakdown. I_{AS} is the maximum allowable avalanche current, and E_{AS} is the maximum allowable avalanche energy.

(1) MOSFET Equivalent Circuit

Figure 1.1 and Figure 1.2 show the cross section and equivalent circuit of a MOSFET.

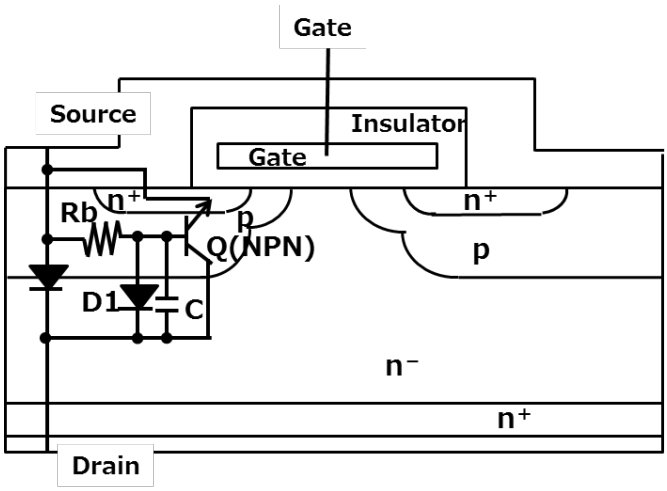


Figure 1.1 Cross Section of a MOSFET (Parasitic NPN Transistor)

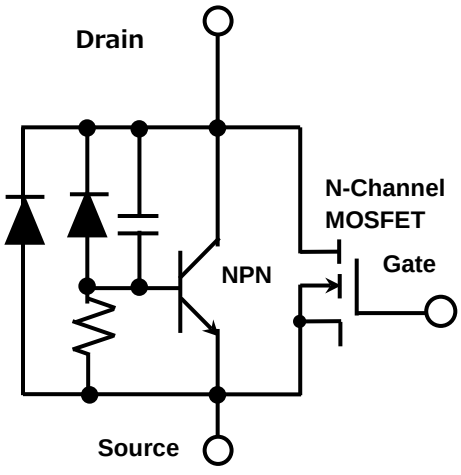


Figure 1.2 MOSFET Equivalent Circuit

(3) Avalanche operation

Avalanche breakdown occurs in the following two modes. Figure 1.3 shows an equivalent circuit model for avalanche current.

(a). Avalanche current breakdown

If a voltage higher than the withstand voltage is applied across drain and source, current i flows through resistor R_b. As a result, a forward voltage, i × R_b, appears across the base and emitter of the transistor. If current i exceeds the permissible level, the parasitic NPN transistor turns on. When this happens, a large current flows through the transistor, resulting in the destruction of the device.

(b). Avalanche energy breakdown

If a voltage higher than the withstand voltage is applied across drain and source, current i flows. Because of this current and the applied voltage (i × BV_{DSS}), a power loss occurs. The resulting energy causes the device temperature to increase. The device is destroyed if it exceeds the rated channel temperature.

(4) Avalanche ruggedness and its measurement

Figure 1.4 shows the test circuit for the avalanche capability of a power MOSFET. Figure 1.5 shows waveforms during avalanche breakdown.

If the gate voltage V_{GS} drops below the threshold at turn-off, the drain current flowing through inductor L decreases, causing a sharp increase in drain-source voltage V_{DS}. When V_{GS} is higher than the threshold voltage, I_D flows through the channel region of a power MOSFET. However, when V_{GS} drops below the threshold voltage, the channel is shut off, causing I_D to flow through the diode between drain and base (Figure 1.3). When this happens, V_{DS} begins to increase. When it reaches the self-breakdown voltage, BV_{DSS} (actual value), the power MOSFET experiences avalanche breakdown, and V_{DS} levels off.

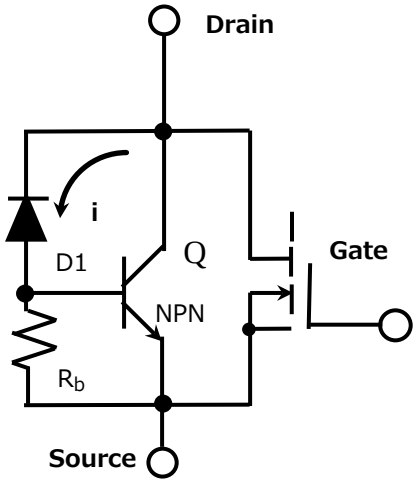


Figure 1.3 Equivalent Circuit Model for Avalanche Current

The energy stored in L is transformed into heat, causing a rise in device temperature. As a result, I_D drops to zero, and V_{DS} becomes equal to the supply voltage, V_{DD}. Avalanche current, I_{AS}, is the peak current allowed during avalanche breakdown. Avalanche energy, E_{AS}, is the maximum energy permissible at this time.

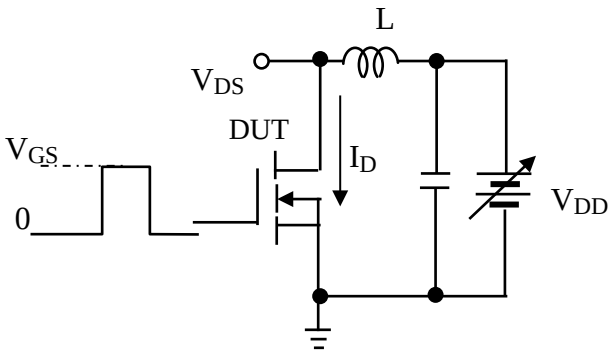


Figure 1.4 Typical Avalanche Test Circuit

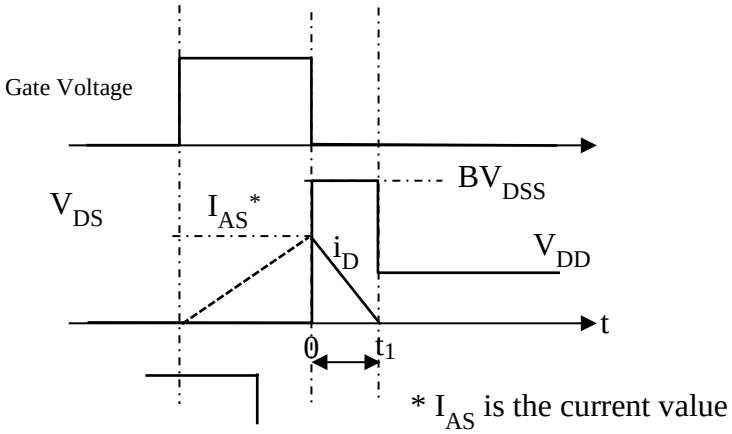


Figure 1.5 Waveforms During Avalanche Breakdown

(5) Avalanche energy calculation

Avalanche energy is calculated as follows:

$$\text{From } \Delta V = -L\frac{di_D}{dt}$$

$$BV_{DSS} - V_{DD} = -L\frac{di_D}{dt}$$

$$di_D = -\frac{BV_{DSS} - V_{DD}}{L}dt$$

$$i_D(t) = I_{AS} - \left(\frac{BV_{DSS} - V_{DD}}{L}\right)t$$

$$E_{AS} = \int_0^{t_1} i_D(t) \cdot BV_{DSS} dt$$
$$= \int_0^{t_1} \left\{ I_{AS} - \left(\frac{BV_{DSS} - V_{DD}}{L} \right) t \right\} \cdot BV_{DSS} dt$$
$$= \left[I_{AS} BV_{DSS} t - \frac{1}{2} \left(\frac{BV_{DSS} - V_{DD}}{L} \right) BV_{DSS} t^2 \right]_0^{t_1}$$

Substituting the following into t_1,

$$t_1 = \frac{I_{AS} L}{BV_{DSS} - V_{DD}}$$

and solving the equation gives:

$$\boldsymbol{E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}}$$

1.2.6. Channel temperature (T_{ch}) and storage temperature (T_{stg})

The materials that constitute a power MOSFET and their reliability determine the maximum channel temperature T_{ch}(max). The maximum channel temperature must be considered not only in terms of the functional operation of the power MOSFET, but also in terms of its reliability such as device degradation and lifetime.

Generally, degradation of the power MOSFET accelerates as the channel temperature increases. Let A and B be constants intrinsic to a transistor. Then, the average life in hours of operation L_m and the channel temperature in Kelvin (K) T_{ch} has the following relationship:

$$\log L_m = A + \frac{B}{T_{ch}}$$

Therefore, for power MOSFETs that must have a long-term guaranteed service life, the maximum channel temperature is determined, considering the defect rate and reliability requirements.

Storage temperature T_{stg} is the temperature range in which a power MOSFET can be stored without voltage applying. The materials that constitute the power MOSFET and their reliability also determine the storage temperature range.

1.2.7. Isolation voltage ($V_{ISO(RMS)}$)

For devices housed in a fully molded package, isolation voltage represents the level of electrical isolation between the designated point on the case and the internal circuit and electrode terminals.

$V_{ISO(RMS)}$ is tested by applying AC voltage to the power MOSFET for a specified period of time. Isolation voltage is specified as the RMS of AC voltage.

1.2.8. Tightening torque (TOR)

When attaching MOSFET devices to a thermal fin, the prescribed tightening torque must be followed.

If the torque is too low, the mounting screws will loosen. If the torque is too high, the device could be damaged.

2. Thermal Resistance

2.1. What Is Thermal Resistance?

Thermal resistance is the ability of a material to resist the flow of thermal energy.

The power consumed by a semiconductor chip is converted into heat, which is transferred to the case (package) and eventually released into ambient air through a thermal fin or other thermally conductive material. An increase in power dissipation (P_D) causes a further increase in the device temperature (ΔT).

ΔT can be calculated as $\Delta T = R_{th} \times P_D$. Here, R_{th} is a constant defining a relationship between ΔT and P_D. This constant is called thermal resistance.

2.2. Thermal Resistance Calculation

The most commonly used thermal resistance values are:

$R_{th(ch\text{-}c)}$: Channel-to-case thermal resistance

$$R_{th(ch-c)} = \frac{T_{ch}(max) - 25°C}{P_D(T_c = 25°C)} \ (°C/W)$$

This is the thermal resistance of a device with an infinite heat sink when the case temperature is kept constant at an ambient temperature of 25°C.

$R_{th(ch\text{-}a)}$: Channel-to-ambient thermal resistance

$$R_{th(ch-a)} = \frac{T_{ch}(max) - 25°C}{P_D(T_a = 25°C)} \ (°C/W)$$

This is a thermal resistance from the channel to the ambient air at 25°C. It is equal to $R_{th(ch\text{-}c)} + R_{th(c\text{-}a)}$.

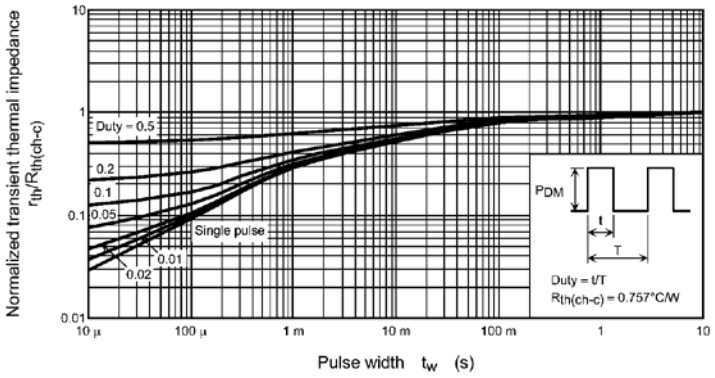
Note, however, that thermal resistance varies with board assembly condition and other factors.

2.3. Transient Thermal Impedance and Steady-State Thermal Resistances

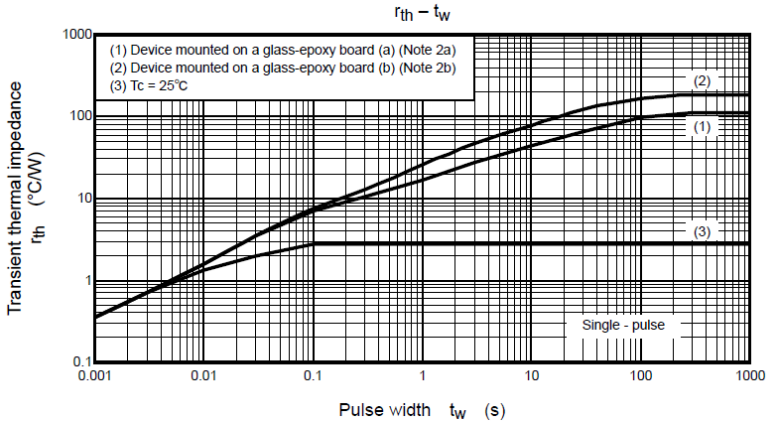
Transient thermal impedance is a function of time while the device is affected by thermal capacitance. It varies with the duty cycle of the pulse being applied.

Steady-state thermal resistance is a property during the time the device is no longer affected by thermal capacitance.

Figure 2.1 (a) and Figure 2.1 (b) show examples of transient thermal impedance curves as normalized and absolute values, respectively.



(a) Transient Thermal Impedance (Normalized)



(b) Transient Thermal Impedance (Absolute)

Figure 2.1. Transient Thermal Impedance Curves

3. Safe Operating Area (SOA)

3.1. Forward-Bias Safe Operating Area

In a power MOSFET, current is not apt to concentrate in a small area. Therefore, unlike bipolar transistors, power MOSFETs are not generally vulnerable to secondary breakdown in a high voltage region.

However, as device geometries shrink, some power MOSFET devices have begun to exhibit a failure mode resembling secondary breakdown. As shown in Figure 3.1, the safe operating area SOA of such power MOSFETs is not limited by a line of a certain fixed power.

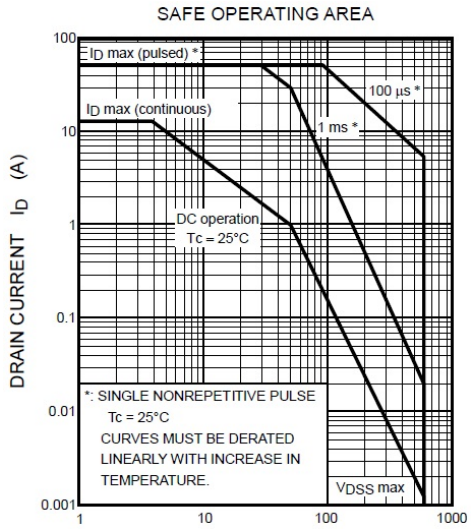


Figure 3.1 Example of an SOA with Varying Power Lines

3.2. Restrictions of a Safe Operating Area

The safe operating area is limited by current, on-state resistance, heat, secondary breakdown and voltage as follows:

1. Current limit

   #1 defines the area limited by the drain current rating. For continuous-current (DC) operation, the SOA is constrained by $I_D$max. For pulsed operation, the SOA is bound by the I_{DP}max line.

2. On-state resistance limit

   #2 defines the area that is theoretically constrained by the on-state resistance ($R_{DS(ON)}$max). I_D is equal to $V_{DS}/R_{DS(ON)}$.

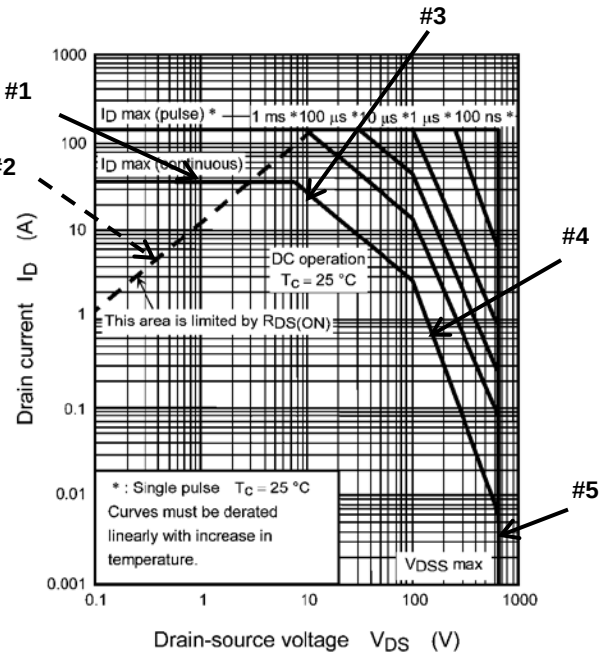


Figure 3.2 Safe Operating Area

3. Thermal limit

   #3 is the area constrained by the power dissipation P_D.

   P_D (power dissipation) = $I_D \times V_{DS}$

4. Limit imposed by secondary breakdown

With shrinking device geometries, some power MOSFETs have exhibited a failure mode resembling secondary breakdown in recent years. #4 represents the SOA bound by the secondary breakdown constraint.

5. Voltage limit

#5 defines the area constrained by the drain-source voltage V_{DSS}.

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