

TC7MZ138FK

Low Voltage 3-to-8 Line Decoder with 5 V Tolerant Inputs and Outputs

The TC7MZ138FK is a high performance CMOS 3-to-8 decoder.

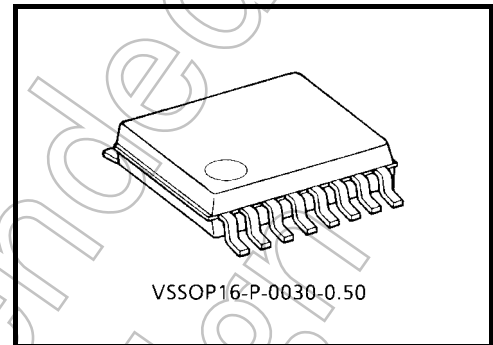
Designed for use in 3.3 V systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

The device is designed for low-voltage (3.3 V) VCC applications, but it could be used to interface to 5 V supply environment for inputs.

When the device is enabled, 3 binary select inputs (A, B and C) determine which one of the outputs ($\bar{Y}0 - \bar{Y}7$) will go low.

When enable input G1 is held low or either $\bar{G}2A$ or $\bar{G}2B$ is held high, decoding function is inhibited and all outputs go high. G1, $\bar{G}2A$, and $\bar{G}2B$ inputs are provided to ease cascade connection and for use as an address decoder for memory systems.

All inputs are equipped with protection circuits against static discharge.

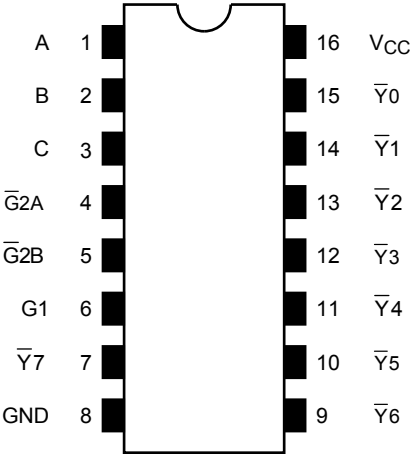


Weight: 0.02 g (typ.)

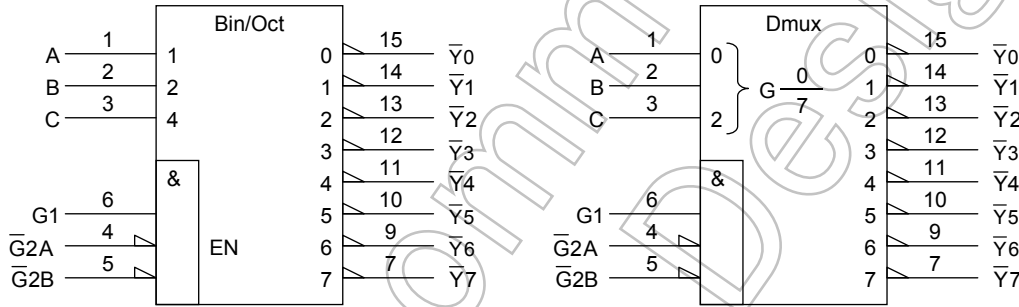
Features

- Low voltage operation: $V_{CC} = 2.0 \sim 3.6$ V
- High speed operation: $t_{pd} = 6.0$ ns (max) ($V_{CC} = 3.0 \sim 3.6$ V)
- Output current: $|I_{OH}|/I_{OL} = 24$ mA (min) ($V_{CC} = 3.0$ V)
- Latch-up performance: -500 mA
- Package: VSSOP (US16)
- Power down protection is provided on all inputs and outputs.
- Pin and function compatible with the 74 series (74AC/VHC/HCF/ALS/LS etc.) 138 type.

Pin Assignment (top view)



IEC Logic Symbol

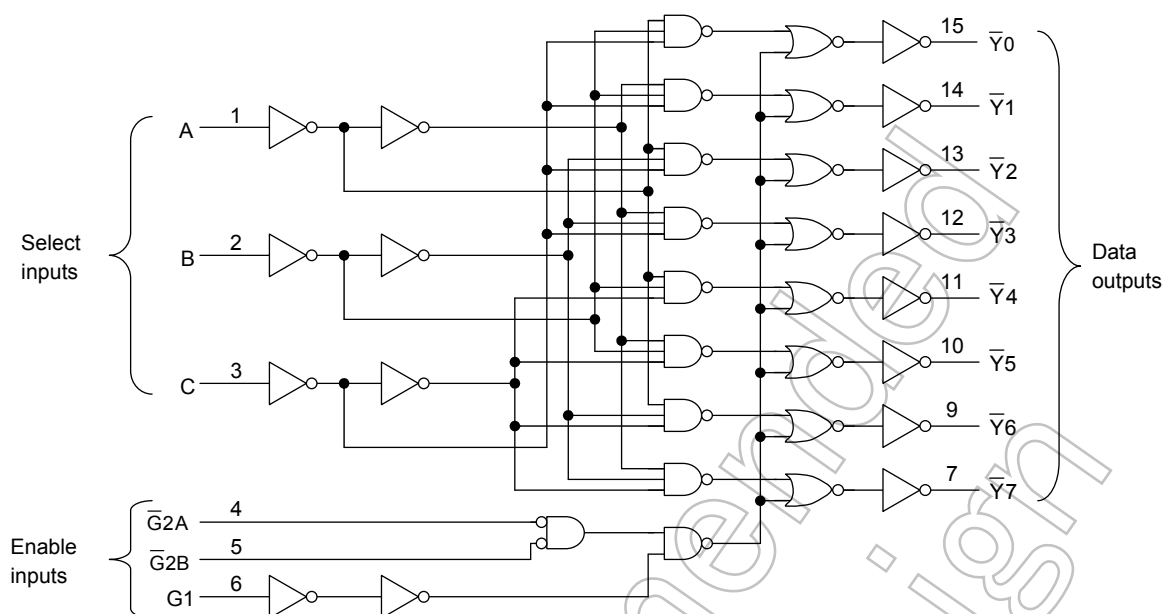


Truth Table

Inputs						Outputs								Selected Output
Enable			Select			$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$	
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A									
L	X	X	X	X	X	H	H	H	H	H	H	H	H	None
X	H	X	X	X	X	H	H	H	H	H	H	H	H	None
X	X	H	X	X	X	H	H	H	H	H	H	H	H	None
H	L	L	L	L	L	L	H	H	H	H	H	H	H	$\overline{Y0}$
H	L	L	L	L	H	H	L	H	H	H	H	H	H	$\overline{Y1}$
H	L	L	L	H	L	H	H	L	H	H	H	H	H	$\overline{Y2}$
H	L	L	L	H	H	H	H	H	L	H	H	H	H	$\overline{Y3}$
H	L	L	H	L	L	H	H	H	H	L	H	H	H	$\overline{Y4}$
H	L	L	H	L	H	H	H	H	H	H	L	H	H	$\overline{Y5}$
H	L	L	H	H	L	H	H	H	H	H	H	L	H	$\overline{Y6}$
H	L	L	H	H	H	H	H	H	H	H	H	H	L	$\overline{Y7}$

X: Don't care

System Diagram



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	$-0.5 \sim 7.0$	V
DC input voltage	V_{IN}	$-0.5 \sim 7.0$	V
DC output voltage	V_{OUT}	$-0.5 \sim 7.0$ (Note 2)	V
		$-0.5 \sim V_{CC} + 0.5$ (Note 3)	
Input diode current	I_{IK}	-50	mA
Output diode current	I_{OK}	± 50 (Note 4)	mA
DC output current	I_{OUT}	± 50	mA
Power dissipation	P_D	180	mW
DC V_{CC} /ground current	I_{CC}/I_{GND}	± 100	mA
Storage temperature	T_{stg}	$-65 \sim 150$	$^{\circ}\text{C}$

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: $V_{CC} = 0 \text{ V}$

Note 3: High or low state. I_{OUT} absolute maximum rating must be observed.

Note 4: $V_{OUT} < \text{GND}$, $V_{OUT} > V_{CC}$

Operating Ranges (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0~3.6	V
		1.5~3.6 (Note 2)	
Input voltage	V_{IN}	0~5.5	V
Output voltage	V_{OUT}	0~5.5 (Note 3)	V
		0~ V_{CC} (Note 4)	
Output current	I_{OH}/I_{OL}	± 24 (Note 5)	mA
		± 12 (Note 6)	
Operating temperature	T_{opr}	-40~85	°C
Input rise and fall time	dt/dv	0~10 (Note 7)	ns/V

Note 1: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either VCC or GND.

Note 2: Data retention only

Note 3: $V_{CC} = 0$ V

Note 4: High or low state

Note 5: $V_{CC} = 3.0\sim 3.6$ V

Note 6: $V_{CC} = 2.7\sim 3.0$ V

Note 7: $V_{IN} = 0.8\sim 2.0$ V, $V_{CC} = 3.0$ V

Electrical Characteristics

DC Characteristics ($T_a = -40\sim 85^\circ\text{C}$)

Characteristics		Symbol	Test Condition		V _{CC} (V)	Min	Max	Unit
Input voltage	High level	V _{IH}			2.7~3.6	2.0	—	V
	Low level	V _{IL}	—		2.7~3.6	—	0.8	
Output voltage	High level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -100 μA	2.7~3.6	V _{CC} - 0.2	—	V
				I _{OH} = -12 mA	2.7	2.2	—	
				I _{OH} = -18 mA	3.0	2.4	—	
				I _{OH} = -24 mA	3.0	2.2	—	
	Low level	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100 μA	2.7~3.6	—	0.2	
				I _{OL} = 12 mA	2.7	—	0.4	
				I _{OL} = 16 mA	3.0	—	0.4	
				I _{OL} = 24 mA	3.0	—	0.55	
Input leakage current		I _{IN}	V _{IN} = 0~5.5 V	2.7~3.6	—	±5.0	μA	
Power off leakage current		I _{OFF}	V _{IN} /V _{OUT} = 5.5 V	0	—	10.0	μA	
Quiescent supply current		I _{CC}	V _{IN} = V _{CC} or GND	2.7~3.6	—	10.0	μA	
			V _{IN} = 3.6~5.5 V	2.7~3.6	—	±10.0		
Increase in I _{CC} per input		ΔI _{CC}	V _{IH} = V _{CC} - 0.6 V	2.7~3.6	—	500		

AC Characteristics (Ta = -40~85°C)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Min	Max	Unit
Propagation delay time (A, B, C- \bar{Y})	t_{pLH}	Figure 1, Figure 2	2.7	—	7.0	ns
	t_{pHL}		3.3 ± 0.3	1.5	6.0	
Propagation delay time (G1- \bar{Y})	t_{pLH}	Figure 1, Figure 2	2.7	—	8.0	ns
	t_{pHL}		3.3 ± 0.3	1.5	7.0	
Propagation delay time ($\bar{G}2$ - \bar{Y})	t_{pLH}	Figure 1, Figure 2	2.7	—	7.0	ns
	t_{pHL}		3.3 ± 0.3	1.5	6.0	
Output to output skew	t_{osLH}	(Note)	2.7	—	—	ns
	t_{osHL}		3.3 ± 0.3	—	1.0	

Note: This parameter is guaranteed by design.

$$(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$$

Dynamic Switching Characteristics

(Ta = 25°C, Input: $t_r = t_f = 2.5$ ns, $C_L = 50$ pF, $R_L = 500 \Omega$)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Typ.	Unit
Quiet output maximum dynamic	V _{OL}	V _{OLP} V _{IH} = 3.3 V, V _{IL} = 0 V	3.3	0.8	V
Quiet output minimum dynamic	V _{OL}	V _{OLV} V _{IH} = 3.3 V, V _{IL} = 0 V	3.3	0.8	V

Capacitive Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Typ.	Unit
Input capacitance	C _{IN}		3.3	7	pF
Output capacitance	C _{OUT}		0	8	pF
Power dissipation capacitance	C _{PD}	f _{IN} = 10 MHz (Note)	3.3	25	pF

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

AC Test Circuit

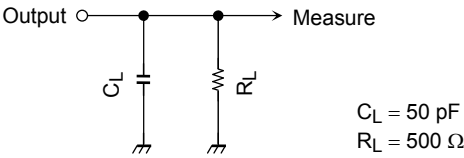


Figure 1

AC Waveform

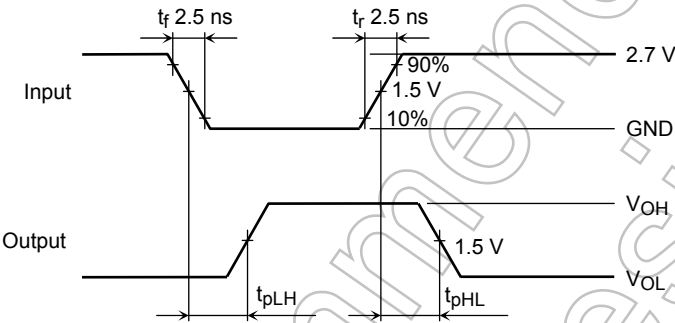
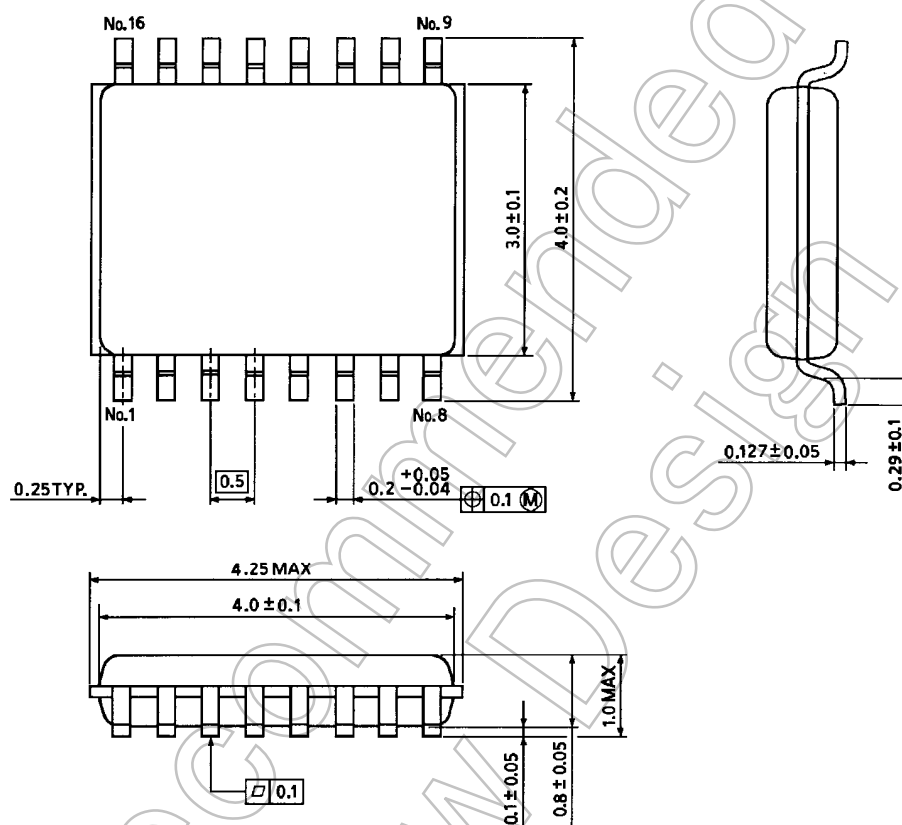


Figure 2 t_{pLH} , t_{pHL}

Package Dimensions

VSSOP16-P-0030-0.50

Unit : mm



Weight: 0.02 g (typ.)

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