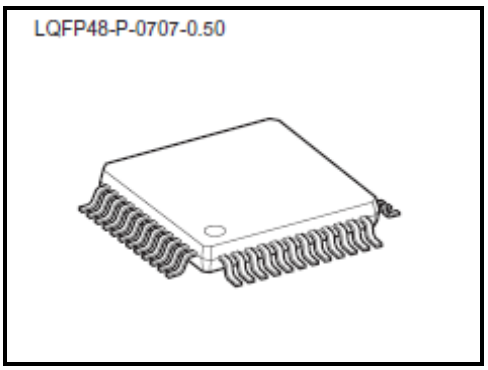
TOSHIBA Bi-CD Integrated Circuit Silicon Monorithic

# TB9068FG

## 3-phase DC Brushless Motor Driver with LIN Driver and 5V Regulator

TB9068FG is a Small size 3-Phase DC Brushless Motor Controller LSI for Automotive which uses ether external HALL sensor or HALL IC for Motor position detection and can directly drive a Motor. For external MCU the TB9068FG build-in 5V Regulator, Watchdog Timer and a LIN Bus transceiver. TB9068FG provide 2 type operation Modes. One mode is to control Motor by Built-in LOGIC controller for 120deg, Square operation The other mode is to control Motor by external MCU which can achieve complicated Motor control.




Weight: 0.189 g (Typ.)

### Features

・ MOTOR Drive
120deg. Square wave operation by internal LOGIC controller (MODE0)
：Motor drive signal is made by internal LOGIC.
Rotation control (CCW/CW), PWM (L-side) INPUT, BRAKE control INPUT
MCU controlled Operation（MODE1）
：MOTOR control signal by 6 INPUTs and PWM by MCU.

・Half Bridge Driver: 3ch Built-in

・Various Abnormal Detection circuits and Diagnostics output.
：Over Current Detection / Over Temp. Detection / Over Voltage Detection

・ On-chip 5V regulator
Output Voltage 5.05V (typ.)
Current Limiter : Limit current is adjusted by external resistor
RESET Function: Under Voltage Detection for 5V／Power On RESET／Watch Dog Timer

・ LIN Transceiver : Ver. 1.3 based

・ Operating Voltage range: 7 to18V

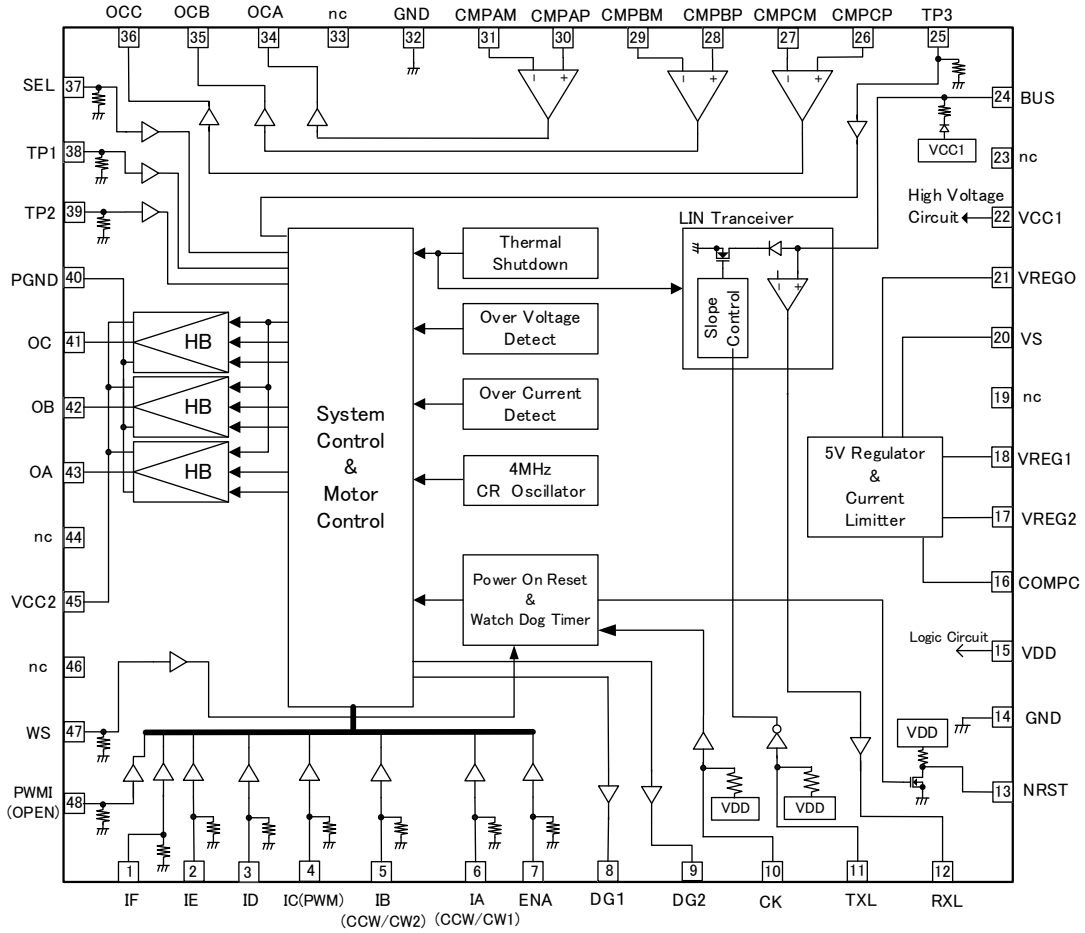
・ Operating TEMP. range : -40 to125℃

・ Built-in CR Oscillator (4MHz)

・ Package : LQFP-48pin (0.5mm pitch)

If there are description that ”[[G]]/RoHS COMPATIBLE”、”[[G]]/RoHS [[Chemical symbol(s) of controlled substance(s)”、”RoHS COMPATIBLE” or ”RoHS COMPATIBLE, [[Chemical symbol(s) of controlled substance(s)]]>MCV” in packing box’s label, the product corresponds to Europe RoHS order (2011 / 65 / EU).

## INTERNAL BLOCK DIAGRAM AND PIN LAYOUT




HB: Half Bridge Driver
nc: No internal connection PIN (open in CHIP)
PWMI (open): External PWM Input for MODE1. Keep open in MODE0
IC(PWM): External PWM Input in MODE0. Motor control Input signal in MODE1
IA(CCW/CW1): Motor rotation direction control in MODE0. Motor control Input signal in MODE1
IB(CCW/CW2): Motor rotation direction control in MODE0. Motor control Input signal in MODE1
Slope Control: Slope control circuit for LIN driver to keep LIN ver.1.3 Slope Spec.

Note: Some of the functional blocks,circuit,or constants in the block diagram may be omitted or simplified for explanatory purpose.

**PIN DESCRIPTION**

| PIN No | PIN NAME | DEFINITION | IN / OUT | CIRCUIT | Notes |
|---|---|---|---|---|---|
| 1 | IF (SC)* | MOTOR control signal input F (SC HALL sensor signal input)* | IN | CMOS | 120kΩ Pull Down |
| 2 | IE (SB)* | MOTOR control signal input E (SB HALL sensor signal input)* | IN | CMOS | 120kΩ Pull Down |
| 3 | ID (SA)* | MOTOR control signal input D (SA HALL sensor signal input)* | IN | CMOS | 120kΩ Pull Down |
| 4 | IC (PWM)* | MOTOR control signal input C (PWM control signal input)* | IN | CMOS | 120kΩ Pull Down |
| 5 | IB (CCW/CW2)* | MOTOR control signal input B (MOTOR rotation control input2)* | IN | CMOS | 120kΩ Pull Down |
| 6 | IA (CCW/CW1)* | MOTOR control signal input A (MOTOR rotation control input1)* | IN | CMOS | 120kΩ Pull Down |
| 7 | ENA (NBRAKE)* | MOTOR control signal enable input(BRAKE control signal input)* | IN | CMOS | 50kΩ Pull Down |
| 8 | DG1 | Diagnostic signal output 1 | OUT | CMOS | - |
| 9 | DG2 | Diagnostic signal output 2 | OUT | CMOS | - |
| 10 | CK | Input signal to detect WATCH DOG error | IN | CMOS | 50kΩ Pull Up |
| 11 | TXL | LIN input signal from MCU | IN | CMOS | 50kΩ Pull Up |
| 12 | RXL | LIN output signal to MCU | OUT | CMOS | - |
| | | | | | |
| 13 | NRST | RESET output signal | OUT | NMOS | 10kΩ Pull Up |
| 14 | GND | Ground | - | - | Ground |
| 15 | VDD | Power input for CMOS LOGIC | - | - | - |
| 16 | COMPC | Terminal of Capacitor for phase compensation | OUT | Bip | - |
| 17 | VREG2 | 5V monitor input | IN | Bip | connected VREG1 and VREG2 in CHIP |
| 18 | VREG1 | 5V monitor input | IN | Bip | connected VREG1 and VREG2 in CHIP |
| 19 | nc | - | - | - | keep open |
| 20 | VS | Monitor input terminal for current of 5V Regulator. | IN | Bip | 70kΩ(VS-VREGO) |
| 21 | VREGO | External PNP Transistor. control output signal | OUT | Bip | |
| 22 | VCC1 | Power input for ANALOG | - | - | - |
| 23 | nc | - | - | - | keep open |
| 24 | BUS | LIN BUS terminal | IN/ OUT | Bip/ HVMOS | 30kΩ Pull Up |

**PIN DESCRIPTION (cont.)**

| PIN No | PIN NAME | DEFINITION | IN / OUT | CIRCUIT | Notes |
|---|---|---|---|---|---|
| 25 | TP3 | TEST enable input | IN | CMOS | 50kΩ Pull Down<br>keep open |
| 26 | CMPCP | C comparator input signal (+) | IN | Bip | operation at 5V |
| 27 | CMPCM | C comparator input signal (-) | IN | Bip | |
| 28 | CMPBP | B comparator input signal (+) | IN | Bip | |
| 29 | CMPBM | B comparator input signal (-) | IN | Bip | |
| 30 | CMPAP | A comparator input signal (+) | IN | Bip | |
| 31 | CMPAM | A comparator input signal (-) | IN | Bip | |
| 32 | GND | Ground | - | - | ground |
| 33 | nc | - | - | - | keep open |
| 34 | OCA | A comparator output signal | OUT | CMOS | operation at 5V |
| 35 | OCB | B comparator output signal | OUT | CMOS | |
| 36 | OCC | C comparator output signal | OUT | CMOS | |
| | | | | | |
| 37 | SEL | MODE select input | IN | CMOS | 50kΩ Pull Down |
| 38 | TP1 | TEST input | IN | CMOS | 50kΩ Pull Down<br>keep open |
| 39 | TP2 | TEST input | IN | CMOS | 50kΩ Pull Down<br>keep open |
| 40 | PGND | MOTOR drive Ground | - | - | - |
| 41 | OC | MOTOR drive output signal C | OUT | Bip /HVMOS | RonH = 1Ω（Typ.）<br>RonL = 1Ω（Typ.） |
| 42 | OB | MOTOR drive output signal B | OUT | Bip /HVMOS | |
| 43 | OA | MOTOR drive output signal A | OUT | Bip /HVMOS | |
| 44 | nc | - | - | - | keep open |
| 45 | VCC2 | Battery power input terminal | - | - | - |
| 46 | nc | - | - | - | keep open |
| 47 | WS | WATCH DOG TIMER enable input signal | IN | CMOS | 50kΩ Pull Down |
| 48 | PWMI (open)* | PWM signal input in MODE1<br>keep open in MODE0 | IN | CMOS | 120kΩ Pull Down<br>keep open in MODE0 |

Note1：HVMS: Pch, Nch MOS work at VCC2

Note2：CMOS: Pch, Nch MOS work at 5V

Note3：Electrically this pin completely open.

Note 4 ：* Sign and “( )” of pin description is in case of MODE0.

## FUNCTIONAL DESCRIPTION

### (1) 5V Regulator Circuit and Current Limiter Circuit

The on-chip linear 5V regulator is designed to operate an external series PNP power transistor to grant thermal stability over a wide range of car battery voltages. The phase compensation capacitor is placed between PIN “COMPC” and collector of the external PNP Transistor. A wide range of output
currents can be realized by choosing an appropriate external PNP transistor.
The maximum base current output is max -1 mA.

The current is controlled via sense resistor between “VS” and “VCC1”. When voltage across the sense resistor exceeds VLIMIT then the terminal “VREGO” is OFF and cut the current to keep the constant output voltage of 5V regulator. It keeps the output alive but limiting to the maximum allowed current trying to keep an external MCU alive even if there is a problem with over current.
It is possible to disable the over current detection by connecting “VS” and “VCC1” directly.

Detected Current: i = (VCC1-VLIMIT)/R VLIMIT: VCC1-0.4 to VCC1-0.15V

Note :

- Make sure driver output “VREGO” is correctly connected to the Base of external PNP transistor. In case this terminal is for example connected to GND the LSI cannot work properly and in worst case may be destroyed.
  When the BASE of this Transistor is connected or shorted to VCC1, external PNP Transistor is OFF and output voltage of Regulator is OFF.
- Connecting PIN “VS” to VCC1,VCC2 or GND will make damage the LSI.
- Do not short the COMPC pin to the VCC1 pin. The 5V power circuit does not work properly. Also, please do not short to GND. It causes IC destruction.
- When PIN ”VREG1”,”VREG2” are open, external PNP Transistor cannot be controlled properly and output Voltage of PIN ”VREG” may exceed 5V. And in worst case destroying the 5V LOGIC. When power is supplied to LSI, please double-check if the collector of external PNP Transistor is connected to PIN ”VREG” properly.

### (2) RESET Circuit（see the following timing charts)

#### 1. 5V Low Voltage Detection (Power On RESET)

This function detects if Output voltage of 5V Regulator has dropped below certain threshold level using the internal BAND GAP as reference.
For system stability a hysteresis voltage was set-up between the RESET detection voltage (VRSTL) and RESET cancelation voltage (VRSTH).
Even when using an external voltage regulator, the voltage drop is detected by comparing to the internal high quality BAND GAP reference.

#### 2. Power On RESET Timer and WATCH DOG TIMER (at internal OSC 4MHz(Typ.))

Output Pin “NRST” will output “L” 25ms (typ.) after power ON or during WATCH DOG Timer released RESET signal.
And after RESET is canceled, PIN “NRST” outputs H which is thru internal Pull Up Resistor (10KΩ). After releasing Power ON RESET (in the case of PIN ”WS”=L) , system changes to WATCH DOG TIMER MODE and waits for an input signal from PIN ”CK” for 50ms.(=TWD Typ.).If the signal from PIN “CK” did not occur during TWD, PIN “NRST” changes output to L for about 5ms (TRST).

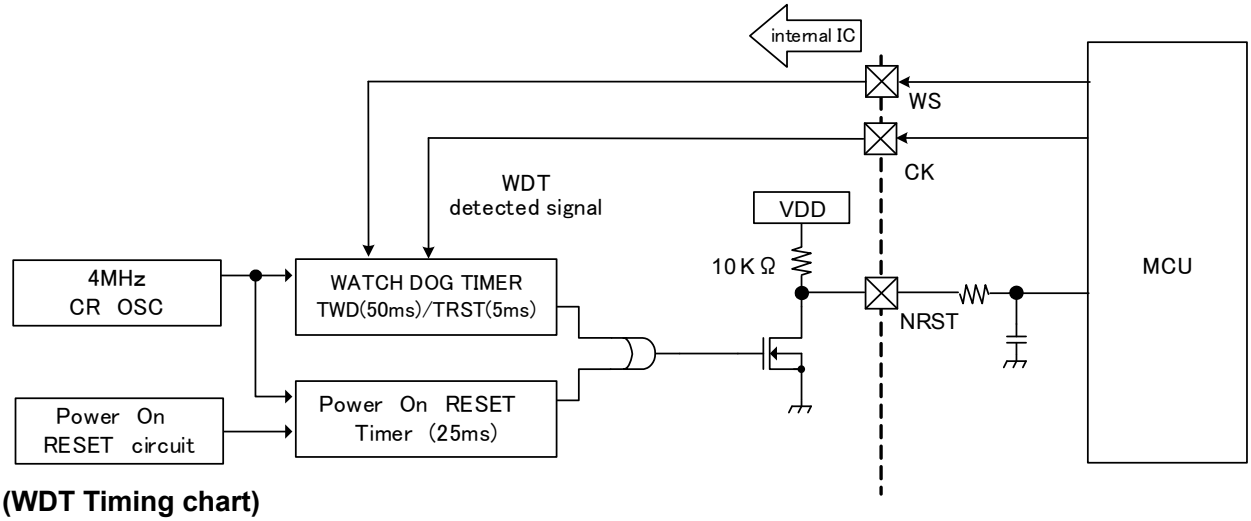
## 3. WATCH DOG TIMER (at internal OSC 4MHz(Typ.))

TB9068FG has a built-in WATCH DOG TIMER (WDT). This function can be enabled/disabled by PIN “WS”.

WS = L: WDT enable
WS = H: WDT disable (but Power ON RESET works independently)

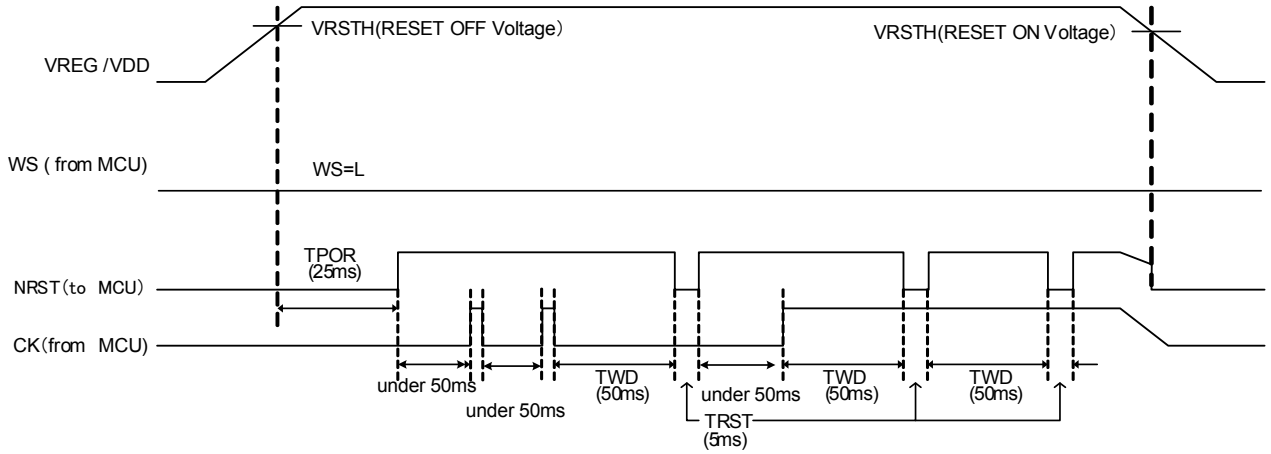
When WDT is enabled (WS=L), it waits for an activity signal from the MCU at the input PIN “CK”. When this signal does not change during 50ms (Typ.), PIN “NRST” outputs L for 5ms (Typ.). After that WDT restarts to count the time.

**(PIN “NRST” circuit configuration and diagram)**

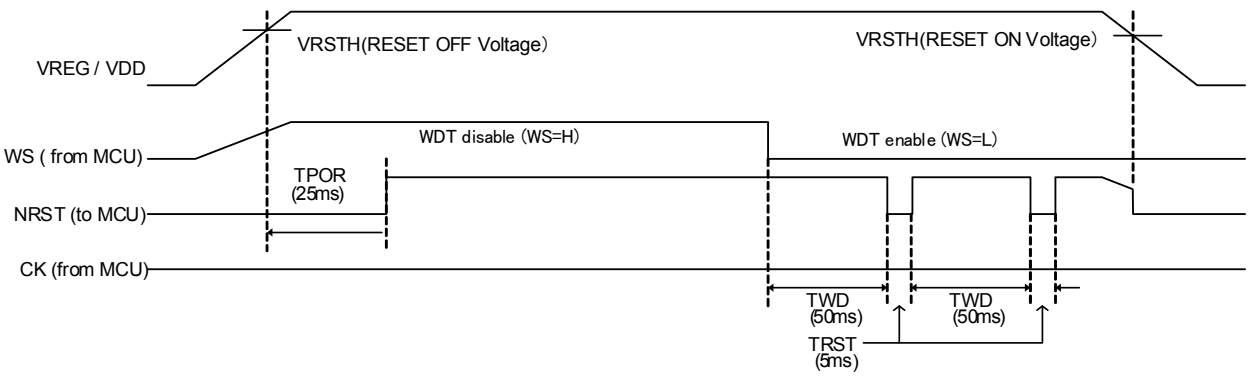



**(WDT Timing chart)**

**(WDT enable: WS=L)**




**(WDT disable: WS=H)**



### (3) 4MHz INTERNAL CR OSCILLATOR

TB9068FG has a built-in 4MHz CR Oscillator which is operated from the internal stable 5V voltage. This clock is used for all internal timing purposes.

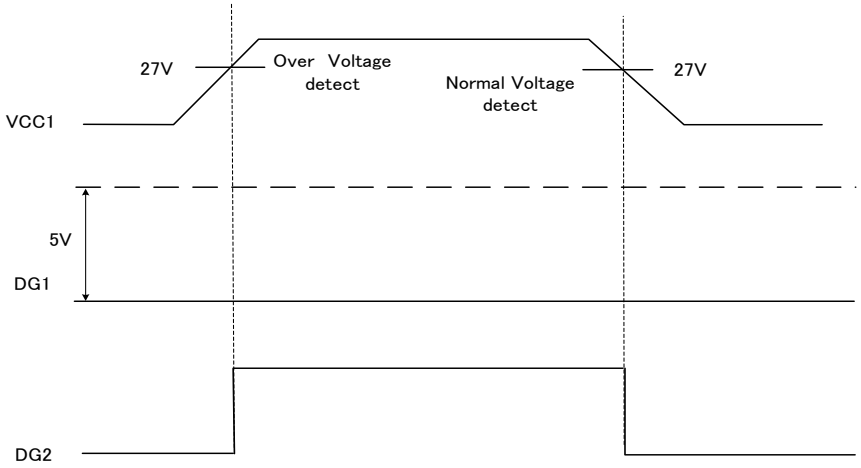
### (4) DIAGNOSTIC CIRCUIT (DG1,DG2)

TB9068FG has the Over Current / Over Voltage / Over Temperature Detection Circuit with a diagnostic monitor output “DG1” and “DG2”. It outputs failures by changing the Level of "DG1" and/or "DG2" from L to H. When respective condition has come to an end (return to normal), each output pin returns to L (Normal).

| PIN “DG1” | PIN “DG2” | Detected abnormal |
|---|---|---|
| L | L | Normal |
| H | L | Detect Over Current |
| L | H | Detect Over Temperature<br>or Over Voltage |
| H | H | Detect Over Current and Over Temperature<br>or Over Voltage |

#### 1. OVER VOLTAGE DETECTION (VCC1)

When VCC1 is over 27V(Typ.), MOTOR Drivers are stopped (OFF, Hi-Z) and PIN “DG2” outputs H. As soon as VCC1 drops under 27V(Typ.) MOTOR Driver returns to normal output and PIN “DG2” outputs L.

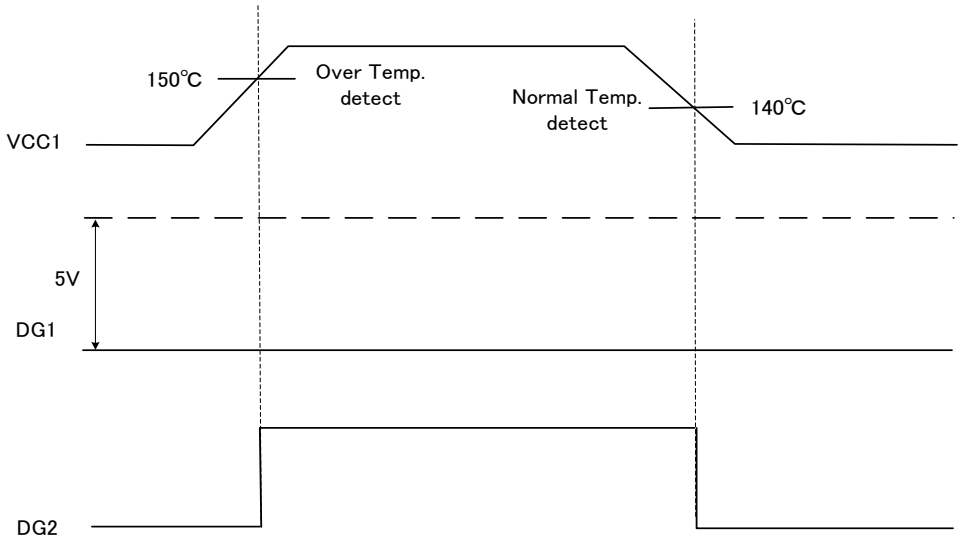



* The above is the case of detecting only Over Voltage (DG1="L", DG2="H").
In the case of detecting Over Current, DG1 outputs "H".

Note: This Over Voltage Detection is not to clamp Battery Voltage for TB9068FG.
Thus, the system should keep lower operation voltage than the Max. rating Spec.

## 2. OVER TEMPERATURE DETECTION

When the junction temperature exceeds 150°C (min), the MOTOR drivers are OFF (Hi-Z), LIN driver is OFF (Hi-Z) and PIN “DG2” outputs H.
When the temperature of the CHIP drops under 140°C (min), MOTOR driver return to normal and PIN “DG2” outputs L.




* The above is the case of detecting only Over Temperature (DG1="L", DG2="H").

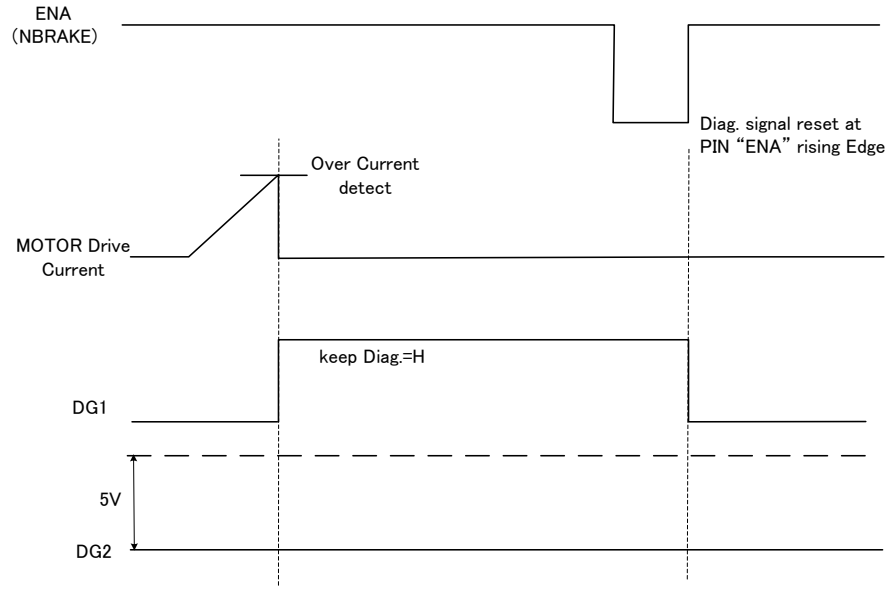
In the case of detecting Over Current, DG1 outputs "H".

Note: The Absolute Maximum Temperature of TB9068FG is 150deg. This Over Temperature Detection function does not intend to limit the CHIP temperature. Thus, TB9068FG must not exceed the above Absolute Maximum Temperature. If the rating would be exceeded during operation, the device electrical characteristics may be irreparably altered and the reliability and lifetime of the device can no longer be guaranteed. Moreover, these operations with exceeded ratings may cause break down, damage and/or degradation to any other equipment. Applications using the device should be designed such that maximum rating will never be exceeded in any operating conditions. Before using, creating and/or producing designs, refer to and comply with the precautions and conditions set forth in this documents. About this function, test in real temperature is not carrying out at the time of shipment.

## 3. OVER CURRENT DETECTION

When MOTOR driver current exceeds ±1.5A (Typ.), the MOTOR drivers are OFF (Hi-Z) and PIN “DG1” outputs H. Over current detection is not reset even when current falls to uncritical value and PIN “DG1” remains at H-level. To reset the Over Current condition a LOW pulse at PIN “ENA(NBRAKE)” is needed. To cancel the detection function, input the signal to the ENA pin (rising edge) to detect the rising edge and return to normal operation.

However, if the over current condition continues or if the ENA terminal rises at the same time as detection, the over current detection function has priority, so wait a while and input the signal to the ENA terminal again.




*The above is the case to detecting only Over Current (DG1=”H”,DG2=”L”).

In case of detecting Over Voltage or Over Temperature, DG2 outputs “H”.

After Voltage or TEMP returns to normal, DG2 changes to output “L”

Note : Over current detection ±1.5A (typ.) is based on overall motor current.

Detected Current = the output current of PIN “OA”
+ the output current of PIN “OB”
+ the output current of PIN “OC”

Note : In MODE0, Motor Driver off(Hi-Z) by Abnormal Detection is higher priority than brake function by PIN”ENA(NBRAKE)” or PIN”IA(CCW/CW1)” / “IB(CCW/CW2)”.

## (5) MODE SELECTION for MOTOR CONTROL

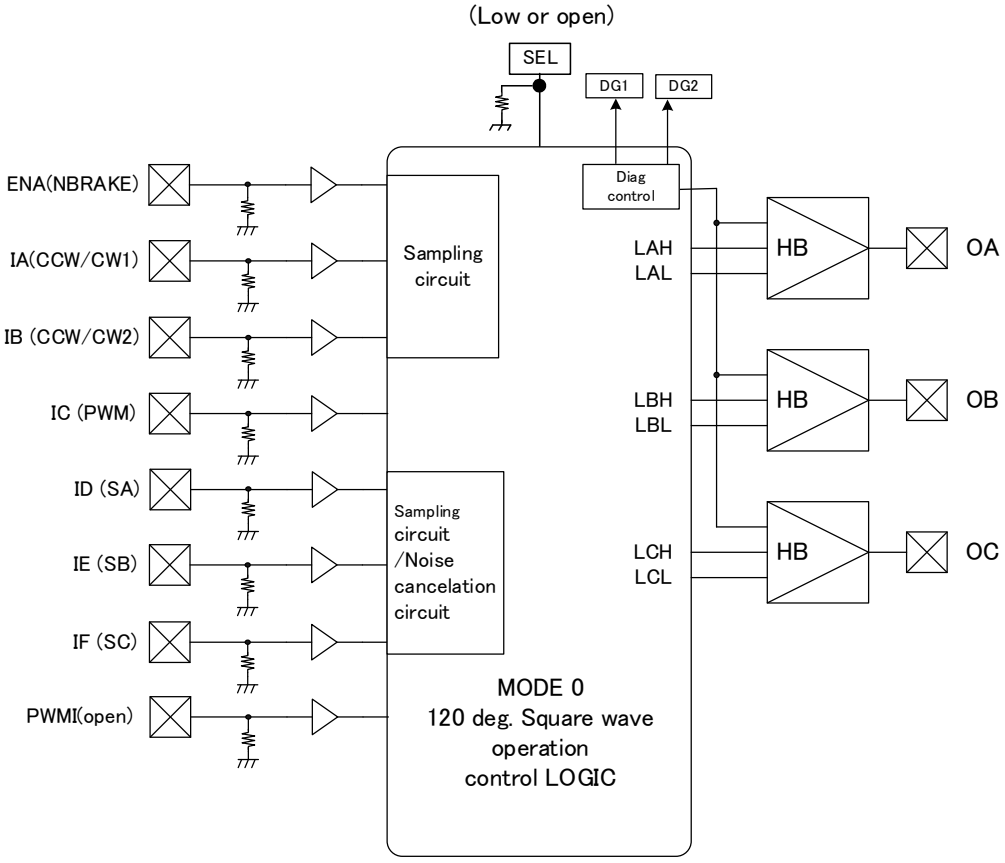
TB9068FG has 2 modes for MOTOR control which are selected by PIN “SEL” as follows

### 1. MODE0 (SEL=L or open)

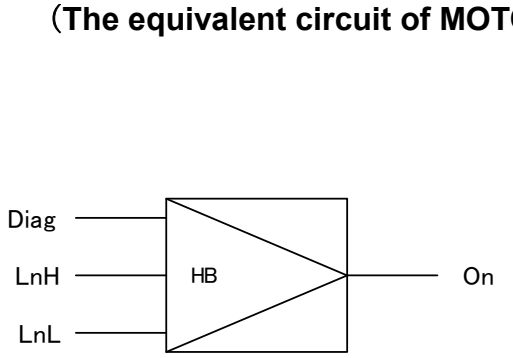
**(3-PHASE BRUSHLESS MOTOR 120 deg. square wave operation)**

The sensor signals which is input at PINs “ID(SA)”, “IE(SB)” and “IF(SC)” are processed by the internal LOGIC and corresponding MOTOR control outputs are available at PINs “OA”, ”OB” and ”OC”. PWM (L-side) MOTOR speed control is available by applying low frequency PWM at the input PIN “ PWMI(open)”.

* Even PWM signal is input from PIN”PWMI(open)” in MODE0, It is ignored and cannot control Motor Speed.
Kept PIN”PWMI(open)” open is recommended in MODE0

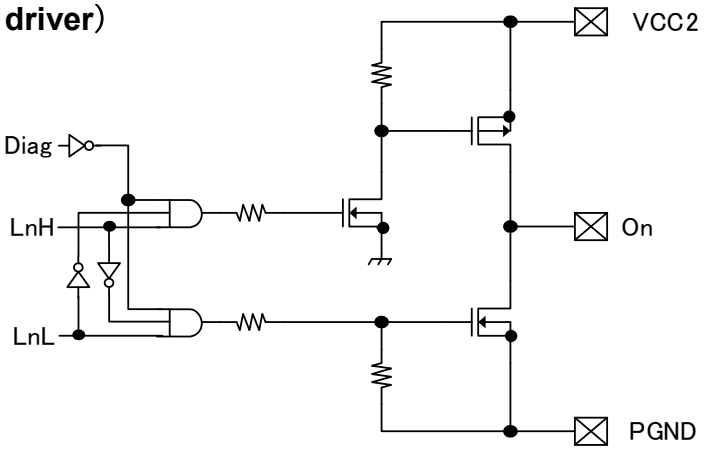



### (The equivalent circuit of MOTOR driver)



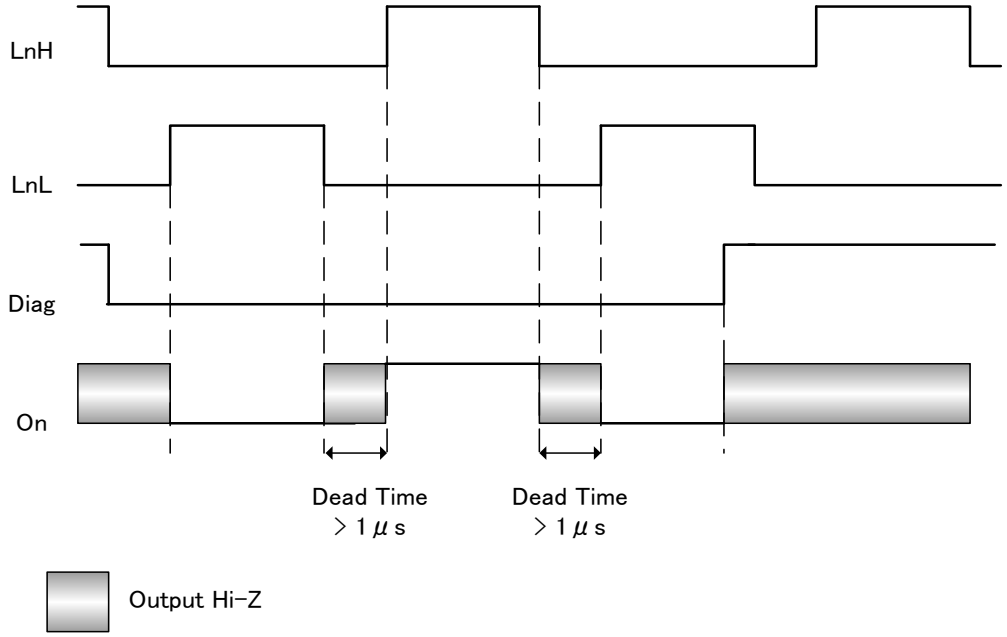

HB : HAlf Bridge Driver

Symbol of Driver Block

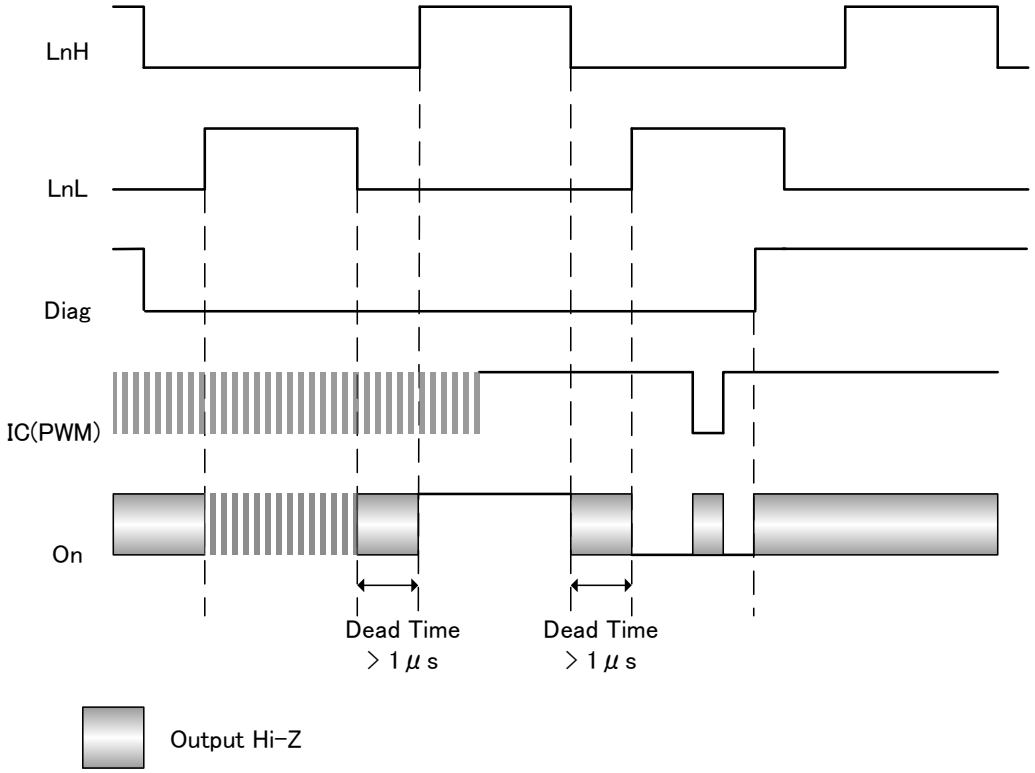



Equivalent Circuit of Driver Block

**(DRIVER TIMING CHART)**



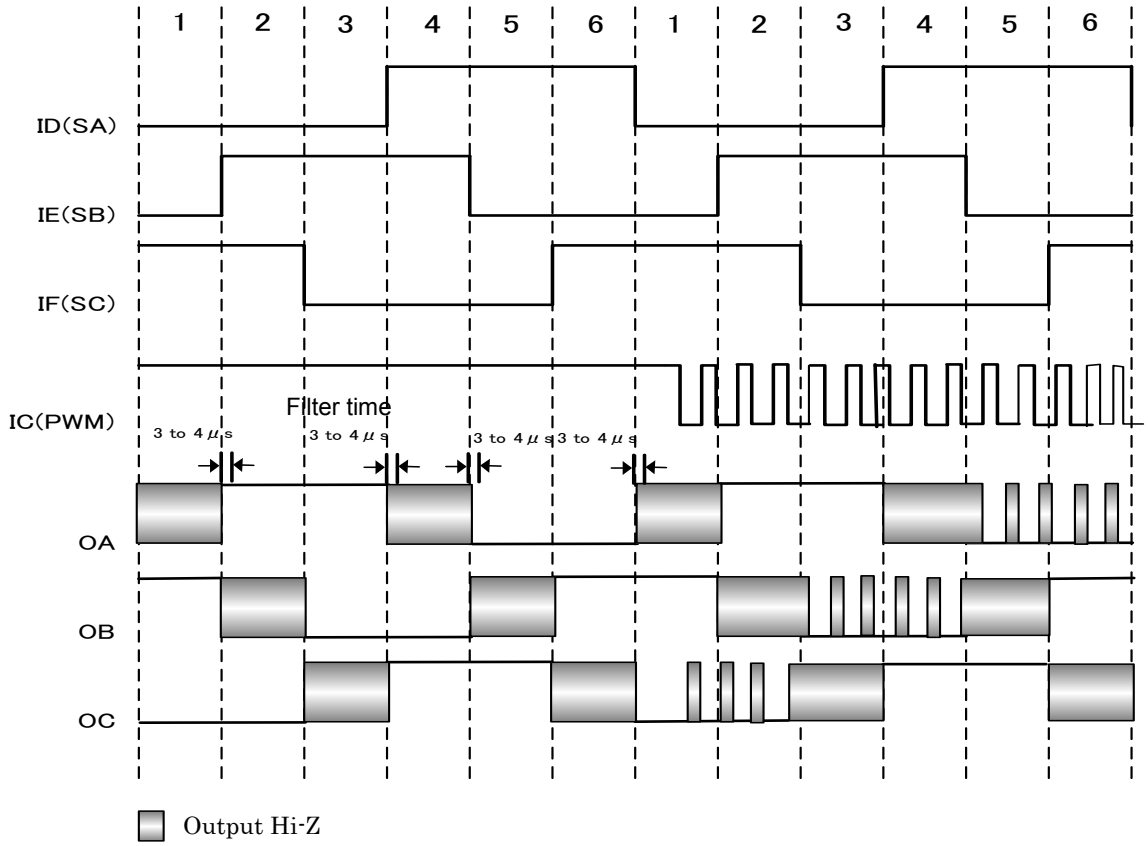

**(DRIVER TIMING CHART in case of external PWM CONROL from PIN"IC(PWM)" )**



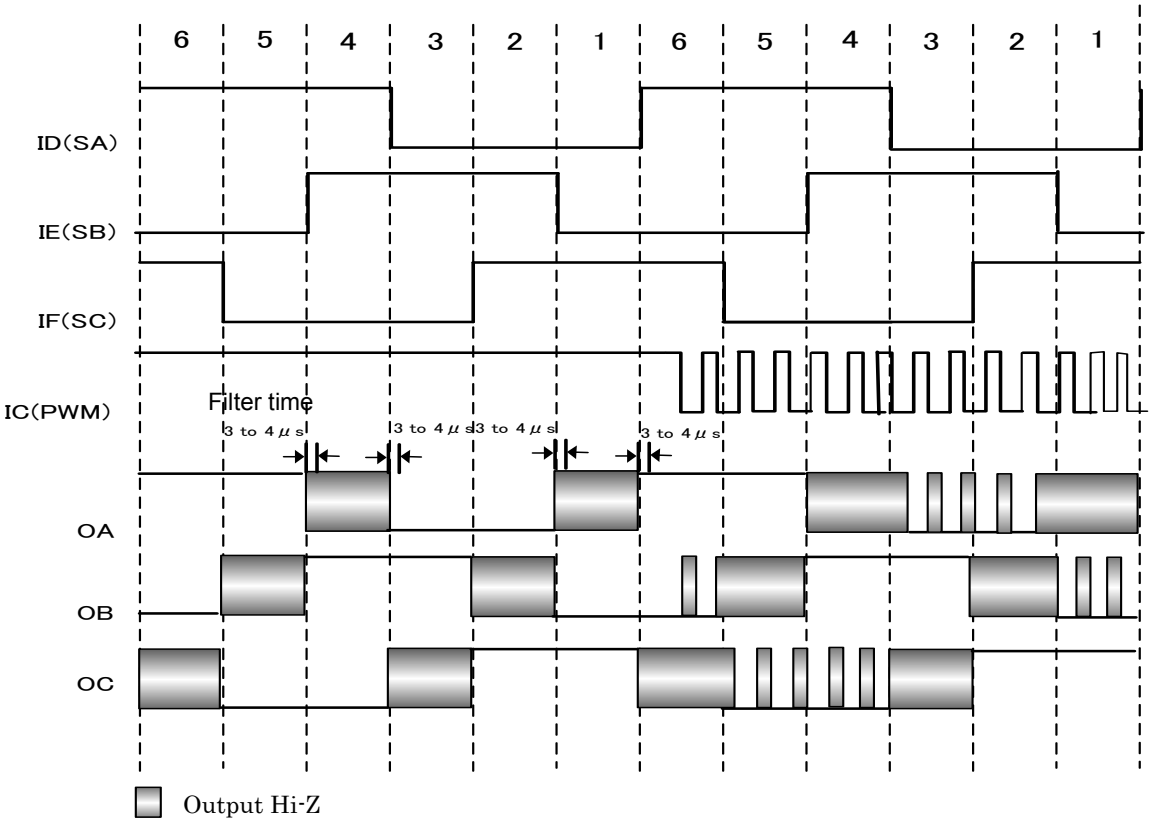

* The above signal "Diag" is TBi061FG internal signal. When Over Voltage, Over Temp. or Over Current is detected, "Diag" is "H".

**（120deg. Square wave Operation Motor control at 4MHz）**

**IA (CCW / CW 1) = L、IB(CW/CCW2) = H　(CLOCKWISE)**




**IA (CCW / CW 1) = H、IB(CW/CCW2) = L　(COUNTERCLOCKWISE)**



The Outputs of Motor Drivers are controlled according to the HALL sensor signals via bouilt-in Comparator as shown in previous figure(6status). Built-in Noise Canceler rejects the HALL signal which is shorter than 3μs(at Internal CR OSC 4MHz(typ.)). The Delay Time of Motor commutation against HALL signal Input is made by this Noise Canceler and Driver's Delay. In MODE0 TB9068FG drives motor in 120deg Square wave operation and DEAD TIME for H-side/L-side on the same Phase is not set. Only in case of Motror driver ON/OFF by Input "ENA(NBRAKE)", the The Outputs of Motor Drivers are set Hi-Z during 1μs after noise cancellation.

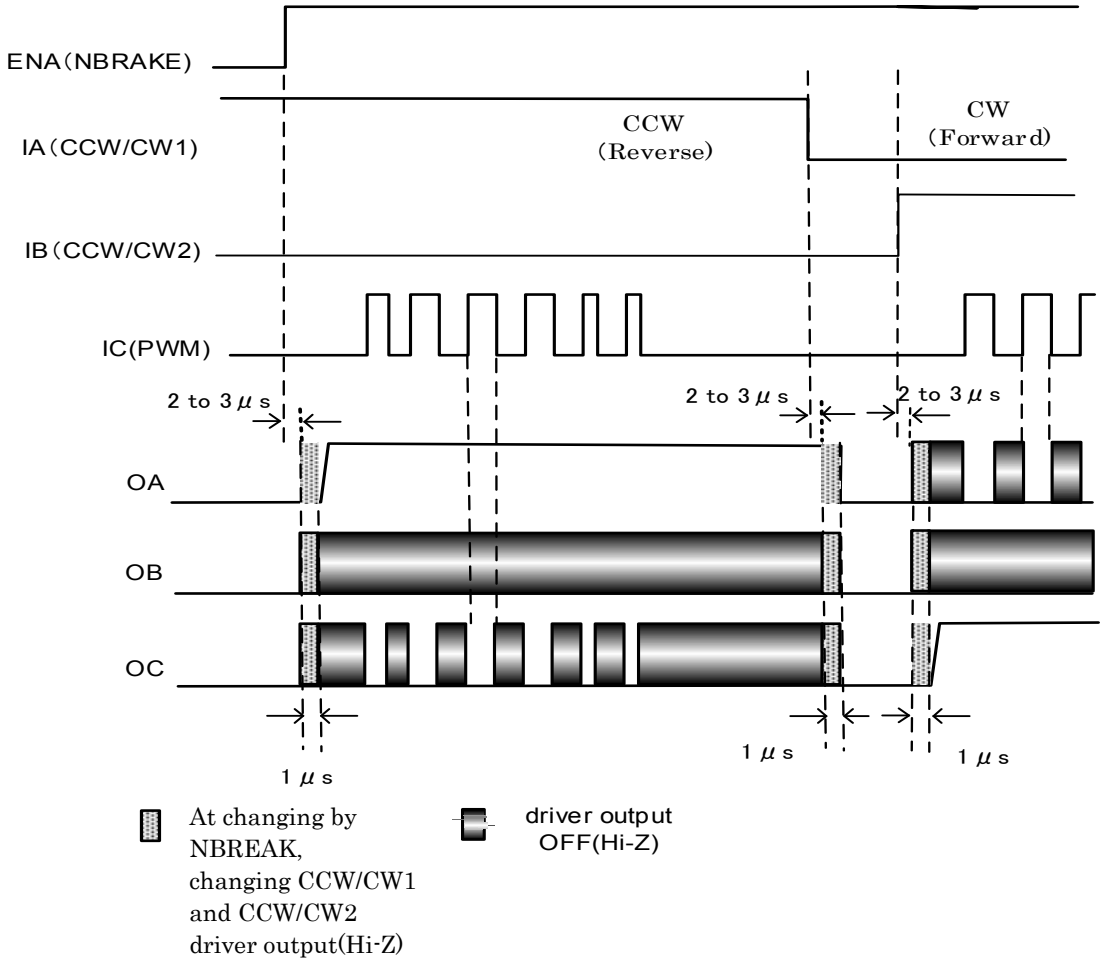
**(Changing rotation direction by PIN"IA(CCW/CW1)" and "IB(CCW/CW2)" in MODE 0)**

The Motor rotation direction is controlled by the inputs "CCW/CW1" and "CCW/CW2" in MODE0, as follows.

| PIN "IA(CCW/CW1)" | PIN "IB(CCW/CW2)" | OPERATION |
|---|---|---|
| L | L | BRAKE (L-side ON) |
| H | L | CCW (Reverse) |
| L | H | CW (Forward) |
| H | H | Hi-Z (H/L-side OFF) |

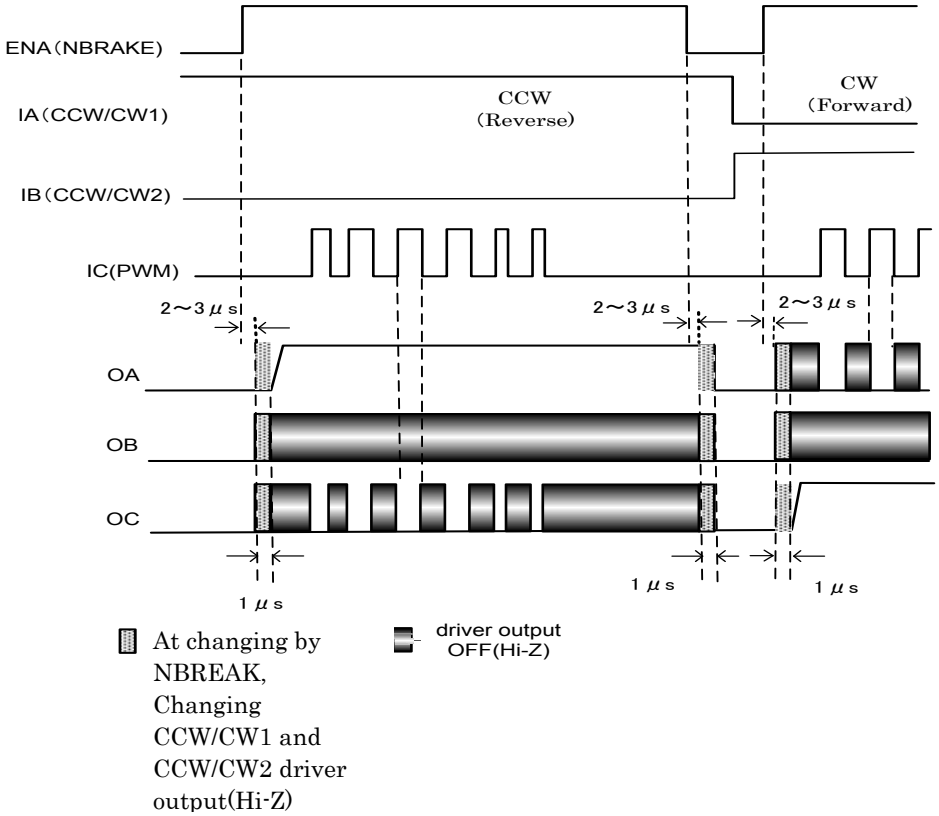
When the MOTOR rotation direction is changed by the input "CCW/CW1" and "CCW/CW2", firstly a braking operation (input "CCW/CW1"="CCW/CW2"= L) is required. At each edge of "CCW/CW1" and "CCW/CW2" Motor driver outputs are OFF(Hi-Z) for 1μs.( at Internal CR OSC 4MHz(typ.)). (see the follows ). If the input "ENA(NBRAKE)" is L when driver outputs return to normal by "IA"=H or "IB"=H, driver outputs wait until input "ENA(NBRAKE)" becomes H.

**(CCW/CW1=CCW/CW2=L: Braking OA=OB=OC=L)**



After that, when CCW / CW1 or CCW / CW2 = L is detected, operation in the specified rotation direction is started.

**(CCW/CW change at PIN“ENA(BRAKE)”=L)**



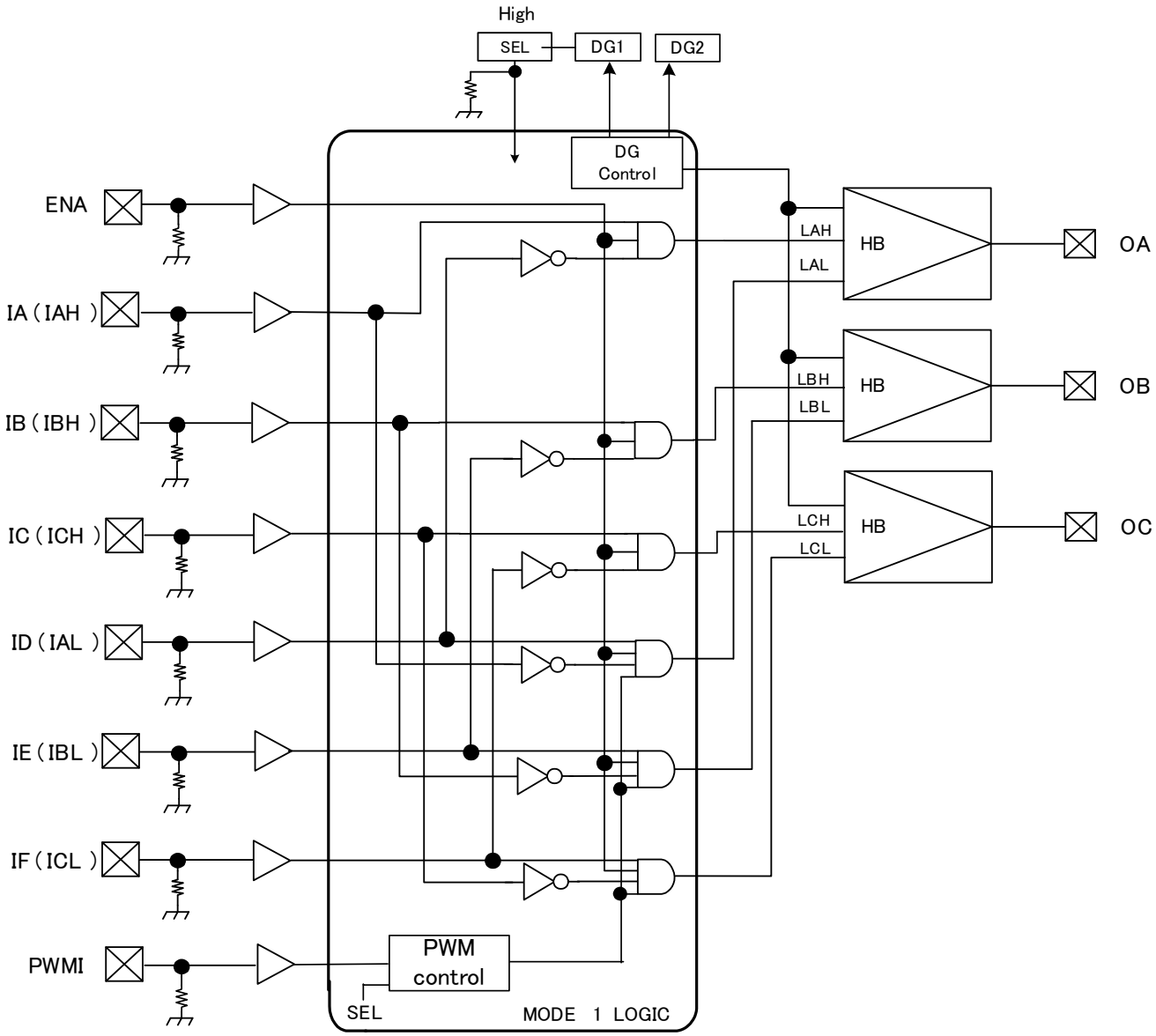

Before Motor rotation direction is changed, once being Brake by PIN”PWMI”=L and “ENA(NBRAKE)”=L is setting. When “ENA(NBRAKE)” is changed, Motor Driver is off(Hi-Z) during 1μs(at Internal CR OSC 4MHz(typ.))

## 2. MODE1(SEL=H) (for 3PHASE BRUSHLESS MOTOR control by MCU)

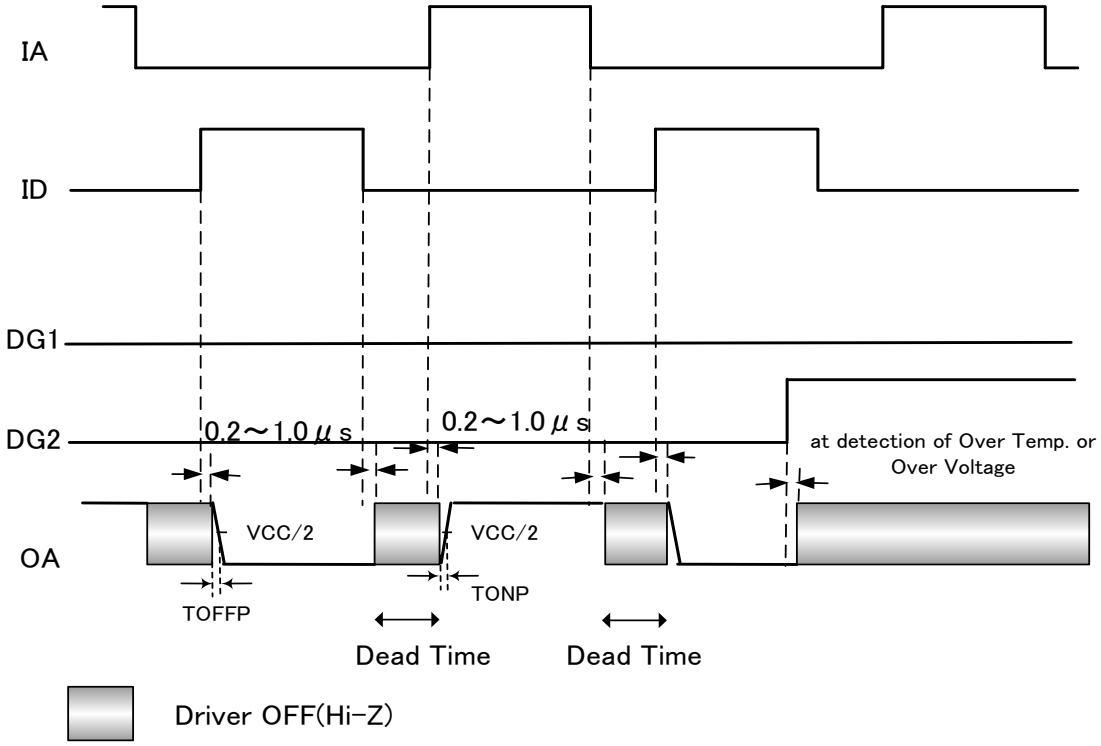
The MOTOR driver output signal is controlled by outside MCU. When the PWM speed control is required, MCU needs to generate and output the MOTOR control signals with PWM pattern or independently input PWM signal from input terminal “PWMI(open)”. In MODE1, TB9068FG does not generate the DEAD TIME. Therefore, MCU needs to control that short circuit current thru the driver Pch and Nch cannot happen (avoid simultaneous occurrence of IA=ID=H, IB=IE=H,IC=IF=H).

Each Motor driver output OA,OB,OC has the delay around 0.2 to 1.0μs against each input signal IA to IF.

| High Side cont. Input | Low Side cont. Input | output |
|---|---|---|
| IA | ID | OA |
| IB | IE | OB |
| IC | IF | OC |

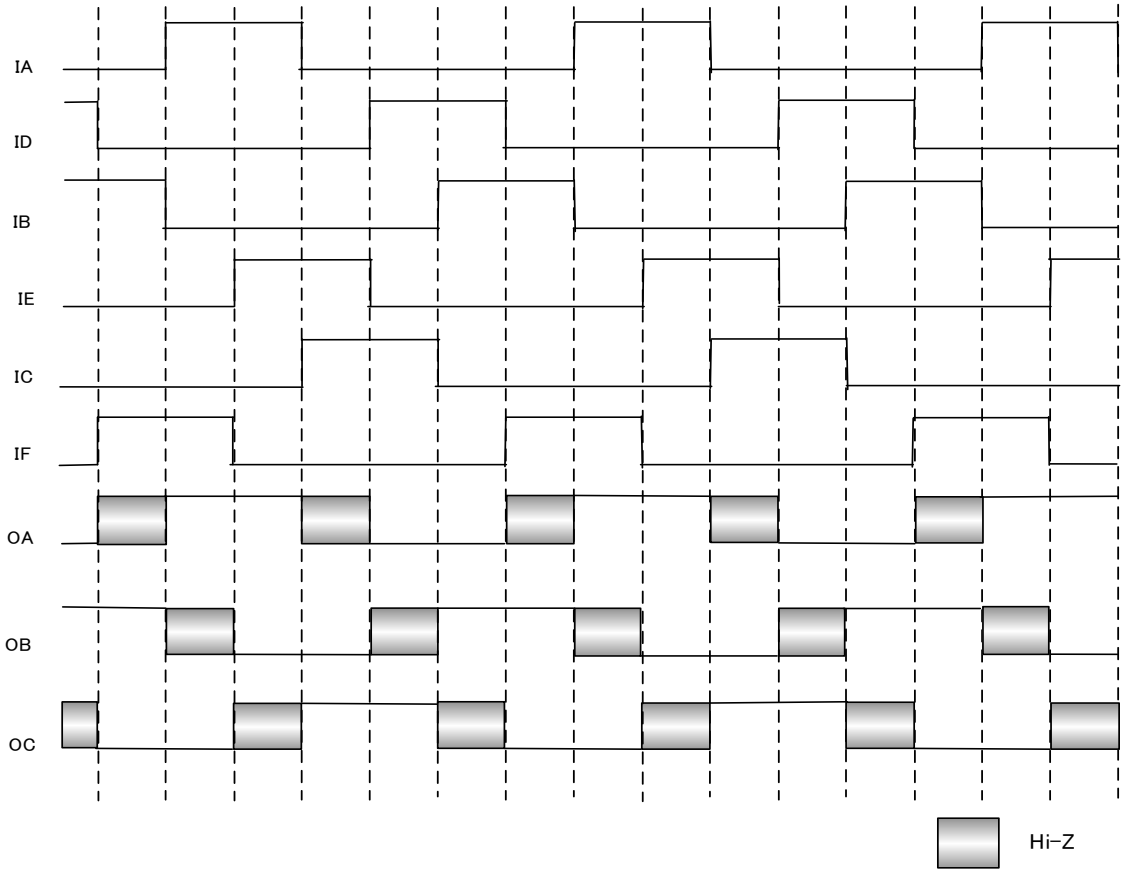


**(TIMING CHART of MOTOR DRIVE OUTPUT SIGNAL in MODE1)**



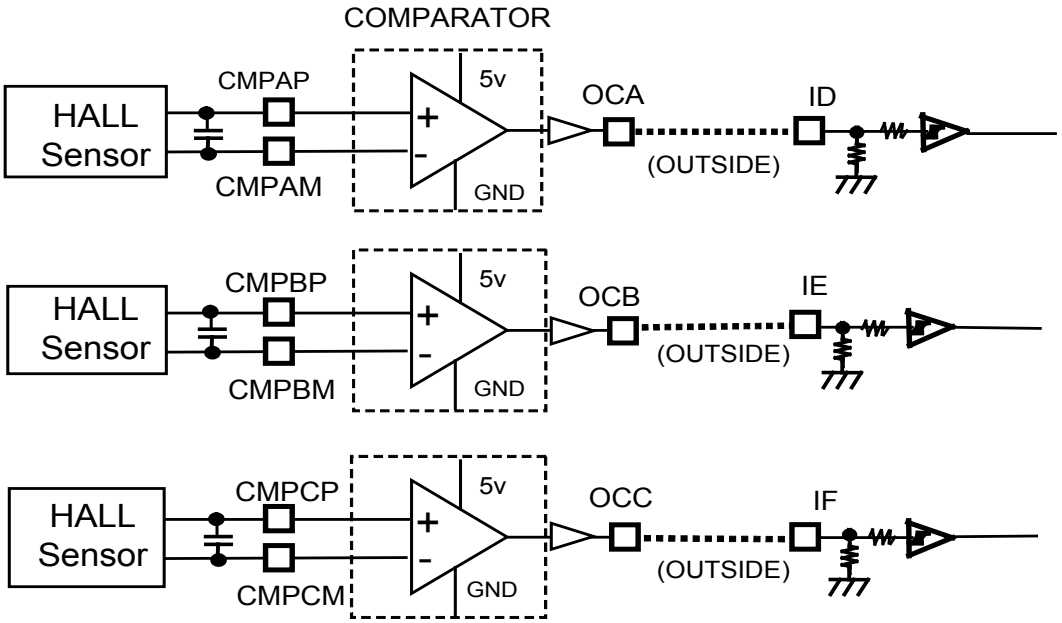

Motor Control Output Signal（OA,OB,OC）has Delay 0.2 to1.0μs (at Internal CR OSC 4MHz(typ.) against Input Signal IA/IB/IC、ID/IE/IF.

**(MOTOR CONTROL SIGNAL and MOTOR DRIVE SIGNAL in MODE1)**



## (6) INTEGRATED ANALOG COMPARATOR for HALL SENSOR

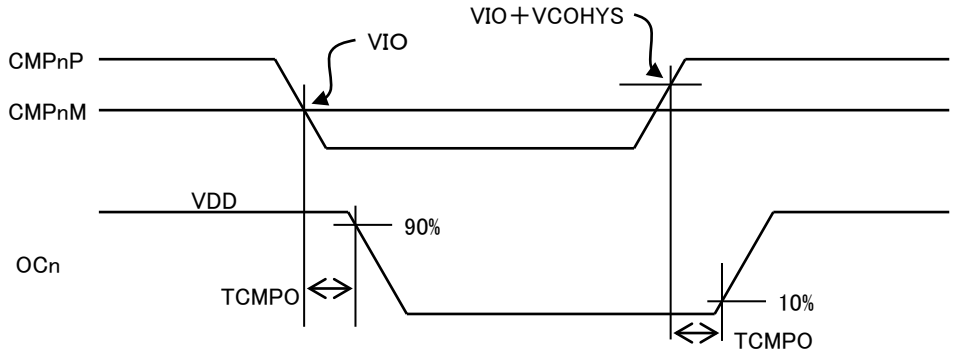
TB9068FG has integrated Analog Comparators for HALL Sensors to detect the MOTOR position. These Analog Comparators convert the analog HALL Sensor output signals into Digital signal pulses. In MODE0, once 3 HALL Sensor signals are input to PINs ”CMPAP”, ”CMPAM”, ”CMPBP”, ”CMPBM”, ”CMPCP” and ”CPMCM” they are converted into Digital and output from PINs “OCA”, “OCB” and “OCC”. Those 3 output signals are input into TB9068FG again through PINs “ID”, “IE” and “IF” for further processing by the commutation LOGIC. All of Comparator outputs are at CMOS level signal (5V) for easy interfacing with outside MCU.



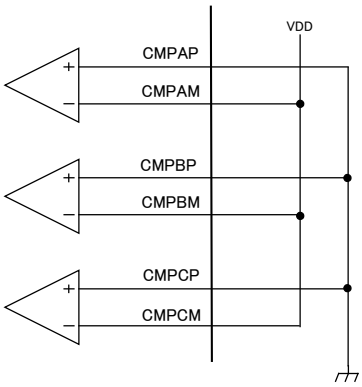

* Comparator ON/OFF has 10mV Hysteresis

* □ are the TB9068FG PIN

**(ANALOG COMPARATOR TIMING CHART)**

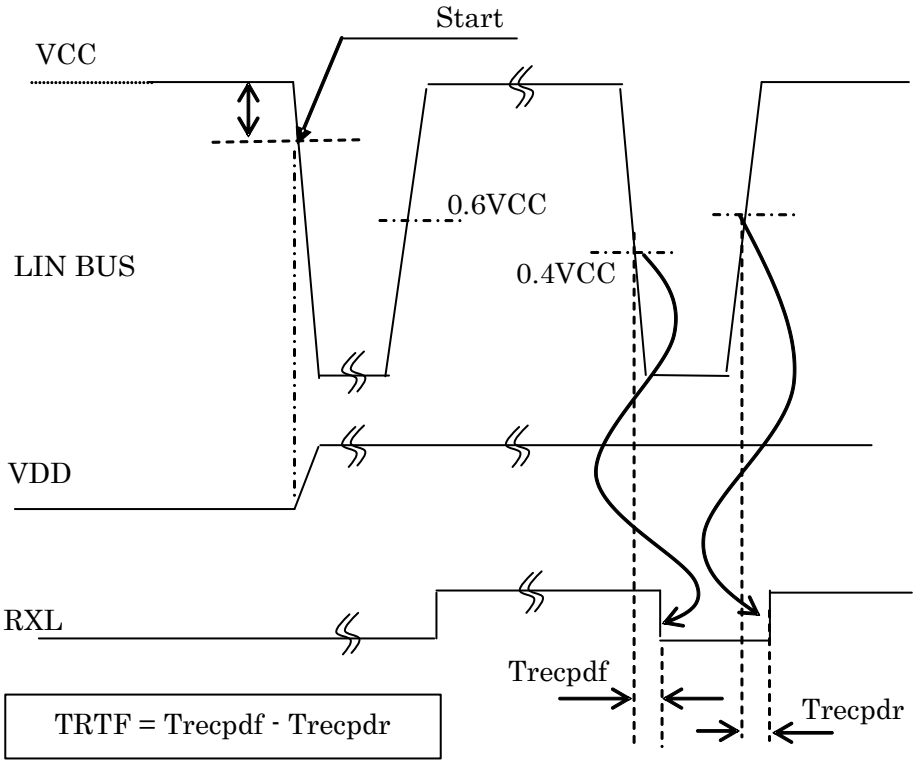


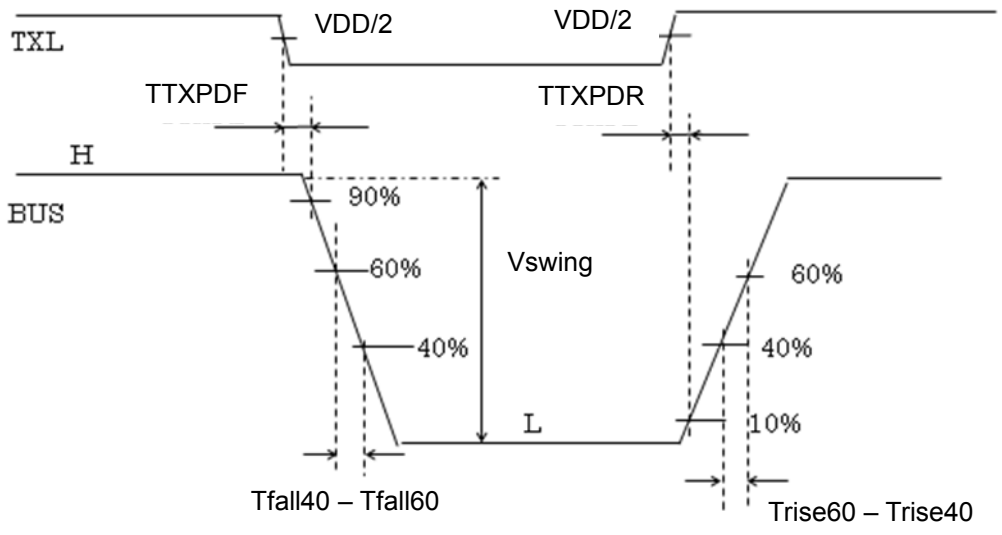

[CAUTION]
In case the integrated OP-AMPs are not used, the vacant input PINs should be connected as shown in right hand diagram.
When setting up Pull Up resistors and CR filters at HALL-sensor outputs or PINs “OCA”,”OCB” and ”OCC” their values should be chosen in accordance with the internal Resistors (62.5kΩ min.) as Resistor Divider.



### (7) INTEGRATED LIN TRANSCEIVER

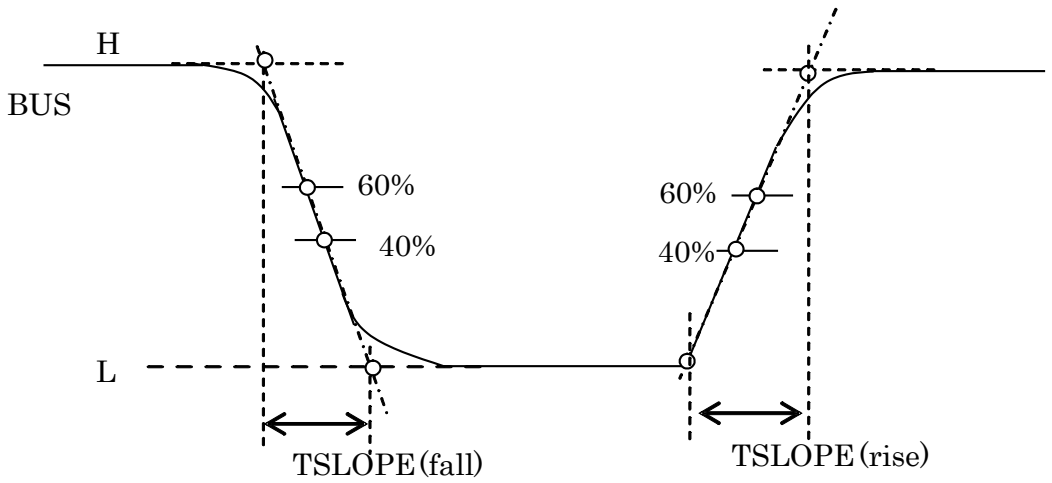
### (AC CHARACTERISTIC of LIN DRIVER)




- VTF/S = 0.2Vswing / ( Tfall40-Tfall60 )
- VTR/S = 0.2Vswing / ( Trise60-Trise40 )

**(AC CHARACTERISTICS CONDITION of LIN DRIVER) (cont.)**




- TSLOPE(fall) = ( Tfall40 - Tfall60 ) /0.2
- TSLOPE(rise) = ( Trise60 - Trise40 ) /0.2

## ABSOLUTE MAXIMUM RATINGS

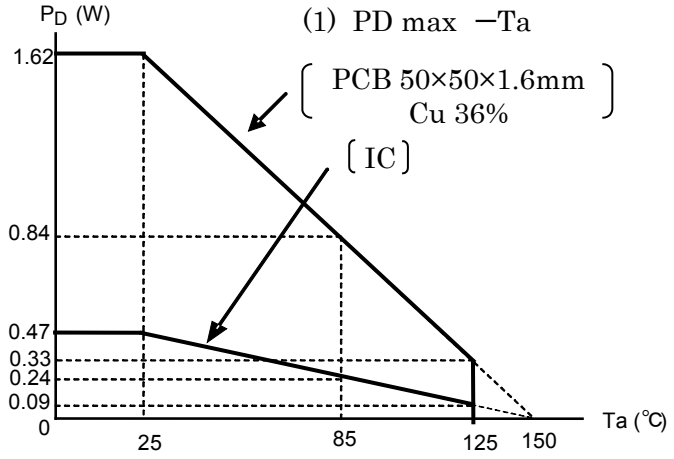
Ta=25℃

| CHARACTERISTIC | SYMBOL | PIN | CONDITION | VALUE | UNIT |
|---|---|---|---|---|---|
| Supply Voltage | VCC | VCC, VCC2 | DC voltage | -0.3 to +40 | V |
| | VDD | VDD | DC voltage | -0.3 to +6 | |
| Protection DIODE Current | $I_{diode}$ | BUS,I/O(except MOTOR drive output) | - | ±10 | mA |
| Output Current | IOUT | BUS | - | 200 | |
| | | OA,OB,OC | at Short Detection | ±1.5 | A |
| | | RXL,DG1,DG2, OCA,OCB,OCC | - | ±10 | mA |
| | | NRST | - | 10 | |
| Input/Output Current | VIN, VOUT | TP1,TP2,TP3 OA,OB,OC | - | -0.3 to VCC+0.3 | V |
| | | CK, NRST, DG1、DG2, RXL, TXL, ENA, IA, IB, IC, ID, IE, IF, SEL、PWMI、WS、CMPAP、CMPAM、CMPBP、CMPBM、CMPCP、CMPCM、 | - | -0.3 to VDD+0.3 | |
| | | VREG1、VREG2 | - | 6.0 | |
| | | BUS | - | GND+30, VCC-30 | |
| | | | VCC=GND=0V | ±30 | |
| Storage Temperature | Tstg | - | - | -55 to +150 | ℃ |
| Soldering Temperature | Tsol | - | Manual soldering | 260（10s） | |
| Maximum Power Dissipation | PD | - | PCB (50×50×1.6mm Cu36%) Ta=25℃ | 1.62 | W |

Note: The absolute maximum ratings of a semiconductor device are a set of specified parameter values, which must not be exceeded during operation, even for an instant. If any of these rating would be exceeded during operation, the device electrical characteristics may be irreparably altered and the reliability and lifetime of the device can no longer be guaranteed. Moreover, these operations with exceeded ratings may cause break down, damage and/or degradation to any other equipment. Applications using the device should be designed such that each maximum rating will never be exceeded in any operating conditions. Before using, creating and/or producing designs, refer to and comply with the precautions and conditions set forth in these documents.

● LQFP48-P-0707-0.50 THERMAL RESISTANCE DATA (for reference only)

| CHARACTERISTIC | Symbol | Value | Condition | Unit |
|---|---|---|---|---|
| Thermal Resistance | Rθ j-a | 266 | IC | ℃／W |
| | Rθ j-a | 77 | PCBN (50×50×1.6mm Cu36%) | ℃／W |




(1) PD max －Ta

$P_D = (150 - Ta)/R_{\theta j\text{-}a}$

Max. Power Dissipation of IC (no PCB) at 25°C

(150-25) / 266 = 0.47 (W)

Max. Power Dissipation of IC on PCB (50×50×1.6mm Cu 36%) at 25°C

(150-25) / 77＝1.62 (W)

## STATIC ELECTRICAL CHARACTERISTICS

### Operating Range

| CHARACTERISTIC | SYMBOL | VALUE | UNIT | Notes |
|---|---|---|---|---|
| Supply Voltage | VCC | 7 to 18 | V | - |
| | VDD | 4 to 5.5 | | Supply Voltage for LOGIC |
| Operating Temperature | Topr | -40 to 125 | ℃ | - |

### IC Characteristics

The follows are under condition VCC=7 to 18V Ta ＝-40 to 125℃ unless otherwise follows.

| CHARACTERISTIC | SYMBOL | PIN | CONDITION | MIN | TYP. | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Current Consumption (VCC) | ICC | VCC1,VCC2 | VCC=14V | - | - | 20 | mA |
| Current Consumption(VDD) | IDD | VDD | VDD=5V | - | 5 | 10 | |
| Output Current “H” Level | IOH1 | RXL,DG1,DG2 OCA,OCB,OCC | VDD=5V VOH=4.5V | - | -5 | -2 | mA |
| Output Current “L” Level | IOL1 | RXL,DG1,DG2,NRST OCA,OCB,OCC | VDD=5V VOL=0.5V | 2 | 5 | - | mA |
| Output Current of NRST “OFF” | ILO | NRST | VDD=5V,VOUT=0V | -1 | -0.5 | -0.2 | mA |
| Input Current “L” Level | IIL1 | TXL,CK | VDD=5V VIN=0V | -200 | -100 | -50 | μA |
| | IIL2 | ENA,WS、SEL,PWMI | | -10 | - | 10 | |
| | IIL3 | IA,IB,IC,ID,IE,IF | | | | | |
| | IIL4 | TP1,TP2,TP3 | VCC=12V, VIN=0V | | | | |
| Input Current “H” Level | IIH1 | TXL,CK | VDD=5V VIN=5V | -10 | - | 10 | |
| | IIH2 | ENA,WS、SEL,PWMI | | 50 | 100 | 200 | |
| | IIH3 | IA,IB,IC,ID,IE,IF | | 20 | 40 | 80 | |
| | IIH4 | TP1,TP2,TP3 | VCC=VIN=12V | - | 240 | 480 | |
| Input Voltage1 “L” Level | VIL1 | TXL,CK SEL,PWMI, IA,IB,IC,ID,IE,IF ENA,WS | - | 0 | - | 0.3VDD | V |
| Input Voltage1 “H” Level | VIH1 | | | 0.7VDD | - | VDD | |
| Hysteresis of Voltage1 | VHYS1 | | | - | 0.4 | - | |

## STATIC ELECTRICAL CHARACTERISTICS (cont.)

### 5V Regulator, RESET, Watch Dog Timer

The follows are under condition VCC=7 to 18V Ta ＝-40 to 125℃ unless otherwise the follows.

| CHARACTERISTICS | SYMBOL | PIN | CONDITION | MIN | TYP. | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Output Voltage of 5V Regulator | VREG | VREG1 VREG2 | with Outside PNP Transistor ILOAD 0mA to 40mA | 4.90 | 5.05 | 5.20 | V |
| LINE Regulation | VLINE | | - | - | 0.1 | 0.5 | % |
| LOAD Regulation | VLOAD | | - | - | 0.2 | 1.0 | |
| BASE Current of PNP Transistor. | IREGBACE | VREG0 | - | - | - | -1 | mA |
| Current Limiter detection Voltage | VLIMIT | VS | with Outside Register | VCC-0.4 | VCC-0.3 | VCC-0.15 | V |
| RESET OFF Voltage (Low VREG OFF) | VRSTH | VREG1 VREG2 | - | 0.90VREG | 0.93VREG | 0.97VREG | V |
| | | | - | - | 4.70 | - | |
| RESET ON Voltage (Low VREG Detection) | VRSTL | | - | 0.88VREG | 0.91VREG | 0.93VREG | |
| | | | - | - | 4.60 | - | |
| RESET Hysteresis Voltage (ON/OFF) | VRSTHY | - | - | - | 0.15 | - | V |
| Power On RESET Time | TPOR | NRST | see Page 6 | 12.5 | 25 | 50 | ms |
| Watch Dog Timer Detection Time | TWD | | | 25 | 50 | 100 | |
| RESET Time | TRST | | | 2.5 | 5 | 10 | |
| “CK” Input Pulse Width | TCK | CK | thru NOISE Canceller | 64 | - | - | μs |

### Comparator

The follows are under condition VCC=7 to 18V Ta ＝-40 to 125℃ unless otherwise the follows

| CHARACTERISTICS | SYMBOL | PIN | CONDITION | MIN | TYP. | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Input Voltage | VINH | CMPAP,CMPAM CMPBP,CMPBM CMPCP,CMPCM | - | VREG-2 | VREG-1.5 | - | V |
| | VINL | | - | -0.3 | - | 0 | V |
| Input Bias Current | IIBIAS | | - | -2 | -0.2 | - | μA |
| Input Offset Current | IIOFST | | - | - | 0.02 | 0.3 | |
| Input Offset Voltage | VIO | | - | -10 | - | 10 | mV |
| COMP Hysteresis * | VCOHYS | | CMPAM=CMPBM =CMPCM=2.5V | 2 | 9 | 15 | mV |
| COMP Output Delay | TCMPO | | AC characteristics based | - | 0.5 | 1.5 | μs |

* COMP. Hysteresis (VCOHYS) is not tested on production line, directly. It is judged by the following VIO and VCOHYS measurement. (see (6) INTEGRATED ANALOG COMPARATOR for HALL SENSOR)

$$VCOHYS = VIO + VCOHYS - VIO$$

## STATIC ELECTRICAL CHARACTERISTICS (cont.)

### MOTOR Driver

The follows are under condition VCC=7 to 18V Ta ＝-40 to 125℃ unless otherwise the follows

| CHARACTERISTICS | SYMBOL | PIN | CONDITION | MIN | TYP. | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Output Voltage | VOH1 | OA, OB, OC | VCC=12V,Output ”H” IOUT=-0.2A | VCC-0.4 | 11.8 | VCC-0.1 | V |
| | VOL1 | | VCC:12V,Output ”L” IOUT=0.2A | 0.1 | 0.2 | 0.4 | |
| Pch Output Impedance1 | RHON1 | | IOUT=-0.2A, T a=25℃ | 0.7 | 0.85 | 1.3 | Ω |
| | | | IOUT=-0.2A,Ta=125℃ | 0.7 | - | 2 | |
| | | | IOUT=-0.2A,Ta=-40℃ | 0.5 | - | 1.3 | |
| Nch Output Impedance1 | RLON1 | | IOUT=0.2A, T a=25℃ | 0.7 | 0.9 | 1.3 | |
| | | | IOUT=0.2A,Ta=125℃ | 0.7 | - | 2 | |
| | | | IOUT=0.2A,Ta=-40℃ | 0.5 | - | 1.3 | |
| Output OFF Leak Current | ILO | | Output OFF,VOUT=0V | -10 | - | 10 | μA |
| | | | Output OFF,VOUT=VCC | | | | |
| Driver ON Time | TONP | | - | - | 1.5 | 3.2 | μs |
| Driver OFF Time | TOFFP | | - | - | 0.5 | 1.5 | |
| Short Circuit Detection Current at GND-Short | IOVERL | | T a=25℃ | -2.3 | -1.5 | -1.3 | A |
| | | | Ta=125℃ | -2.0 | - | -1.2 | |
| | | | Ta=-40℃ | -2.5 | - | -1.4 | |
| Short Circuit Detection Current at VDD-Short | IOVERH | | T a=25℃ | 1.3 | 1.5 | 2.3 | |
| | | | Ta=125℃ | 1.2 | - | 2.0 | |
| | | | Ta=-40℃ | 1.4 | - | 2.5 | |
| Over Voltage Detection(VCC1) | VSD | VCC1 | - | 24 | 27 | 30 | V |

## STATIC ELECTRICAL CHARACTERISTICS (cont.)

### LIN Receiver

The follows are under condition VCC=7 to 18V Ta ＝-40 to 125℃ unless otherwise the follows

| CHARACTERISTICS | SYMBOL | PIN | CONDITION | MIN | TYP. | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| BUS Current | IIHRX | BUS | VIN=VCC | -10 | - | 10 | μA |
| | IILRX | | VCC=12V,VIN=0V | -600 | - | -255 | |
| | IBUSPASREC | | Driver OFF, VCC=7.3 to 18V, VBUS=8 to 18V, VBUS>VCC | - | - | 20 | |
| | IBUS | | VCC=0V VBUS=0 to 18V | - | - | 100 | |
| | IBUSNOGND | | at GND/VCC Short VBUS=8 to 18V, VCC=12V | -1 | - | 1 | mA |
| Input Voltage | VIHRX | | - | 0.4VCC | 0.5VCC | 0.6VCC | V |
| | VILRX | | - | 0.4VCC | 0.5VCC | 0.6VCC | |
| Input Hysteresis | VHYS | | - | - | - | 0.175VCC | |
| DOMINANT Voltage Range | VDOM | | - | -8 | - | 0.4VCC | |
| RECESSIVE Voltage Range | VREC | | - | 0.6VCC | - | 18 | |
| Output Delay Time Symmetry | TRTF | | Trecpdf- Trecpdr AC Characteristics based | -2 | - | 2 | μs |

Note: TB9068FG integrate 30kΩ (Typ.) Pull Up Register as LIN SLAVE.

### LIN Driver

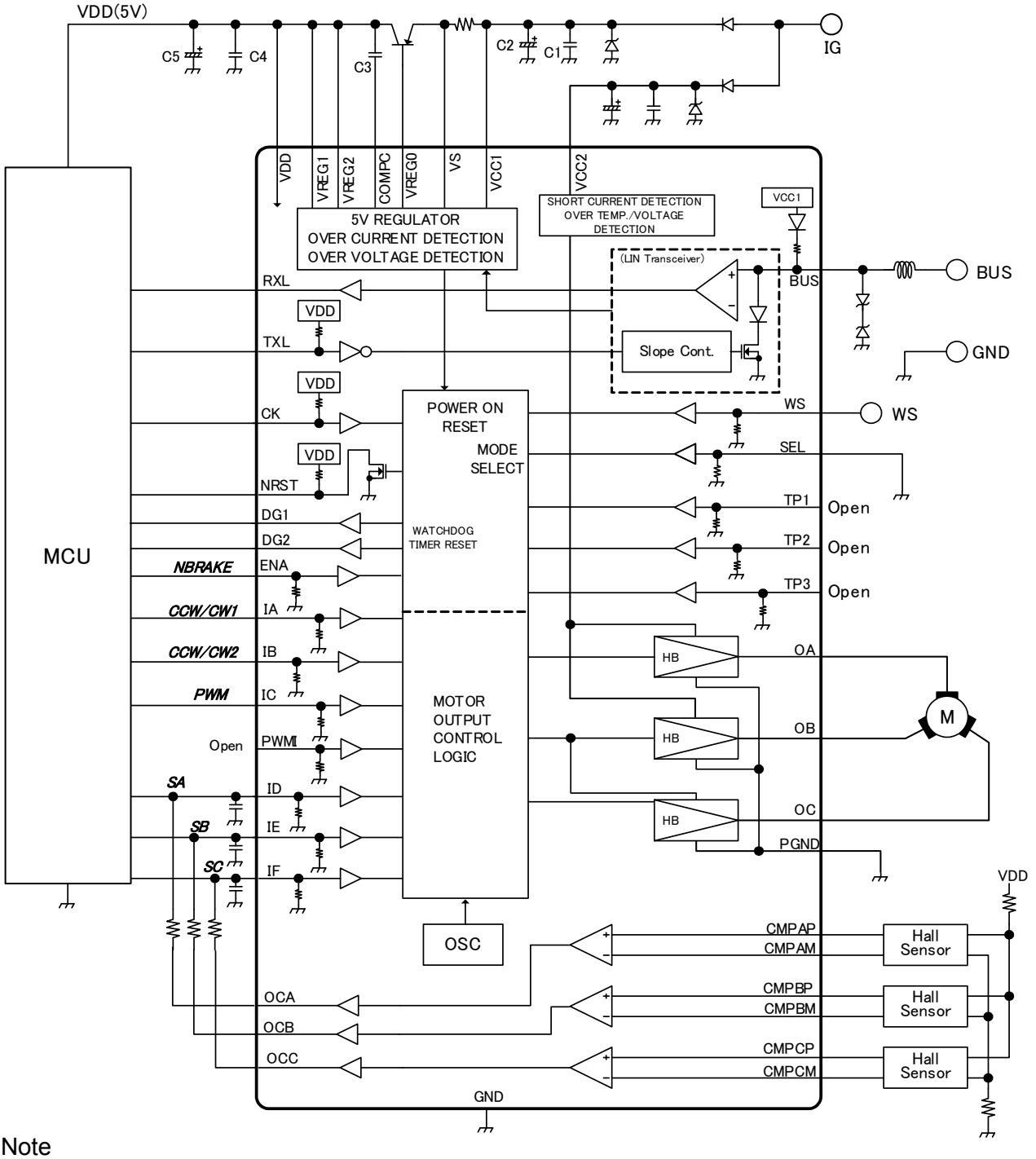
The follows are under condition VCC=7 to 18V Ta ＝-40 to 125℃ unless otherwise the follows

| CHARACTERISTICS | SYMBOL | PIN | CONDITION | | MIN | TYP. | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| Output Current | IOLIN | BUS | TXL=0V , VOUT=VCCx0.4 | | 40 | 100 | 200 | mA |
| Constant Slew Rate Transceiver | VTF/S | | AC CONDITION | VCC=18V | 1 | 1.6 | 3 | V/μs |
| | VTR/S | | | VCC=7.3V | 0.5 | 0.8 | 3 | |
| Output Delay Time | TTXPDF | | | - | - | 1 | 4 | μs |
| | TTXPDR | | | | | | | |
| Constant Slope Time Transceiver | TSYS | | | VCC=18V | -5 | - | 5 | |
| | | | | VCC=7.3V | -4 | - | 4 | |
| | TSLOPE | | | - | 3.5 | - | 22.5 | |
| Output Delay Time Symmetry | TRTF | | | - | -2 | - | 2 | |
| | TRXPD | | | - | - | - | 7.25 | |
| Driver Dominant Voltage | VOLBUS | | | VCC=7.3V,LOAD=600Ω | - | - | 1.2 | V |
| | | | | VCC=18V,LOAD=600Ω | - | - | 2.0 | |
| | | | | VCC=7.3V,LOAD=1kΩ | 0.6 | - | - | |
| | | | | VCC=18V,LOAD=1kΩ | 0.8 | - | - | |
| Output OFF Leak Current | ITXOFF1 | | | VOUT=VCC ( Note2 ) | - | - | 10 | μA |
| | ITXOFF2 | | VCC=0V,VOUT=-12V | | -1 | -0.6 | - | mA |
| Short Circuit detection Current | IOSHORT | | ( Note1 ) | | 40 | 100 | 200 | mA |

Note1：SHORT DETECTION CIRCUIT does not provide the time to recover.
Note2：The value of the LIN Receiver Input Current include the Output OFF Leak Current.

## Application circuit example

### MODE 0（120deg. rotation、with HALL Sensor ）




Note

*1 C1, C2, C4, and C5 are for NOISE reduction. They should be set near IC.

*2 C3 is for PHASE COMPENSATION. It should be set near IC.（C3：4700pF Recommendation）

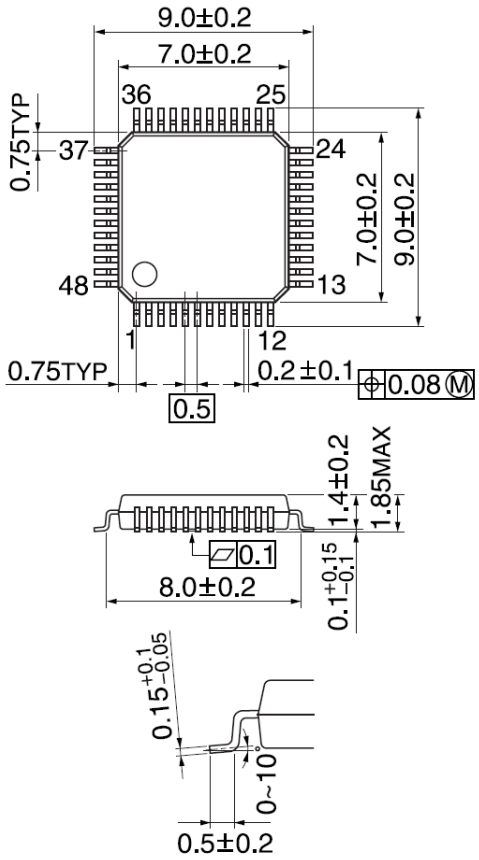
*3 Some of the functional blocks, circuit, or constants in the block diagram may be omitted or simplified for explanatory purpose.

*4 Install the product correctly. Otherwise, it may result in break down, damage and/or deterioration to the product or equipment.

*5 The application circuits shown in this document are provided for reference purposes only. Especially, a thorough evaluation is required on the phase of mass production design. Toshiba does not grant the use of any industrial property rights with these examples of application circuits.

## PACKAGE

LQFP48-P-0707-0.50 Unit: mm




Weight: 0.189 g (Typ.)

**Note**

- Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purpose.
- The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purpose.
- Timing charts may be simplified for explanatory purpose.
- The absolute maximum ratings of a semiconductor device are a set of specified parameter values, which must not be exceeded during operation, even for an instant. If any of these rating would be exceeded during operation, the device electrical characteristics may be irreparably altered and the reliability and lifetime of the device can no longer be guaranteed. Moreover, these operations with exceeded ratings may cause break down, damage and/or degradation to any other equipment. Applications using the device should be designed such that each maximum rating will never be exceeded in any operating conditions. Before using, creating and/or producing designs, refer to and comply with the precautions and conditions set forth in this documents.
- Ensure that the IC is mounted correctly. Failing to do so may result in the IC or target equipment being damage

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