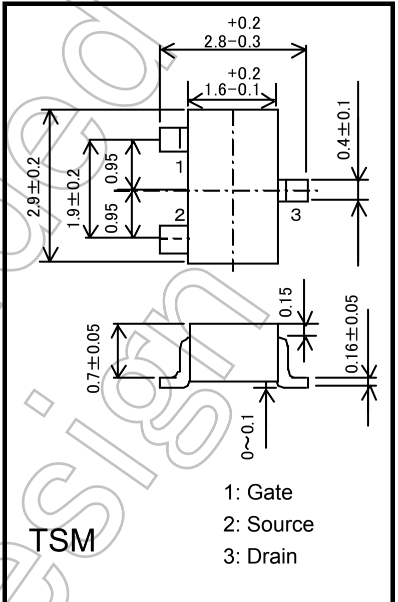
TOSHIBA Field-Effect Transistor Silicon N-Channel MOS Type (U-MOSⅣ)

SSM3K315T

○ High-Speed Switching Applications

- 4.5-V drive
- Low ON-resistance : R_{on} = 41.5 mΩ (max) (@V_{GS} = 4.5 V)
  : R_{on} = 27.6 mΩ (max) (@V_{GS} = 10 V)

Unit: mm



JEDEC	—
JEITA	—
TOSHIBA	2-3S1A

Weight: 10 mg (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
Drain-Source voltage		V_{DSS}	30	V
Gate-Source voltage		V_{GSS}	±20	V
Drain current	DC	I_D (Note 1)	6.0	A
	Pulse	I_{DP} (Note 1)	12.0	
Drain power dissipation		P_D (Note 1)	700	mW
		t = 10 s	1250	
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: The junction temperature should not exceed 150°C during use.

Note 2: Mounted on an FR4 board.
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 645 mm^2)

Electrical Characteristics (Ta = 25°C)

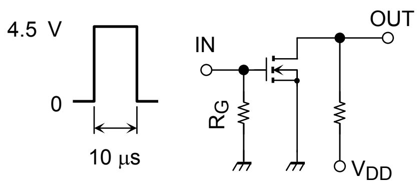
Characteristic		Symbol	Test Conditions	Min	Typ.	Max	Unit
Drain-Source breakdown voltage		$V_{(BR)DSS}$	I_D = 10 mA, V_{GS} = 0 V	30	—	—	V
		$V_{(BR)DSX}$	I_D = 10 mA, V_{GS} = -20 V	15	—	—	
Drain cut-off current		I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V	—	—	1	μA
Gate leakage current		I_{GSS}	V_{GS} = ± 20 V, V_{DS} = 0 V	—	—	±0.1	μA
Gate threshold voltage		V_{th}	V_{DS} = 5 V, I_D = 1 mA	1.3	—	2.5	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 5 V, I_D = 4 A (Note 3)	11.5	23.0	—	S
Drain–source ON-resistance		$R_{DS(ON)}$	I_D = 4.0 A, V_{GS} = 10 V (Note 3)	—	20.5	27.6	mΩ
			I_D = 2.0 A, V_{GS} = 4.5 V (Note 3)	—	27.0	41.5	
Input capacitance		C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	—	450	—	pF
Output capacitance		C_{oss}		—	120	—	
Reverse transfer capacitance		C_{rss}		—	77	—	
Total Gate Charge		Q_g	V_{DS} = 15 V, I_D =6.0 A, V_{GS} = 10 V	—	10.1	—	nC
Gate-Source Charge		Q_{gs}		—	7.6	—	
Gate-Drain Charge		Q_{gd}		—	2.5	—	
Switching time	Turn-on time	t_{on}	V_{DD} = 15 V, I_D = 2.0 A, V_{GS} = 0 to 4.5 V, R_G = 10 Ω	—	21	—	ns
	Turn-off time	t_{off}		—	15	—	
Drain-Source forward voltage		V_{DSF}	I_D = -6.0 A, V_{GS} = 0 V (Note 3)	—	-0.85	-1.2	V

Note 3: Pulse test

Start of commercial production
2008-09

Switching Time Test Circuit

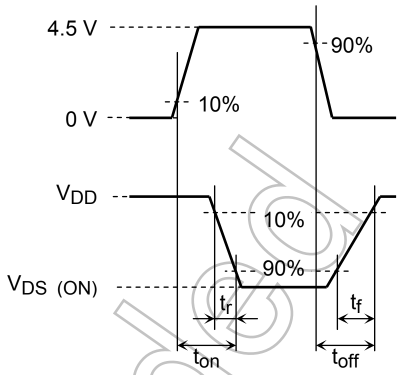
(a) Test Circuit



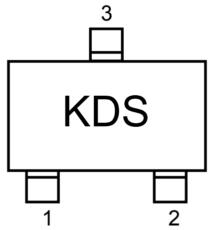
V_{DD} = 15 V
R_G = 10 Ω
Duty ≤ 1%
V_{IN}: t_r, t_f < 5 ns
Common Source
Ta = 25°C

(b) V_{IN}

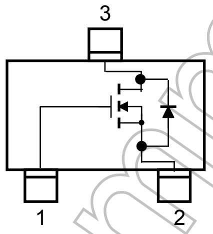
(c) V_{OUT}



Marking



Equivalent Circuit (top view)



Handling Precaution

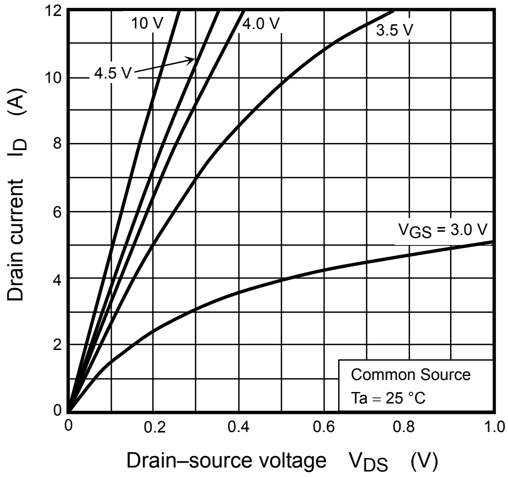
When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

Usage Consideration

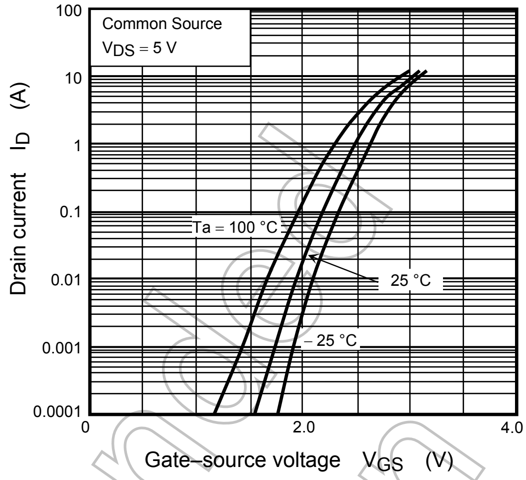
Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to be low (1 mA for the SSM3K315T). Then, for normal switching operation, $V_{GS(on)}$ must be higher than V_{th}, and $V_{GS(off)}$ must be lower than V_{th}. This relationship can be expressed as: $V_{GS(off)} < V_{th} < V_{GS(on)}$.

Take this into consideration when using the device

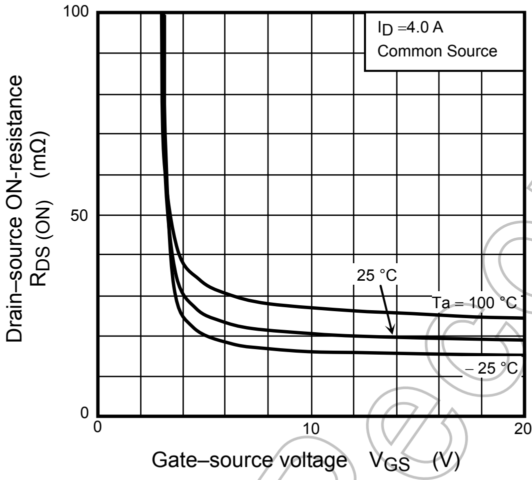
I_D – V_{DS}



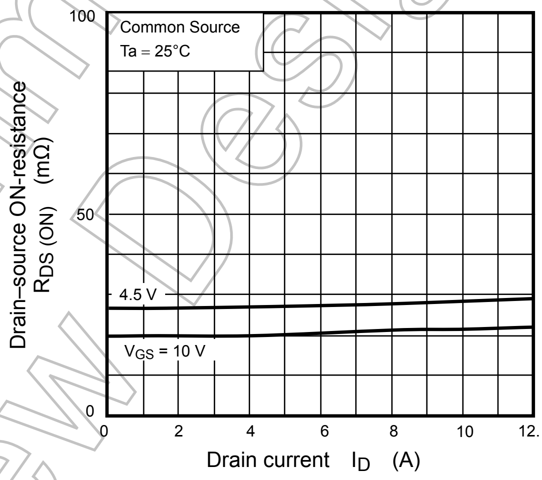
I_D – V_{GS}



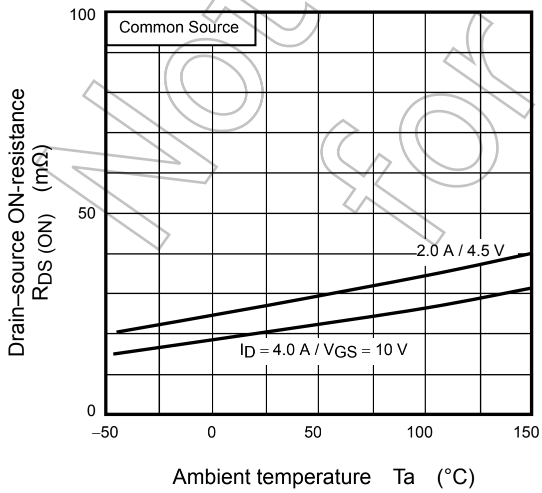
$R_{DS (ON)}$ – V_{GS}



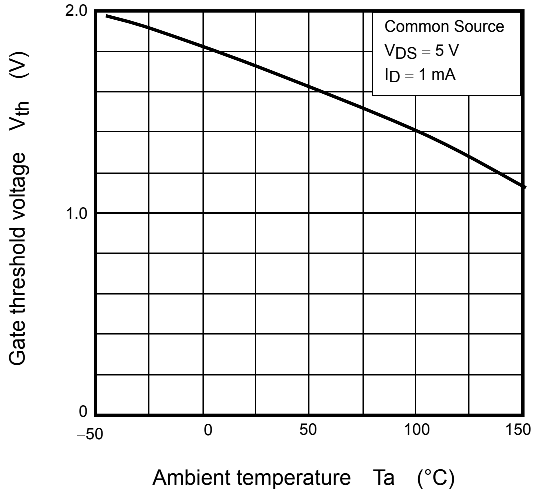
$R_{DS (ON)}$ – I_D



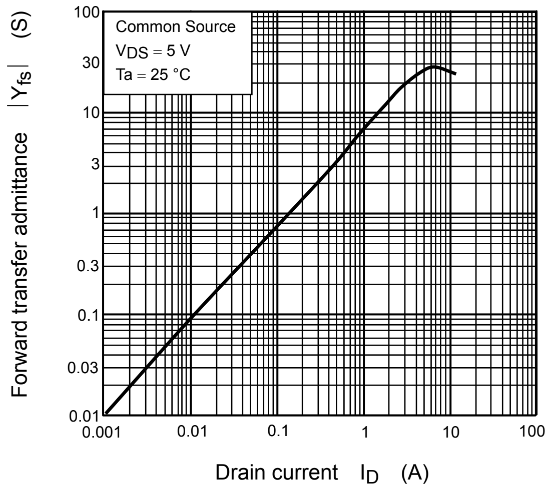
$R_{DS (ON)}$ – Ta



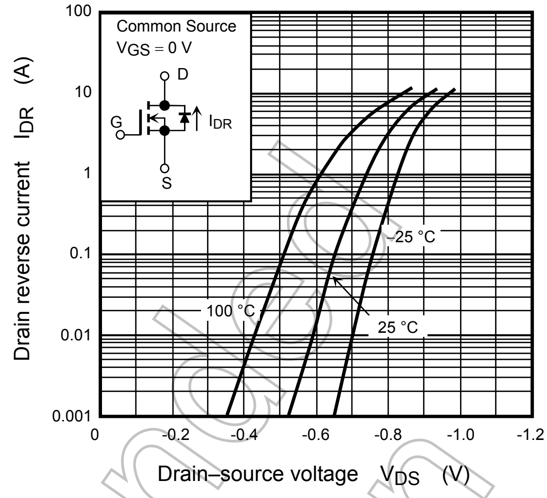
V_{th} – Ta



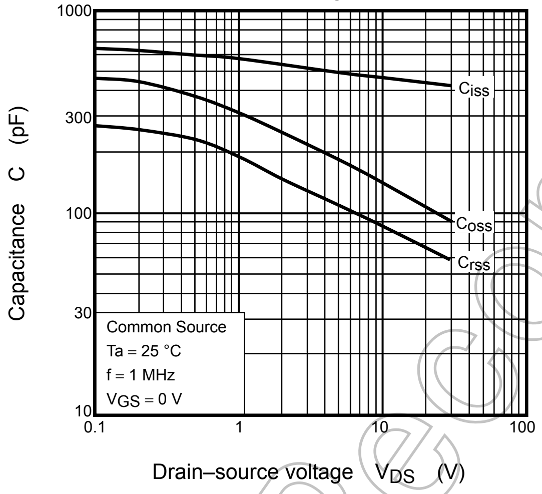
|Yfs| – ID



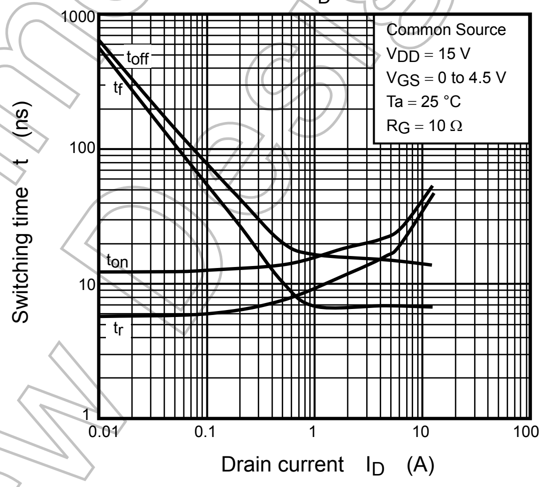
IDR – VDS



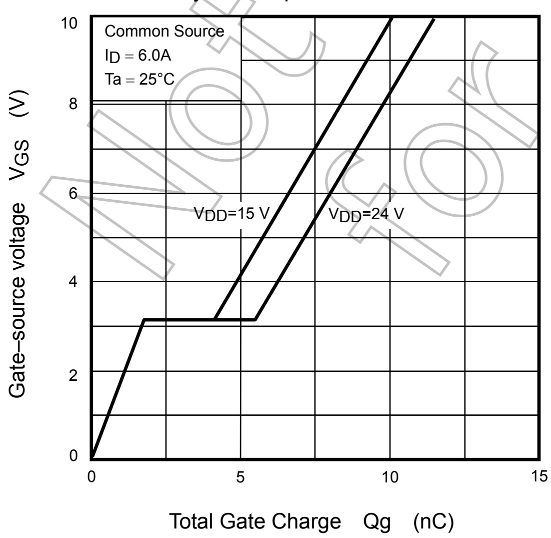
C – VDS

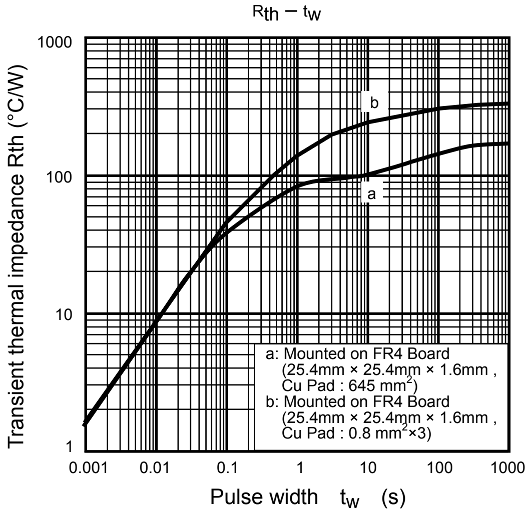


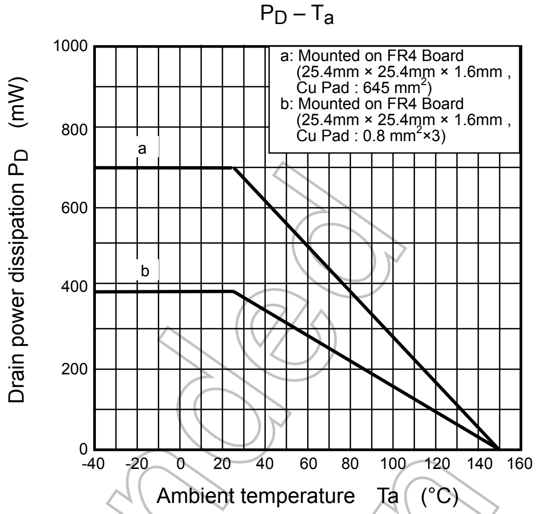
t – ID



Dynamic Input Characteristic




Rth – tw
Transient thermal impedance Rth (°C/W)
1000
100
10
1
0.001
0.01
0.1
1
10
100
1000
Pulse width tw (s)
b
a
a: Mounted on FR4 Board
(25.4mm × 25.4mm × 1.6mm ,
Cu Pad : 645 mm2)
b: Mounted on FR4 Board
(25.4mm × 25.4mm × 1.6mm ,
Cu Pad : 0.8 mm2×3)


PD – Ta
Drain power dissipation PD (mW)
1000
800
600
400
200
0
-40
-20
0
20
40
60
80
100
120
140
160
Ambient temperature Ta (°C)
a
b
a: Mounted on FR4 Board
(25.4mm × 25.4mm × 1.6mm ,
Cu Pad : 645 mm2)
b: Mounted on FR4 Board
(25.4mm × 25.4mm × 1.6mm ,
Cu Pad : 0.8 mm2×3)

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