

# TC74HC191AP, TC74HC191AF

## 4-Bit Binary Up/Down Counter

The TC74HC191A are high speed CMOS 4-BIT UP/DOWN COUNTERs fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The TC74HC191A is 4-bit binary up/down counter.

They have an asynchronous load input (LOAD) which is active low.

The direction of counting is determined by the level of DOWN/UP. When D/U is low, the counter counts up; when D/U is high, it counts down. Counting occurs on the positive going transition of the clock input.

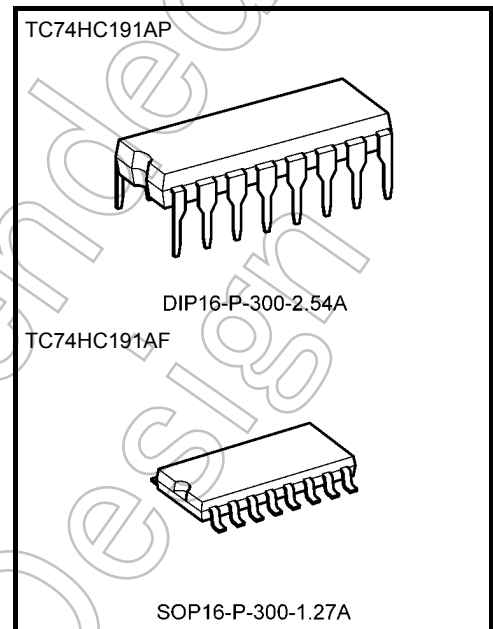
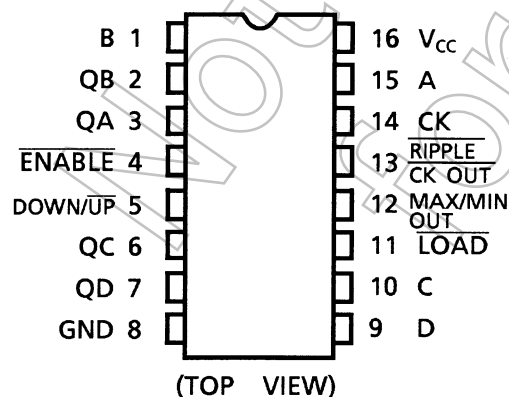
Enable input (ENABLE) and two carry inputs (RIPPLE CLOCK OUT, MAX/MIN) are provided to permit easy cascading of the counters, which facilitates easy implementation of N-bit counters without using external gates.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

### Features

- High speed:  $f_{max} = 48 \text{ MHz (typ.) at } V_{CC} = 5 \text{ V}$
- Low power dissipation:  $I_{CC} = 4 \mu\text{A (max) at } T_a = 25^\circ\text{C}$
- High noise immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (min)}$
- Output drive capability: 10 LSTTL loads
- Symmetrical output impedance:  $|I_{OH}| = I_{OL} = 4 \text{ mA (min)}$
- Balanced propagation delays:  $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range:  $V_{CC} \text{ (opr)} = 2 \text{ to } 6 \text{ V}$
- Pin and function compatible with 74LS191

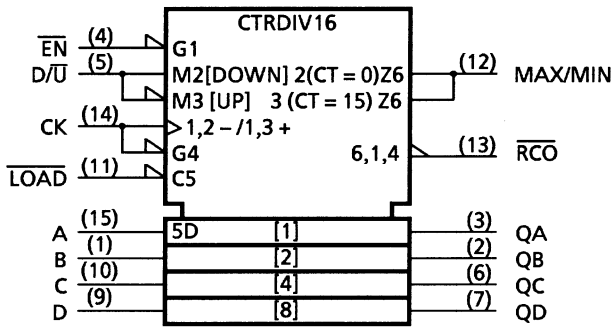
### Pin Assignment



Weight		
DIP16-P-300-2.54A	:	1.00 g (typ.)
SOP16-P-300-1.27A	:	0.18 g (typ.)

Start of commercial production  
1988-11

**IEC Logic Symbol**



**Truth Table**

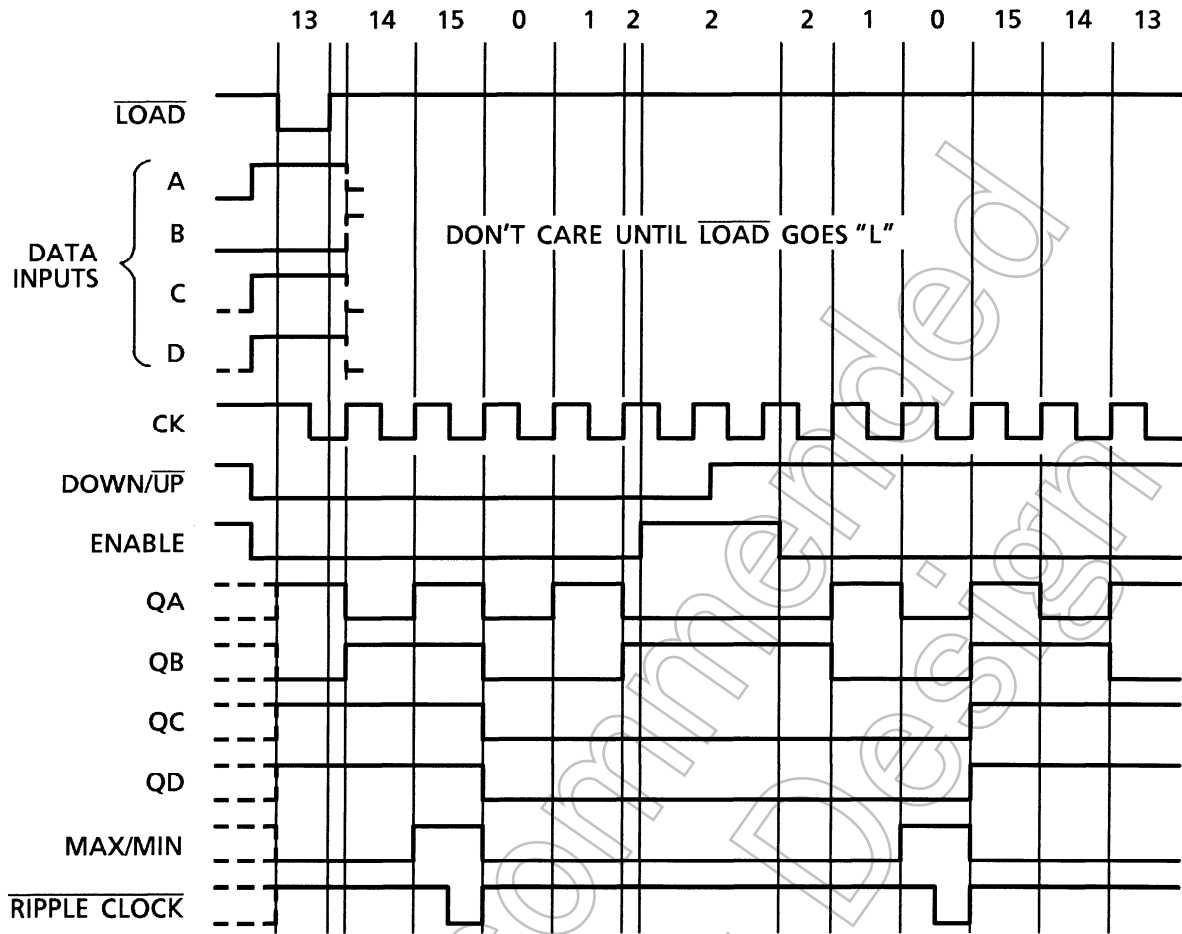
Inputs				Outputs				Function
LOAD	ENABLE	D/ $\bar{U}$	CK	QA	QB	QC	QD	
L	X	X	X	a	b	c	d	Preset Data
H	L	L	$\uparrow$	Up Count				Up Count
H	L	H	$\uparrow$	Down Count				Down Count
H	H	X	$\uparrow$	No Change				No Count
H	X	X	$\downarrow$	No Change				No Count

X: Don't care

a to d: Inputs level of A to D

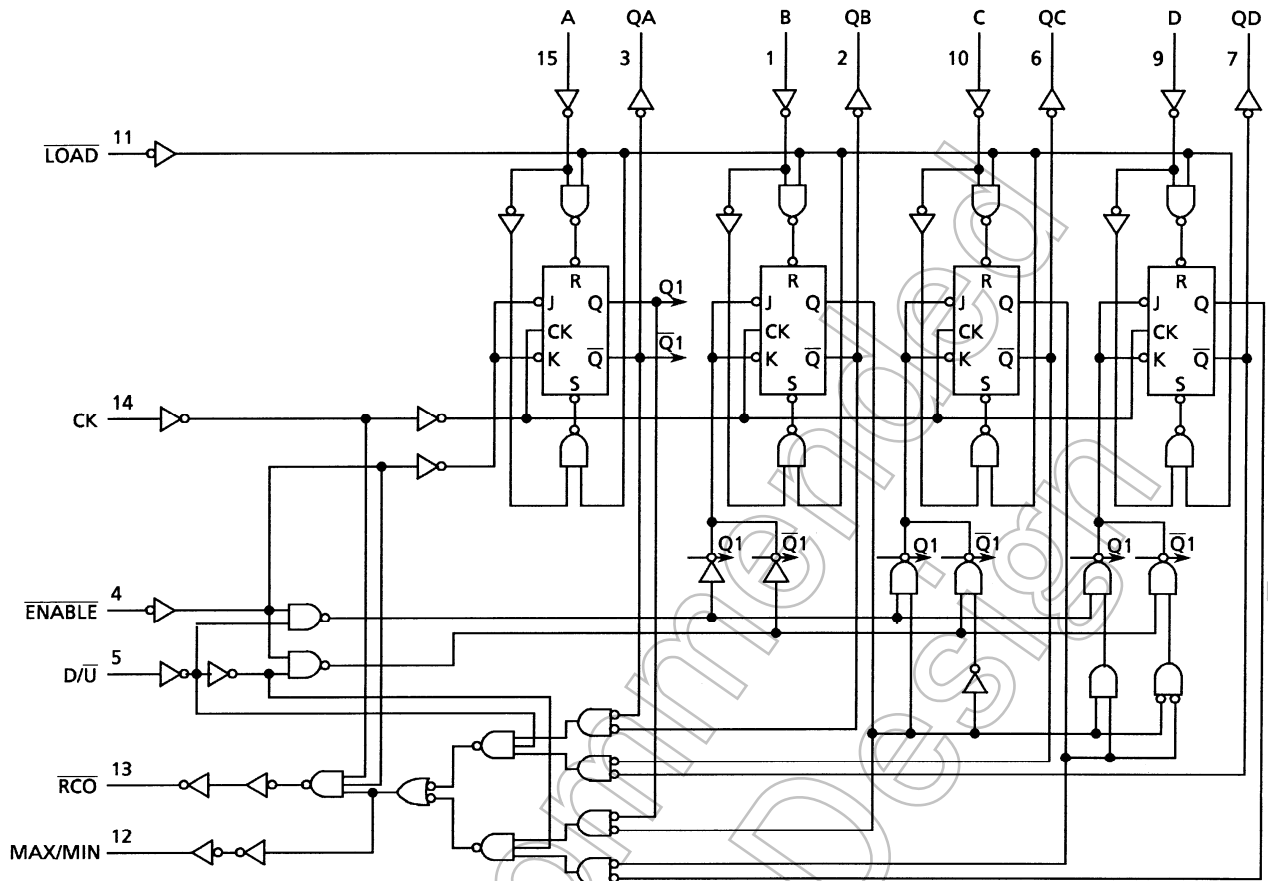
Not Recommended for New Design

**Timing Chart**



Not Recommended for New

System Diagram



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**Absolute Maximum Ratings (Note 1)**

Characteristics	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	-0.5 to 7	V
DC input voltage	$V_{IN}$	-0.5 to $V_{CC} + 0.5$	V
DC output voltage	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$	$\pm 20$	mA
Output diode current	$I_{OK}$	$\pm 20$	mA
DC output current	$I_{OUT}$	$\pm 25$	mA
DC $V_{CC}$ /ground current	$I_{CC}$	$\pm 50$	mA
Power dissipation	$P_D$	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	$T_{stg}$	-65 to 150	$^{\circ}\text{C}$

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of  $T_a = -40$  to  $65^{\circ}\text{C}$ . From  $T_a = 65$  to  $85^{\circ}\text{C}$  a derating factor of  $-10$  mW/ $^{\circ}\text{C}$  shall be applied until 300 mW.

**Operating Ranges (Note)**

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	2 to 6	V
Input voltage	$V_{IN}$	0 to $V_{CC}$	V
Output voltage	$V_{OUT}$	0 to $V_{CC}$	V
Operating temperature	$T_{opr}$	-40 to 85	$^{\circ}\text{C}$
Input rise and fall time	$t_r, t_f$	0 to 1000 ( $V_{CC} = 2.0$ V) 0 to 500 ( $V_{CC} = 4.5$ V) 0 to 400 ( $V_{CC} = 6.0$ V)	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either  $V_{CC}$  or GND.

## Electrical Characteristics

### DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit	
				V <sub>CC</sub> (V)	Min	Typ.	Max	Min		Max
High-level input voltage	V <sub>IH</sub>	—		2.0	1.50	—	—	1.50	—	V
				4.5	3.15	—	—	3.15	—	
				6.0	4.20	—	—	4.20	—	
Low-level input voltage	V <sub>IL</sub>	—		2.0	—	—	0.50	—	0.50	V
				4.5	—	—	1.35	—	1.35	
				6.0	—	—	1.80	—	1.80	
High-level output voltage	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	2.0	1.9	2.0	—	1.9	—	V
				4.5	4.4	4.5	—	4.4	—	
				6.0	5.9	6.0	—	5.9	—	
			I <sub>OH</sub> = -4 mA	4.5	4.18	4.31	—	4.13	—	
				6.0	5.68	5.80	—	5.63	—	
Low-level output voltage	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	2.0	—	0.0	0.1	—	0.1	V
				4.5	—	0.0	0.1	—	0.1	
				6.0	—	0.0	0.1	—	0.1	
			I <sub>OL</sub> = 4 mA	4.5	—	0.17	0.26	—	0.33	
				6.0	—	0.18	0.26	—	0.33	
Input leakage current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		6.0	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		6.0	—	—	4.0	—	40.0	μA

Not Recommended for New

**Timing Requirements (input:  $t_r = t_f = 6 \text{ ns}$ )**

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C	Unit
			VCC (V)	Typ.	Limit	Limit	
Minimum pulse width (CK)	$t_W (H)$ $t_W (L)$	—	2.0	—	100	125	ns
			4.5	—	20	25	
			6.0	—	17	21	
Minimum pulse width ( $\overline{\text{LOAD}}$ )	$t_W (L)$	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum set-up time ( $\overline{\text{ENABLE}}$ , D/ $\overline{U}$ )	$t_s$	—	2.0	—	150	190	ns
			4.5	—	30	38	
			6.0	—	26	33	
Minimum set-up time (DATA- $\overline{\text{LOAD}}$ )	$t_s$	—	2.0	—	50	65	ns
			4.5	—	10	13	
			6.0	—	9	11	
Minimum hold time ( $\overline{\text{ENABLE}}$ , D/ $\overline{U}$ )	$t_h$	—	2.0	—	0	0	ns
			4.5	—	0	0	
			6.0	—	0	0	
Minimum hold time (DATA- $\overline{\text{LOAD}}$ )	$t_h$	—	2.0	—	0	0	ns
			4.5	—	0	0	
			6.0	—	0	0	
Minimum removal time	$t_{rem}$	—	2.0	—	50	65	ns
			4.5	—	10	13	
			6.0	—	9	11	
Clock frequency	f	—	2.0	—	5	4	MHz
			4.5	—	25	20	
			6.0	—	29	24	

Not Recommended for New Design

AC Characteristics ( $C_L = 15 \text{ pF}$ ,  $V_{CC} = 5 \text{ V}$ ,  $T_a = 25^\circ\text{C}$ , input:  $t_r = t_f = 6 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time	$t_{TLH}$ $t_{THL}$	—	—	4	8	ns
Propagation delay time (CK-Q)	$t_{pLH}$ $t_{pHL}$	—	—	18	31	ns
Propagation delay time (CK- $\overline{\text{RCO}}$ )	$t_{pLH}$ $t_{pHL}$	—	—	10	20	ns
Propagation delay time (CK-MAX/MIN)	$t_{pLH}$ $t_{pHL}$	—	—	23	42	ns
Propagation delay time ( $\overline{\text{LOAD}}$ -Q)	$t_{pLH}$ $t_{pHL}$	—	—	21	35	ns
Propagation delay time (DATA-Q)	$t_{pLH}$ $t_{pHL}$	—	—	17	30	ns
Propagation delay time ( $\overline{\text{ENABLE}}$ - $\overline{\text{RCO}}$ )	$t_{pLH}$ $t_{pHL}$	—	—	11	17	ns
Propagation delay time (D/ $\overline{\text{U}}$ - $\overline{\text{RCO}}$ )	$t_{pLH}$ $t_{pHL}$	—	—	17	31	ns
Propagation delay time (D/ $\overline{\text{U}}$ - MAX/MIN)	$t_{pLH}$ $t_{pHL}$	—	—	15	27	ns
Maximum clock frequency	$f_{\text{max}}$	—	27	48	—	MHz

Not Recommended  
for New Design



## AC Characteristics (C<sub>L</sub> = 50 pF, input: t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C		Unit	
			V <sub>CC</sub> (V)	Min	Typ.	Max	Min		Max
Output transition time	t <sub>TLH</sub> t <sub>THL</sub>	—	2.0	—	30	75	—	95	ns
			4.5	—	8	15	—	19	
			6.0	—	7	13	—	16	
Propagation delay time (CK-Q)	t <sub>pLH</sub> t <sub>pHL</sub>	—	2.0	—	88	180	—	225	ns
			4.5	—	22	36	—	45	
			6.0	—	19	31	—	38	
Propagation delay time (CK-RCO)	t <sub>pLH</sub> t <sub>pHL</sub>	—	2.0	—	52	120	—	150	ns
			4.5	—	13	24	—	30	
			6.0	—	11	20	—	26	
Propagation delay time (CK-MAX/MIN)	t <sub>pLH</sub> t <sub>pHL</sub>	—	2.0	—	108	240	—	300	ns
			4.5	—	27	48	—	60	
			6.0	—	23	41	—	51	
Propagation delay time (LOAD-Q)	t <sub>pLH</sub> t <sub>pHL</sub>	—	2.0	—	100	205	—	255	ns
			4.5	—	25	41	—	51	
			6.0	—	22	35	—	43	
Propagation delay time (DATA-Q)	t <sub>pLH</sub> t <sub>pHL</sub>	—	2.0	—	84	175	—	220	ns
			4.5	—	21	35	—	44	
			6.0	—	18	30	—	37	
Propagation delay time (ENABLE-RCO)	t <sub>pLH</sub> t <sub>pHL</sub>	—	2.0	—	56	105	—	130	ns
			4.5	—	14	21	—	26	
			6.0	—	12	18	—	22	
Propagation delay time (D/Ü-RCO)	t <sub>pLH</sub> t <sub>pHL</sub>	—	2.0	—	84	180	—	225	ns
			4.5	—	21	36	—	45	
			6.0	—	18	31	—	38	
Propagation delay time (D/Ü-MAX/MIN)	t <sub>pLH</sub> t <sub>pHL</sub>	—	2.0	—	72	160	—	200	ns
			4.5	—	18	32	—	40	
			6.0	—	15	27	—	34	
Maximum clock frequency	f <sub>max</sub>	—	2.0	5	11	—	4	—	MHz
			4.5	25	44	—	20	—	
			6.0	29	52	—	24	—	
Input capacitance	C <sub>IN</sub>	—	—	5	10	—	10	pF	
Power dissipation capacitance	C <sub>PD</sub> (Note)	—	—	101	—	—	—	pF	

Note: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

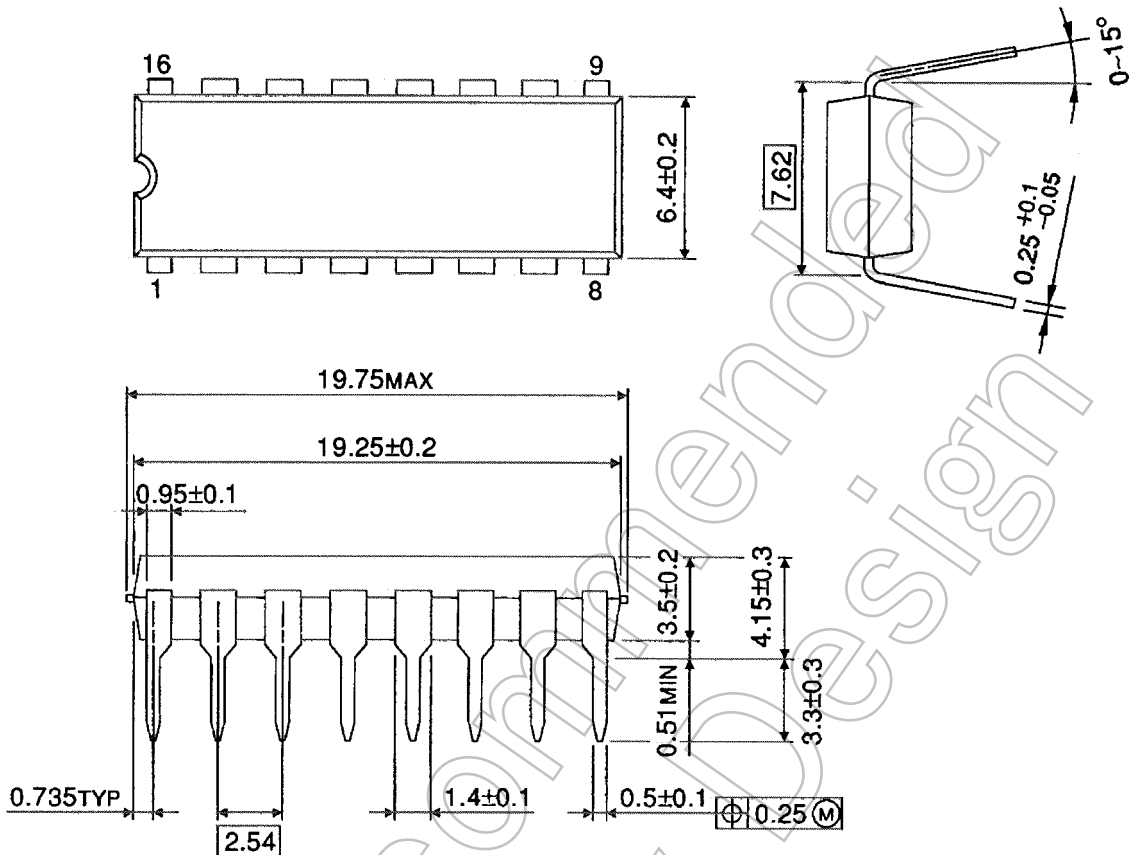
Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

**Package Dimensions**

DIP16-P-300-2.54A

Unit : mm



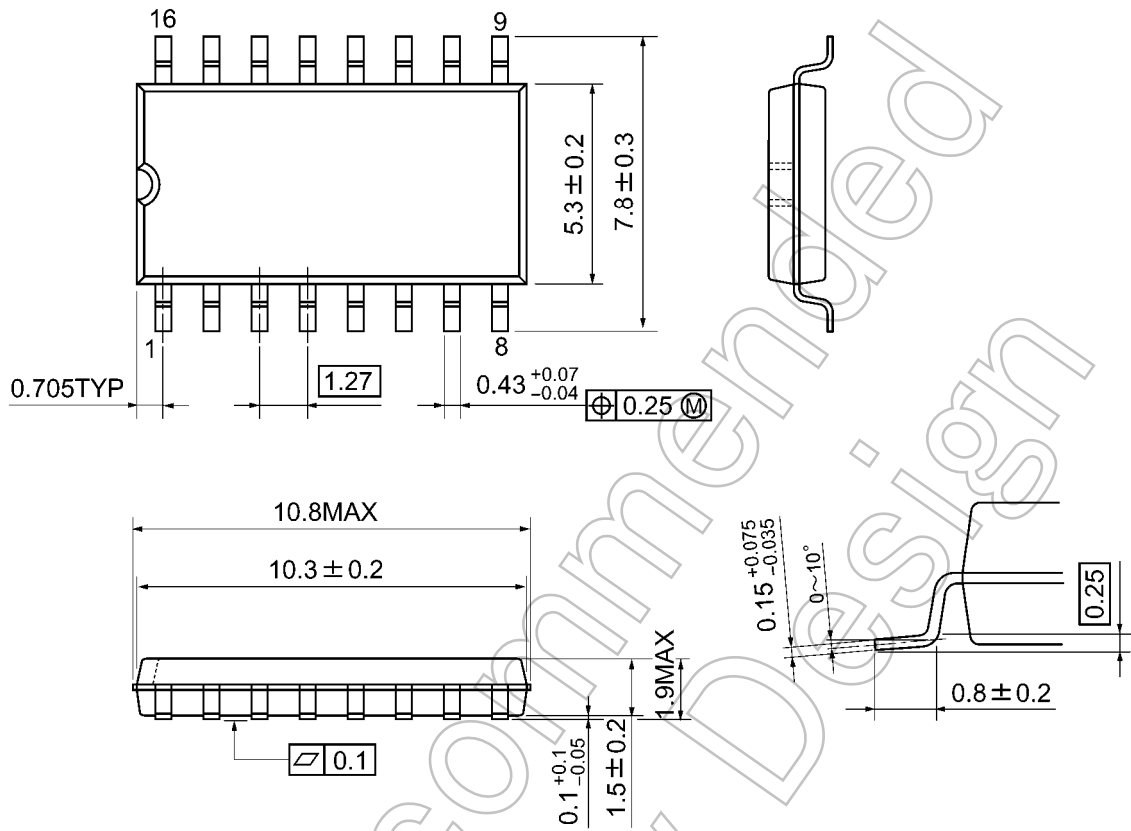
Weight: 1.00 g (typ.)

Not Recommended for New Design

**Package Dimensions**

SOP16-P-300-1.27A

Unit: mm



Weight: 0.18 g (typ.)

Not Recommended for New Design

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