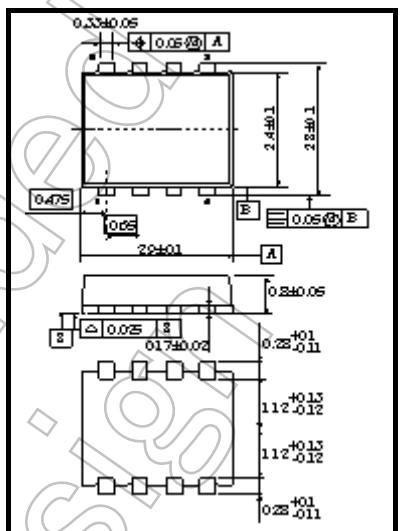
TOSHIBA Field Effect Transistor Silicon N-Channel MOS Type (U-MOSⅥ-H)

# TPCP8007-H

Switching Regulator Applications
Motor Drive Applications
DC-DC Converter Applications

- Small footprint due to a small and thin package
- High-speed switching
- Small gate charge: $Q_{SW}$ = 2.7 nC (typ.)
- Low drain-source ON-resistance:
  $R_{DS\ (ON)}$ = 40 mΩ (typ.)
- High forward transfer admittance: $|Y_{fs}|$ = 16 S (typ.)
- Low leakage current: $I_{DSS}$ = 10 μA (max) ($V_{DS}$ = 60 V)
- Enhancement mode: $V_{th}$ = 1.3 to 2.3 V ($V_{DS}$ = 10 V, $I_D$ = 0.1 mA)

Unit: mm




| | |
|---|---|
| JEDEC | ― |
| JEITA | ― |
| TOSHIBA | 2-3V1K |

Weight: 0.017g (typ.)

## Absolute Maximum Ratings (Ta = 25°C)

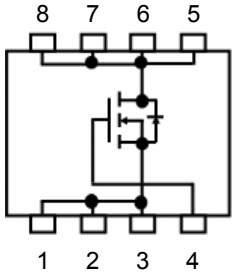
| Characteristic | | Symbol | Rating | Unit |
|---|---|---|---|---|
| Drain-source voltage | | $V_{DSS}$ | 60 | V |
| Drain-gate voltage ($R_{GS}$ = 20 kΩ) | | $V_{DGR}$ | 60 | V |
| Gate-source voltage | | $V_{GSS}$ | ±20 | V |
| Drain current | DC (Note 1) | $I_D$ | 5 | A |
| | Pulsed (Note 1) | $I_{DP}$ | 20 | |
| Drain power dissipation (t = 5 s) (Note 2a) | | $P_D$ | 1.68 | W |
| Drain power dissipation (t = 5 s) (Note 2b) | | $P_D$ | 0.84 | W |
| Single-pulse avalanche energy (Note 3) | | $E_{AS}$ | 9 | mJ |
| Avalanche current | | $I_{AR}$ | 5 | A |
| Repetitive avalanche energy (Tc = 25°C) (Note 4) | | $E_{AR}$ | 0.05 | mJ |
| Channel temperature | | $T_{ch}$ | 150 | °C |
| Storage temperature range | | $T_{stg}$ | −55 to 150 | °C |

Note: For Notes 1 to 5, refer to the next page.

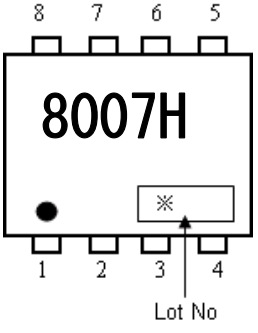
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

This transistor is an electrostatic-sensitive device. Handle with care.

## Circuit Configuration




## Marking (Note 5)




Start of commercial production
2009-09

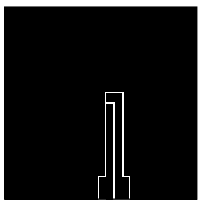
Not Recommended for New Design

## Thermal Characteristics

| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| Thermal resistance, channel to ambient (t = 5 s) (Note 2a) | $R_{th\ (ch\text{-}a)}$ | 74.4 | °C/W |
| Thermal resistance, channel to ambient (t = 5 s) (Note 2b) | $R_{th\ (ch\text{-}a)}$ | 148.8 | °C/W |

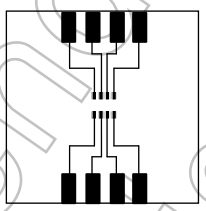
Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: (a) Device mounted on a glass-epoxy board (a) (b) Device mounted on a glass-epoxy board (b)



FR-4
25.4 × 25.4 × 0.8
(Unit: mm)

(a)



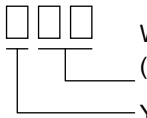
FR-4
25.4 × 25.4 × 0.8
(Unit: mm)

(b)

Note 3: $V_{DD}$ = 24 V, $T_{ch}$ = 25°C (initial), L = 500 μH, $R_G$ = 1 Ω, $I_{AR}$ = 5 A

Note 4: Repetitive rating: pulse width limited by maximum channel temperature

Note 5: * Weekly code: (Three digits)



Week of manufacture
(01 for the first week of the year, continuing up to 52 or 53)

Year of manufacture
(The last digit of the year)

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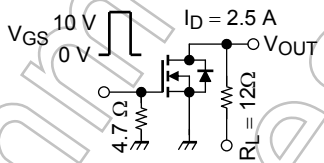
## Electrical Characteristics (Ta = 25°C)

| Characteristic | | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| Gate leakage current | | $I_{GSS}$ | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | — | — | ±100 | nA |
| Drain cutoff current | | $I_{DSS}$ | $V_{DS}$ = 60 V, $V_{GS}$ = 0 V | — | — | 10 | μA |
| Drain-source breakdown voltage | | $V_{(BR)\ DSS}$ | $I_D$ = 10 mA, $V_{GS}$ = 0 V | 60 | — | — | V |
| | | $V_{(BR)\ DSX}$ | $I_D$ = 10 mA, $V_{GS}$ = −20 V | 45 | — | — | |
| Gate threshold voltage | | $V_{th}$ | $V_{DS}$ = 10 V, $I_D$ = 0.1 mA | 1.3 | — | 2.3 | V |
| Drain-source ON-resistance | | $R_{DS\ (ON)}$ | $V_{GS}$ = 4.5 V, $I_D$ = 2.5 A | — | 47 | 64 | mΩ |
| | | | $V_{GS}$ = 10 V, $I_D$ = 2.5 A | — | 40 | 57 | |
| Forward transfer admittance | | $\|Y_{fs}\|$ | $V_{DS}$ = 10 V, $I_D$ = 2.5 A | 8 | 16 | — | S |
| Input capacitance | | $C_{iss}$ | $V_{DS}$ = 10 V, $V_{GS}$ = 0 V, f = 1 MHz | — | 640 | 900 | pF |
| Reverse transfer capacitance | | $C_{rss}$ | | — | 25 | 40 | |
| Output capacitance | | $C_{oss}$ | | — | 90 | — | |
| Gate resistance | | rg | $V_{DS}$ = 10 V, $V_{GS}$ = 0 V, f = 1 MHz | — | 3.2 | 4.6 | Ω |
| Switching time | Rise time | $t_r$ |  | — | 2.4 | — | ns |
| | Turn-on time | $t_{on}$ | | — | 7.8 | — | |
| | Fall time | $t_f$ | | — | 2.4 | — | |
| | Turn-off time | $t_{off}$ | | — | 18 | — | |
| Total gate charge (gate-source plus gate-drain) | | $Q_g$ | $V_{DD}$ ≈ 48 V, $V_{GS}$ = 10 V, $I_D$ = 5 A | — | 11 | — | nC |
| | | | $V_{DD}$ ≈ 48 V, $V_{GS}$ = 5 V, $I_D$ = 5 A | — | 5.8 | — | |
| Gate-source charge 1 | | $Q_{gs1}$ | $V_{DD}$ ≈ 48 V, $V_{GS}$ = 10 V, $I_D$ = 5 A | — | 2.3 | — | |
| Gate-drain (“Miller”) charge | | $Q_{gd}$ | | — | 1.7 | — | |
| Gate switch charge | | $Q_{SW}$ | | — | 2.7 | — | |



## Source-Drain Ratings and Characteristics (Ta = 25°C)

| Characteristic | | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| Peak forward current | Pulse (Note 1) | $I_{FP}$ | — | — | — | 20 | A |
| Forward voltage (diode) | | $V_{DSF}$ | $I_{DR}$ = 5 A, $V_{GS}$ = 0 V | — | — | −1.2 | V |

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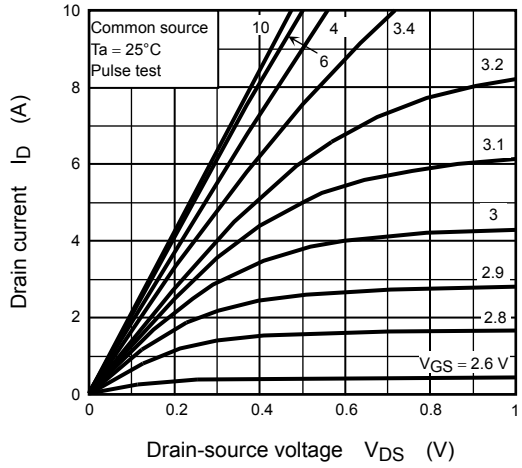
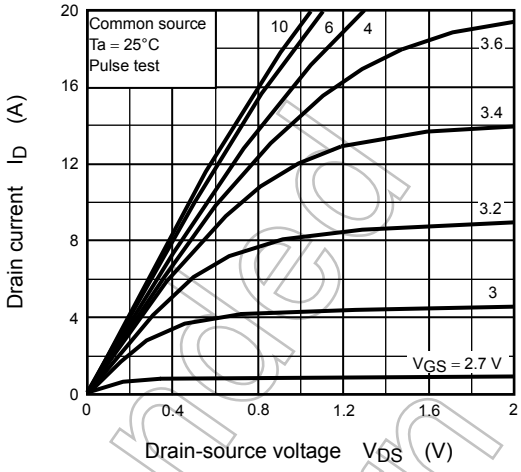
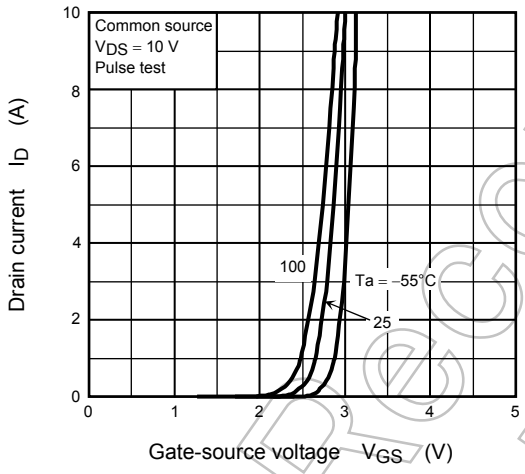
$I_D - V_{DS}$



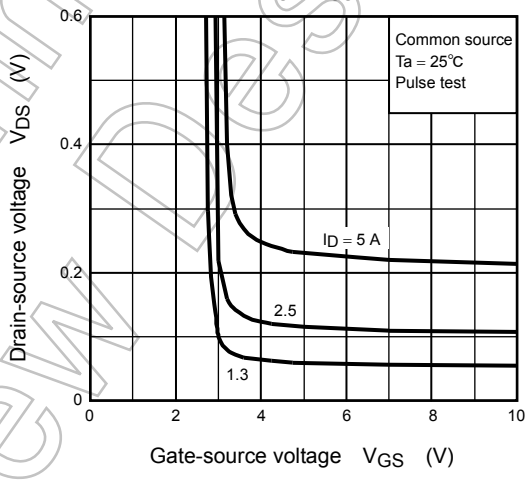

$I_D - V_{DS}$



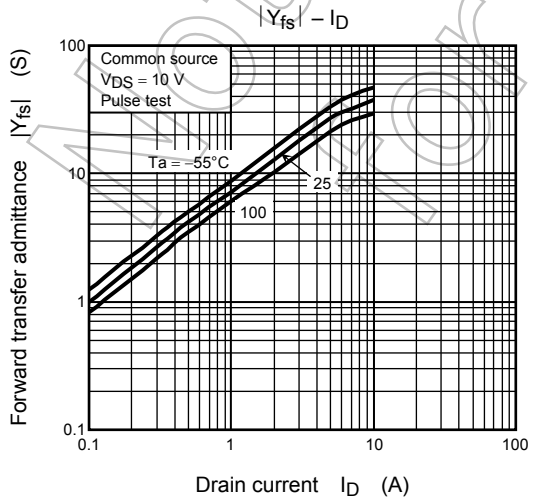

$I_D - V_{GS}$



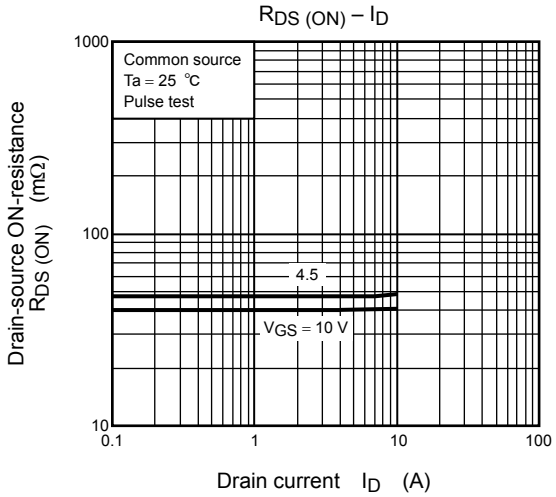

$V_{DS} - V_{GS}$




$|Y_{fs}| - I_D$




$R_{DS\ (ON)} - I_D$

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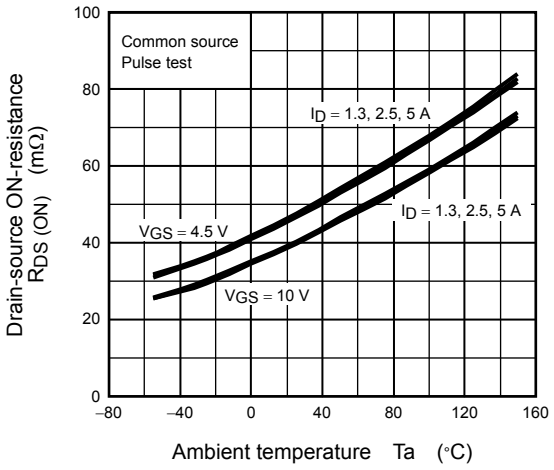
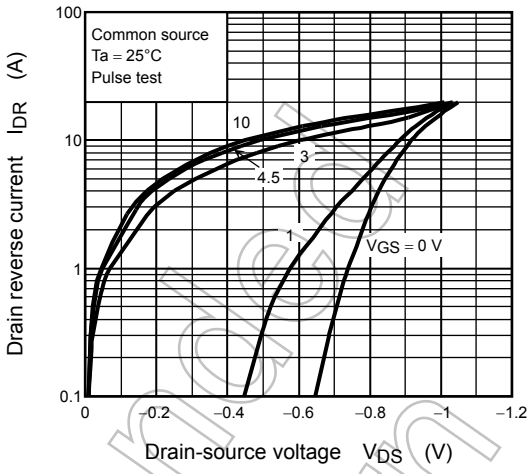
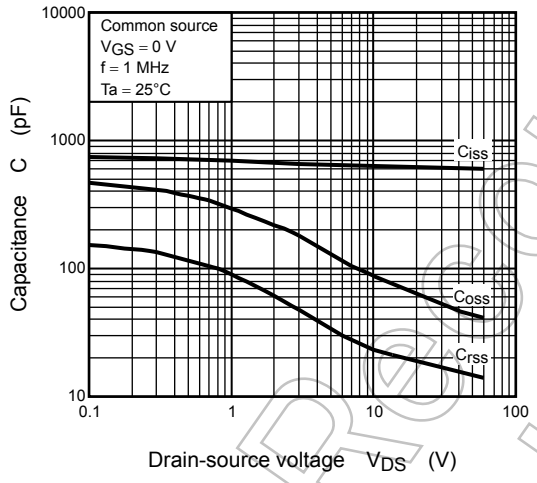
$R_{DS\ (ON)}$ – Ta



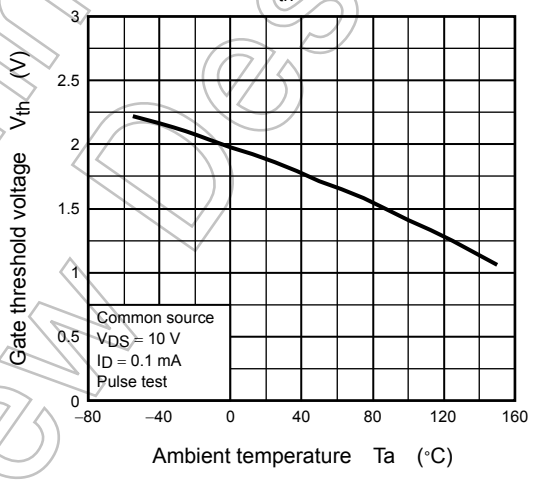

$I_{DR}$ – $V_{DS}$



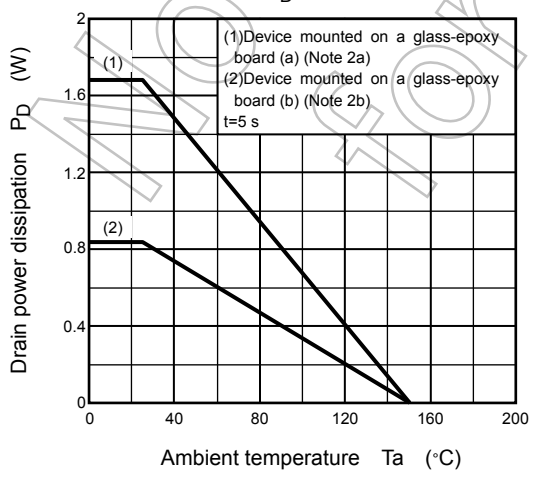

Capacitance – $V_{DS}$



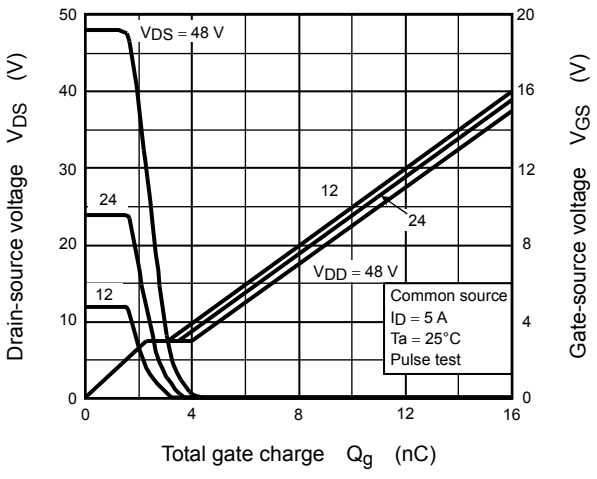

$V_{th}$ – Ta




$P_D$ – Ta




Dynamic input/output characteristics

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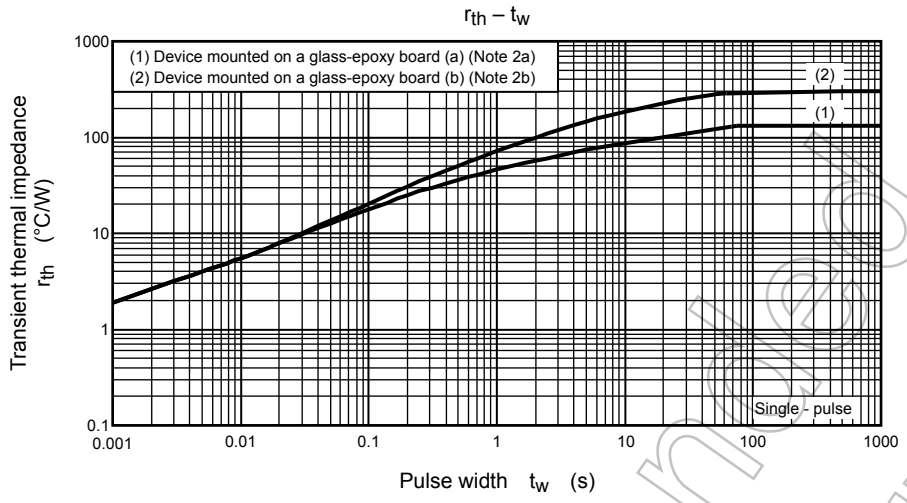


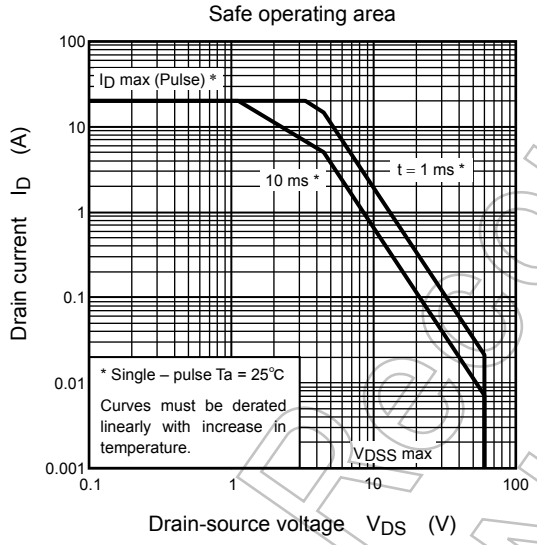


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