TOSHIBA

TOSHIBA Original CMOS 16-Bit Microcontroller

TLCS-900 Series

TMP96C041BFG

TOSHIBA CORPORATION

Semiconductor Company

Preface

Thank you very much for making use of Toshiba microcomputer LSIs.
Before use this LSI, refer the section, "Points of Note and Restrictions".
Especially, take care below cautions.

CAUTION

How to release the HALT mode

Usually, interrupts can release all halts status. However, the interrupts = ($\overline{\text{NMI}}$, INT0), which can release the HALT mode may not be able to do so if they are input during the period CPU is shifting to the HALT mode (for about 3 clocks of X1) with IDLE or STOP mode. (In this case, an interrupt request is kept on hold internally.)

If another interrupt is generated after it has shifted to HALT mode completely, halt status can be released without difficultly. The priority of this interrupt is compare with that of the interrupt kept on hold internally, and the interrupt with higher priority is handled first followed by the other interrupt.

Document Change Notification

The purpose of this notification is to inform customers about the launch of the Pb-free version of the device. The introduction of a Pb-free replacement affects the datasheet. Please understand that this notification is intended as a substitute for a revision of the datasheet.

Changes to the datasheet may include the following, though not all of them may apply to this particular device.

1. Part number

   Example: TMPxxxxxxF → TMPxxxxxxFG

   All references to the previous part number were left unchanged in body text. The new part number is indicated on the prelims pages (cover page and this notification).

2. Package code and package dimensions

   Example: LQFP100-P-1414-0.50C → LQFP100-P-1414-0.50F

   All references to the previous package code and package dimensions were left unchanged in body text. The new ones are indicated on the prelims pages.

3. Addition of notes on lead solderability

   Now that the device is Pb-free, notes on lead solderability have been added.

4. RESTRICTIONS ON PRODUCT USE

   The previous (obsolete) provision might be left unchanged on page 1 of body text. A new replacement is included on the next page.

5. Publication date of the datasheet

   The publication date at the lower right corner of the prelims pages applies to the new device.

1. Part number

Previous Part Number (in Body Text)	New Part Number
TMP96C041BF	TMP96C041BFG

2. Package code and dimensions

Previous Package Code (in Body Text)	New Package Code
QFP80-P-1420-0.80B	QFP80-P-1420-0.80M

*: For the dimensions of the new package, see the attached Package Dimensions diagram.

3. Addition of notes on lead solderability

The following solderability test is conducted on the new device.

Solderability of lead free products

Test Parameter	Test Condition	Note
Solderability	Use of Sn-37Pb solder Bath Solder bath temperature = 230°C, Dipping time = 5 seconds The number of times = one, Use of R-type flux	Pass: Solderability rate until forming ≥ 95%
	Use of Sn-3.0Ag-0.5Cu solder bath Solder bath temperature = 245°C, Dipping time = 5 seconds The number of times = one, Use of R-type flux (use of lead free)	

4. RESTRICTIONS ON PRODUCT USE

The following replaces the "RESTRICTIONS ON PRODUCT USE" on page 1 of body text.

RESTRICTIONS ON PRODUCT USE 20070701-EN

- The information contained herein is subject to change without notice.
- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.
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- For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance/Handling Precautions.

5. Publication date of the datasheet

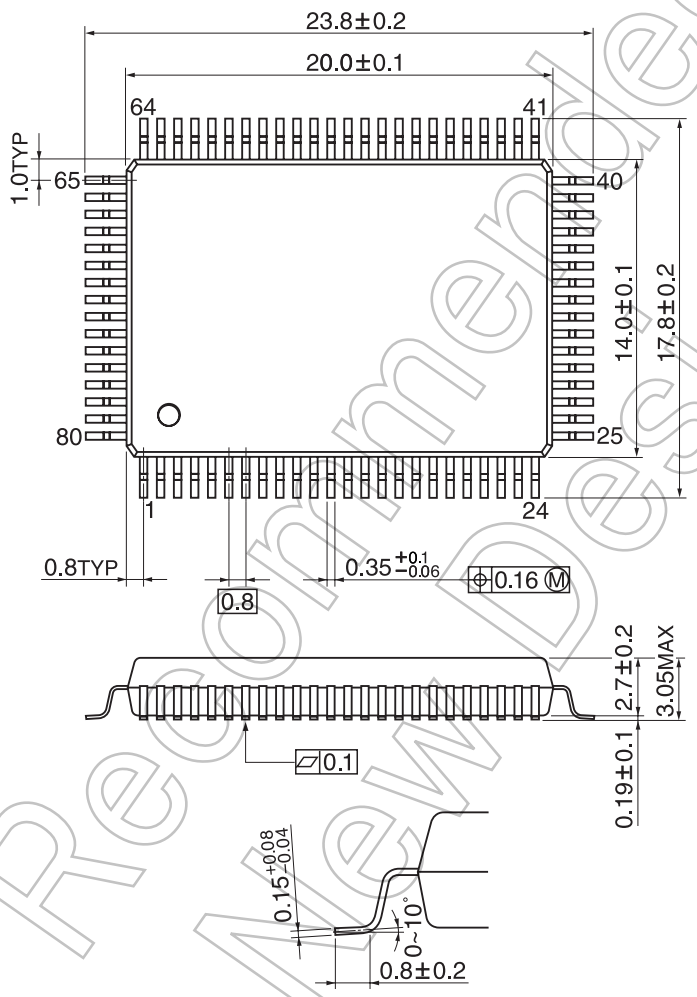
The publication date of this datasheet is printed at the lower right corner of this notification.

(Annex)

Package Dimensions

QFP80-P-1420-0.80M

Unit: mm



CMOS 16-bit Microcontrollers

TMP96C041BF

1. Outline and Device Characteristics

TMP96C041BF is high-speed advanced 16-bit microcontrollers developed for controlling medium to large-scale equipment. The TMP96C041B has RAMless for TMP96C141BF. Otherwise, the devices function in the same way.

TMP96C041BF is housed in an 80-pin flat package.

Device characteristics are as follows:

(1) Original 16-bit CPU
- TLCS-90 instruction mnemonic upward compatible.
- 16M-byte linear address space
- General-purpose registers and register bank system
- 16-bit multiplication / division and bit transfer/arithmetic instructions
- High-speed micro DMA : 4 channels (1.6 μs/2 bytes @ 20 MHz)

(2) Minimum instruction execution time : 200 ns @ 20 MHz

(3) Internal RAM : None
Internal ROM : None

(4) External memory expansion
- Can be expanded up to16M bytes (for both programs and data).
- Can mix 8- and 16-bit external data buses.

(5) 8-bit timers : 2 channels

(6) 8-bit PWM timers : 2 channels

(7) 16-bit timers : 2 channels

(8) Pattern generators : 4 bits, 2 channels

(9) Serial interface : 2 channels

(10) 10-bit A/D converter : 4 channels

(11) Watchdog timer

(12) Chip select/wait controller : 3 blocks

(13) Interrupt functions
- 3 CPU interrupts··· SWI instruction, priviledged violation, and Illegal instruction
- 14 internal interrupts
- 6 external interrupts

7-level priority can be set.

(14) I/O ports
47 pins

(15) Standby function : 3 halt modes (RUN, IDLE, STOP)

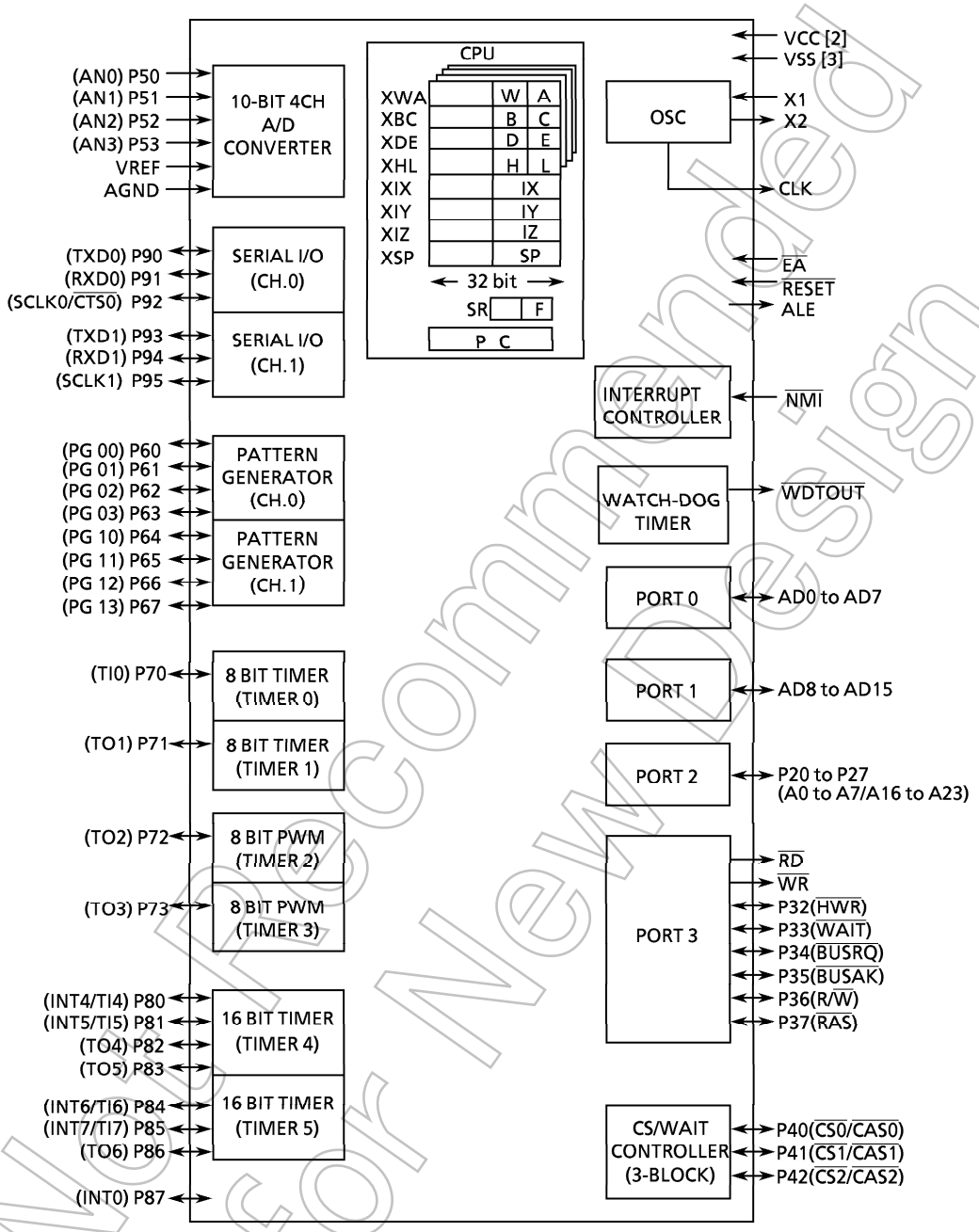


Figure1 TMP96C041B Block Diagram

2. Pin Assignment and Functions

The assignment of input / output pins for TMP96C041B, their name and outline functions are described below.

2.1 Pin Assignment

Figure 2.1 shows pin assignment of TMP96C041BF.

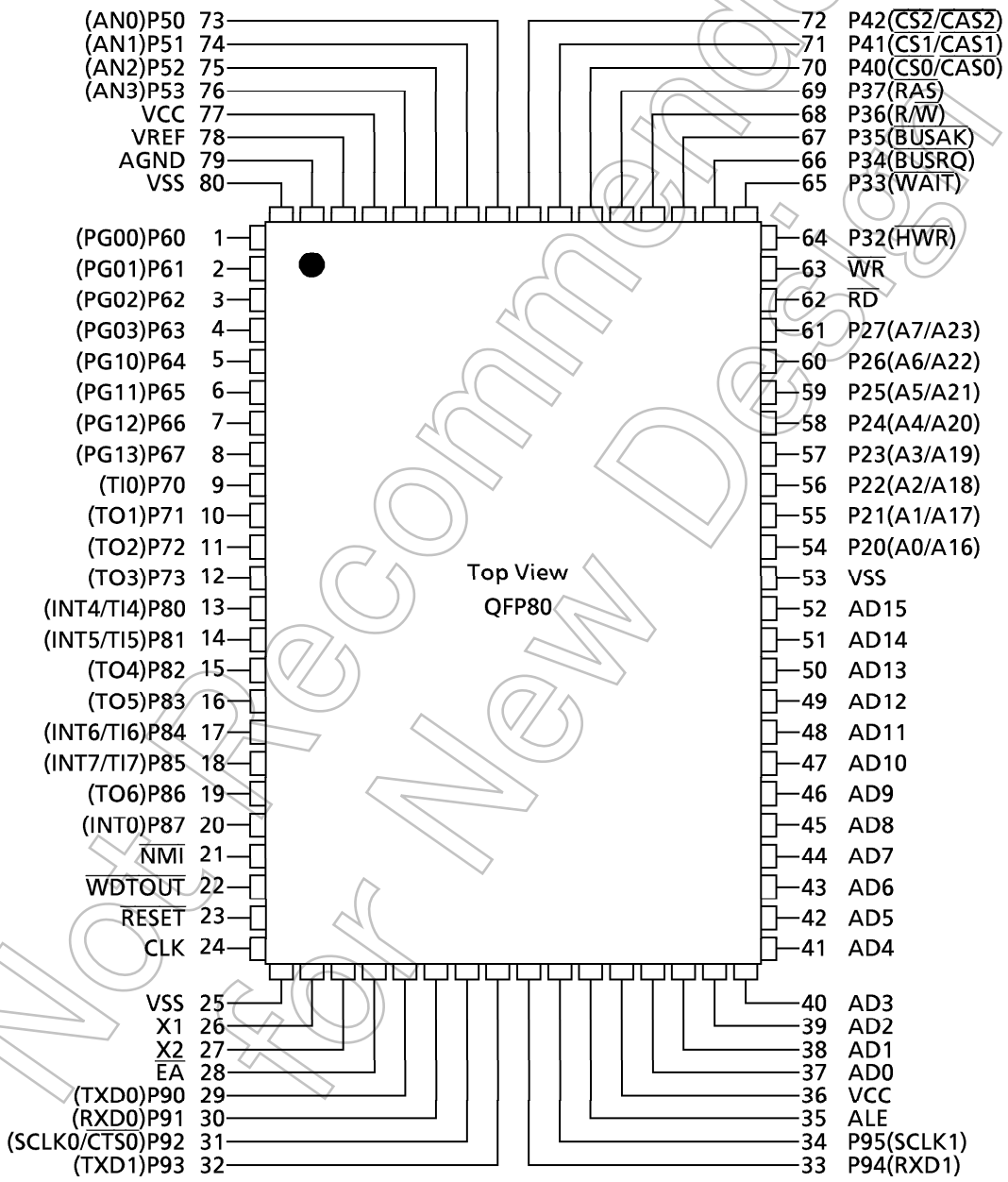


Figure 2.1 Pin Assignment (80-pin QFP)

2.2 Pin Names and Functions

The names of input/output pins and their functions are described below.

Table 2.2 Pin Names and Functions.

Pin name	Number of pins	I/O	Functions
AD0 to AD7	8	Tri-state	Address/data (lower): 0 to 7 for address/data bus
AD8 to AD15	8	Tri-state	Address data (upper): 8 to 15 for address/data bus
P20 to P27 A0 to A7 A16 to A23	8	I/O Output Output	Port 2: I/O port that allows selection of I/O on a bit basis (with pull-down resistor) Address: 0 to 7 for address bus Address: 16 to 23 for address bus
$\overline{RD}$	1	Output	Read: Strobe signal for reading external memory
$\overline{WR}$	1	Output	Write: Strobe signal for writing data on pins AD0 to 7
P32 $\overline{HWR}$	1	I/O Output	Port 32: I/O port (with pull-up resistor) High write: Strobe signal for writing data on pins AD8 to 15
P33 $\overline{WAIT}$	1	I/O Input	Port 33: I/O port (with pull-up resistor) Wait: Pin used to request CPU bus wait
P34 $\overline{BUSRQ}$	1	I/O Input	Port34: I/O port (with pull-up resistor) Bus request: Signal used to request high impedance for AD0 to 15, A0 to 23, $\overline{RD}$, $\overline{WR}$,$\overline{HWR}$, R/$\overline{W}$, $\overline{RAS}$, $\overline{CS0}$, $\overline{CS1}$, and $\overline{CS2}$ pins. (For external DMAC)
P35 $\overline{BUSAK}$	1	I/O Output	Port 35: I/O port (with pull-up resistor) Bus acknowledge: Signal indicating that AD0 to 15, A0 to 23, $\overline{RD}$, $\overline{WR}$,$\overline{HWR}$, R/$\overline{W}$, $\overline{RAS}$, $\overline{CS0}$, $\overline{CS1}$, and $\overline{CS2}$ pins are at high impedance after receiving BUSRQ. (For external DMAC)
P36 R/$\overline{W}$	1	I/O Output	Port 36: I/O port (with pull-up resistor) Read/write: 1 represents read or dummy cycle; 0, write cycle.
P37 $\overline{RAS}$	1	I/O Output	Port 37: I/O port (with pull-up resistor) Row address strobe: Outputs RAS strobe for DRAM.
P40 $\overline{CS0}$ $\overline{CAS0}$	1	I/O Output Output	Port 40: I/O port (with pull-up resistor) Chip select 0: Outputs 0 when address is within specified address area. Column address strobe 0: Outputs CAS strobe for DRAM when address is within specified address area.

Note : With the external DMA controller, this device's built-in memory or built-in I/O cannot be accessed using the $\overline{BUSRQ}$ and $\overline{BUSAK}$ pins.

Pin name	Number of pins	I/O	Functions
P41 $\overline{CS1}$ $\overline{CAS1}$	1	I/O Output Output	Port 41: I/O port (with pull-up resistor) Chip select 1: Outputs 0 if address is within specified address area. Column address strobe 1: Outputs $\overline{CAS}$ strobe for DRAM if address is within specified address area.
P42 $\overline{CS2}$ $\overline{CAS2}$	1	I/O Output Output	Port 42: I/O port (with pull-down resistor) (Note) Chip select 2: Outputs 0 if address is within specified address area. Column address strobe 2: Outputs $\overline{CAS}$ strobe for DRAM if address is within specified address area.
P50~P53 AN0~AN3	4	Input Input	Port 5: Input port Analog input: Input to A/D converter
VREF	1	Input	Pin for reference voltage input to A/D converter
AGND	1	Input	Ground pin for A/D converter
P60~P63 PG00~PG03	4	I/O Output	Ports 60 to 63: I/O ports that allow selection of I/O on a bit basis (with pull-up resistor) Pattern generator ports: 00 to 03
P64~P67 PG10~PG13	4	I/O Output	Ports 64 to 67: I/O ports that allow selection of I/O on a bit basis (with pull-up resistor) Pattern generator ports: 10 to 13
P70 TI0	1	I/O Input	Port 70: I/O port (with pull-up resistor) Timer input 0: Timer 0 input
P71 TO1	1	I/O Output	Port 71: I/O port (with pull-up resistor) Timer output 1: Timer 0 or 1 output
P72 TO2	1	I/O Output	Port 72: I/O port (with pull-up resistor) PWM output 2: 8-bit PWM timer 2 output
P73 TO3	1	I/O Output	Port 73: I/O port (with pull-up resistor) PWM output 3: 8-bit PWM timer 3 output
P80 TI4 INT4	1	I/O Input Input	Port 80: I/O port (with pull-up resistor) Timer input 4: Timer 4 count/capture trigger signal input Interrupt request pin 4: Interrupt request pin with programmable rising/falling edge
P81 TI5 INT5	1	I/O Input Input	Port 81: I/O port (with pull-up resistor) Timer input 5: Timer 4 count/capture trigger signal input Interrupt request pin 5: Interrupt request pin with rising edge
P82 TO4	1	I/O Output	Port 82: I/O port (with pull-up resistor) Timer output 4: Timer 4 output pin
P83 TO5	1	I/O Output	Port 83: I/O port (with pull-up resistor) Timer output 5: Timer 4 output pin

Note : Case of the settable $\overline{CS2}$ or $\overline{CAS2}$; when TMP96C041BF is bus release, this pin is not added the internal pull-down resistor but is added the internal pull-up resistor.

Pin name	Number of pins	I/O	Functions
P84 TI6 INT6	1	I/O Input Input	Port 84: I/O port (with pull-up resistor) Timer input 6: Timer 5 count/capture trigger signal input Interrupt request pin 6: Interrupt request pin with programmable rising/falling edge
P85 TI7 INT7	1	I/O Input Input	Port 85: I/O port (with pull-up resistor) Timer input 7: Timer 5 count/capture trigger signal input Interrupt request pin 7: Interrupt request pin with rising edge
P86 TO6	1	I/O Output	Port 86: I/O port (with pull-up resistor) Timer output 6: Timer 5 output pin
P87 INT0	1	I/O Input	Port 87: I/O port (with pull-up resistor) Interrupt request pin 0: Interrupt request pin with programmable level/rising edge
P90 TXD0	1	I/O Output	Port 90: I/O port (with pull-up resistor) Serial send data 0
P91 RXD0	1	I/O Input	Port 91: I/O port (with pull-up resistor) Serial receive data 0
P92 $\overline{CTS0}$ SCLK0	1	I/O Input	Port 92: I/O port (with pull-up resistor) Serial data send enable 0 (Clear to Send) Serial clock I/O 0
P93 TXD1	1	I/O Output	Port 93: I/O port (with pull-up resistor) Serial send data 1
P94 RXD1	1	I/O Input	Port 94: I/O port (with pull-up resistor) Serial receive data 1
P95 SCLK1	1	I/O I/O	Port 95: I/O port (with pull-up resistor) Serial clock I/O 1
$\overline{WDTOUT}$	1	Output	Watchdog timer output pin
$\overline{NMI}$	1	Input	Non-maskable interrupt request pin: Interrupt request pin with falling edge. Can also be operated at rising edge by program.
CLK	1	Output	Clock output: Outputs「X1÷4」clock. Pulled-up during reset.
$\overline{EA}$	1	Input	External access: 0 should be inputted with TMP96C041B.
ALE	1	Output	Address latch enable
$\overline{RESET}$	1	Input	Reset: Initializes LSI. (With pull-up resistor)
X1/X2	2	I/O	Oscillator connecting pin
VCC	2		Power supply pin (+ 5 V) (All Vcc pins should be connected with the power supply pin.)
VSS	3		GND pin (0 V) (All Vss pins should be connected with GND (0 V).)

Note : Pull-up/pull-down resistor can be released from the pin by software (except the $\overline{RESET}$ pin).

3. Operation

This section describes the functions and basic operations of TMP96C041B device.

The function of CPU and internal I/O devices are the same function as TMP96C141B. Check the 「7. Care Points and Restriction of TMP96C141B 」because of the Care described.

Regarding the functions of TMP96C041B (not described), see the part of TMP96C141B.

TMP96C141B/TMP96C041B have much the same function but they are different from following points.

Parameter	TMP96C141B	TMP96C041B
Interrnal RAM	1 Kbyte	not exist
Mapping area of CS1 defult setting (B1C1/0: 00)	480H to 7FFFH	80H to 7FFFH

3.1 CPU

TMP96C041B device has a built-in high-performance 16-bit CPU (900-CPU). (For CPU operation, see TLCS-900 CPU in the previous section.)

3.2 Memory Map

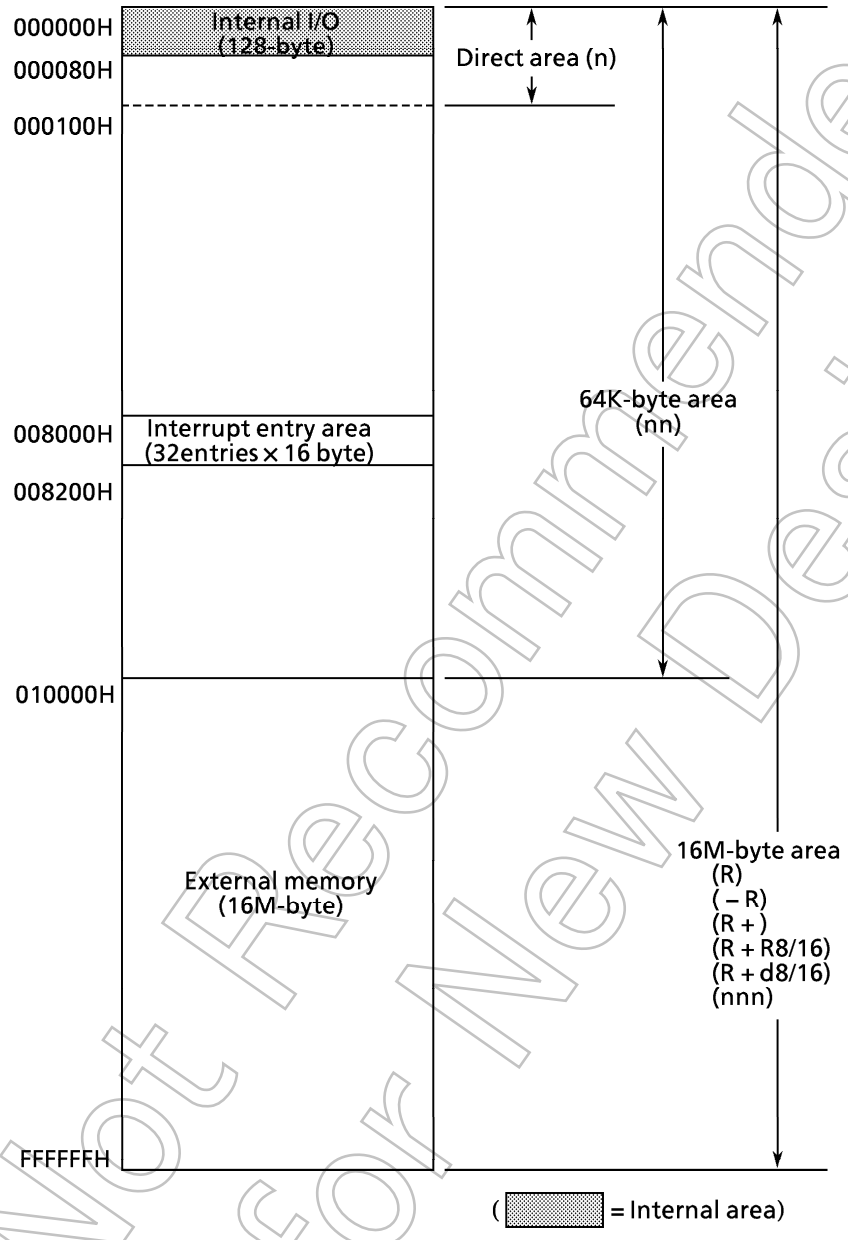
TMP96C041B has two register modes. One is a minimum mode; in this mode, the area of program memory is 64 Kbytes maximum. The other is a maximum mode; in this mode, the area of program memory is 16 Mbytes maximum.

Both minimum and maximum modes are the data memory area of 16 Mbytes maximum.

That is, the program memory can locate 0H to FFFFH in minimum mode and can locate 0H to FFFFFFH in maximum mode.

Memory Map

Figure 3.2 (1) is a memory map of the TMP96C041B.



Note : The start address after reset is 8000H. Resetting sets the stack pointer (XSP) on the system mode side to 100H.

Figure3.2 (1) Memory map

(2) $\overline{CS1}$ area (Chip select / wait controller)

TMP96C041B is expanded the part of address area for $\overline{CS1}$ (only B1C1.0 = "00"). Show the address area of $\overline{CS1}$ in Fig 3.2 (2).

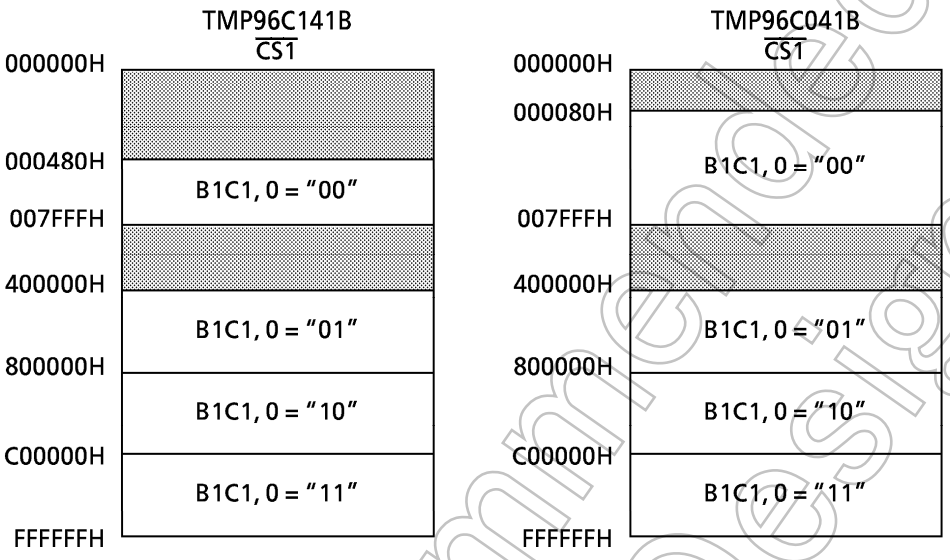


Fig.3.2 (2) $\overline{CS1}$ address area

4. Electrical Characteristics

4.1 Absolute Maximum Ratings (TMP96C041BF)

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V cc	– 0.5 to 6.5	V
Input Voltage	V IN	– 0.5 to Vcc + 0.5	V
Output Current (total)	Σ IOL	100	mA
Output Current (total)	Σ IOH	– 100	mA
Power Dissipation (Ta = 85℃)	P D	500	mW
Soldering Temperature (10 s)	T SOLDER	260	℃
Storage Temperature	T STG	– 65 to 150	℃
Operating Temperature	T OPR	– 40 to 85	℃

Note : The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

4.2 DC Characteristics (TMP96C041BF)

Vcc = 5 V ± 10%, TA = – 40 to 85℃ (4 to 16 MHz) TA = – 20 to 70℃ (4 to 20 MHz)

(Typical values are for Ta = 25℃ and Vcc = 5 V)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Low Voltage (AD0 to 15) P2, P3, P4, P5, P6, P7, P8, P9 RESET,NMI,INT0(P87) EA X1	V IL V IL1 V IL2 V IL3 V IL4		– 0.3 – 0.3 – 0.3 – 0.3 – 0.3	0.8 0.3 Vcc 0.25 Vcc 0.3 0.2 Vcc	V V V V V
Input High Voltage (AD0 – 15) P2, P3, P4, P5, P6, P7, P8, P9 RESET, NMI, INT0 (P87) EA X1	V IH V IH1 V IH2 V IH3 V IH4		2.2 0.7 Vcc 0.75 Vcc Vcc – 0.3 0.8 Vcc	Vcc + 0.3 Vcc + 0.3 Vcc + 0.3 Vcc + 0.3 Vcc + 0.3	V V V V V
Output Low Voltage	V OL	I OL = 1.6 mA		0.45	V
Output High Voltage	V OH V OH1 V OH2	I OH = – 400 μA I OH = – 100 μA I OH = – 20 μA	2.4 0.75 Vcc 0.9 Vcc		V V V
Darlington Drive Current (8 Output Pins max.)	I DAR	V EXT = 1.5 V R EXT = 1.1 kΩ	– 1.0	– 3.5	mA
Input Leakage Current Output Leakage Current	I LI I LO	0.0 ≦ Vin ≦ Vcc 0.2 ≦ Vin ≦ Vcc – 0.2	0.02 (Typ) 0.05 (Typ)	± 5 ± 10	μA μA
Operating Current (RUN) IDLE STOP (Ta = – 40 to 85℃) STOP (Ta = 0 to 50℃)	I cc	t osc = 20 MHz 0.2 ≦ Vin ≦ Vcc – 0.2 0.2 ≦ Vin ≦ Vcc – 0.2	21 (Typ) 1.7 (Typ) 0.2 (Typ)	50 10 50 10	mA mA μA μA
Power Down Voltage (@ STOP, RAM Back up)	V STOP	V IL2 = 0.2 Vcc, V IH2 = 0.8 Vcc	2.0	6.0	V
RESET Pull Up Resistor	R RST		50	150	kΩ
Pin Capacitance	C IO	tosc = 1 MHz		10	pF
Schmitt Width RESET, NMI, INT0 (P87)	V TH		0.4	1.0 (Typ)	V
Programmable Pull Down Resistor	R KL		10	80	kΩ
Programmable Pull Up Resistor	R KH		50	150	kΩ

Note : I-DAR is guaranteed for a total of up to 8 ports.

4.3 AC Electrical Characteristics (TMP96C041BF)

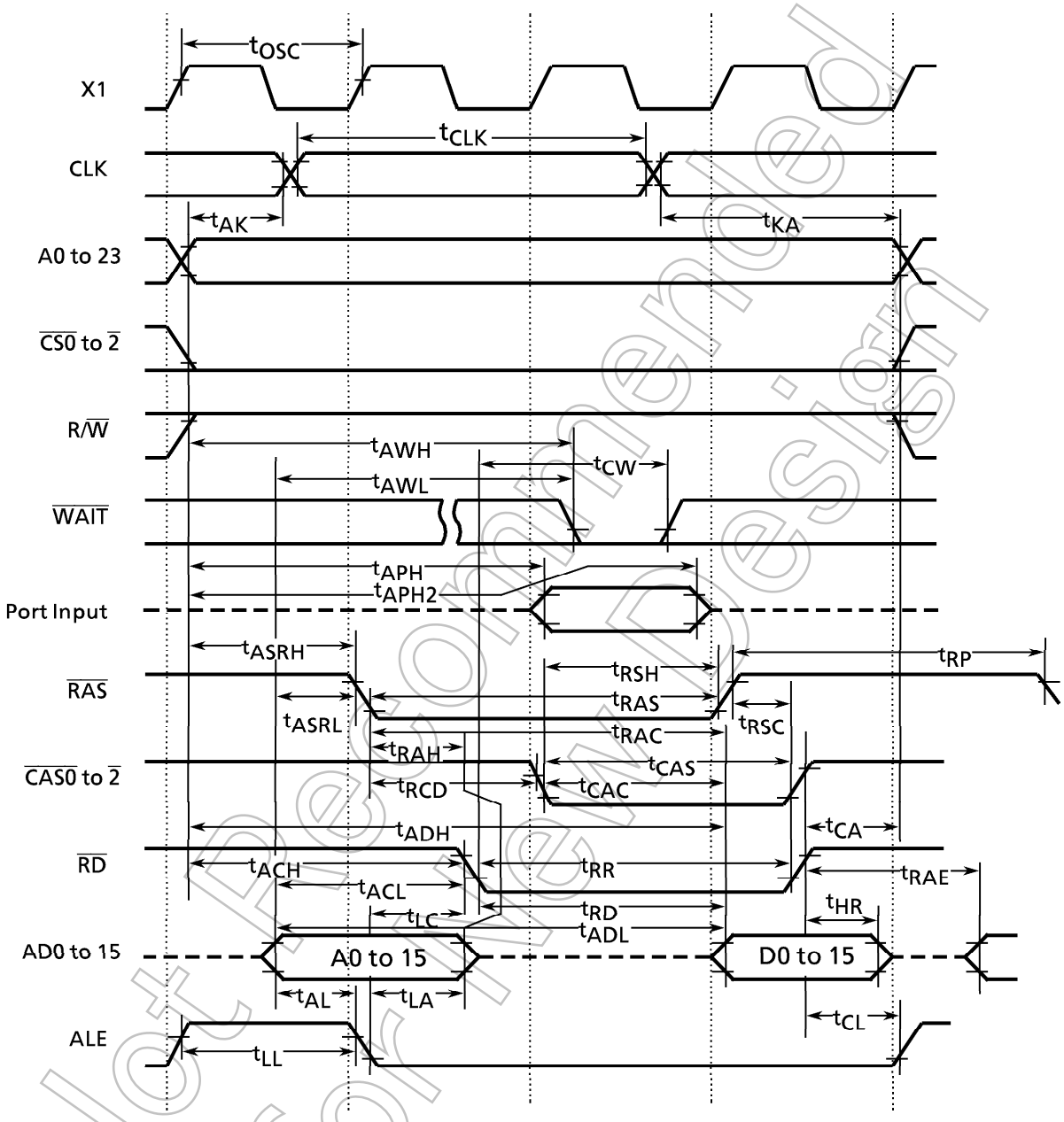
Vcc = 5 V ± 10%, TA = − 40 to 85℃ (4 to 16 MHz) TA = − 20 to 70℃ (4 to 20 MHz)

No.	Parameter	Symbol	Variavle		16 MHz		20 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	Osc. Period (= x)	t_{OSC}	50	250	62.5		50		ns
2	CLK width	t_{CLK}	2x − 40		85		60		ns
3	A0 to 23 Valid → CLK Hold	t_{AK}	0.5x − 20		11		5		ns
4	CLK Valid → A0 to 23 Hold	t_{KA}	1.5x − 70		24		5		ns
5	A0 to 15 Valid → ALE fall	t_{AL}	0.5x − 15		16		10		ns
6	ALE fall → A0 to 15 Hold	t_{LA}	0.5x − 15		16		10		ns
7	ALE High width	t_{LL}	x − 40		23		10		ns
8	ALE fall → $\overline{RD}/\overline{WR}$ fall	t_{LC}	0.5x − 30		1		-5		ns
9	$\overline{RD}/\overline{WR}$ rise → ALE rise	t_{CL}	0.5x − 20		11		5		ns
10	A0 to 15 Valid → $\overline{RD}/\overline{WR}$ fall	t_{ACL}	x − 25		38		25		ns
11	A0 to 23 Valid → $\overline{RD}/\overline{WR}$ fall	t_{ACH}	1.5x − 50		44		25		ns
12	$\overline{RD}/\overline{WR}$ rise → A0 to 23 Hold	t_{CA}	0.5x − 20		11		5		ns
13	A0 to 15 Valid → D0 to 15 input	t_{ADL}		3.0x − 45		143		105	ns
14	A0 to 23 Valid → D0 to 15 input	t_{ADH}		3.5x − 65		154		110	ns
15	$\overline{RD}$fall → D0 to 15 input	t_{RD}		2.0x − 50		75		50	ns
16	$\overline{RD}$ Low width	t_{RR}	2.0x − 40		85		60		ns
17	$\overline{RD}$rise → D0 to 15 Hold	t_{HR}	0		0		0		ns
18	$\overline{RD}$rise → A0 to 15output	t_{RAE}	x − 15		48		35		ns
19	$\overline{WR}$ Low width	t_{WW}	2.0x − 40		85		60		ns
20	D0 to 15 Valid → $\overline{WR}$ rise	t_{DW}	2.0x − 50		75		50		ns
21	$\overline{WR}$ rise → D0 to 15 Hold	t_{WD}	0.5x − 10		21		15		ns
22	A0 to 23 Valid → $\overline{WAIT}$ input ($^{1WAIT}_{+n\ mode}$)	t_{AEH}		3.5x − 90		129		85	ns
23	A0 to 15 Valid → $\overline{WAIT}$ input ($^{1WAIT}_{+n\ mode}$)	t_{AWL}		3.0x − 80		108		70	ns
24	$\overline{RD}/\overline{WR}$ fall → $\overline{WAIT}$ Hold ($^{1WAIT}_{+n\ mode}$)	t_{CW}	2.0x + 0		125		100		ns
25	A0 to 23 Valid → PORT input	t_{APH}		2.5x − 120		36		5	ns
26	A0 to 23 Valid → PORT Hold	t_{APH2}	2.5x + 50		206		175		ns
27	$\overline{WR}$ rise → PORT Valid	t_{CP}		200		200		200	ns
28	A0 to 23 Valid → $\overline{RAS}$ fall	t_{ASRH}	1.0x − 40		23		10		ns
29	A0 to 15 Valid → $\overline{RAS}$ fall	t_{ASRL}	0.5x − 15		16		10		ns
30	$\overline{RAS}$ fall → D0 to 15 input	t_{RAC}		2.5x − 70		86		55	ns
31	$\overline{RAS}$ fall → A0 to 15 Hold	t_{RAH}	0.5x − 15		16		10		ns
32	$\overline{RAS}$ Low width	t_{RAS}	2.0x − 40		85		60		ns
33	$\overline{RAS}$ High width	t_{RP}	2.0x − 40		85		60		ns
34	$\overline{CAS}$ fall → $\overline{RAS}$ rise	t_{RSH}	1.0x − 35		28		15		ns
35	$\overline{RAS}$ rise → $\overline{CAS}$ rise	t_{RSC}	0.5x − 25		6		0		ns
36	$\overline{RAS}$ fall → $\overline{CAS}$ fall	t_{RCD}	1.0x − 40		23		10		ns
37	$\overline{CAS}$ fall → D0 to 15 input	t_{CAC}		1.5x − 65		29		10	ns
38	$\overline{CAS}$ Low width	t_{CAS}	1.5x − 30		64		40		ns
39	D0 to 15 Valid → $\overline{CAS}$ fall	t_{DS}	0.5x − 15		16		10		ns

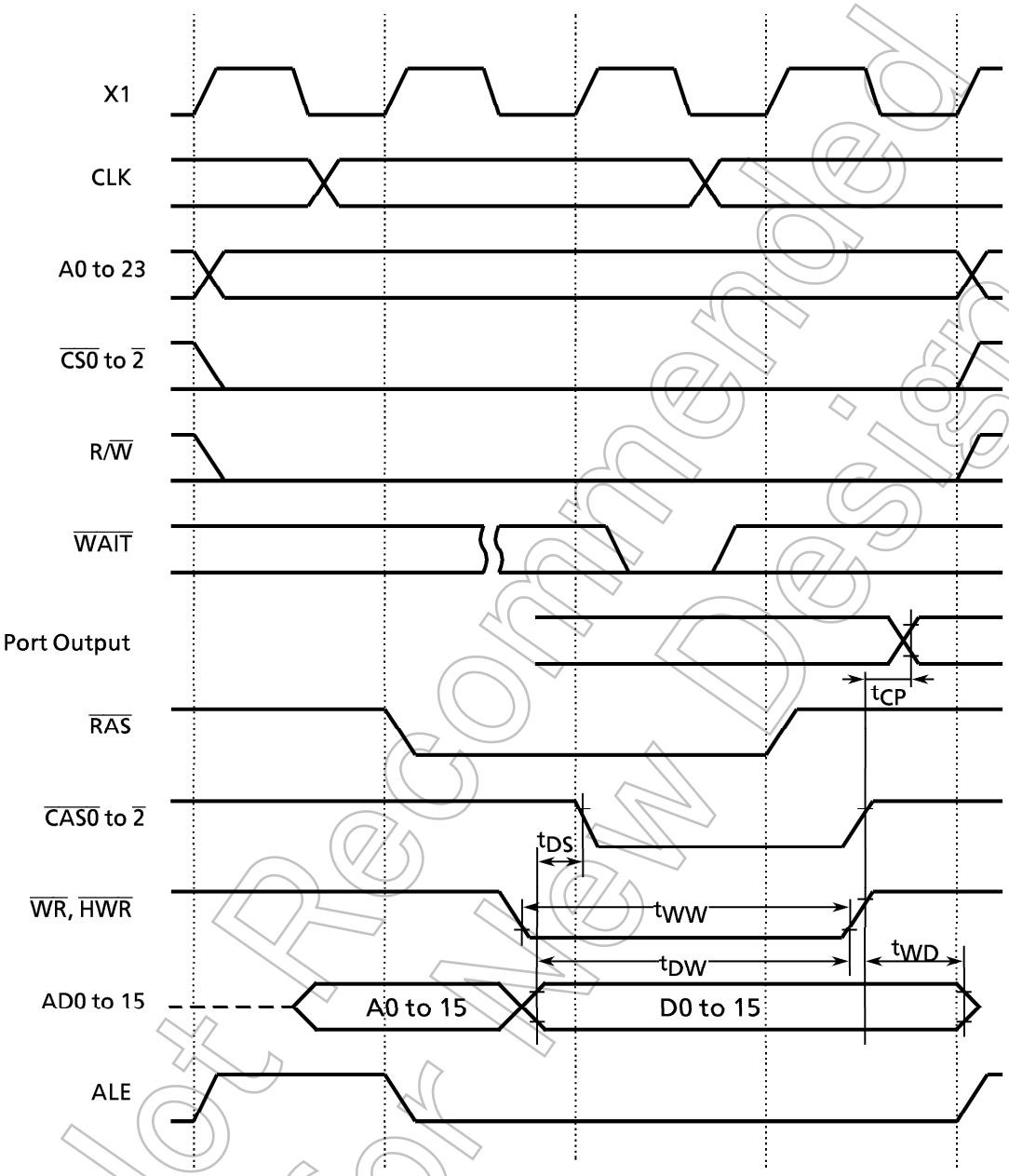
AC Measuring Conditions

- Output Level : High 2.2 V / Low 0.8 V, CL50 pF
  (However CL = 100pF for AD0 to AD15, A0 to A23, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, R/$\overline{W}$, CLK, $\overline{RAS}$, $\overline{CAS0}$ to $\overline{CAS2}$)
- Input Level : High 2.4 V / Low 0.45 V (AD0 to AD15)
  High 0.8 Vcc / Low 0.2 Vcc (Except for AD0 to AD15)

(1) Read Cycle



(2) Write Cycle



4.4 A/D Conversion Characteristics (TMP96C041BF)

Vcc = 5 V ± 10%, TA = − 40 to 85℃ (4 to 16 MHz) TA = − 20 to 70℃ (4 to 20 MHz)

Parameter		Symbol	Min	Typ.	Max	Unit
Analog reference voltage		V_{REF}	Vcc − 1.5		Vcc	V
Analog reference voltage		A_{GND}	Vss		Vss	
Analog input voltage range		V_{AIN}	Vss		Vcc	
Anlog current for analog reference voltage		I_{REF}		0.5	1.5	mA
4 ≦ fc ≦ 16 MHz	Low change mode	Total error (Quantize error of ± 0.5 LSB not included)		± 1.5	± 4.0	LSB
	High change mode			± 3.0	± 6.0	
16 < fc ≦ 20 MHz	Low change mode			± 1.5	± 4.0	
	High change mode			± 4.0	± 8.0	

4.5 Serial Channel Timing – I/O Interface Mode

(1) SCLK Input Mode Vcc = 5 V ± 10%, TA = − 40 to 85℃ (4 to 16 MHz) TA = − 20 to 70℃ (4 to 20 MHz)

Parameter	Symbol	Variable		16 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK cycle	t_{SCY}	16X		1		0.8		μs
Output Data → Rising edge of SCLK	t_{OSS}	t_{SCY}/2 − 5X − 50		137		100		ns
SCLK rising edge→ Output Data hold	t_{OHS}	5X − 100		212		150		ns
SCLK rising edge→ Input Data hold	t_{HSR}	0		0		0		ns
SCLK rising edge→ effective data input	t_{SRD}		t_{SCY} − 5X − 100		587		450	ns

(2) SCLK Output Mode Vcc = 5 V ± 10%, TA = − 40 to 85℃ (4 to 16 MHz) TA = − 20 to 70℃ (4 to 20 MHz)

Parameter	Symbol	Variable		16 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK cycle (programmable)	t_{SCY}	16X	8192X	1	512	0.8	409.6	μs
Output Data → SCLK rising edge	t_{OSS}	t_{SCY} − 2X − 150		725		550		ns
SCLK rising edge→ Output Data hold	t_{OHS}	2X − 80		45		20		ns
SCLK rising edge→ Input Data hold	t_{HSR}	0		0		0		ns
SCLK rising edge→ effective data input	t_{SRD}		t_{SCY} − 2X − 150		725		550	ns

4.6 Timer/Counter Input Clock (TI0, TI4, TI5, TI6, TI7)

Vcc = 5 V ± 10%, TA = − 40 to 85℃ (4 to 16 MHz) TA = − 20 to 70℃ (4 to 20 MHz)

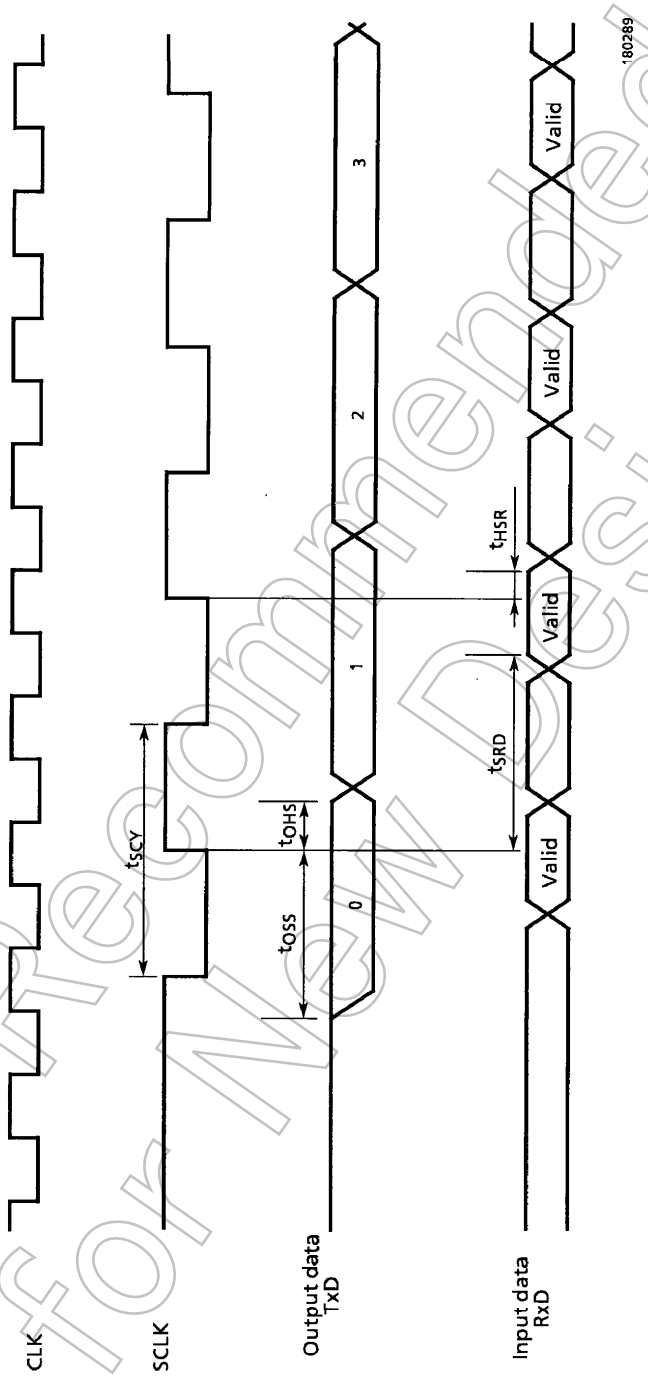
Parameter	Symbol	Variable		16 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
Clock Cycle	t_{VCK}	8X + 100		600		500		ns
Low level clock Pulse width	t_{VCKL}	4X + 40		290		240		ns
High level clock Pulse width	t_{VCKH}	4X + 40		290		240		ns

4.7 Interrupt Operation

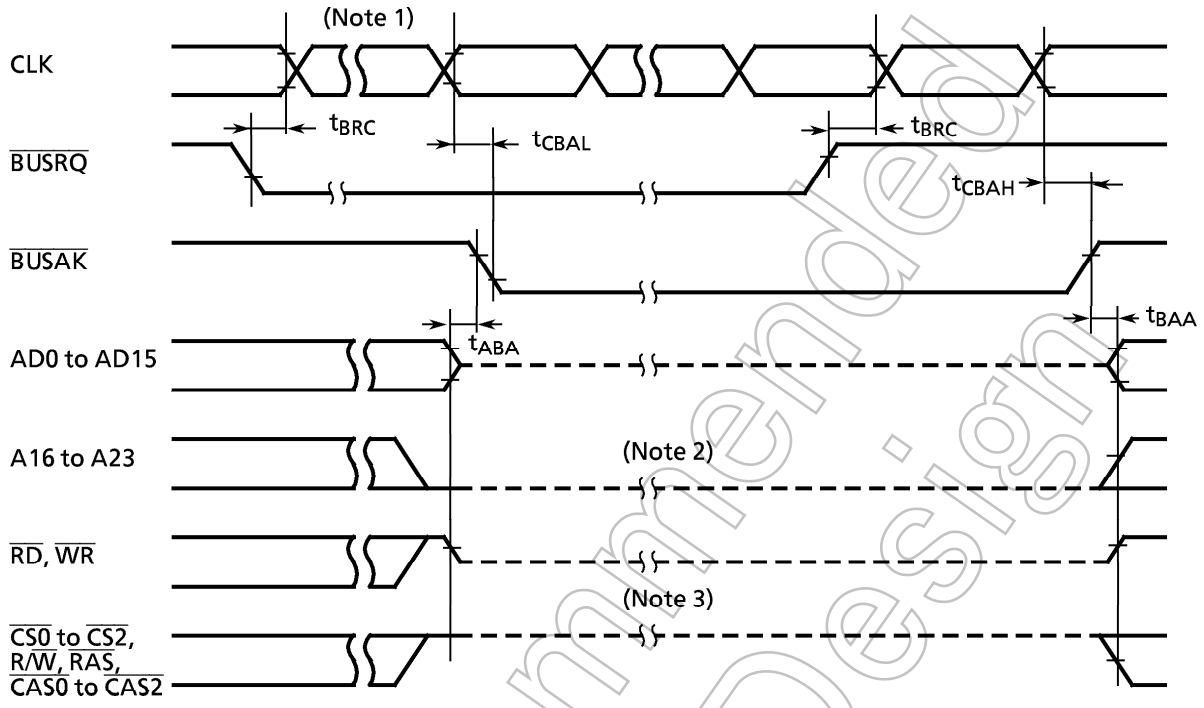
Vcc = 5 V ± 10%, TA = − 40 to 85℃ (4 to 16 MHz) TA = − 20 to 70℃ (4 to 20 MHz)

Parameter	Symbol	Variable		16 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{NMI}$, INT0 Low level Pulse width	t_{INTAL}	4X		250		200		ns
$\overline{NMI}$, INT0 High level Pulse width	t_{INTAH}	4X		250		200		ns
INT4 to INT7 Low level Pulse width	t_{INTBL}	8X + 100		600		500		ns
INT4 to INT7 High level Pulse width	t_{INTBH}	8X + 100		600		500		ns

4.8 Timing Chart for I/O Interface Mode



4.9 Timing Chart for Bus Request ($\overline{BUSRQ}$) / Bus Acknowledge ($\overline{BUSAK}$)



Parameter	Symbol	Variable		16 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{BUSRQ}$ set-up time for CLK	t_{BRC}	120		120		120		ns
CLK→ $\overline{BUSAK}$ falling edge	t_{CBAL}	2.0x + 120			245		220	ns
CLK→ $\overline{BUSAK}$ rising edge	t_{CBAH}	0.5x + 40			71		65	ns
Output Buffer is off to $\overline{BUSAK}$ ↓	t_{ABA}	0	80	0	80	0	80	ns
$\overline{BUSAK}$ ↑ to Output Buffer is on.	t_{BAA}	0	80	0	80	0	80	ns

Note 1: The Bus will be released after the $\overline{WAIT}$ request is inactive, when the $\overline{BUSRQ}$ is set to "0" during "Wait" cycle.

Note 2: The internal programmable pull-down resistor is added.

Note 3: The internal programmable pull-up resistor is added.
But the $\overline{CS2}$/$\overline{CAS2}$ pin does not have the internal programmable pull-up resistor. And in the condition of bus release, this pin is added the internal pull-up resistor.