

**TOSHIBA**

TOSHIBA Original CMOS 16-Bit Microcontroller

**TLCS-900 Series**

**TMP96CM40FG**

Not Recommended  
for New Design

**TOSHIBA CORPORATION**

Semiconductor Company

# Preface

Thank you very much for making use of Toshiba microcomputer LSIs.  
Before use this LSI, refer the section, "Points of Note and Restrictions".  
Especially, take care below cautions.

## **\*\*CAUTION\*\***

### How to release the HALT mode

Usually, interrupts can release all halts status. However, the interrupts = ( $\overline{NMI}$ , INT0), which can release the HALT mode may not be able to do so if they are input during the period CPU is shifting to the HALT mode (for about 3 clocks of X1) with IDLE or STOP mode. (In this case, an interrupt request is kept on hold internally.)

If another interrupt is generated after it has shifted to HALT mode completely, halt status can be released without difficulty. The priority of this interrupt is compare with that of the interrupt kept on hold internally, and the interrupt with higher priority is handled first followed by the other interrupt.

## Document Change Notification

The purpose of this notification is to inform customers about the launch of the Pb-free version of the device. The introduction of a Pb-free replacement affects the datasheet. Please understand that this notification is intended as a substitute for a revision of the datasheet.

Changes to the datasheet may include the following, though not all of them may apply to this particular device.

1. Part number

Example: TMPxxxxxF → TMPxxxxxFG

All references to the previous part number were left unchanged in body text. The new part number is indicated on the prelims pages (cover page and this notification).

2. Package code and package dimensions

Example: LQFP100-P-1414-0.50C → LQFP100-P-1414-0.50F

All references to the previous package code and package dimensions were left unchanged in body text. The new ones are indicated on the prelims pages.

3. Addition of notes on lead solderability

Now that the device is Pb-free, notes on lead solderability have been added.

4. RESTRICTIONS ON PRODUCT USE

The previous (obsolete) provision might be left unchanged on page 1 of body text. A new replacement is included on the next page.

5. Publication date of the datasheet

The publication date at the lower right corner of the prelims pages applies to the new device.

## 1. Part number

Previous Part Number (in Body Text)	New Part Number
TMP96CM40F	TMP96CM40FG

## 2. Package code and dimensions

Previous Package Code (in Body Text)	New Package Code
QFP80-P-1420-0.80B	QFP80-P-1420-0.80B

\*: For the dimensions of the new package, see the attached Package Dimensions diagram.

## 3. Addition of notes on lead solderability

The following solderability test is conducted on the new device.

Solderability of lead free products

Test Parameter	Test Condition	Note
Solderability	Use of Sn-37Pb solder Bath Solder bath temperature = 230°C, Dipping time = 5 seconds The number of times = one, Use of R-type flux	Pass: Solderability rate until forming ≥ 95%
	Use of Sn-3.0Ag-0.5Cu solder bath Solder bath temperature = 245°C, Dipping time = 5 seconds The number of times = one, Use of R-type flux (use of lead free)	

## 4. RESTRICTIONS ON PRODUCT USE

The following replaces the “RESTRICTIONS ON PRODUCT USE” on page 1 of body text.

**RESTRICTIONS ON PRODUCT USE**

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- For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance/Handling Precautions.

## 5. Publication date of the datasheet

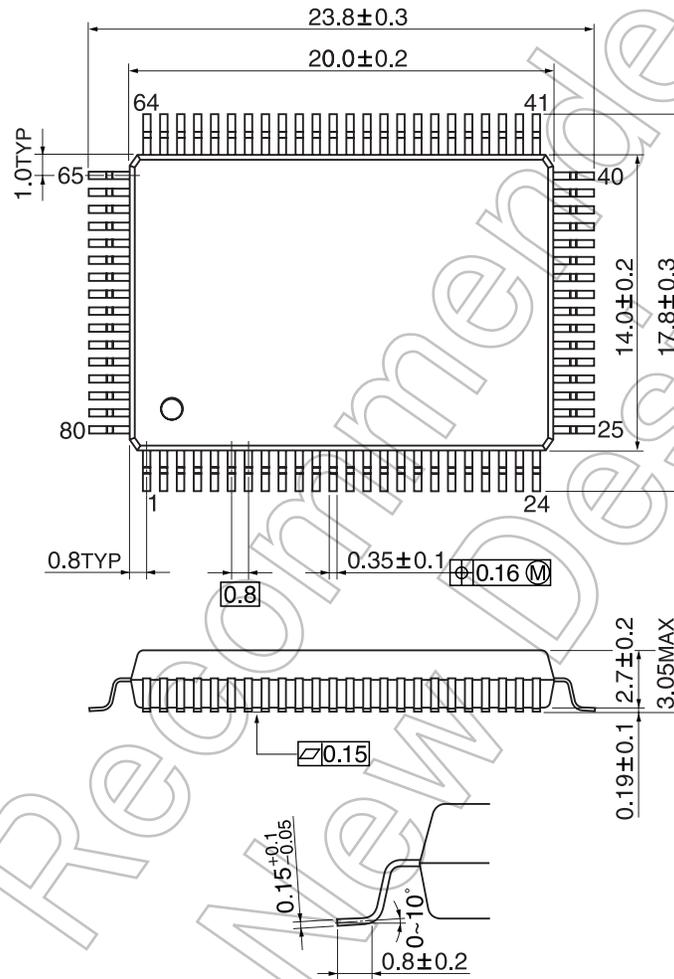
The publication date of this datasheet is printed at the lower right corner of this notification.

(Annex)

Package Dimensions

QFP80-P-1420-0.80B

Unit: mm



Not Recommended for New Design

## CMOS 16-bit Microcontrollers

## TMP96CM40F

## 1. Outline and Device Characteristics

TMP96CM40F is high-speed advanced 16-bit microcontrollers developed for controlling medium to large-scale equipment. The TMP96C141BF does not have a ROM, the TMP96CM40F has a built-in ROM of 32K-byte, and the TMP96PM40 has a built-in OTP of 32K-byte.

TMP96CM40F is housed in an 80-pin flat package.

Device characteristics are as follows:

- (1) Original 16-bit CPU
  - TLCS-90 instruction mnemonic upward compatible.
  - 16M-byte linear address space
  - General-purpose registers and register bank system
  - 16-bit multiplication / division and bit transfer/arithmetic instructions
  - High-speed micro DMA : 4 channels (1.6  $\mu$ s/2 bytes @ 20 MHz)
- (2) Minimum instruction execution time : 200 ns @ 20 MHz
- (3) Internal RAM : 1 Kbyte  
Internal ROM : 32 Kbyte
- (4) External memory expansion
  - Can be expanded up to 16 Mbytes (for both programs and data).
  - Can mix 8- and 16-bit external data buses.
- (5) 8-bit timers : 2 channels
- (6) 8-bit PWM timers : 2 channels
- (7) 16-bit timers : 2 channels
- (8) Pattern generators : 4 bits, 2 channels
- (9) Serial interface : 2 channels
- (10) 10-bit A/D converter : 4 channels
- (11) Watchdog timer
- (12) Chip select/wait controller : 3 blocks
- (13) Interrupt functions
  - 3 CPU interrupts (SWI instruction, privileged violation, and Illegal instruction)
  - 14 internal interrupts
  - 6 external interrupts } 7-level priority can be set.
- (14) I/O ports : 65 pins
- (15) Standby function : 3 halt modes (RUN, IDLE, STOP)

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- For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance / Handling Precautions.
- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.  
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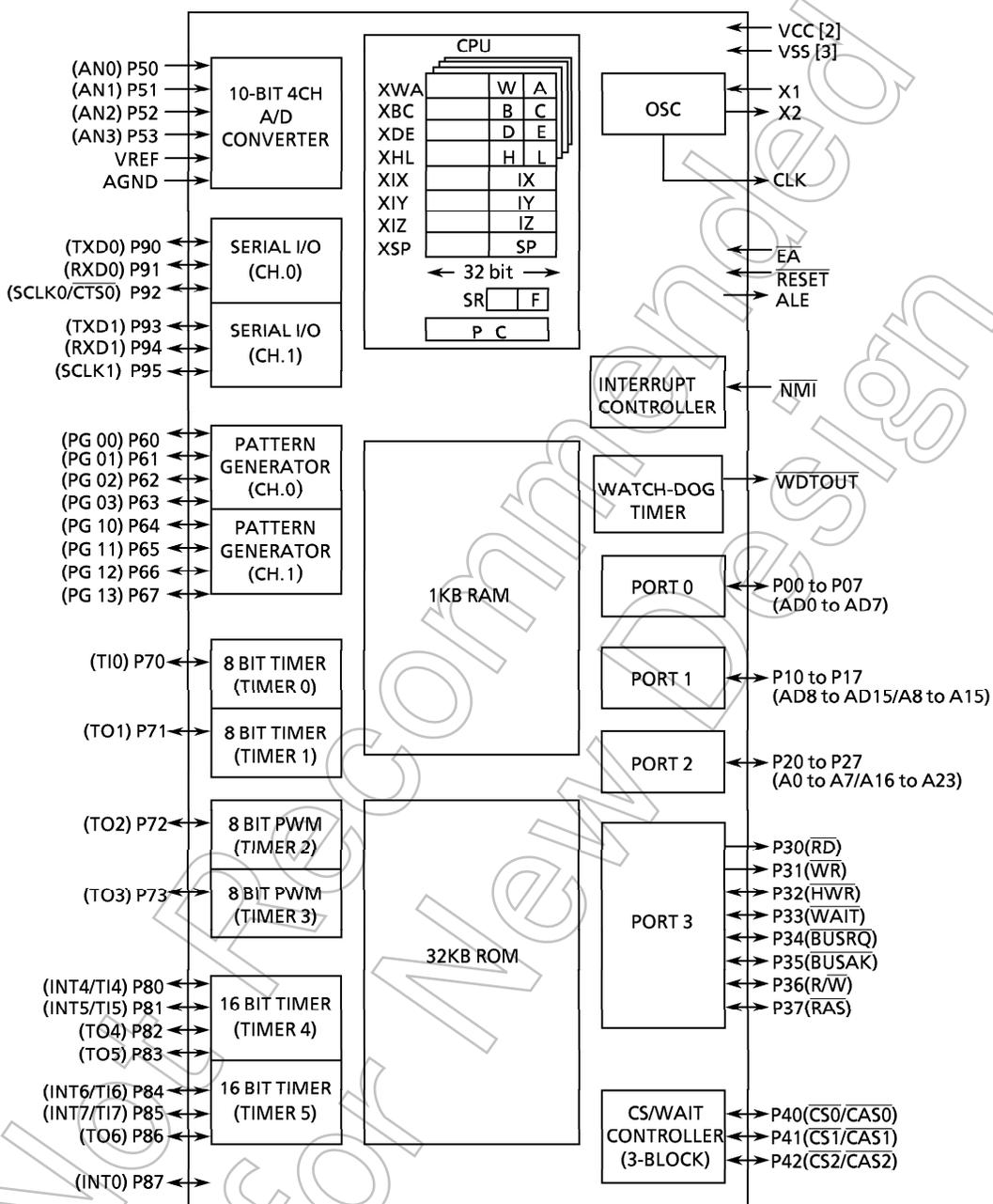


Figure1 TMP96CM40 Block Diagram

## 2. Pin Assignment and Functions

The assignment of input / output pins for TMP96CM40, their name and outline functions are described below.

### 2.1 Pin Assignment

Figure 2.1 shows pin assignment of TMP96CM40F.

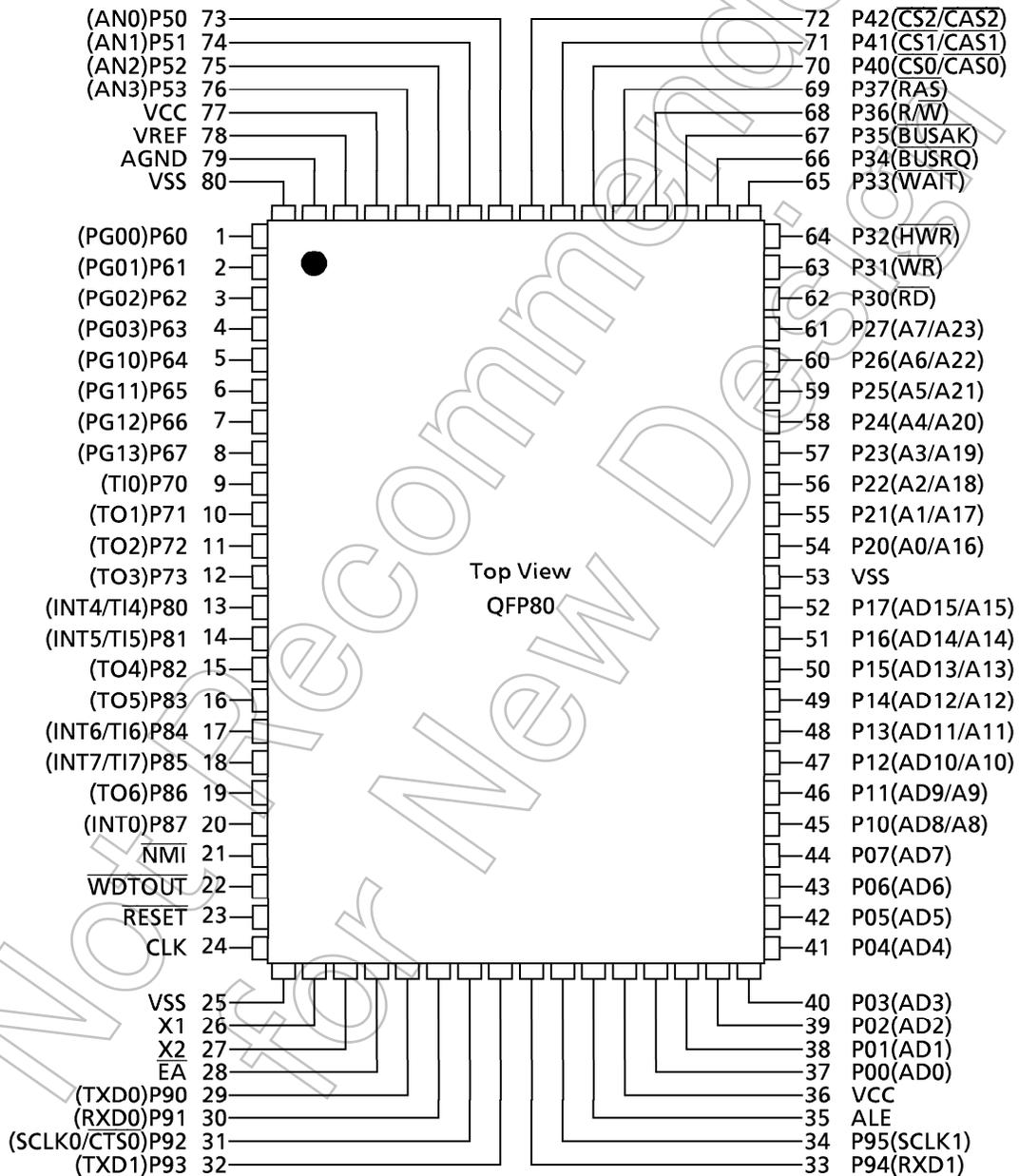


Figure 2.1 Pin Assignment (80-pin QFP)

## 2.2 Pin Names and Functions

The names of input/output pins and their functions are described below.

Table 2.2 Pin Names and Functions.

Pin name	Number of pins	I/O	Functions
P00 to P07 AD0 to AD7	8	I/O Tri-state	Port 0: I/O port that allows I/O to be selected on a bit basis Address/data (lower): 0 to 7 for address/data bus
P10 to P17 AD8 to AD15 A8 to A15	8	I/O Tri-state Output	Port 1: I/O port that allows I/O to be selected on a bit basis Address data (upper): 8 to 15 for address/data bus Address: 8 to 15 for address bus
P20 to P27 A0 to A7 A16 to A23	8	I/O Output Output	Port 2: I/O port that allows selection of I/O on a bit basis (with pull-down resistor) Address: 0 to 7 for address bus Address: 16 to 23 for address bus
P30 $\overline{RD}$	1	Output Output	Port 30: Output port Read: Strobe signal for reading external memory
P31 $\overline{WR}$	1	Output Output	Port 31: Output port Write: Strobe signal for writing data on pins AD0 to 7
P32 $\overline{HWR}$	1	I/O Output	Port 32: I/O port (with pull-up resistor) High write: Strobe signal for writing data on pins AD8 to 15
P33 $\overline{WAIT}$	1	I/O Input	Port 33: I/O port (with pull-up resistor) Wait: Pin used to request CPU bus wait
P34 $\overline{BUSRQ}$	1	I/O Input	Port 34: I/O port (with pull-up resistor) Bus request: Signal used to request high impedance for AD0 to 15, A0 to 23, $\overline{RD}$ , $\overline{WR}$ , $\overline{HWR}$ , $\overline{R/W}$ , $\overline{RAS}$ , $\overline{CS0}$ , $\overline{CS1}$ , and $\overline{CS2}$ pins. (For external DMAC)
P35 $\overline{BUSAK}$	1	I/O Output	Port 35: I/O port (with pull-up resistor) Bus acknowledge: Signal indicating that AD0 to 15, A0 to 23, $\overline{RD}$ , $\overline{WR}$ , $\overline{HWR}$ , $\overline{R/W}$ , $\overline{RAS}$ , $\overline{CS0}$ , $\overline{CS1}$ , and $\overline{CS2}$ pins are at high impedance after receiving $\overline{BUSRQ}$ . (For external DMAC)
P36 $\overline{R/W}$	1	I/O Output	Port 36: I/O port (with pull-up resistor) Read/write: 1 represents read or dummy cycle; 0, write cycle.
P37 $\overline{RAS}$	1	I/O Output	Port 37: I/O port (with pull-up resistor) Row address strobe: Outputs $\overline{RAS}$ strobe for DRAM.
P40 $\overline{CS0}$ $\overline{CAS0}$	1	I/O Output Output	Port 40: I/O port (with pull-up resistor) Chip select 0: Outputs 0 when address is within specified address area. Column address strobe 0: Outputs $\overline{CAS0}$ strobe for DRAM when address is within specified address area.

Note : With the external DMA controller, this device's built-in memory or built-in I/O cannot be accessed using the  $\overline{BUSRQ}$  and  $\overline{BUSAK}$  pins.

Pin name	Number of pins	I/O	Functions
P41 CS1 CAS1	1	I/O Output Output	Port 41: I/O port (with pull-up resistor) Chip select 1: Outputs 0 if address is within specified address area. Column address strobe 1: Outputs CAS strobe for DRAM if address is within specified address area.
P42 CS2 CAS2	1	I/O Output Output	Port 42: I/O port (with pull-down resistor) (Note) Chip select 2: Outputs 0 if address is within specified address area. Column address strobe 2: Outputs CAS strobe for DRAM if address is within specified address area.
P50 to P53 AN0 to AN3	4	Input Input	Port 5: Input port Analog input: Input to A/D converter
VREF	1	Input	Pin for reference voltage input to A/D converter
AGND	1	Input	Ground pin for A/D converter
P60 to P63 PG00 to PG03	4	I/O Output	Ports 60 to 63: I/O ports that allow selection of I/O on a bit basis (with pull-up resistor) Pattern generator ports: 00 to 03
P64 to P67 PG10 to PG13	4	I/O Output	Ports 64 to 67: I/O ports that allow selection of I/O on a bit basis (with pull-up resistor) Pattern generator ports: 10 to 13
P70 TI0	1	I/O Input	Port 70: I/O port (with pull-up resistor) Timer input 0: Timer 0 input
P71 TO1	1	I/O Output	Port 71: I/O port (with pull-up resistor) Timer output 1: Timer 0 or 1 output
P72 TO2	1	I/O Output	Port 72: I/O port (with pull-up resistor) PWM output 2: 8-bit PWM timer 2 output
P73 TO3	1	I/O Output	Port 73: I/O port (with pull-up resistor) PWM output 3: 8-bit PWM timer 3 output
P80 TI4 INT4	1	I/O Input Input	Port 80: I/O port (with pull-up resistor) Timer input 4: Timer 4 count/capture trigger signal input Interrupt request pin 4: Interrupt request pin with programmable rising/falling edge
P81 TI5 INT5	1	I/O Input Input	Port 81: I/O port (with pull-up resistor) Timer input 5: Timer 4 count/capture trigger signal input Interrupt request pin 5: Interrupt request pin with rising edge
P82 TO4	1	I/O Output	Port 82: I/O port (with pull-up resistor) Timer output 4: Timer 4 output pin
P83 TO5	1	I/O Output	Port 83: I/O port (with pull-up resistor) Timer output 5: Timer 4 output pin

Note : Case of the settable  $\overline{CS2}$  or  $\overline{CAS2}$  ; when TMP96CM40F is bus release, this pin is not added the internal pull-down resistor but is added the internal pull-up resistor.

Pin name	Number of pins	I/O	Functions
P84 TI6 INT6	1	I/O Input Input	Port 84: I/O port (with pull-up resistor) Timer input 6: Timer 5 count/capture trigger signal input Interrupt request pin 6: Interrupt request pin with programmable rising/falling edge
P85 TI7 INT7	1	I/O Input Input	Port 85: I/O port (with pull-up resistor) Timer input 7: Timer 5 count/capture trigger signal input Interrupt request pin 7: Interrupt request pin with rising edge
P86 TO6	1	I/O Output	Port 86: I/O port (with pull-up resistor) Timer output 6: Timer 5 output pin
P87 INT0	1	I/O Input	Port 87: I/O port (with pull-up resistor) Interrupt request pin 0: Interrupt request pin with programmable level/rising edge
P90 TXD0	1	I/O Output	Port 90: I/O port (with pull-up resistor) Serial send data 0
P91 RXD0	1	I/O Input	Port 91: I/O port (with pull-up resistor) Serial receive data 0
P92 $\overline{\text{CTS0}}$ SCLK0	1	I/O Input I/O	Port 92: I/O port (with pull-up resistor) Serial data send enable 0 (Clear to Send) Serial clock I/O 0
P93 TXD1	1	I/O Output	Port 93: I/O port (with pull-up resistor) Serial send data 1
P94 RXD1	1	I/O Input	Port 94: I/O port (with pull-up resistor) Serial receive data 1
P95 SCLK1	1	I/O I/O	Port 95: I/O port (with pull-up resistor) Serial clock I/O 1
$\overline{\text{WDTOUT}}$	1	Output	Watchdog timer output pin
$\overline{\text{NMI}}$	1	Input	Non-maskable interrupt request pin: Interrupt request pin with falling edge. Can also be operated at rising edge by program.
CLK	1	Output	Clock output: Outputs $\lceil X1 \div 4 \rceil$ clock. Pulled-up during reset.
$\overline{\text{EA}}$	1	Input	External access: 0 should be inputted with TMP96C141B. 1, with TMP96CM40 / TMP96PM40.
ALE	1	Output	Address latch enable
$\overline{\text{RESET}}$	1	Input	Reset: Initializes LSI. (With pull-up resistor)
X1/X2	2	I/O	Oscillator connecting pin
VCC	2		Power supply pin (+ 5 V) (All Vcc pins should be connected with the power supply pin.)
VSS	3		GND pin (0 V) (All Vss pins should be connected with GND (0 V).)

Note : Pull-up/pull-down resistor can be released from the pin by software (except the  $\overline{\text{RESET}}$  pin).

### 3. Operation

This section describes the functions and basic operations of TMP96M40 device. The function of CPU and internal I/O devices are the same function as TMP96C141B.

Check the 「7. Care Points and Restriction of TMP96C141B」 because of the Care described. Regarding the function of TMP96CM40 (not described), see the part of TMP96C141B.

TMP96C141B/TMP96CM40/TMP96PM40 have much the same function but they are different from following points.

Parameter	TMP96C141B	TMP96CM40	TMP96PM40
Internal ROM	Not exist	Mask ROM32 Kbyte	PROM32 Kbyte
P00 to P07, AD0 to AD7	Only AD0 to AD7	After reset P00 to P07	
P10 to P17, AD8 to AD15, A8 to A15	Only AD8 to AD15	After reset P10 to P17	
P30, $\overline{RD}$	Only $\overline{RD}$	After reset P30	
P31, $\overline{WR}$	Only $\overline{WR}$	After reset P31	
Pin state at the bus release	TMP96C141B see Table 3.5 (1)	TMP96CM40 see Table 3.3 (1)	

#### 3.1 CPU

TMP96CM40 device has a built-in high-performance 16-bit CPU (900-CPU). (For CPU operation, see TLCS-900 CPU in the previous section.)

#### 3.2 Memory Map

TMP96CM40 has two register modes. One is a minimum mode; in this mode, the area of program memory is 64 Kbytes maximum. The other is a maximum mode; in this mode, The area of program memory is 16 Mbytes maximum.

Both minimum and maximum modes are the data memory area of 16 Mbytes maximum.

That is, the program memory can locate 0H to FFFFH in minimum mode and can locate 0H to FFFFFFFH in maximum mode.

##### (1) Internal ROM

TMP96CM40 has the ROM of 32 Kbytes. This ROM is located to 8000H to FFFFH. After the RESET operation, instruction execution starts from address 8000H.

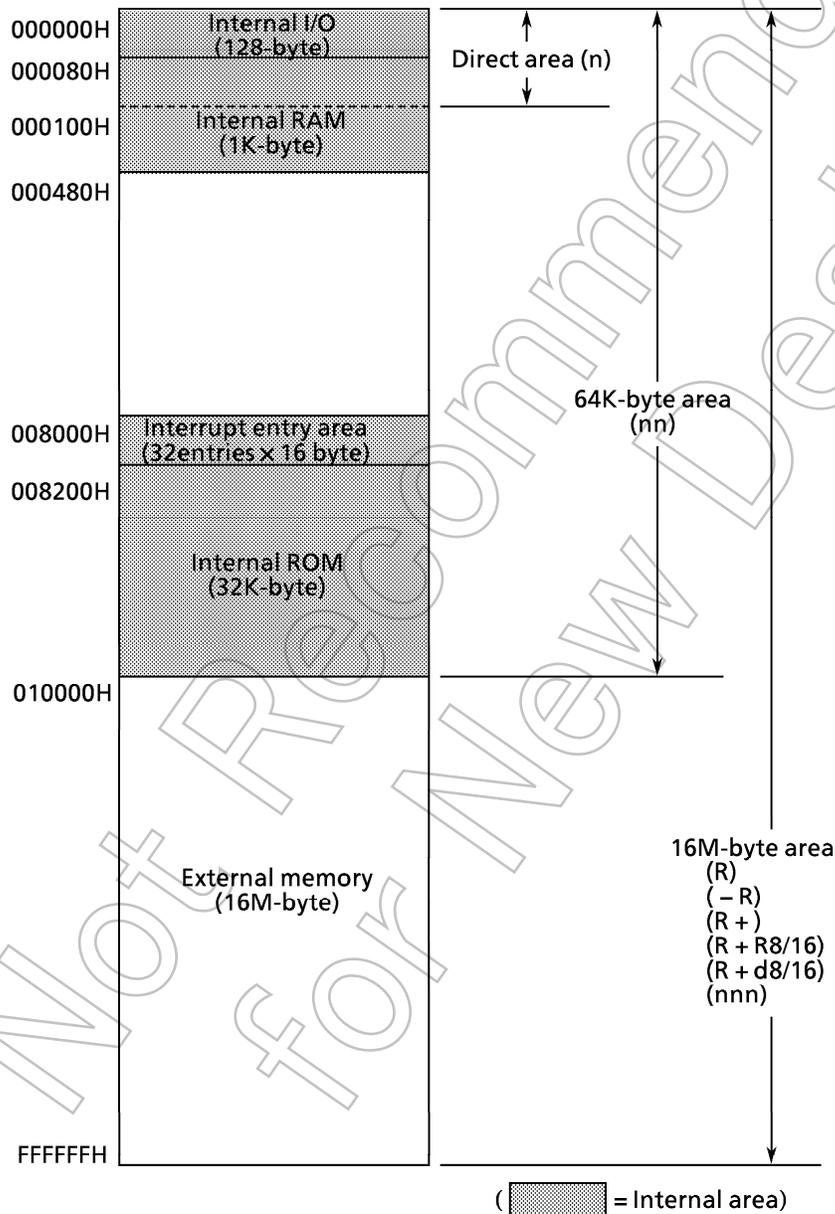
A part of the internal ROM area (8000H to 81FFH) is interrupt entry area.

(2) Internal RAM

TMP96CM40 has the RAM of 1 Kbytes. This RAM is located to 80H to 47FH. The CPU can access the part of RAM (80H to FFH, 128 bytes) with using the short instruction code of direct addressing mode.

Memory Map

Figure 3.1 is a memory map of the TMP96CM40.



Note: The start address after reset is 8000H. Resetting sets the stack pointer (XSP) on the system mode side to 100H.

Figure3.1 Memory map

## 3.3 Functions of Ports

The TMP96CM40/TMP96PM40 has 65 bits for I/O ports.

These port pins have I/O functions for the built-in CPU and internal I/Os as well as general-purpose I/O port functions. Table 3.3 lists the function of each port pin.

Table 3.3 Functions of Ports

(R: ↑ = With programmable pull-up resistor  
↓ = With programmable pull-down)

Port name	Pin name	Number of pins	Direction	R	Direction setting unit	Pin name for built-in function
Port0	P00 to P07	8	I/O	–	Bit	AD0 to AD7
Port1	P10 to P17	8	I/O	–	Bit	AD8 to AD15/A8 to A15
Port2	P20 to P27	8	I/O	↓	Bit	A0 to A7/A16 to A23
Port3	P30	1	Output	–	(Fixed)	$\overline{RD}$
	P31	1	Output	–	(Fixed)	$\overline{WR}$
	P32	1	I/O	↑	Bit	$\overline{HWR}$
	P33	1	I/O	↑	Bit	$\overline{WAIT}$
	P34	1	I/O	↑	Bit	$\overline{BUSRQ}$
	P35	1	I/O	↑	Bit	$\overline{BUSAK}$
	P36	1	I/O	↑	Bit	$\overline{R/W}$
	P37	1	I/O	↑	Bit	$\overline{RAS}$
Port4	P40	1	I/O	↑	Bit	$\overline{CS0} / \overline{CAS0}$
	P41	1	I/O	↑	Bit	$\overline{CS1} / \overline{CAS1}$
	P42	1	I/O	↓	Bit	$\overline{CS2} / \overline{CAS2}$
Port5	P50 to P53	4	Input	–	(Fixed)	AN0 to AN3
Port6	P60 to P67	8	I/O	↑	Bit	PG00 to PG03, PG10 to PG13
Port7	P70	1	I/O	↑	Bit	TI0
	P71	1	I/O	↑	Bit	TO1
	P72	1	I/O	↑	Bit	TO2
	P73	1	I/O	↑	Bit	TO3
Port8	P80	1	I/O	↑	Bit	TI4/INT4
	P81	1	I/O	↑	Bit	TI5/INT5
	P82	1	I/O	↑	Bit	TO4
	P83	1	I/O	↑	Bit	TO5
	P84	1	I/O	↑	Bit	TI6/INT6
	P85	1	I/O	↑	Bit	TI7/INT7
	P86	1	I/O	↑	Bit	TO6
	P87	1	I/O	↑	Bit	INT0
Port9	P90	1	I/O	↑	Bit	TXD0
	P91	1	I/O	↑	Bit	RXD0
	P92	1	I/O	↑	Bit	$\overline{CTS0} / \overline{SCLK0}$
	P93	1	I/O	↑	Bit	TXD1
	P94	1	I/O	↑	Bit	RXD1
	P95	1	I/O	↑	Bit	SCLK1

## I/O port Setting

X : Don't care

Port	Pin Name	Port (I/O) or FUnction	I/O Register		
			Pn	PnCR	PnFC
Port 0	P0 (0 : 7)	Input Port	x	0	-
		Output Port	x	1	
		AD (0 : 7) Bus	x	x	
Port 1	P1 (0 : 7)	Input Port	x	0	0
		Output Port	x	1	0
		AD (8 : 15) Bus	x	0	1
		A (8 : 15) Output	x	1	0
Port 2	P2 (0 : 7)	Input Port (No Pull-down)	1	0	0
		Input Port (With Pull-down)	0	0	0
		Output Port	x	1	0
		A (0 : 7) Output	1	0	1
		A (16 : 23) Output	1	1	0
Port 3	P30	Output Port	x	-	0
		$\overline{RD}$ Output (at external access only)	1	-	1
		$\overline{RD}$ Output (always)	0	-	1
	P31	Output Port	x	-	0
		$\overline{WR}$ Output (at external access only)	x	-	1
	P3 (2 : 7)	Input Port (No Pull-up)	0	0	0
		Input Port (With Pull-up)	1	0	0
		Output Port	x	1	0
	P32	HWR Output	x	1	1
	P33	WAIT Input (No Pull-up)	0	0	-
		WAIT Input (With Pull-up)	1	0	
	P34	$\overline{BUSRQ}$ Input (No Pull-up)	0	0	1
		$\overline{BUSRQ}$ Input (With Pull-up)	1	0	1
	P35	$\overline{BUSAK}$ Output	x	1	1
	P36	R/W Output	x	1	1
P37	$\overline{RAS}$ Output	x	1	1	
Port 4	P4 (0 : 1)	Input Port (No Pull-up)	0	0	0
		Input Port (With Pull-up)	1	0	0
		Output Port	x	1	0
	P42	Input Port (No Pull-down)	1	0	0
		Input Port (With Pull-down)	0	0	0
		Output Port	x	1	0
	P40	$\overline{CS0}$ Output (Note 1)	x	1	1
	P41	$\overline{CS1}$ Output (Note 1)	x	1	1
	P42	$\overline{CS2}$ Output (Note 1)	x	1	1
	Port 5	P5 (0 : 3)	Input Port	x	-
AN (0 : 3) Input (Note 2)			x		
Port 6	P6 (0 : 7)	Input Port (No Pull-up)	0	0	0
		Input Port (With Pull-up)	1	0	0
		Output Port	x	1	0
		PGn Output	x	1	1

Note 1: The function of P40 to P42 ( $\overline{CS0}$  to  $\overline{CS2}$ ,  $\overline{CAS0}$  to  $\overline{CAS2}$ ) is selected using CS/WAIT control register BnCS<BnCAS>.

Note 2: Select the input channels for the A/D converter in ADMOD2<ADChn>.

Port	Pin Name	Port (I/O) or Function	I/O Register		
			Pn	PnCR	PnFC
Port 7	P7 (0 : 3)	Input Port (No Pull-up)	0	0	0
		Input Port (With Pull-up)	1	0	0
		Output Port	x	1	0
	P70	TI0 Input (No Pull-up)	0	0	-
		TI0 Input (With Pull-up)	1	0	-
	P71	TO1Output	x	1	1
	P72	TO2Output	x	1	1
P73	TO3Output	x	1	1	
Port 8	P8 (0 : 7)	Input Port (No Pull-up)	0	0	0
		Input Port (With Pull-up)	1	0	0
		Output Port	x	1	0
	P80	TI4/INT4 Input (No Pull-up)	0	0	-
		TI4/INT4 Input (With Pull-up)	1	0	-
	P81	TI5/INT5 Input (No Pull-up)	0	0	-
		TI5/INT5 Input (With Pull-up)	1	0	-
	P84	TI6/INT6 Input (No Pull-up)	0	0	-
		TI6/INT6 Input (With Pull-up)	1	0	-
	P85	TI7/INT7 Input (No Pull-up)	0	0	-
		TI7/INT7 Input (With Pull-up)	1	0	-
	P82	TO4Output	x	1	1
	P83	TO5Output	x	1	1
	P86	TO6Output	x	1	1
	P87 (NOTE 3)	INT0 Input (No Pull-up)	0	0	-
INT0 Input (With Pull-up)		1	0	-	
Port 9	P9 (0 : 5)	Input Port (No Pull-up)	0	0	0
		Input Port (With Pull-up)	1	0	0
		Output Port	x	1	0
	P90	TXD0Output	x	1	1
	P93	TXD1Output	x	1	1
	P91	RXD0 Input (No Pull-up)	0	0	-
		RXD0 Input (With Pull-up)	1	0	-
	P94	RXD1 Input (No Pull-up)	0	0	-
		RXD1 Input (With Pull-up)	1	0	-
	P92	SCLK0Output	x	1	1
		CTS0/SCLK0 Input (No Pull-up)	0	0	0
		CTS0/SCLK0 Input (With Pull-up)	1	0	0
P95	SCLK1Output	x	1	1	
	SCLK1 Input (No Pull-up)	0	0	0	
	SCLK1 Input (With Pull-up)	1	0	0	

Note 3: When P87 pin is used as INT0 pin, set IIMC<IOIE> to "1" (Input enable) .

Resetting makes the port pins listed below function as general-purpose I/O ports.  
I/O pins programmable for input or output function as input ports.  
To set port pins for built-in functions, a program is required.

※ Note about the Bus Release and programmable pull-up / down I/O ports.

When the bus is released ( $\overline{\text{BUSAK}} = "0"$ ), the output buffer of AD0 to 15, A0 to 23, control signal ( $\overline{\text{RD}}$ ,  $\overline{\text{WR}}$ ,  $\overline{\text{HWR}}$ ,  $\text{R}/\overline{\text{W}}$ ,  $\overline{\text{RAS}}$ ,  $\overline{\text{CS0}} / \overline{\text{CAS0}}$  to  $\overline{\text{CS2}} / \overline{\text{CAS2}}$ ) is off and their state become high-impedance.

However, the output of built-in programmable pull up / down resistors are kept before the bus is released. These programmable pull up / down resistors can be selected ON/OFF by programmable when they are used as the input ports.

The case of they are used as the output ports, they can not be selected ON/OFF by programmable.

The following is the pin state when the bus is released ( $\overline{\text{BUSAK}} = "0"$ )

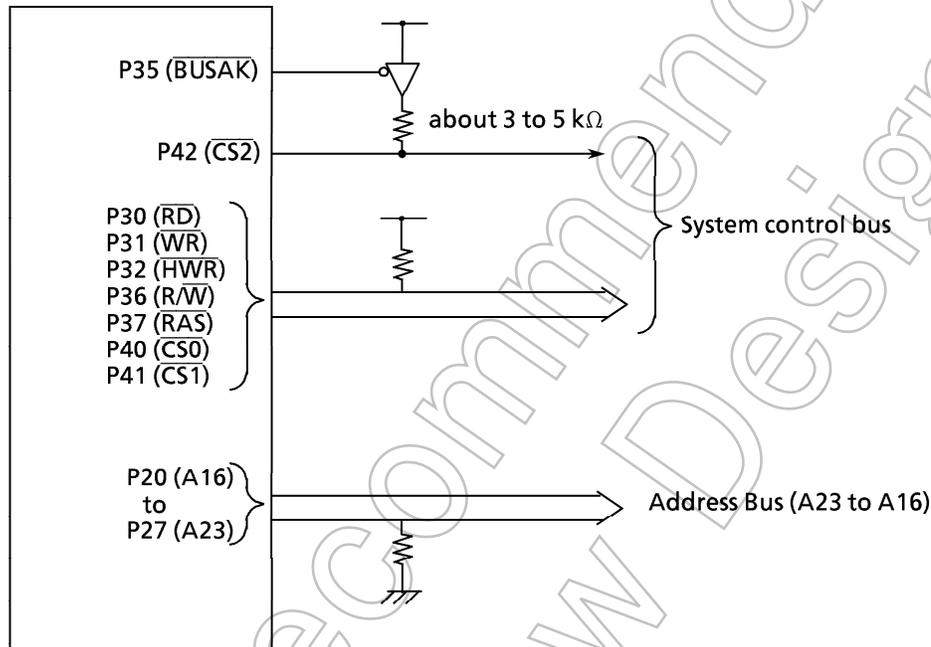
Table 3.3 (1) The condition of pins at the bus release ( $\overline{\text{BUSAK}} = "L"$ )

Pin Name	The Pin State (when the bus is released)	
	Used as the port	Used as the function
P00 to P07 (AD0 to AD7) P10 to P17 (AD8 to 15 / A8 to 15)	The state is not changed. (do not become to high-impedance (HZ).)	become high-impedance (HZ).
P30 ( $\overline{\text{RD}}$ ) P31 ( $\overline{\text{WR}}$ )	becomes high-impedance (HZ).	←
P32 ( $\overline{\text{HWR}}$ ) P37 ( $\overline{\text{RAS}}$ )	The output buffer is OFF. The programmable pull up resistor is ON the case of only the output latch is equal to "1".	The output buffer is OFF. The programmable pull up resistor is ON irrespective of the output latch.
P36 ( $\text{R}/\overline{\text{W}}$ ) P40 ( $\overline{\text{CS0}} / \overline{\text{CAS0}}$ ) P41 ( $\overline{\text{CS1}} / \overline{\text{CAS1}}$ )	↑	The output buffer is OFF. The programmable pull up resistor is undefined.
P42 ( $\overline{\text{CS2}} / \overline{\text{CAS2}}$ )	The output buffer is OFF. The programmable pull down resistor is ON the case of only the output latch is equal to "0".	The output buffer is OFF. The programmable pull down resistor is undefined.
P20 to P27 (A16 to 23)	The state is not changed. (do not become to high-impedance (HZ).)	The output buffer is OFF. The programmable pull down resistor is ON the case of only the output latch is equal to "0".

The following are the example of the interface circuit about above pins the case of the bus releasing function is used.

When the bus is released, both internal memory and internal I/O can not be accessed. But the internal I/O continues to operate.

So, the watch dog timer also continues to run. Therefore, be care about bus releasing time and set the detection time of WDT.



Example of the interface circuit (The case of using bus releasing function)

The above circuit is necessary to fix the signal level the case of the bus is released.

Resetting sets P30 ( $\overline{RD}$ ), P31 ( $\overline{WR}$ ) to output, P40 ( $\overline{CS0}$ ), P41 ( $\overline{CS1}$ ), P32 ( $\overline{HWR}$ ), P36 ( $\overline{R/W}$ ), P37 ( $\overline{RAS}$ ), and P35 ( $\overline{BUSAK}$ ) to input with pull up resistor, P42 ( $\overline{CS2}$ ) and P20 to 27 (A16 to 23) to input with pull down resistor.

The above circuit is necessary to fix the signal level after reset because of the external pull up resistor collisions with the internal pull down resistor.

The value of this external pull up resistor must be 3 to 5 k $\Omega$ . (the value of the internal pull down resistor is about 50 to 150 k $\Omega$ )

P20 to P27 (A16 to 23) also needs circuit like P42 ( $\overline{CS2}$ ) to fix the signal level.

But for the P20 to 27 (A16 to 23) which does not have means ("L" is active), add pull down directly like above circuit.

## 3.3.1 Port 0 (P00 to P07)

Port 0 is an 8-bit general-purpose I/O port. I/O can be set on a bit basis using the control register P0CR. Resetting resets all bits of P0CR to 0 and sets Port 0 to input mode.

In addition to functioning as a general-purpose I/O port, Port 0 also functions as an address data bus (AD0 to 7). To access external memory, Port 0 functions as an address data bus (AD0 to 7) and all bits of the control register P0CR are cleared to 0.

Don't write 16 bit data in this port for TMP96CM40/TMP96PM40. Execute NOP instruction just after execution of instructions to write data in this port (which include read-modify-write instructions).

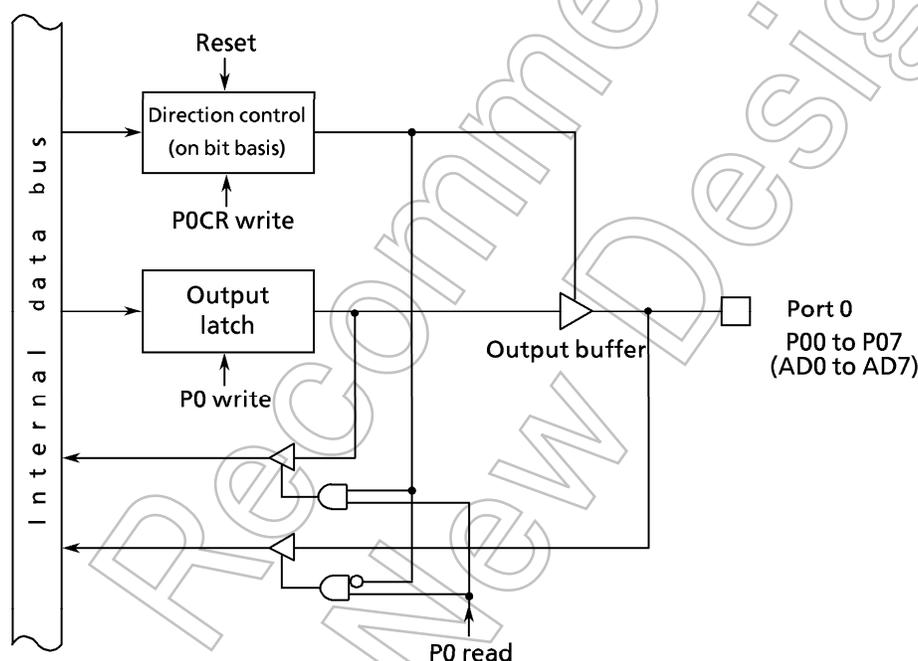


Figure 3.3 (1) Port 0

3.3.2 Port 1 (P10 to P17)

Port 1 is an 8-bit general-purpose I/O port. I/O can be set on a bit basis using control register P1CR and function register P1FC. Resetting resets all bits of output latch P1, control register P1CR, and function register P1FC to 0 and sets Port 1 to input mode.

In addition to functioning as a general-purpose I/O port, Port 1 also functions as an address data bus (AD8 to 15) or an address bus (A8 to 15).

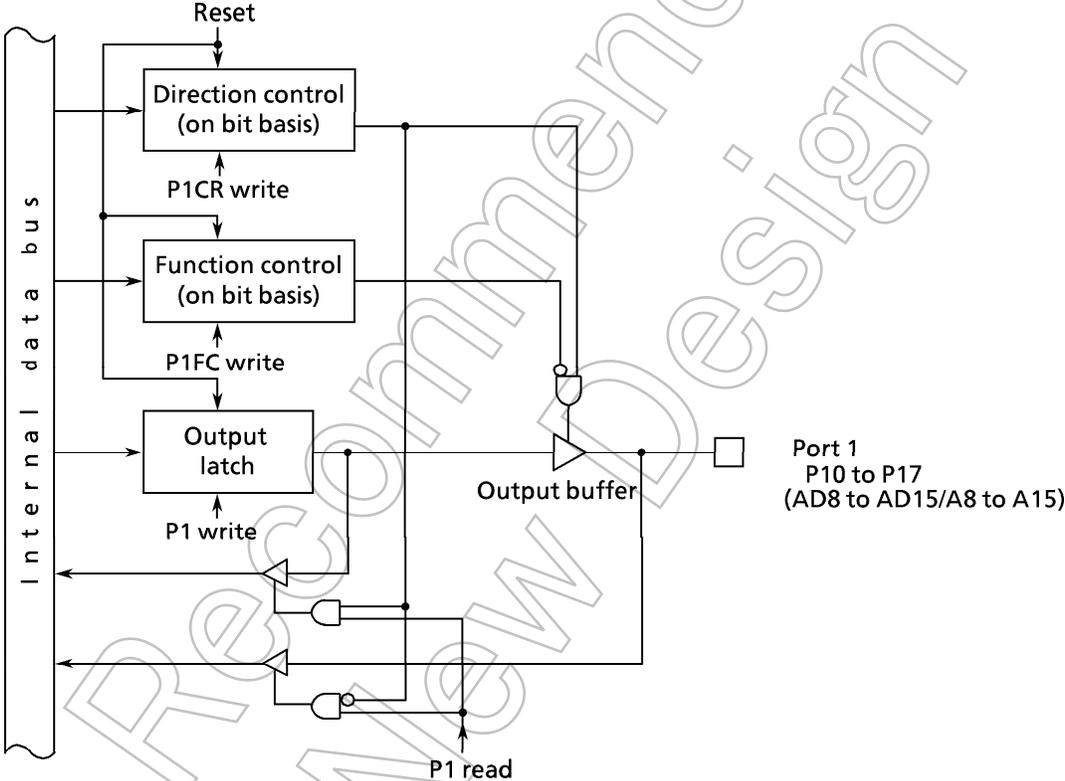
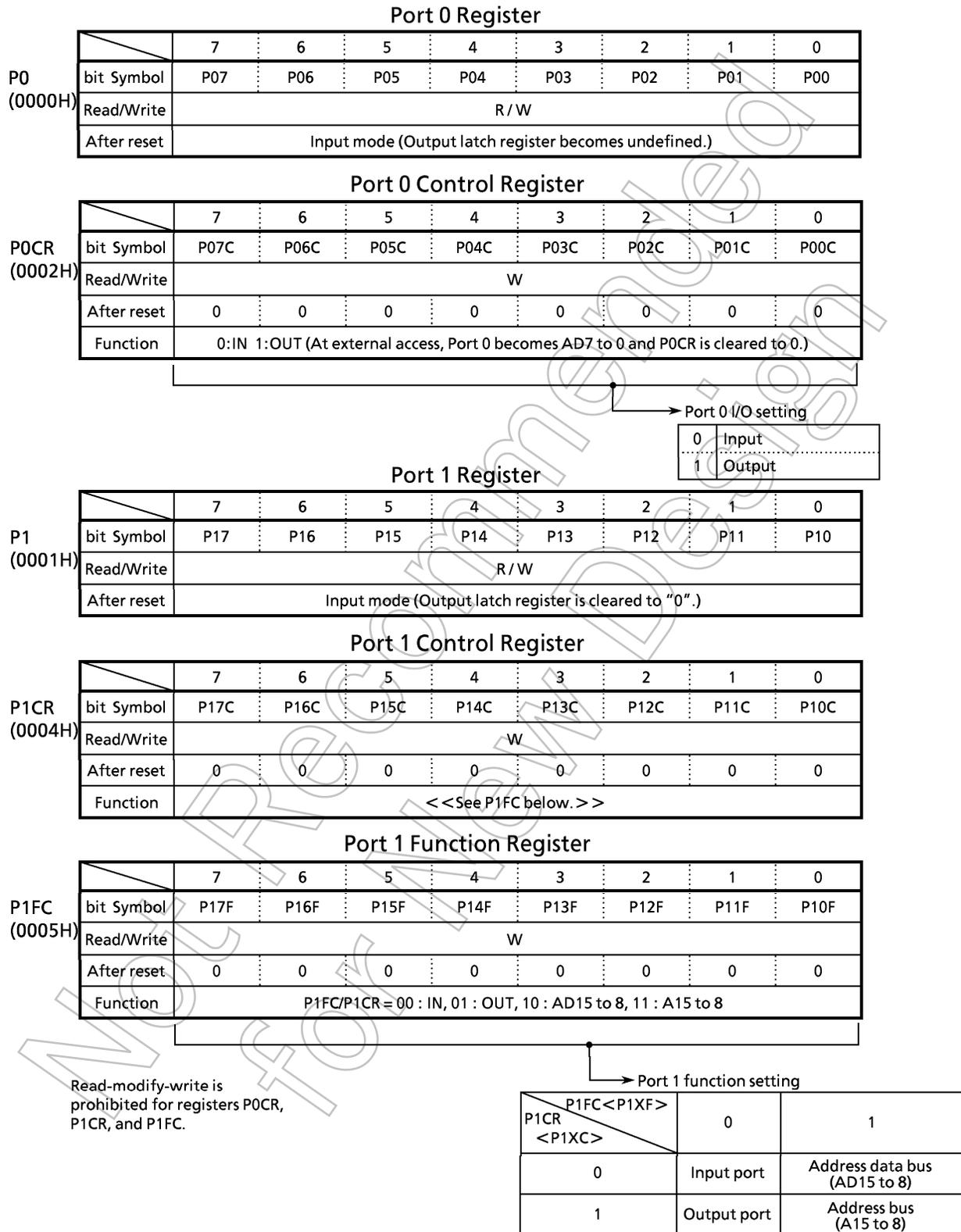


Figure 3.3 (2) Port 1

Not for Reference Design



Note: <P1XF> is bit X in register P1FC; <P1XC>, in register P1CR.

Figure 3.3 (3) Registers for Ports 0 and 1

3.3.3 Port 2 (P20 to P27)

Port 2 is an 8-bit general-purpose I/O port. I/O can be set on bit basis using the control register P2CR and function register P2FC. Resetting resets all bits of output latch P2, control register P2CR and function register P2FC to 0. It also sets Port 2 to input mode and connects a pull-down resistor.

In addition to functioning as a general-purpose I/O port, Port 2 also functions as an address data bus (A0 to 7) and an address bus (A16 to 23). Using Port 2 as address bus (A0 to 7 or A16 to 23), write "1" to output latches and off the programmable pull-down resistors. Setting to address bus, set P2CR and P2FC register in a row.

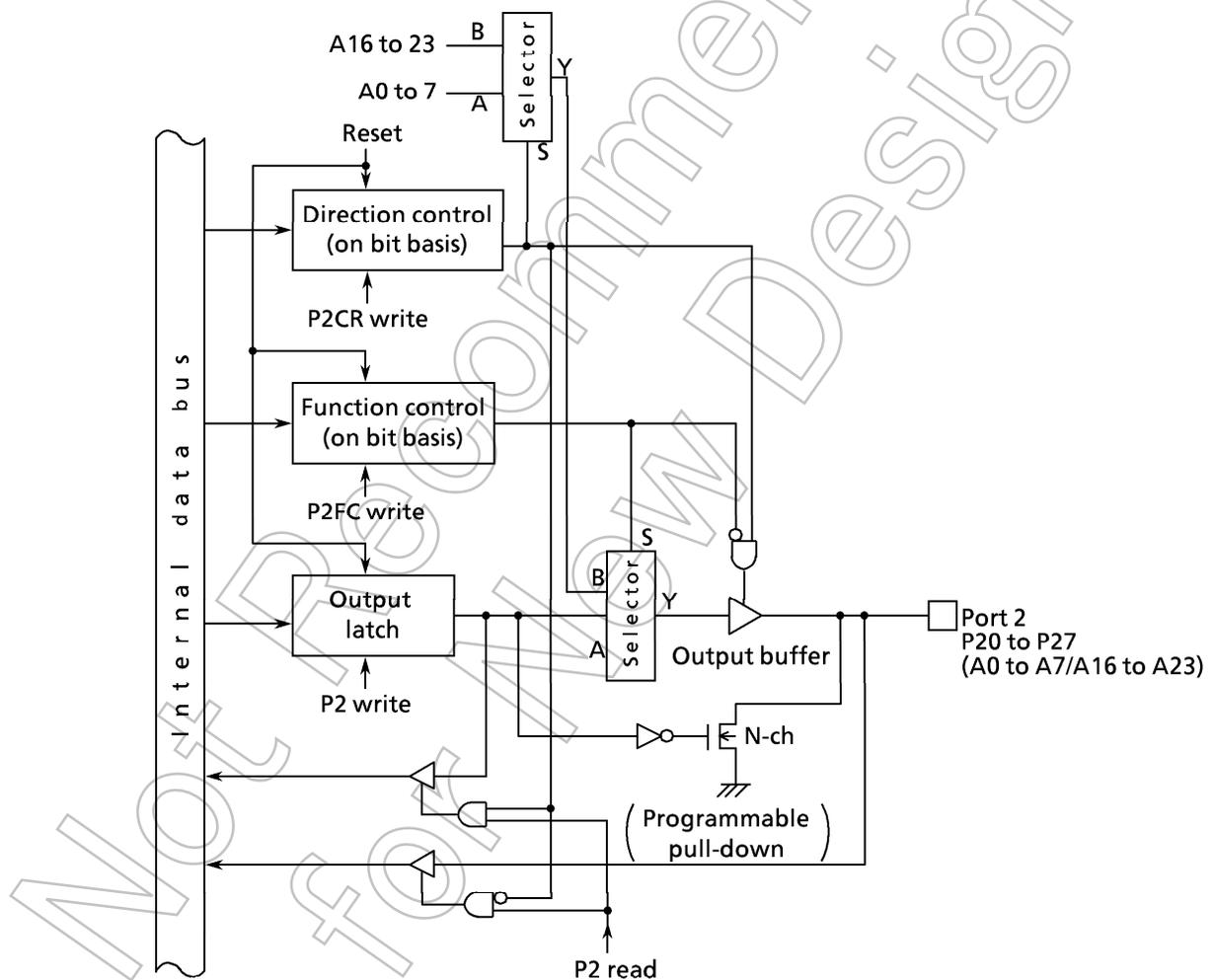


図 3.3 (4) Port 2

Port 2 Register

	7	6	5	4	3	2	1	0
bit Symbol	P27	P26	P25	P24	P23	P22	P21	P20
Read/Write	R/W							
After reset	Input mode (Output latch register is cleared to "0".)							

Port 2 Control Register

	7	6	5	4	3	2	1	0
bit Symbol	P27C	P26C	P25C	P24C	P23C	P22C	P21C	P20C
Read/Write	W							
After reset	0	0	0	0	0	0	0	0
Function	<<See P2FC below.>>							

Port 2 Function Register

	7	6	5	4	3	2	1	0
bit Symbol	P27F	P26F	P25F	P24F	P23F	P22F	P21F	P20F
Read/Write	W							
After reset	0	0	0	0	0	0	0	0
Function	P2FC/P2CR = 00 : IN, 01 : OUT, 10 : A7 to 0, 11 : A23 to 16							

- Read-modify-write is prohibited for registers P2CR and P2FC.
- Read-modify-write is prohibited for controlling ON/OFF of the pull-down resistor for register P2.

→ Port 2 function setting

	P2FC<P2XF>	
P2CR <P2XC>	0	1
0	Input	address bus (A7 to 0)
1	Output	address bus (A23 to 16)

Note : <P2XF> is bit X in register P2FC; <P2XC>; in register P2CR. To set as an address bus A23 to 16, set P2FC after setting P2CR.

Figure 3.3 (5) Registers for Port 2

### 3.3.4 Port 3 (P30 to P37)

Port 3 is an 8-bit general-purpose I/O port.

I/O can be set on a bit basis, but note that P30 and P31 are used for output only. I/O is set using control register P3CR and function register P3FC. Resetting resets all bits of output latch P3, control register P3CR (bits 0 and 1 are unused), and function register P3FC to 0. Resetting also outputs 1 from P30 and P31, sets P32 to P37 to input mode, and connects a pull-up resistor.

In addition to functioning as a general-purpose I/O port, Port 3 also functions as an I/O for the CPU's control/status signal.

When P30 pin is defined as  $\overline{RD}$  signal output mode ( $\langle P30F \rangle = 1$ ), clearing the output latch register  $\langle P30 \rangle$  to 0 outputs the  $\overline{RD}$  strobe (used for the pseudo static RAM) from the P30 pin even when the internal address area is accessed.

If the output latch register  $\langle P30 \rangle$  remains 1, the  $\overline{RD}$  strobe signal is output only when the external address area is accessed.

Not Recommended  
for New Designs

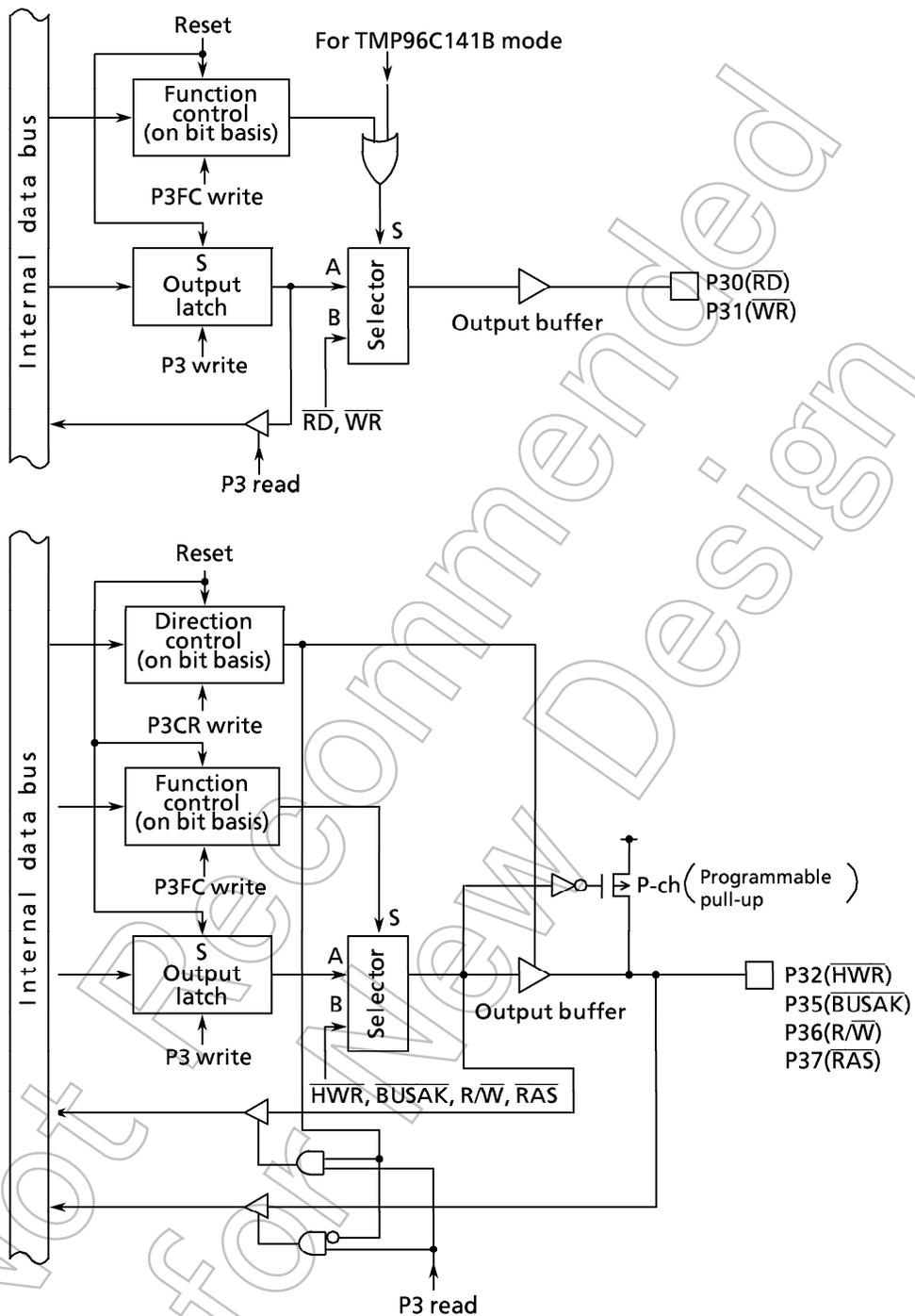


Figure 3.3 (6) Port 3 (P30, P31, P32, P35, P36, P37)

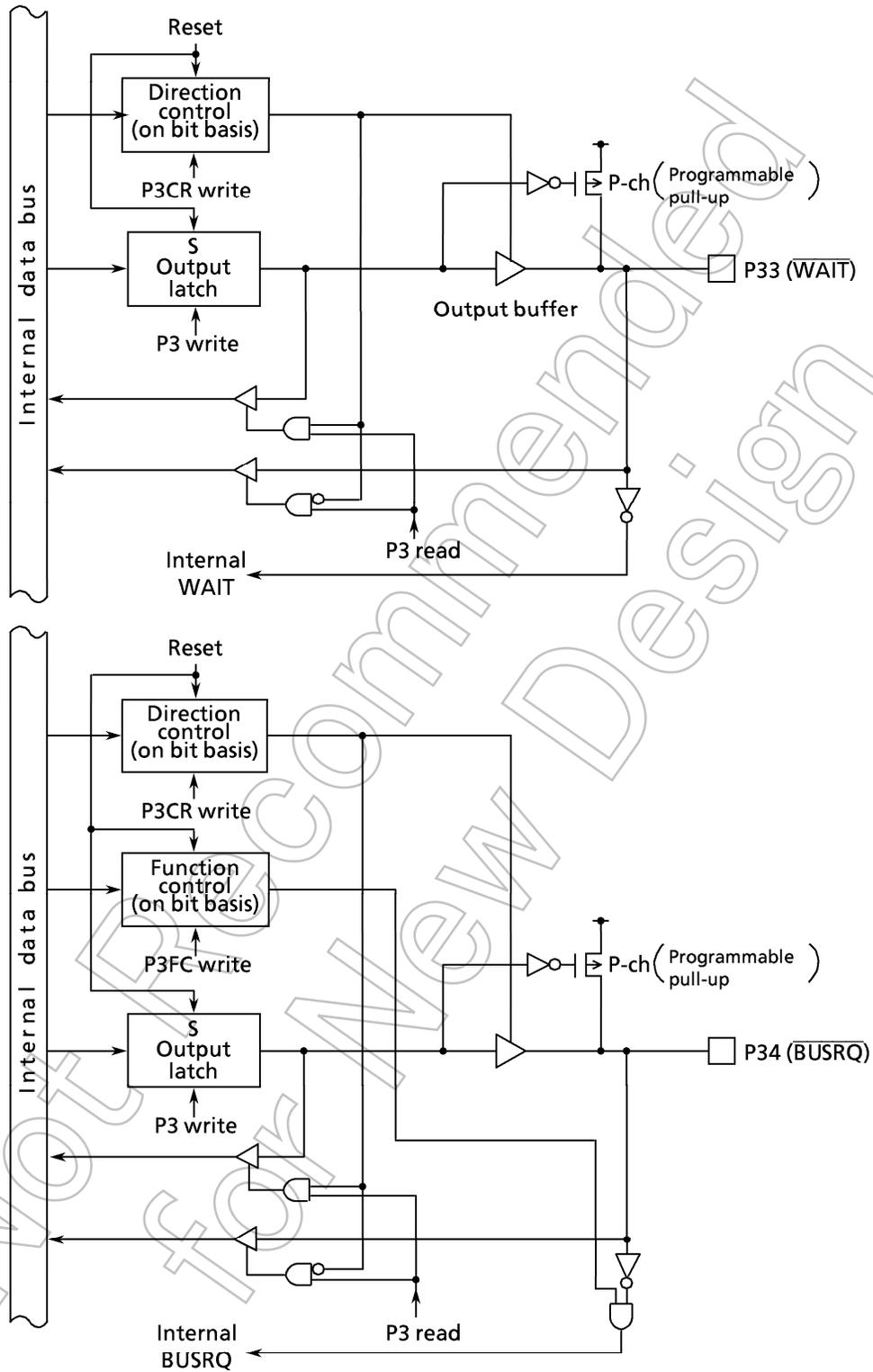
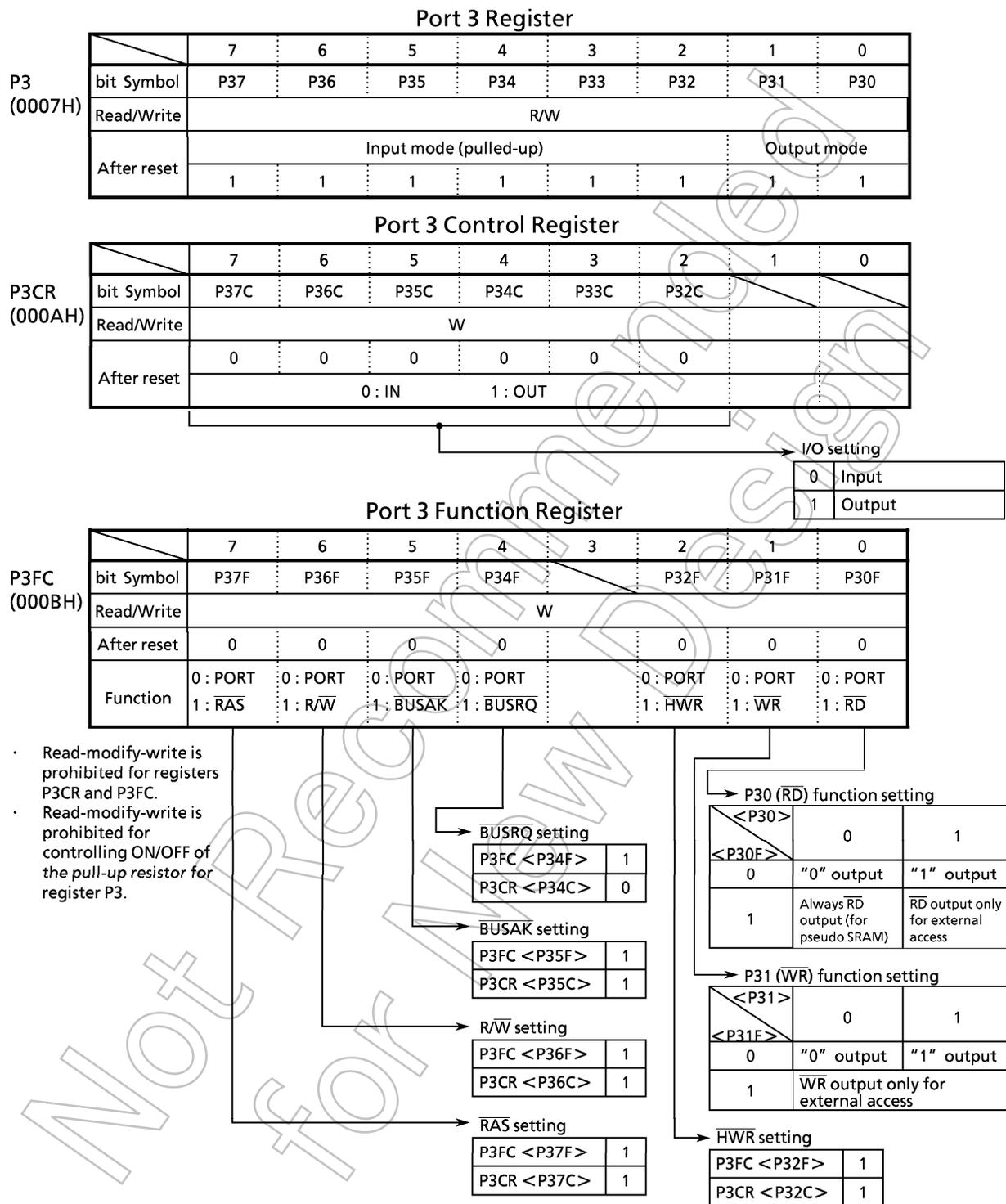


Figure 3.3 (7) Port3 (P33, P34)



Note : When P33/ $\overline{WAIT}$  pin is used as a  $\overline{WAIT}$  pin, set P3CR<P33C> to "0" and Chip Select /  $\overline{WAIT}$  control register <BnW1, 0> to "10".

Figure3.3 (8) Registers for Port 3

### 3.3.5 Port 4 (P40 to P42)

Port 4 is a 3-bit general-purpose I/O port. I/O can be set on a bit basis using control register P4CR and function register P4FC. Resetting does the following:

- Sets the P40 and P42 output latch registers to 1.
- Resets all bits of the P42 output latch register, the control register P4CR, and the function register P4FC to 0.
- Sets P40 and P41 to input mode and connects a pull-up resistor.
- Sets P42 to input mode and connects a pull-down resistor.

In addition to functioning as a general-purpose I/O port, Port 4 also functions as a chip select output signal ( $\overline{CS0}$  to  $\overline{CS2}$  or  $\overline{CAS0}$  to  $\overline{CAS2}$ ).

Not Recommended  
for New Design

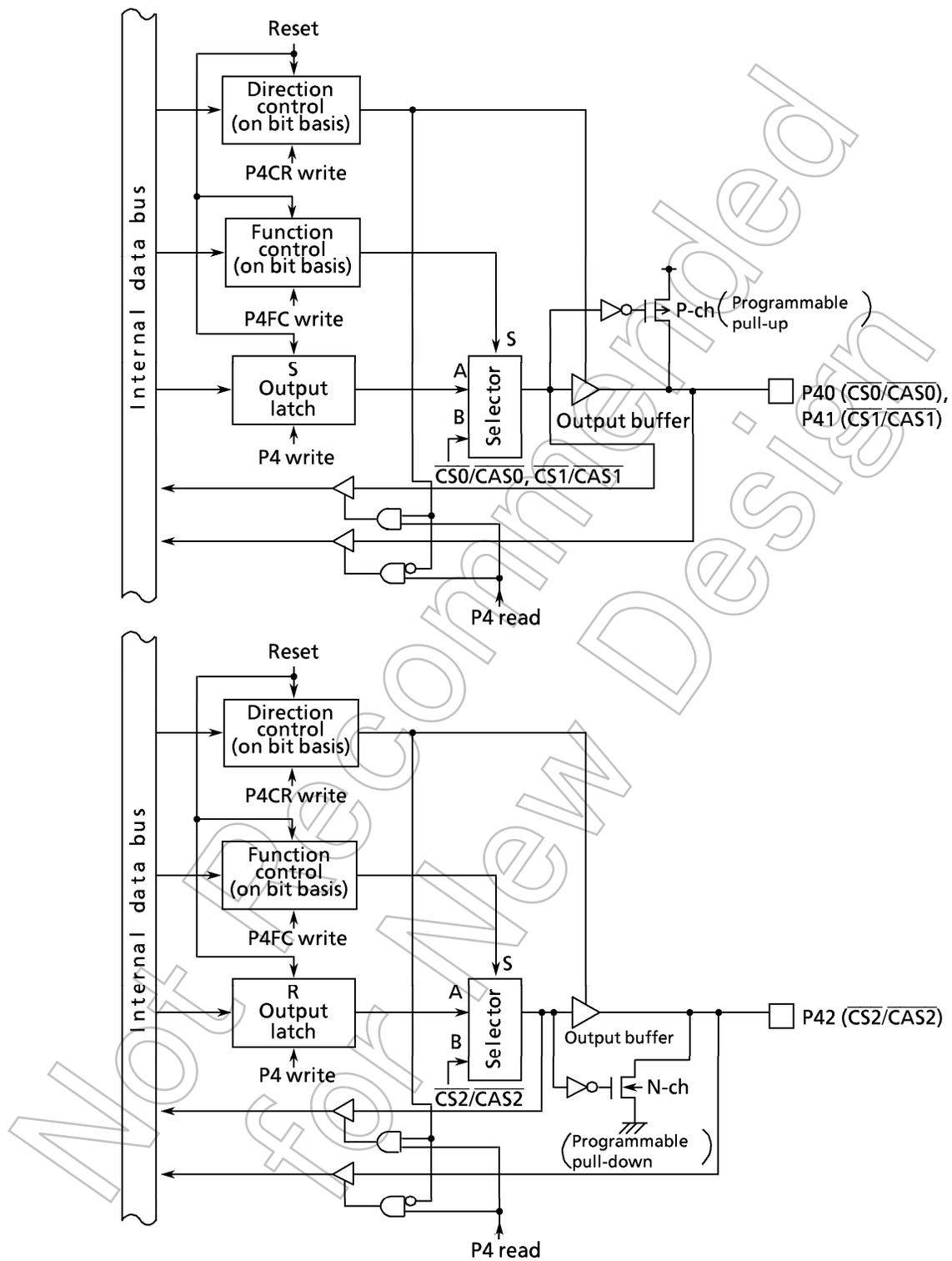
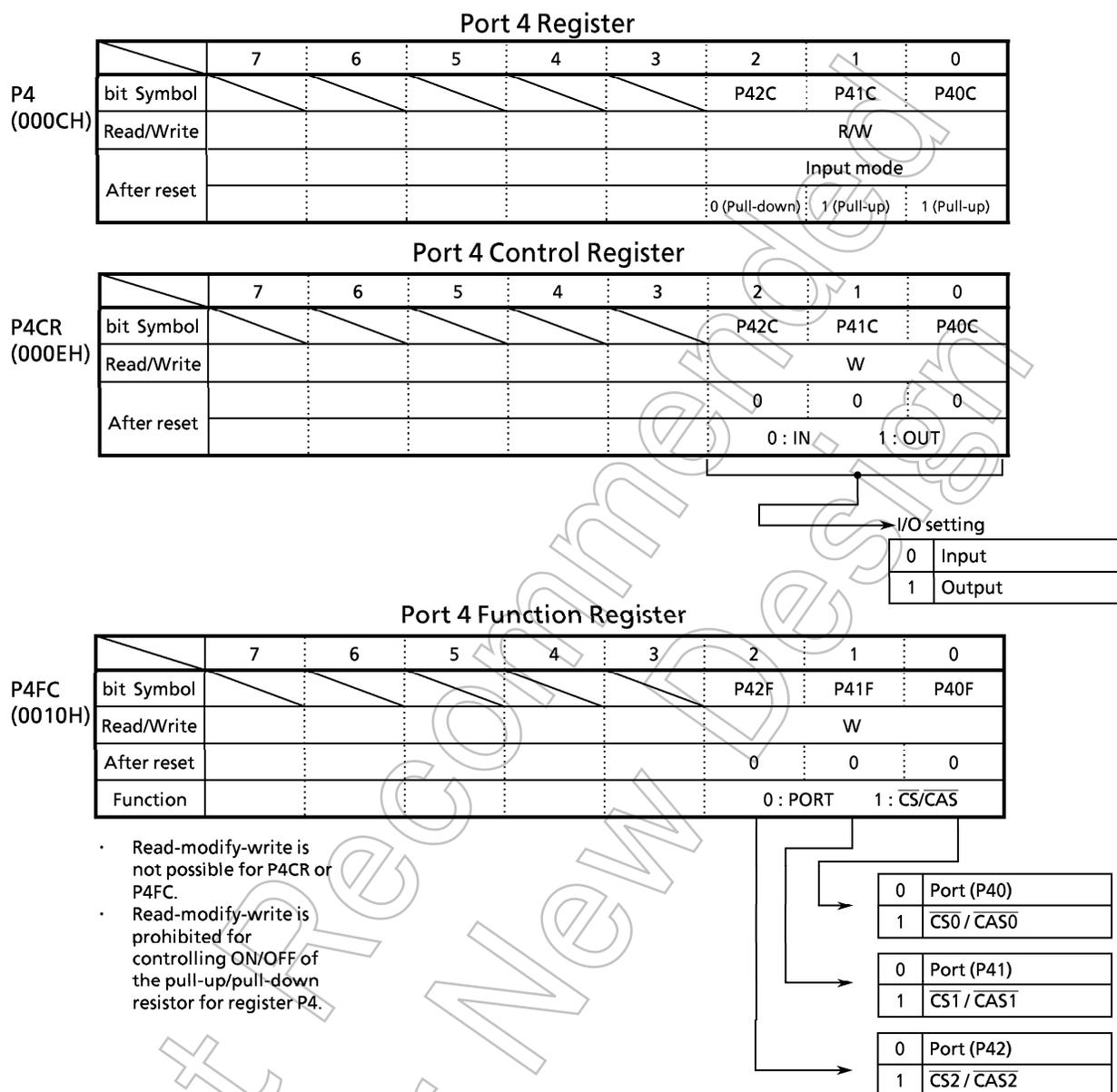


Figure 3.3 (9) Port 4



Note : To output chip select signal ( $\overline{CS0}/\overline{CAS0}$  to  $\overline{CS2}/\overline{CAS2}$ ), set the corresponding bits of the control register P4CR and the function register P4FC.  
 The B0CS, B1CS, and B2CS registers of the chip select / wait controller are used to select the  $\overline{CS}/\overline{CAS}$  function.

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Figure 3.3 (10) Registers for Port 4

3.3.6 Port 5 (P50 to P53)

Port 5 is a 4-bit input port, also used as an analog input pin.

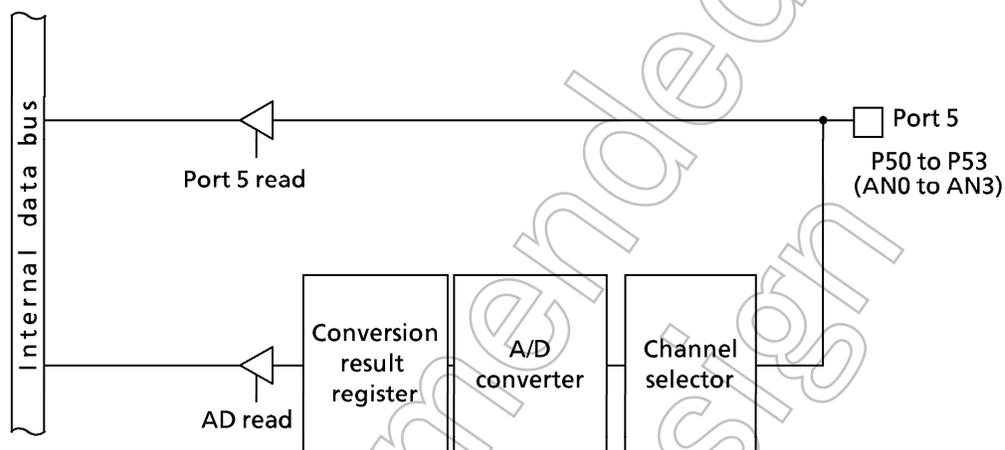


Figure3.3 (11) Port 5

**Port 5 Register**

	7	6	5	4	3	2	1	0	
P5 (000DH) bit Symbol	/			/		P53	P52	P51	P50
Read/Write	R								
After reset	Input mode								

Note : The input channel selection of A/D Converter is set by A/D Converter mode register ADMOD.

Figure 3.3 (12) Registers for Port 5

## 3.3.7 Port 6 (P60 to P67)

Port 6 is an 8-bit general-purpose I/O port. I/O can be set on bit basis. Resetting sets Port 6 as an input port and connects a pull-up resistor. It also sets all bits of the output latch to 1. In addition to functioning as a general-purpose I/O port, Port 6 also functions as a pattern generator PG0/PG1 output. PG0 is assigned to P60 to P63; PG1, to P64 to P67. Writing 1 in the corresponding bit of the port 6 function register (P6FC) enables PG output. Resetting resets the function register P6FC value to 0, and sets all bits to ports.

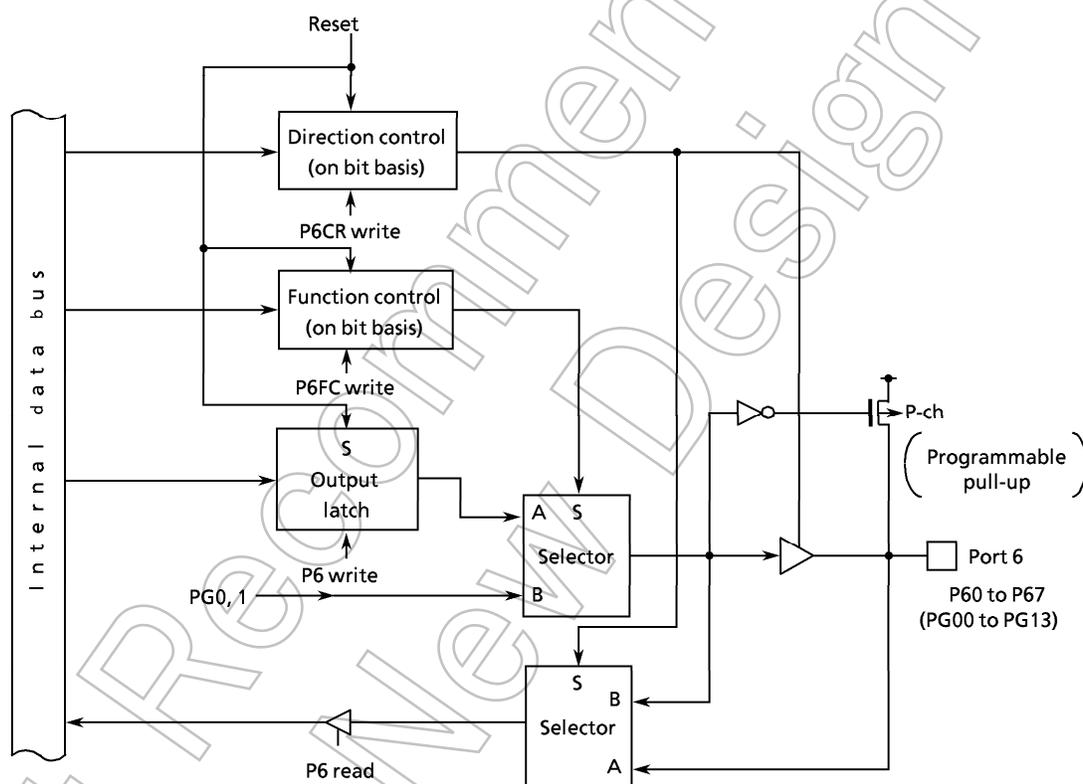


Figure 3.3 (13) Port 6

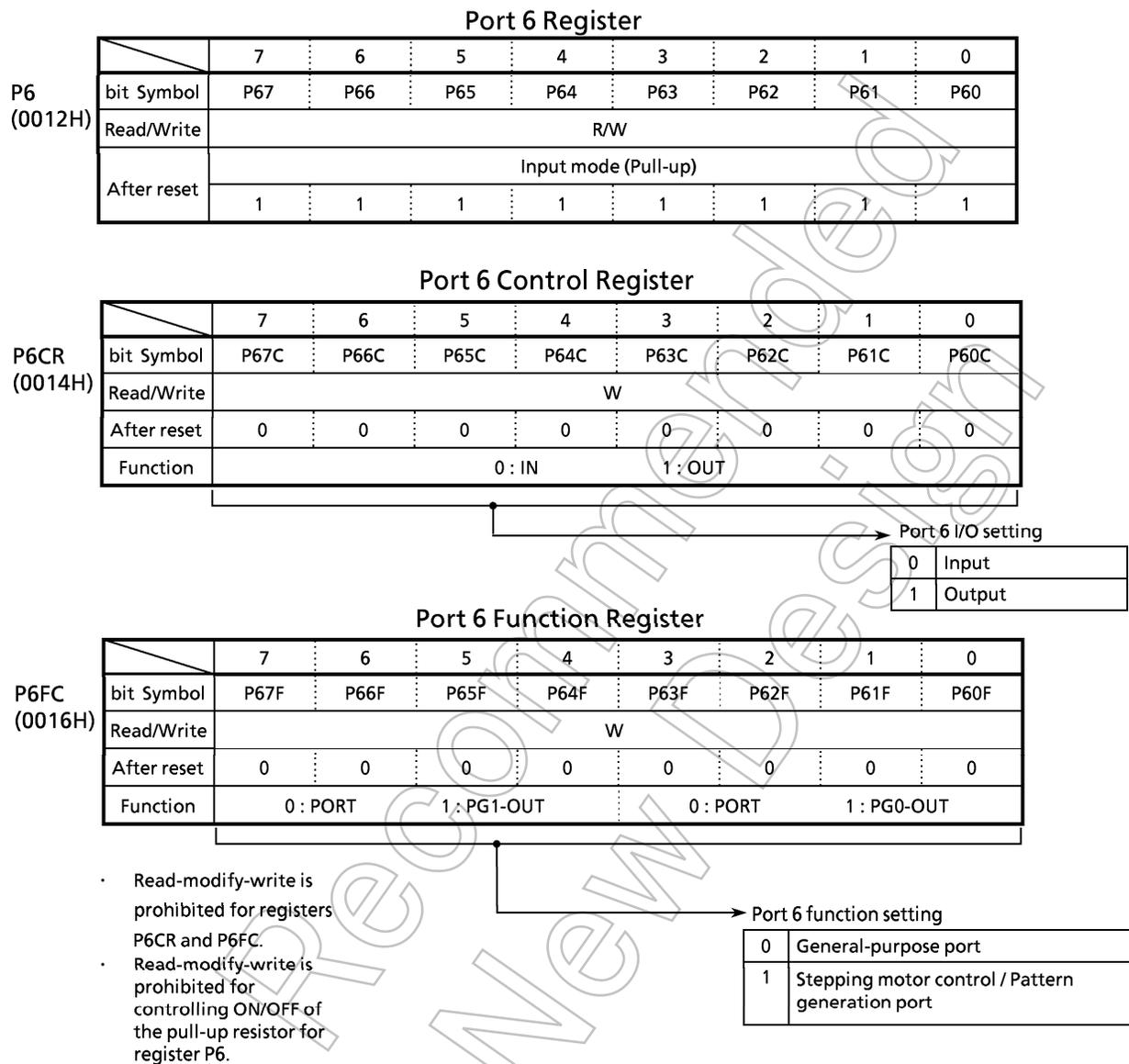


Figure3.3 (14) Registers for Port 6

3.3.8 Port 7 (P70 to P73)

Port 7 is a 4-bit general-purpose I/O port. I/O can be set on bit basis. Resetting sets Port 7 as an input port and connects a pull-up resistor. In addition to functioning as a general-purpose I/O port, Port 70 also functions as an input clock pin TIO; Port 71 as an 8-bit timer output (TO1), Port 72 as a PWM0 output (TO2), and Port 73 as a PWM1 output (TO3) pin. Writing 1 in the corresponding bit of the Port 7 function register (P7FC) enables output of the timer. Resetting resets the function register P7FC value to 0, and sets all bits to ports.

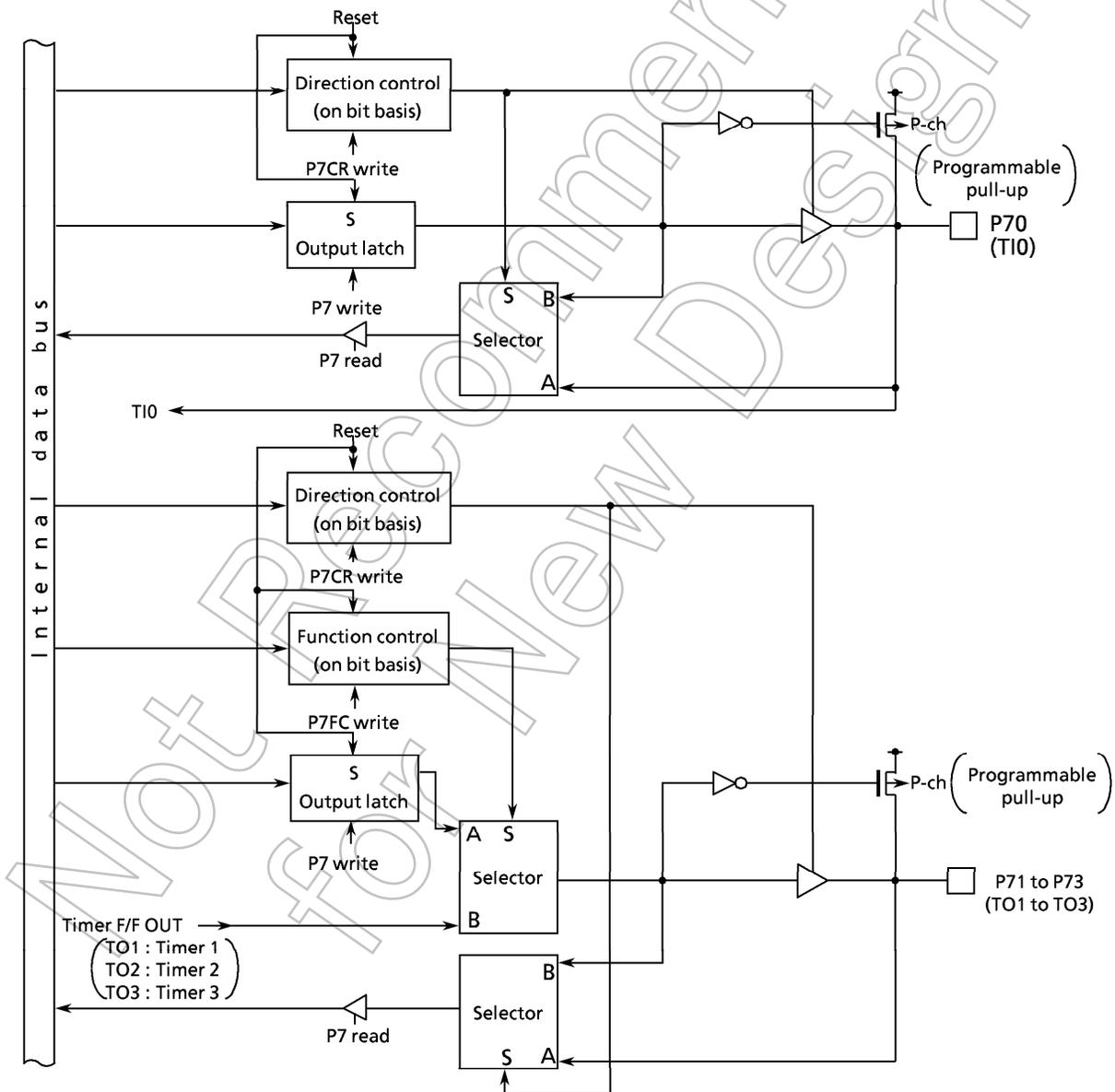


Figure 3.3 (15) Port 7

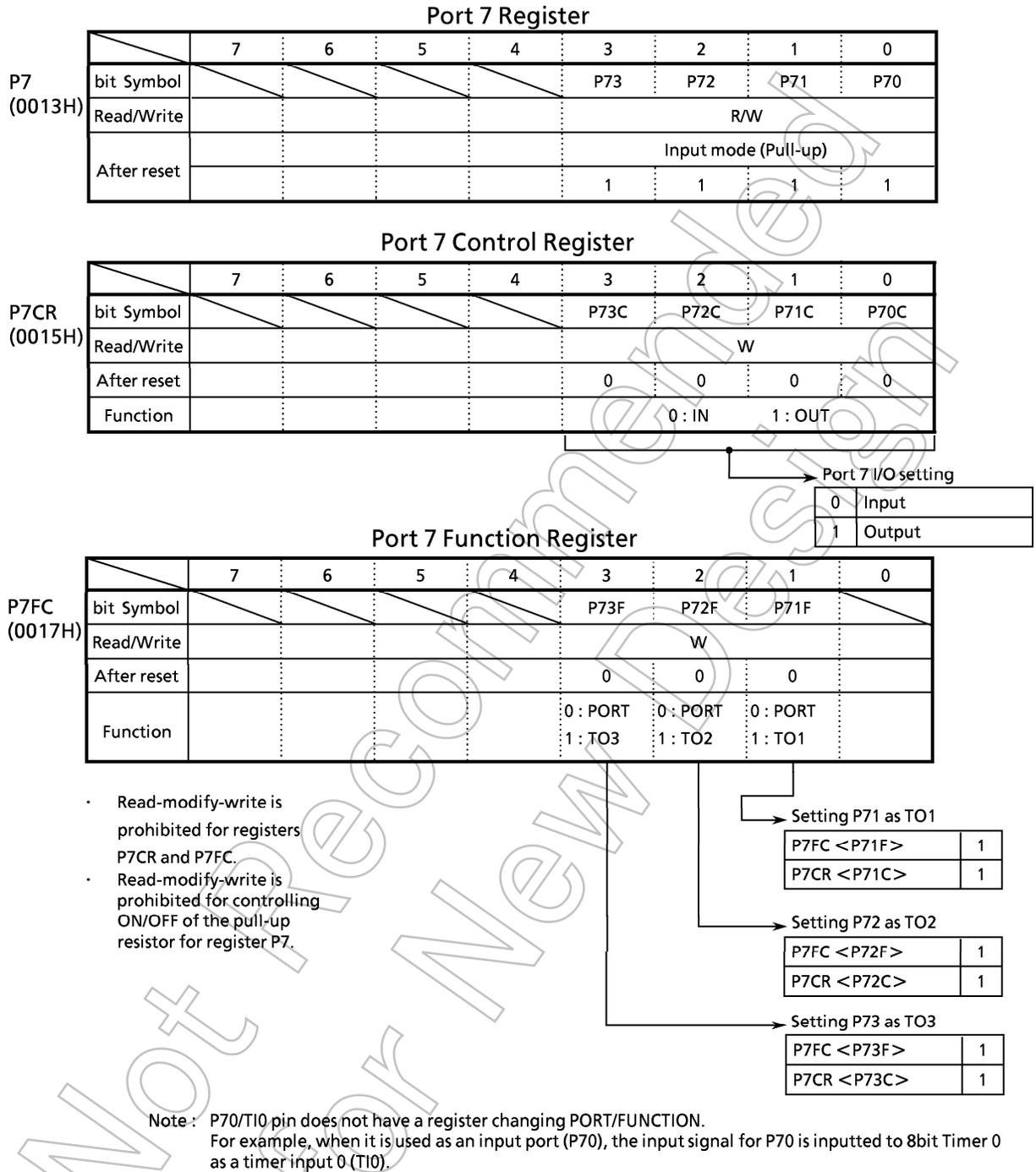


Figure3.3 (16) Registers for Port 7

3.3.9 Port 8 (P80 to P83)

Port 8 is an 8-bit general-purpose I/O port. I/O can be set on a bit basis. Resetting sets Port 8 as an input port and connects a pull-up resistor. It also sets all bits of the output latch register P8 to 1. In addition to functioning as a general-purpose I/O port, Port 8 also functions as an input for 16-bit timer 4, 5 clocks, an output for 16-bit timer F/F 4, 5, and 6 output, and an input for INT0. Writing 1 in the corresponding bit of the Port 8 function register (P8FC) enables those functions. Resetting resets the function register P8FC value to 0 and sets all bits to ports.

(1) P80 to P86

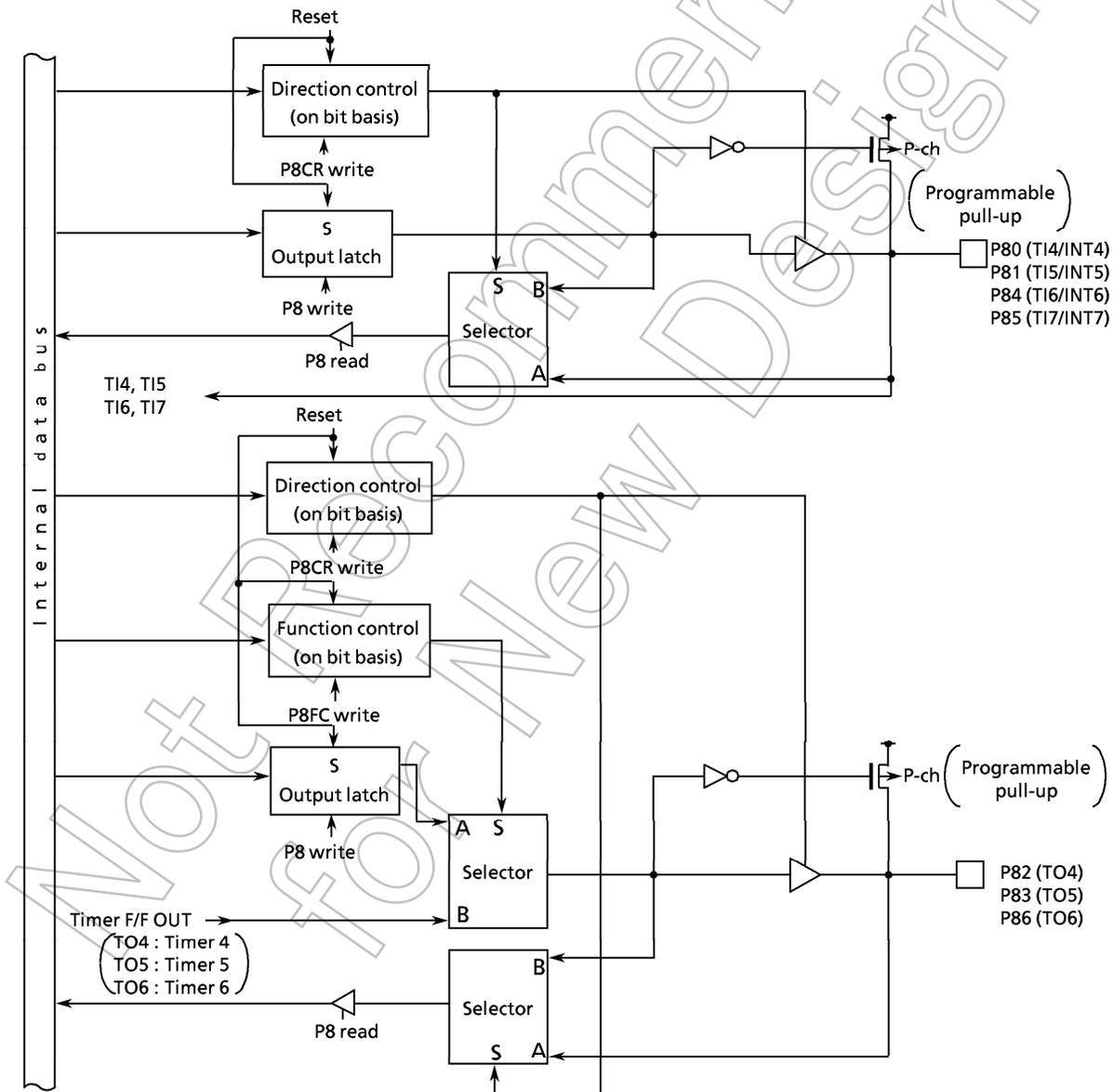


Figure 3.3 (17) Port 8 (P80 to P86)

(2) P87 (INT0)

Port 87 is a general-purpose I/O port, and also used as an INT0 pin for external interrupt request input.

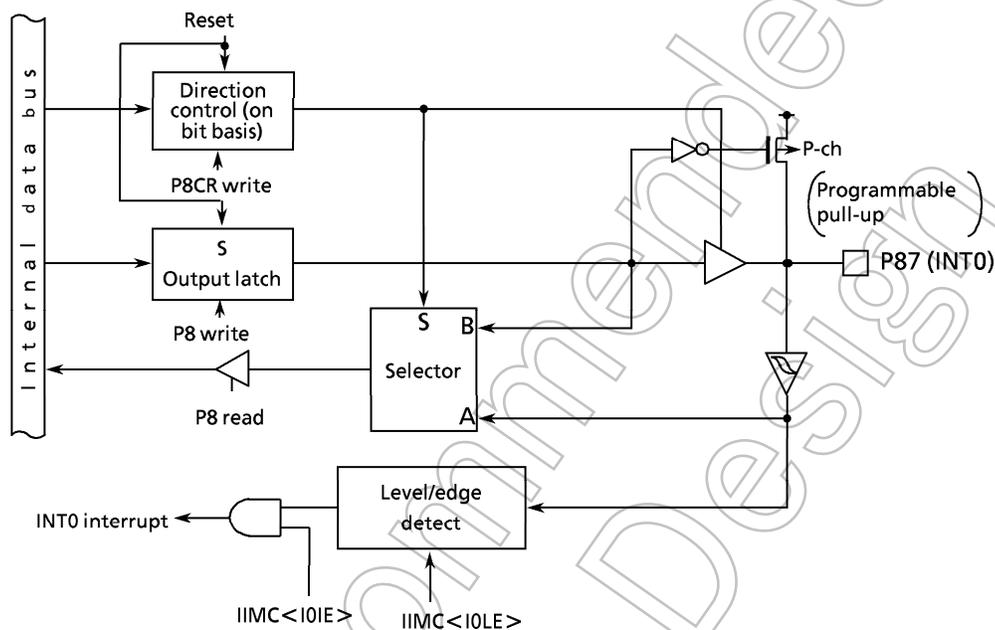


Figure 3.3 (18) Port 87

Not Recommended for New Design

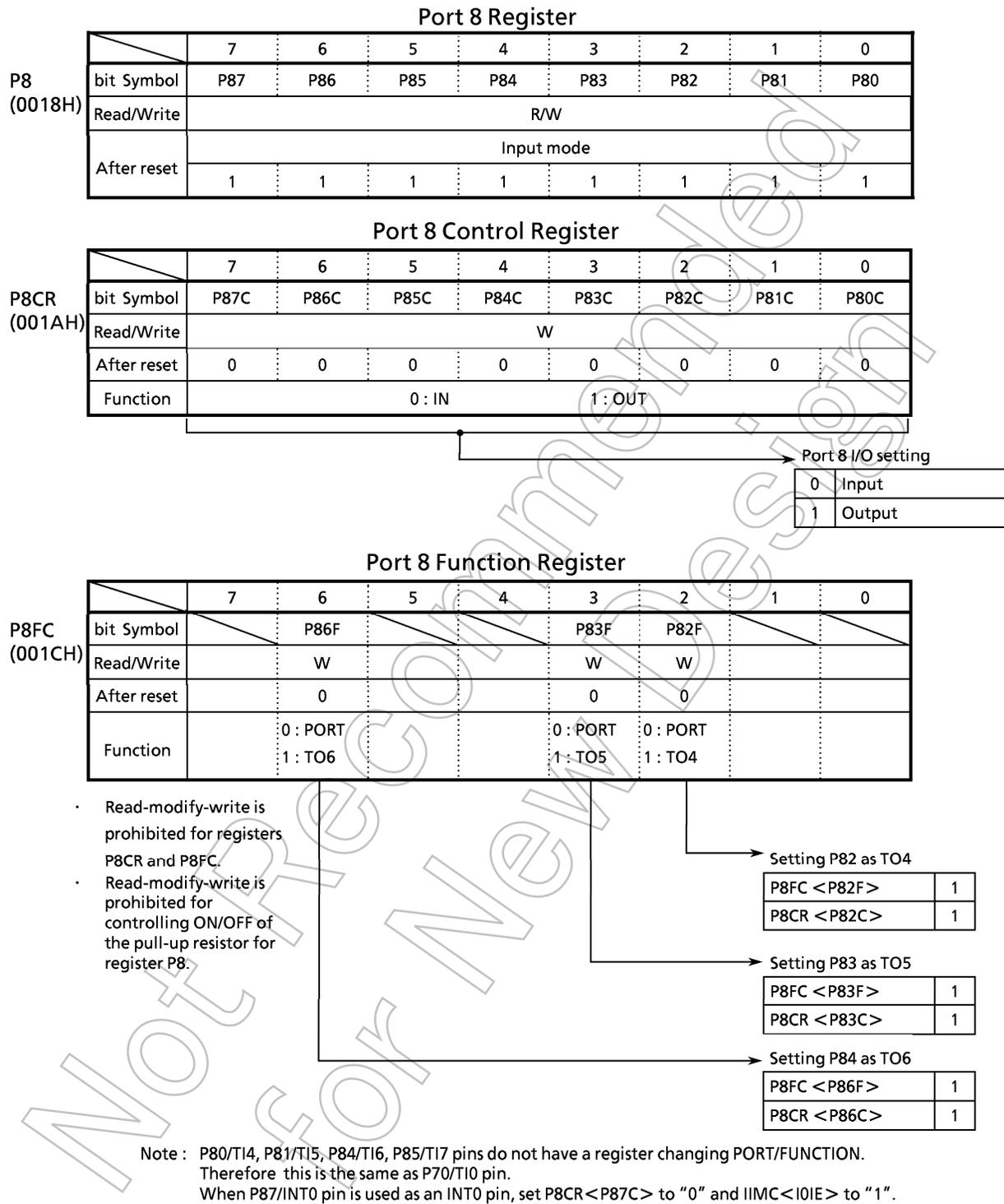


Figure3.3 (19) Registers for Port 8

### 3.3.10 Port 9 (P90 to P95)

Port 9 is a 6-bit general-purpose I/O port. I/Os can be set on a bit basis.

Resetting sets Port 9 to an input port and connects a pull-up resistor.

It also sets all bits of the output latch register to 1.

In addition to functioning as a general-purpose I/O port, Port 9 can also function as an I/O for serial channels 0 and 1. Writing 1 in the corresponding bit of the port 9 function register (P9FC) enables this function.

Resetting resets the function register value to 0 and sets all bits to ports.

#### (1) Port 90 & 93 (TXD0/TXD1)

Ports 90 and 93 also function as serial channel TXD output pins in addition to I/O ports.

They have a programmable open drain function.

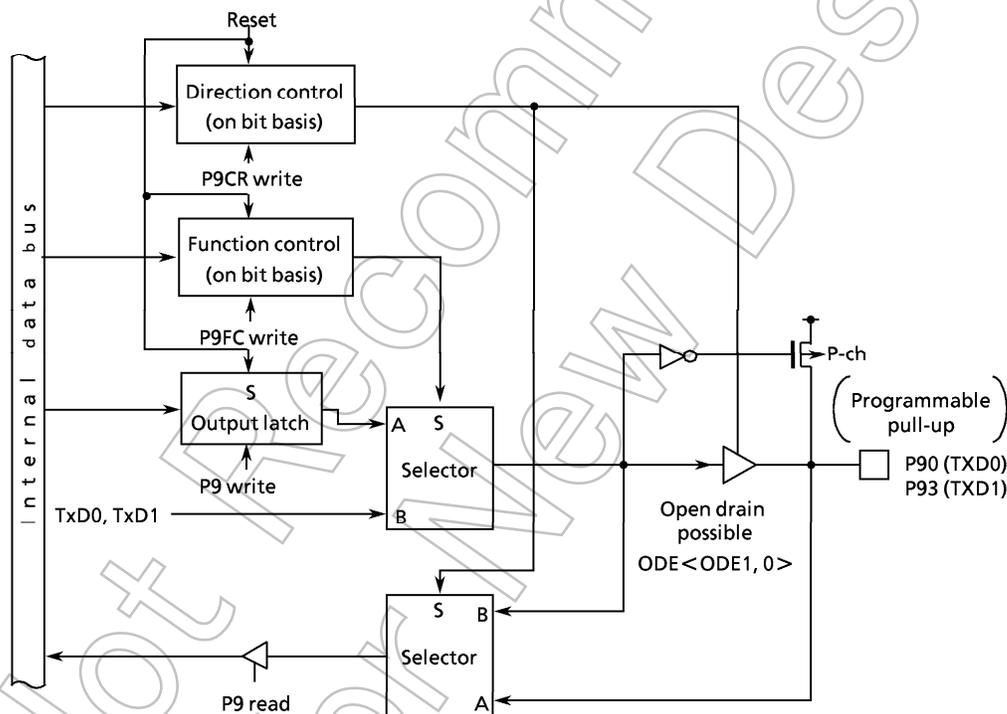


Figure 3.3 (20) Ports 90 and 93

(2) Ports 91 and 94 (RXD0, 1)

Ports 91 and 94 are I/O ports, and also used as RXD input pins for serial channels.

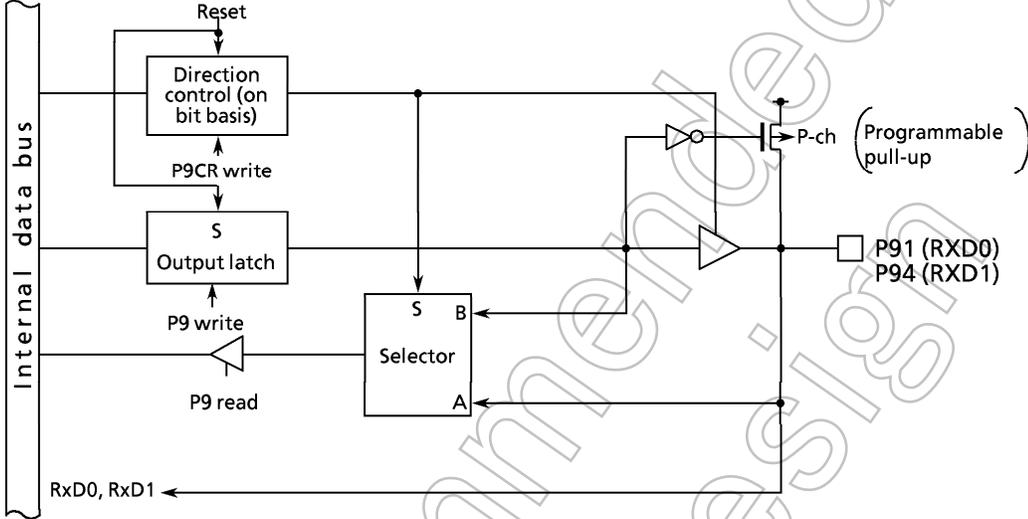


Figure3.3 (21) Ports 91 and 94

Not Recommended for New Design

(3) Port 92 ( $\overline{CTS0}/SCLK0$ )

Port 92 is an I/O port, and also used as a  $\overline{CTS0}$  input pin for serial channel0. Additionally, the  $\overline{CTS0}$  pin, and also as a SCLK0 I/O port.

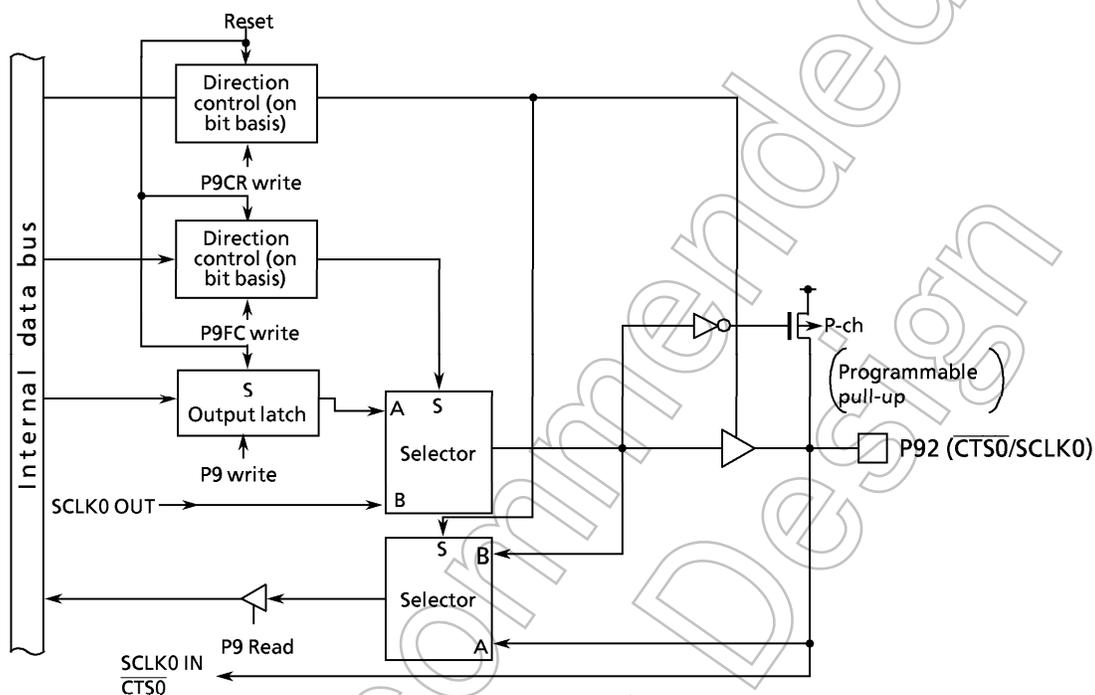


Figure3.3 (22) Ports 92

Not Recommended for New

(4) Port 95 (SCLK1)

Port 95 is a general-purpose I/O port. It is also used as an SCLK1 I/O pin for serial channel 1.

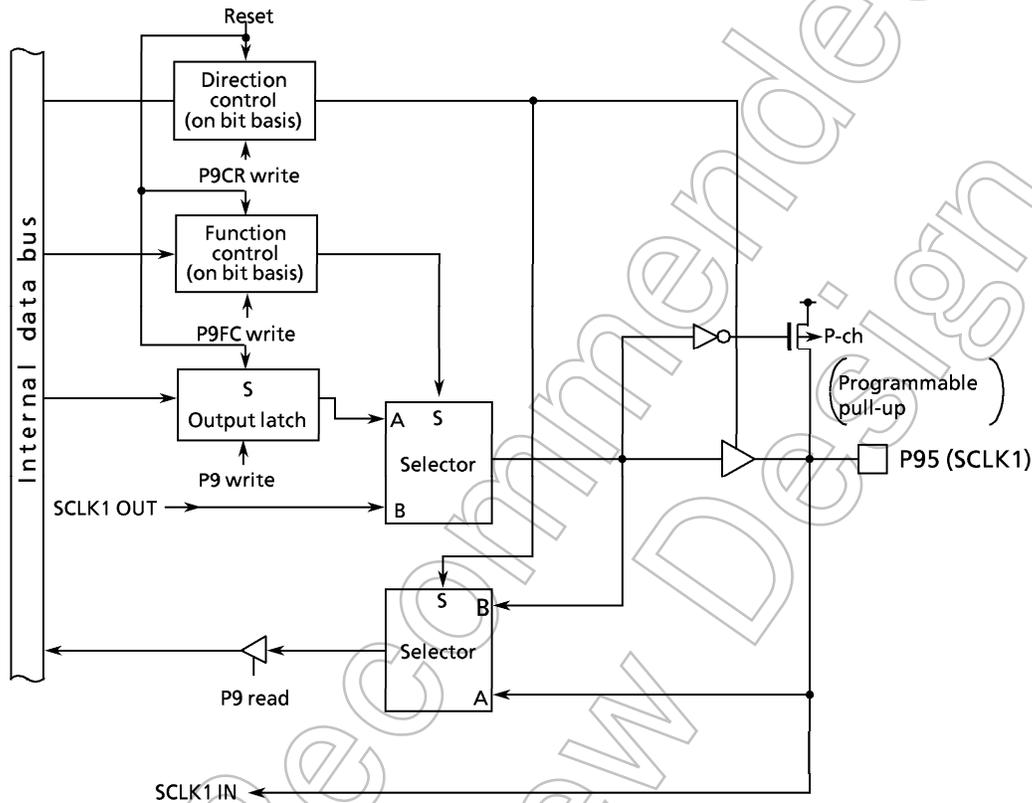


Figure3.3 (23) Port 95

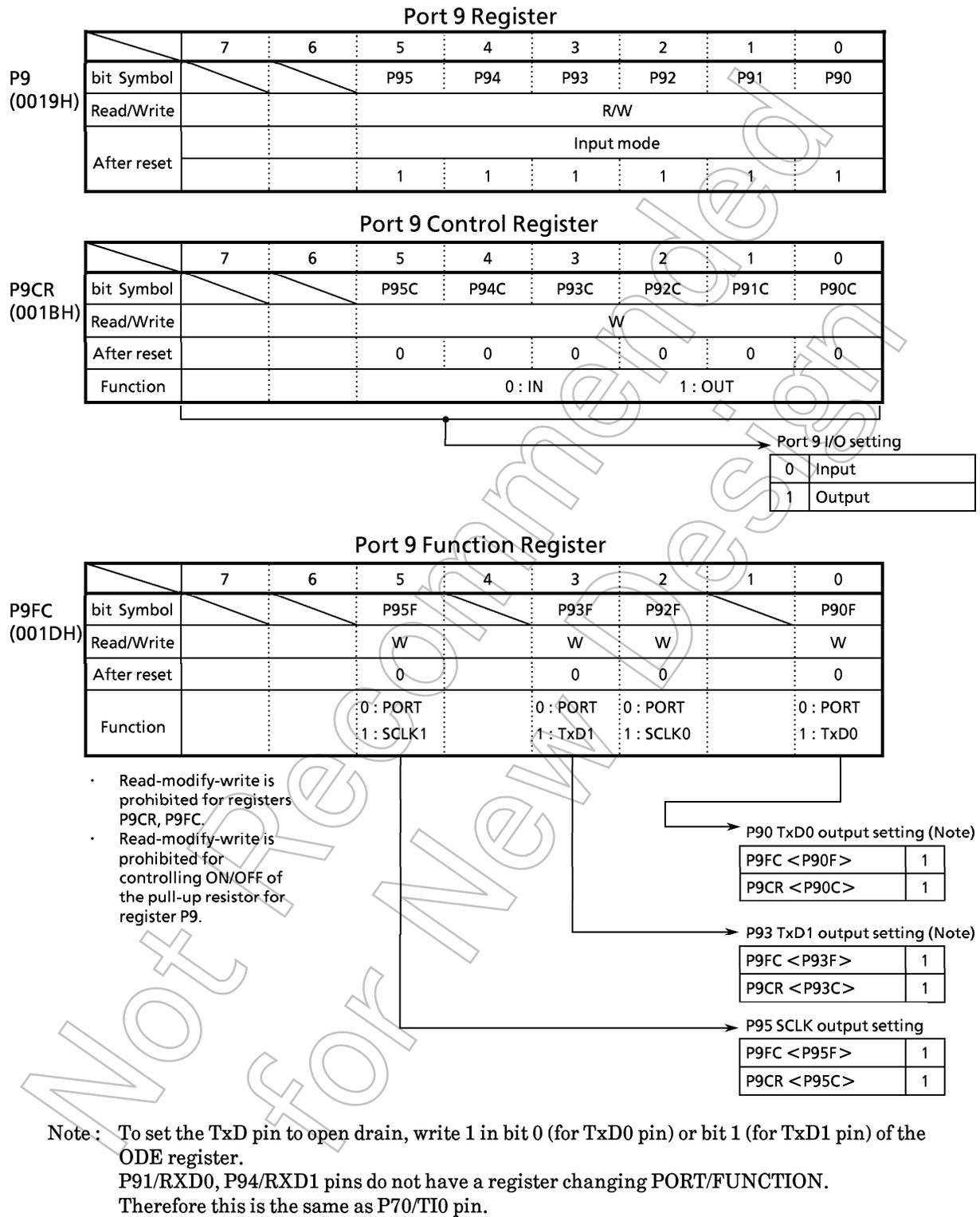


Figure 3.3 (24) Registers for Port 9

## 4. Electrical Characteristics

### 4.1 Absolute Maximum Ratings (TMP96CM40)

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V <sub>CC</sub>	- 0.5 to 6.5	V
Input Voltage	V <sub>IN</sub>	- 0.5 to V <sub>CC</sub> + 0.5	V
Output Current (total)	∑ I <sub>OL</sub>	100	mA
Output Current (total)	∑ I <sub>OH</sub>	- 100	mA
Power Dissipation (T <sub>a</sub> = 85°C)	P <sub>D</sub>	500	mW
Soldering Temperature (10 s)	T <sub>SOLDER</sub>	260	°C
Storage Temperature	T <sub>STG</sub>	- 65 to 150	°C
Operating Temperature	T <sub>OPR</sub>	- 40 to 85	°C

Note : The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Not Recommended for New Design

## 4.2 DC Characteristics (TMP96CM40)

 $V_{CC} = 5\text{ V} \pm 10\%$ ,  $T_A = -40\text{ to }85^\circ\text{C}$  (4 to 16 MHz)  $T_A = -20\text{ to }70^\circ\text{C}$  (4 to 20 MHz)
(Typical values are for  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 5\text{ V}$ )

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Low Voltage (AD0 to 15)	V <sub>IL</sub>		-0.3	0.8	V
P2, P3, P4, P5, P6, P7, P8, P9	V <sub>IL1</sub>		-0.3	0.3 V <sub>CC</sub>	V
RESET, NMI, INT0 (P87)	V <sub>IL2</sub>		-0.3	0.25 V <sub>CC</sub>	V
EA	V <sub>IL3</sub>		-0.3	0.3	V
X1	V <sub>IL4</sub>		-0.3	0.2 V <sub>CC</sub>	V
Input High Voltage (AD0 - 15)	V <sub>IH</sub>		2.2	V <sub>CC</sub> + 0.3	V
P2, P3, P4, P5, P6, P7, P8, P9	V <sub>IH1</sub>		0.7 V <sub>CC</sub>	V <sub>CC</sub> + 0.3	V
RESET, NMI, INT0 (P87)	V <sub>IH2</sub>		0.75 V <sub>CC</sub>	V <sub>CC</sub> + 0.3	V
EA	V <sub>IH3</sub>		V <sub>CC</sub> - 0.3	V <sub>CC</sub> + 0.3	V
X1	V <sub>IH4</sub>		0.8 V <sub>CC</sub>	V <sub>CC</sub> + 0.3	V
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 1.6 mA		0.45	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -400 $\mu$ A	2.4		V
	V <sub>OH1</sub>	I <sub>OH</sub> = -100 $\mu$ A	0.75 V <sub>CC</sub>		V
	V <sub>OH2</sub>	I <sub>OH</sub> = -20 $\mu$ A	0.9 V <sub>CC</sub>		V
Darlington Drive Current (8 Output Pins max.)	I <sub>DAR</sub>	V <sub>EXT</sub> = 1.5 V R <sub>EXT</sub> = 1.1 k $\Omega$	-1.0	-3.5	mA
Input Leakage Current	I <sub>LI</sub>	0.0 $\leq$ V <sub>in</sub> $\leq$ V <sub>CC</sub>	0.02 (Typ)	$\pm$ 5	$\mu$ A
Output Leakage Current	I <sub>LO</sub>	0.2 $\leq$ V <sub>in</sub> $\leq$ V <sub>CC</sub> - 0.2	0.05 (Typ)	$\pm$ 10	$\mu$ A
Operating Current (RUN)	I <sub>CC</sub>	f <sub>c</sub> = 20 MHz	30 (Typ)	TBD	mA
IDLE			2.0 (Typ)	10	mA
STOP (T <sub>a</sub> = -40 to 85 $^\circ$ C)		0.2 $\leq$ V <sub>in</sub> $\leq$ V <sub>CC</sub> - 0.2	0.2 (Typ)	50	$\mu$ A
STOP (T <sub>a</sub> = 0 to 50 $^\circ$ C)		0.2 $\leq$ V <sub>in</sub> $\leq$ V <sub>CC</sub> - 0.2		10	$\mu$ A
Power Down Voltage (@ STOP, RAM Back up)	V <sub>STOP</sub>	V <sub>IL2</sub> = 0.2 V <sub>CC</sub> , V <sub>IH2</sub> = 0.8 V <sub>CC</sub>	2.0	6.0	V
RESET Pull Up Resistor	R <sub>RST</sub>		50	150	k $\Omega$
Pin Capacitance	C <sub>IO</sub>	f <sub>c</sub> = 1 MHz		10	pF
Schmitt Width RESET, NMI, INT0 (P87)	V <sub>TH</sub>		0.4	1.0 (Typ)	V
Programmable Pull Down Resistor	R <sub>KL</sub>		10	80	k $\Omega$
Programmable Pull Up Resistor	R <sub>KH</sub>		50	150	k $\Omega$

Note : I-DAR is guaranteed for a total of up to 8 ports.

## 4.3 AC Electrical Characteristics (TMP96CM40)

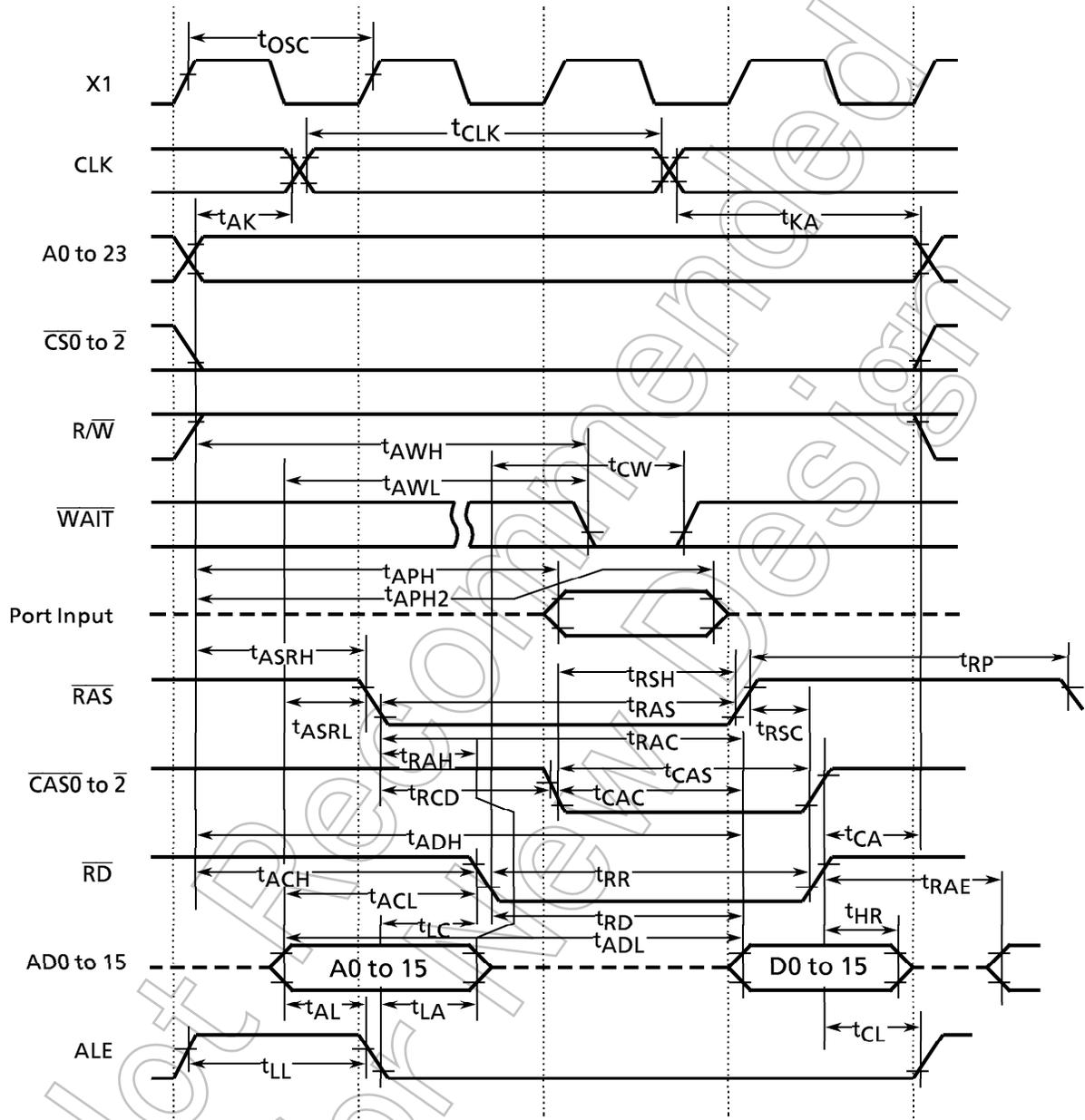
 $V_{CC} = 5\text{ V} \pm 10\%$ ,  $T_A = -40$  to  $85^\circ\text{C}$  (4 to 16 MHz)  $T_A = -20$  to  $70^\circ\text{C}$  (4 to 20 MHz)

No.	Parameter	Symbol	Variable		16 MHz		20 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	Osc. Period (= x)	$t_{OSC}$	50	250	62.5		50		ns
2	CLK width	$t_{CLK}$	$2x - 40$		85		60		ns
3	A0 to 23 Valid → CLK Hold	$t_{AK}$	$0.5x - 20$		11		5		ns
4	CLK Valid → A0 to 23 Hold	$t_{KA}$	$1.5x - 70$		24		5		ns
5	A0 to 15 Valid → ALE fall	$t_{AL}$	$0.5x - 15$		16		10		ns
6	ALE fall → A0 to 15 Hold	$t_{LA}$	$0.5x - 15$		16		10		ns
7	ALE High width	$t_{LL}$	$x - 40$		23		10		ns
8	ALE fall → RD/WR fall	$t_{LC}$	$0.5x - 30$		1		-5		ns
9	RD/WR rise → ALE rise	$t_{CL}$	$0.5x - 20$		11		5		ns
10	A0 to 15 Valid → RD/WR fall	$t_{ACL}$	$x - 25$		38		25		ns
11	A0 to 23 Valid → RD/WR fall	$t_{ACH}$	$1.5x - 50$		44		25		ns
12	RD/WR rise → A0 to 23 Hold	$t_{CA}$	$0.5x - 20$		11		5		ns
13	A0 to 15 Valid → D0 to 15 input	$t_{ADL}$		$3.0x - 45$		143		105	ns
14	A0 to 23 Valid → D0 to 15 input	$t_{ADH}$		$3.5x - 65$		154		110	ns
15	RDfall → D0 to 15 input	$t_{RD}$		$2.0x - 50$		75		50	ns
16	RD Low width	$t_{RR}$	$2.0x - 40$		85		60		ns
17	RDrise → D0 to 15 Hold	$t_{HR}$	0		0		0		ns
18	RDrise → A0 to 15output	$t_{RAE}$	$x - 15$		48		35		ns
19	WR Low width	$t_{WW}$	$2.0x - 40$		85		60		ns
20	D0 to 15 Valid → WR rise	$t_{DW}$	$2.0x - 50$		75		50		ns
21	WR rise → D0 to 15 Hold	$t_{WD}$	$0.5x - 10$		21		15		ns
22	A0 to 23 Valid → WAIT input <sup>(1WAIT + n mode)</sup>	$t_{AEH}$		$3.5x - 90$		129		85	ns
23	A0 to 15 Valid → WAIT input <sup>(1WAIT + n mode)</sup>	$t_{AWL}$		$3.0x - 80$		108		70	ns
24	RD/WR fall → WAIT Hold <sup>(1WAIT + n mode)</sup>	$t_{CW}$	$2.0x + 0$		125		100		ns
25	A0 to 23 Valid → PORT input	$t_{APH}$		$2.5x - 120$		36		5	ns
26	A0 to 23 Valid → PORT Hold	$t_{APH2}$	$2.5x + 50$		206		175		ns
27	WR rise → PORT Valid	$t_{CP}$		200		200		200	ns
28	A0 to 23 Valid → RAS fall	$t_{ASRH}$	$1.0x - 40$		23		10		ns
29	A0 to 15 Valid → RAS fall	$t_{ASRL}$	$0.5x - 15$		16		10		ns
30	RAS fall → D0 to 15 input	$t_{RAC}$		$2.5x - 70$		86		55	ns
31	RAS fall → A0 to 15 Hold	$t_{RAH}$	$0.5x - 15$		16		10		ns
32	RAS Low width	$t_{RAS}$	$2.0x - 40$		85		60		ns
33	RAS High width	$t_{RP}$	$2.0x - 40$		85		60		ns
34	CAS fall → RAS rise	$t_{RSH}$	$1.0x - 35$		28		15		ns
35	RAS rise → CAS rise	$t_{RSC}$	$0.5x - 25$		6		0		ns
36	RAS fall → CAS fall	$t_{RCD}$	$1.0x - 40$		23		10		ns
37	CAS fall → D0 to 15 input	$t_{CAC}$		$1.5x - 65$		29		10	ns
38	CAS Low width	$t_{CAS}$	$1.5x - 30$		64		40		ns

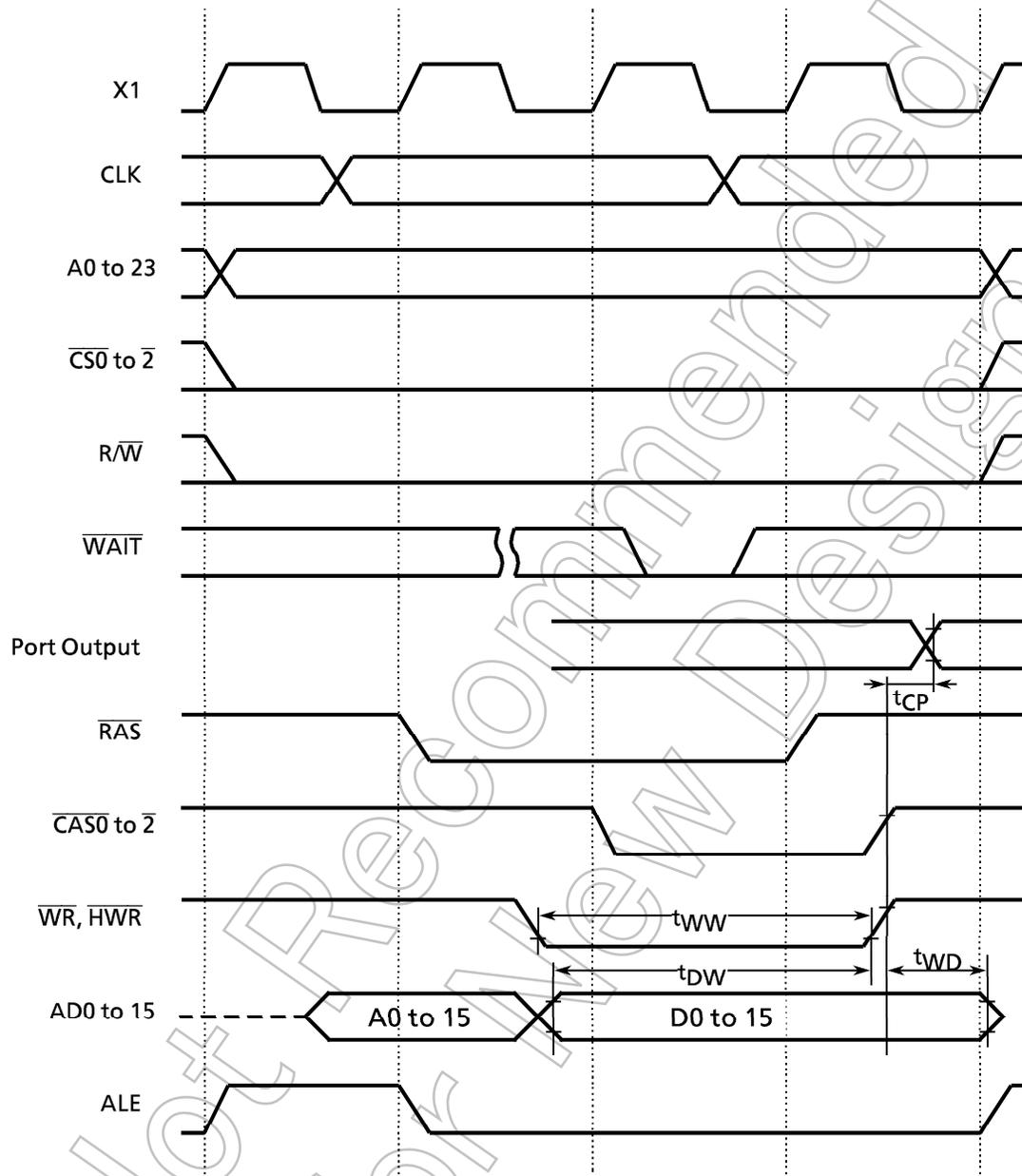
## AC Measuring Conditions

- Output Level : High 2.2 V / Low 0.8 V , CL50 pF  
(However CL = 100 pF for AD0 to AD15, A0 to A23, ALE, RD, WR, HWR, R/W, CLK, RAS, CAS0 to CAS2)
- Input Level : High 2.4 V / Low 0.45 V (AD0 to AD15)  
High 0.8 V<sub>CC</sub> / Low 0.2 V<sub>CC</sub> (Except for AD0 to AD15)

(1) Read Cycle



(2) Write Cycle



## 4.4 A/D Conversion Characteristics (TMP96CM40)

 $V_{CC} = 5V \pm 10\%$ ,  $T_A = -40$  to  $85^\circ\text{C}$  (4 to 16 MHz)  $T_A = -20$  to  $70^\circ\text{C}$  (4 to 20 MHz)

Parameter		Symbol	Min	Typ.	Max	Unit
Analog reference voltage		$V_{REF}$	$V_{CC} - 1.5$		$V_{CC}$	V
Analog reference voltage		$A_{GND}$	$V_{SS}$		$V_{SS}$	
Analog input voltage range		$V_{AIN}$	$V_{SS}$		$V_{CC}$	
Analog current for analog reference voltage		$I_{REF}$		0.5	1.5	mA
$4 \leq f_c \leq 16$ MHz	Low change mode	Total error (Quantize error of $\pm 0.5$ LSB not included)		$\pm 1.5$	$\pm 4.0$	LSB
	High change mode			$\pm 3.0$	$\pm 6.0$	
$16 < f_c \leq 20$ MHz	Low change mode			$\pm 1.5$	$\pm 4.0$	
	High change mode			$\pm 4.0$	$\pm 8.0$	

## 4.5 Serial Channel Timing – I/O Interface Mode

## (1) SCLK Input Mode

 $V_{CC} = 5V \pm 10\%$ ,  $T_A = -40$  to  $85^\circ\text{C}$  (4 to 16 MHz)  $T_A = -20$  to  $70^\circ\text{C}$  (4 to 20 MHz)

Parameter	Symbol	Variable		16 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK cycle	$t_{SCY}$	16X		1		0.8		$\mu\text{s}$
Output Data → Rising edge of SCLK	$t_{OSS}$	$t_{SCY}/2 - 5X - 50$		137		100		ns
SCLK rising edge → Output Data hold	$t_{OHS}$	$5X - 100$		212		150		ns
SCLK rising edge → Input Data hold	$t_{HSR}$	0		0		0		ns
SCLK rising edge → effective data input	$t_{SRD}$		$t_{SCY} - 5X - 100$		587		450	ns

## (2) SCLK Output Mode

 $V_{CC} = 5V \pm 10\%$ ,  $T_A = -40$  to  $85^\circ\text{C}$  (4 to 16 MHz)  $T_A = -20$  to  $70^\circ\text{C}$  (4 to 20 MHz)

Parameter	Symbol	Variable		16 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK cycle (programmable)	$t_{SCY}$	16X	8192X	1	512	0.8	409.6	$\mu\text{s}$
Output Data → SCLK rising edge	$t_{OSS}$	$t_{SCY} - 2X - 150$		725		550		ns
SCLK rising edge → Output Data hold	$t_{OHS}$	$2X - 80$		45		20		ns
SCLK rising edge → Input Data hold	$t_{HSR}$	0		0		0		ns
SCLK rising edge → effective data input	$t_{SRD}$		$t_{SCY} - 2X - 150$		725		550	ns

## 4.6 Timer/Counter Input Clock (TI0, TI4, TI5, TI6, TI7)

 $V_{CC} = 5V \pm 10\%$ ,  $T_A = -40$  to  $85^\circ\text{C}$  (4 to 16 MHz)  $T_A = -20$  to  $70^\circ\text{C}$  (4 to 20 MHz)

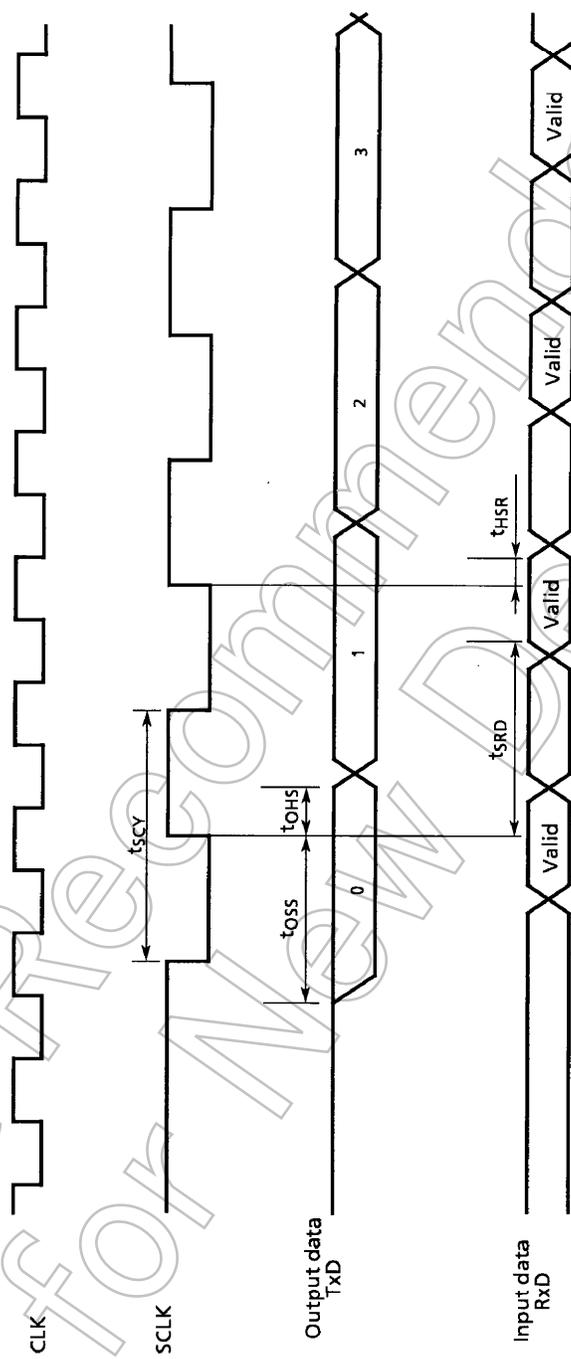
Parameter	Symbol	Variable		16 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
Clock Cycle	$t_{VCK}$	$8X + 100$		600		500		ns
Low level clock Pulse width	$t_{VCKL}$	$4X + 40$		290		240		ns
High level clock Pulse width	$t_{VCKH}$	$4X + 40$		290		240		ns

## 4.7 Interrupt Operation

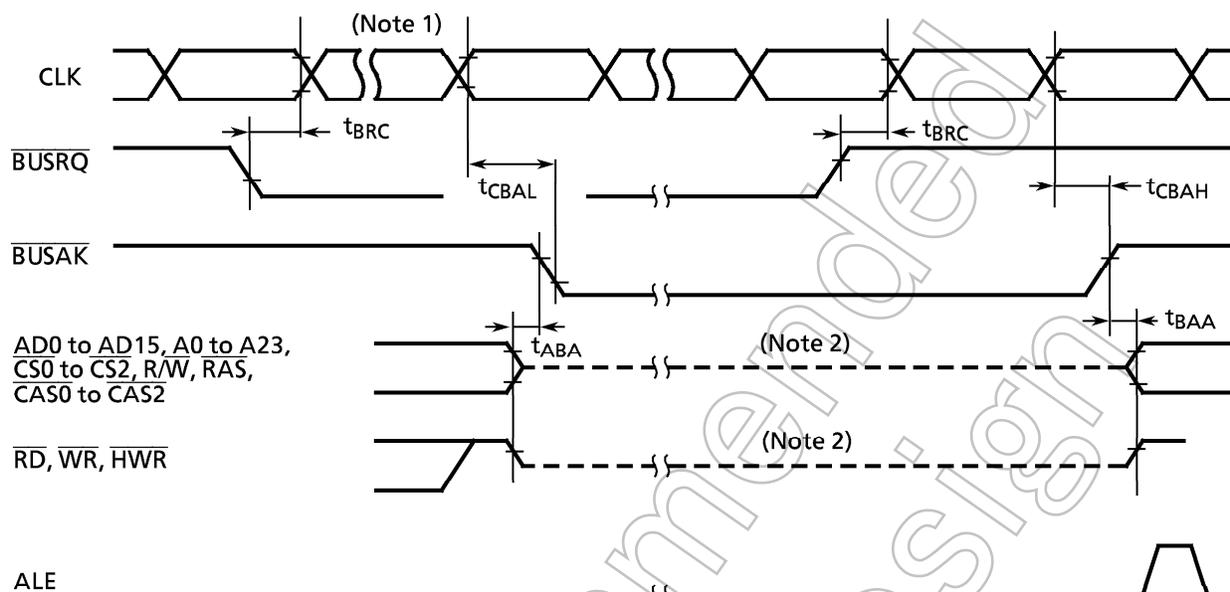
 $V_{CC} = 5V \pm 10\%$ ,  $T_A = -40$  to  $85^\circ\text{C}$  (4 to 16 MHz)  $T_A = -20$  to  $70^\circ\text{C}$  (4 to 20 MHz)

Parameter	Symbol	Variable		16 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
NMI, INT0 Low level Pulse width	$t_{INTAL}$	4X		250		200		ns
NMI, INT0 High level Pulse width	$t_{INTAH}$	4X		250		200		ns
INT4 to INT7 Low level Pulse width	$t_{INTBL}$	$8X + 100$		600		500		ns
INT4 to INT7 High level Pulse width	$t_{INTBH}$	$8X + 100$		600		500		ns

4.8 Timing Chart for I/O Interface Mode



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4.9 Timing Chart for Bus Request ( $\overline{\text{BUSRQ}}$ ) / Bus Acknowledge ( $\overline{\text{BUSAK}}$ )

Symbol	Parameter	Variable		16 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$t_{\text{BRC}}$	$\overline{\text{BUSRQ}}$ set-up time for CLK	120		120		120		ns
$t_{\text{CBAL}}$	CLK $\rightarrow$ $\overline{\text{BUSAK}}$ falling edge		$1.5x + 120$		214		195	ns
$t_{\text{CBAH}}$	CLK $\rightarrow$ $\overline{\text{BUSAK}}$ rising edge		$0.5x + 40$		71		65	ns
$t_{\text{ABA}}$	Output Buffer is off to $\overline{\text{BUSAK}}$	0	80	0	80	0	80	ns
$t_{\text{BAA}}$	$\overline{\text{BUSAK}}$ to Output Buffer is on.	0	80	0	80	0	80	ns

Note 1 : The Bus will be released after the  $\overline{\text{WAIT}}$  request is inactive, when the  $\overline{\text{BUSRQ}}$  is set to "0" during "Wait" cycle.

Note 2 : This line only shows the output buffer is off-state.

They don't indicate the signal level is fixed.

After the bus is released, the signal level is kept dynamically before the bus is released by the external capacitance.

Therefore, to fix the signal level by an external resistance under the bus is releasing, the design must be carefully because of the level-fix will be delayed.

The internal programmable pull-up/pull-down resistance is switched active/non-active by the internal signal.

4.10 Typical characteristics

$V_{CC}=5\text{ V}$ ,  $T_a=25\text{ }^\circ\text{C}$  unless other wise noted.

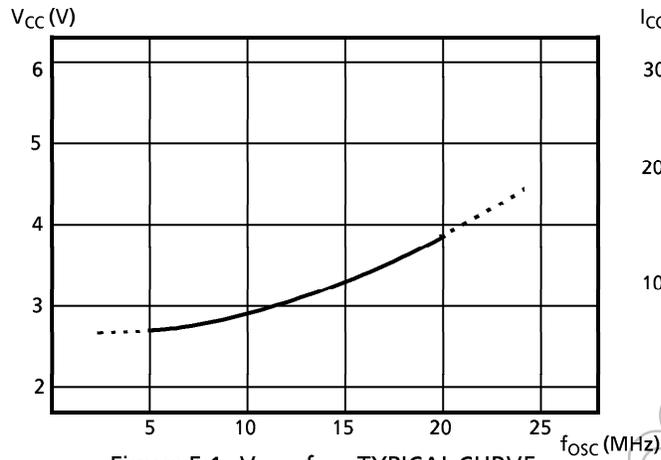


Figure 5.1  $V_{CC} - f_{osc}$  TYPICAL CURVE

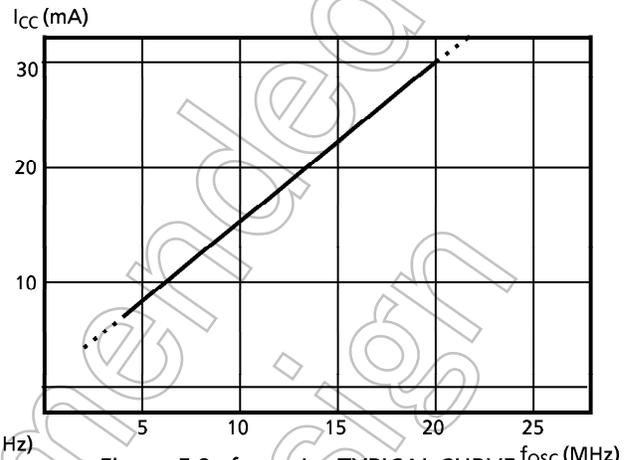


Figure 5.2  $f_{osc} - I_{CC}$  TYPICAL CURVE

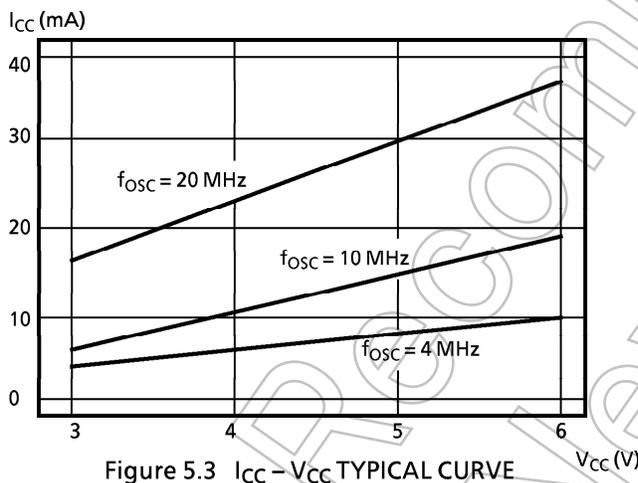


Figure 5.3  $I_{CC} - V_{CC}$  TYPICAL CURVE

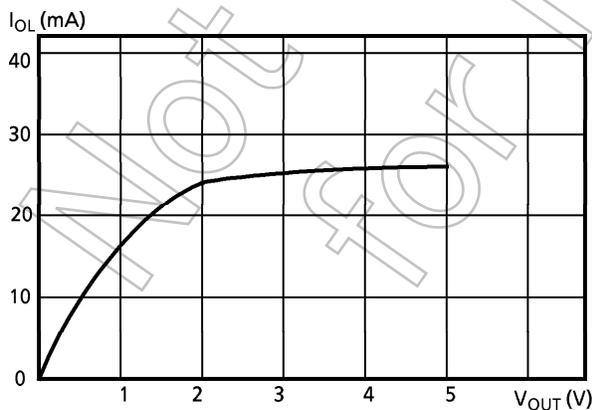


Figure 5.4  $V_{OUT} - I_{OL}$  TYPICAL CURVE

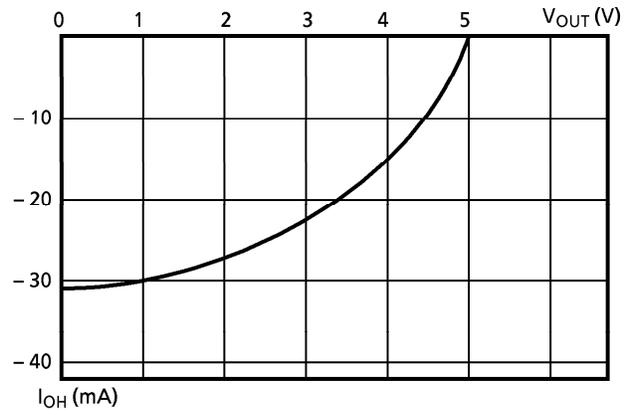


Figure 5.5  $V_{OUT} - I_{OH}$  TYPICAL CURVE

Not Recommended  
for New Design