TOSHIBA

TOSHIBA Original CMOS 8-Bit Microcontroller

TLCS-870 Series

TMP87PH40ANG
TMP87PH40AFG
TMP87PM40ANG
TMP87PM40AFG

TOSHIBA CORPORATION

Semiconductor Company

Important Notices

Thank you for your continued patronage of Toshiba microcontrollers.

This page gives you important information on using Toshiba microcontrollers. Please be sure to check each item for proper use of our products.

Toshiba Microcontrollers 870 Family
(TMP87PM40) (TMP87PM40A)

Dear Customer

Note on Using the TLCS-870 Series OTP Products

With regard to the TLCS-870 Series OTP microcontrollers listed above, the following problem has been identified. If this issue presents you with any problem, please contact your local Toshiba sales office.

[Problem]

When the power supply start-up is over 10ms, a maximum of approximately 25 μA of DC current may pass through the OTP control circuit in some rare cases. On these rare occations, the supply current values in SLOW, SLEEP and STOP modes cannot meet the values specified in the technical datasheet.

There is no problem in other DC characteristics, and operational functions and mask ROM products.

[Alternative products]

When a set can be developed newly, we will recommend the following alternate products.

Object products	Alternative products
TMP87PM40	TMP86PM49
TMP87PM40A	TMP86PM49

Document Change Notification

The purpose of this notification is to inform customers about the launch of the Pb-free version of the device. The introduction of a Pb-free replacement affects the datasheet. Please understand that this notification is intended as a temporary substitute for a revision of the datasheet.

Changes to the datasheet may include the following, though not all of them may apply to this particular device.

1. Part number

   Example: TMPxxxxxxF → TMPxxxxxxFG

   All references to the previous part number were left unchanged in body text. The new part number is indicated on the prelims pages (cover page and this notification).

2. Package code and package dimensions

   Example: LQFP100-P-1414-0.50C → LQFP100-P-1414-0.50F

   All references to the previous package code and package dimensions were left unchanged in body text. The new ones are indicated on the prelims pages.

3. Addition of notes on lead solderability

   Now that the device is Pb-free, notes on lead solderability have been added.

4. RESTRICTIONS ON PRODUCT USE

   The previous (obsolete) provision might be left unchanged on page 1 of body text. A new replacement is included on the next page.

5. Publication date of the datasheet

   The publication date at the lower right corner of the prelims pages applies to the new device.

1. Part number

2. Package code and dimensions

Previous Part Number (in Body Text)	Previous Package Code (in Body Text)	New Part Number	New Package Code	OTP
TMP87PH40AN	SDIP64-P-750-1.78	TMP87PH40ANG	SDIP64-P-750-1.78	—
TMP87PH40AF	QFP64-P-1420-1.00A	TMP87PH40AFG	QFP64-P-1420-1.00A	—
TMP87PM40AN	SDIP64-P-750-1.78	TMP87PM40ANG	SDIP64-P-750-1.78	—
TMP87PM40AF	QFP64-P-1420-1.00A	TMP87PM40AFG	QFP64-P-1420-1.00A	—

*: For the dimensions of the new package, see the attached Package Dimensions diagram.

3. Addition of notes on lead solderability

The following solderability test is conducted on the new device.

Lead solderability of Pb-free devices (with the G suffix)

Test	Test Conditions	Remark
Solderability	(1) Use of Lead (Pb) ·solder bath temperature = 230°C ·dipping time = 5 seconds ·the number of times = once ·use of R-type flux (2) Use of Lead (Pb)-Free ·solder bath temperature = 245°C ·dipping time = 5 seconds ·the number of times = once ·use of R-type flux	Leads with over 95% solder coverage till lead forming are acceptable.

4. RESTRICTIONS ON PRODUCT USE

The following replaces the "RESTRICTIONS ON PRODUCT USE" on page 1 of body text.

RESTRICTIONS ON PRODUCT USE 20070701-EN

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- For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance/Handling Precautions.

5. Publication date of the datasheet

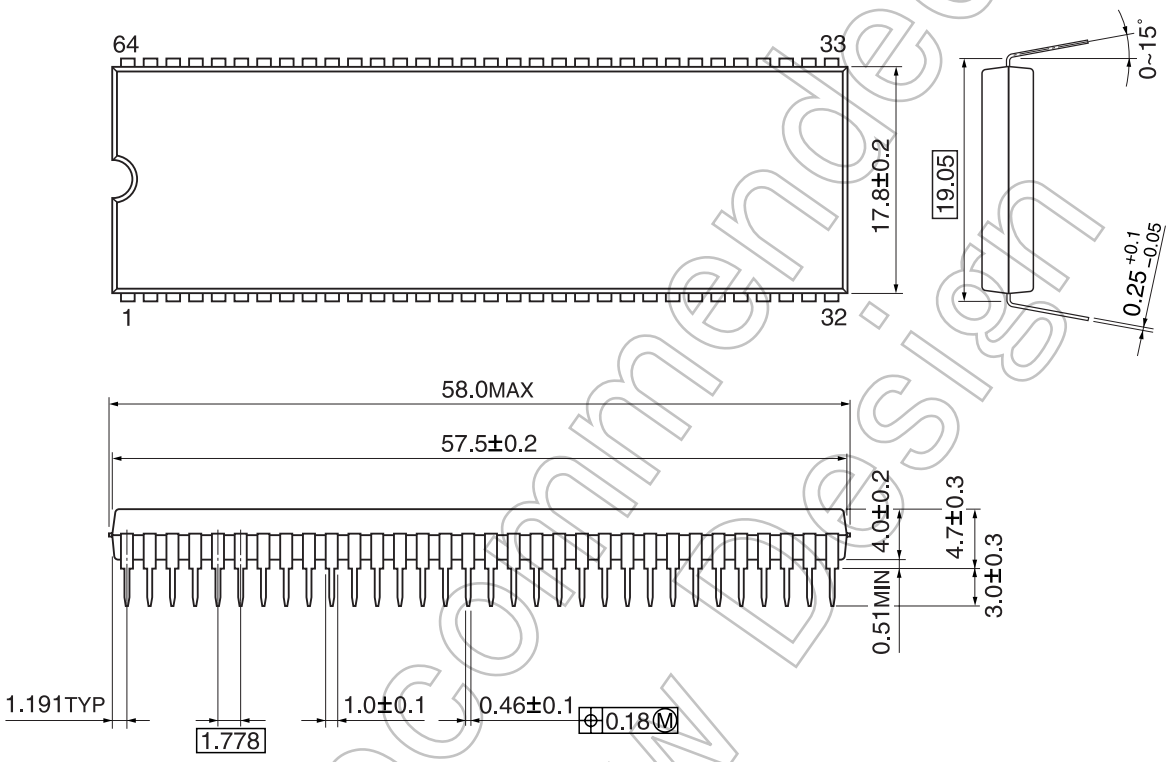
The publication date of this datasheet is printed at the lower right corner of this notification.

(Annex)

Package Dimensions

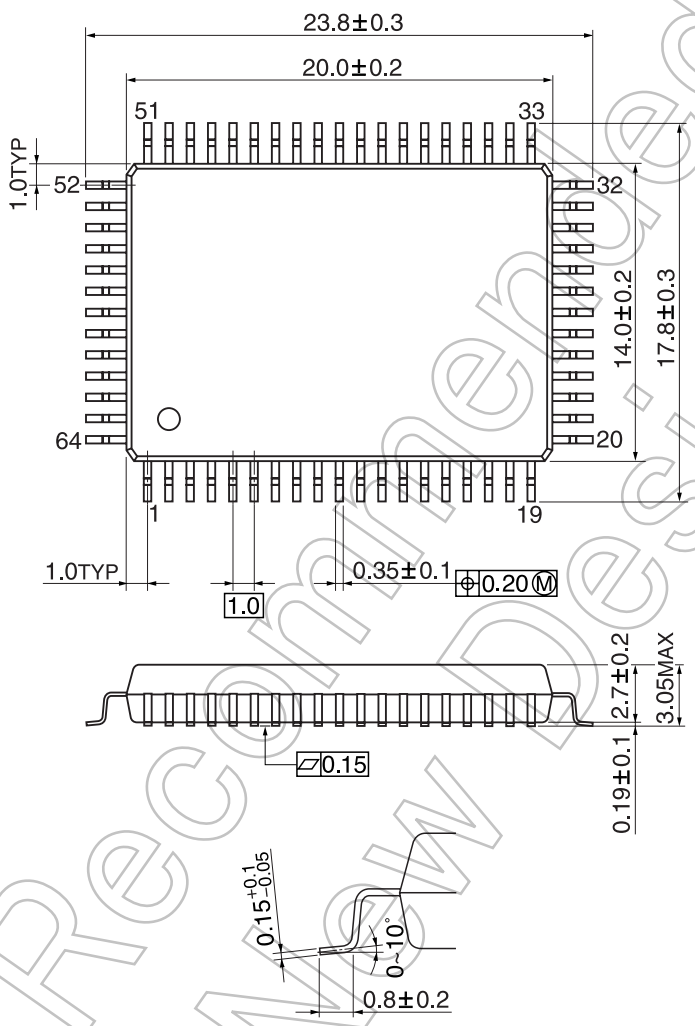
SDIP64-P-750-1.78

Unit: mm



QFP64-P-1420-1.00A

Unit: mm



CMOS 8-Bit Microcontroller

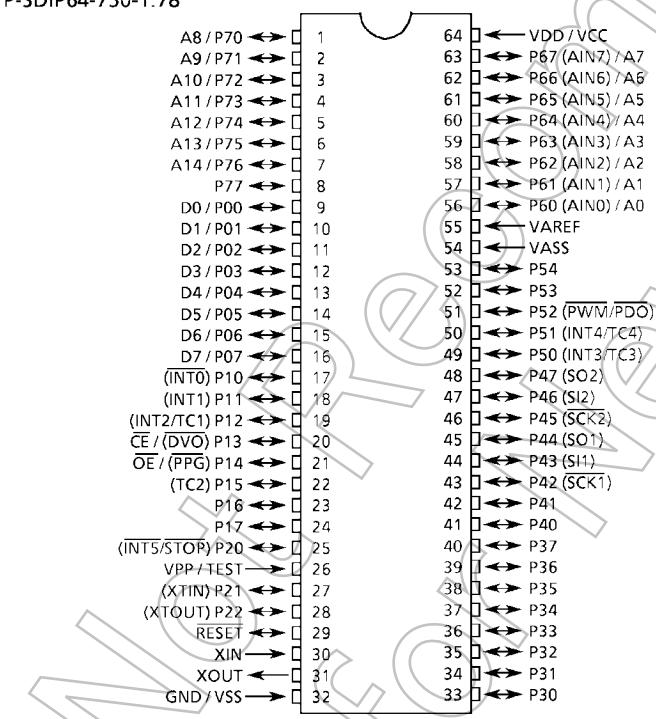
TMP87PH40AN, TMP87PH40AF, TMP87PM40AN, TMP87PM40AF

The 87PH40A is a One-Time PROM microcontroller with low-power 128 K bits (16 Kbytes) electrically programmable read only memory for the 87C840/CC40/CH40 system evaluation. The 87PM40A is a One-time PROM microcontroller with low-power 256 K bits (32 Kbytes) electrically programmable read only memory for the 87CK40A/M40A system evaluation. The 87PH40A/PM40A are pin compatible with the 87C840/CC40/CH40/CK40A/CM40A. The operations possible with the 87C840/CC40/CH40/CK40A/CM40A can be performed by writing programs to PROM. The 87PH40A/PM40A can write and verify in the same way as the TC57256AD using an adaptor socket BM1136/BM1137/BM11714 and an EPROM programmer.

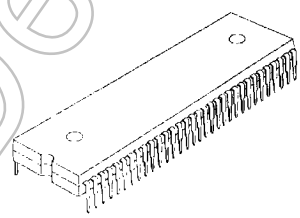
Part No	OTP	RAM	Package	Adapter socket
TMP87PH40AN	16 K × 8-bit	512 × 8-bit	P-SDIP64-750-1.78	BM1136
TMP87PH40AF			P-QFP64-1420-1.00A	BM1137
TMP87PM40AN	32 K × 8-bit	1K × 8-bit	P-SDIP64-750-1.78	BM11714
TMP87PM40AF			P-QFP64-1420-1.00A	BM1137

Pin Assignments (Top View) - (1)

P-SDIP64-750-1.78



P-SDIP64-750-1.78



TMP87PH40AN
TMP87PM40AN

980910EBP1

- For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance / Handling Precautions.
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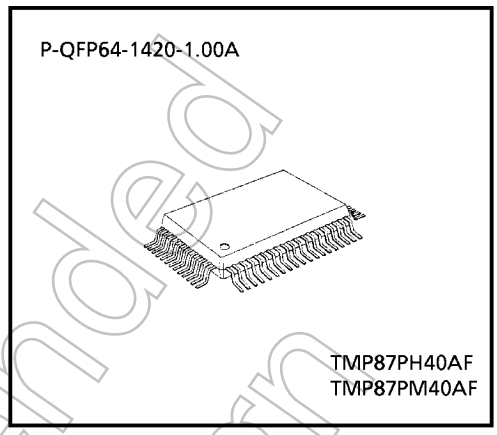
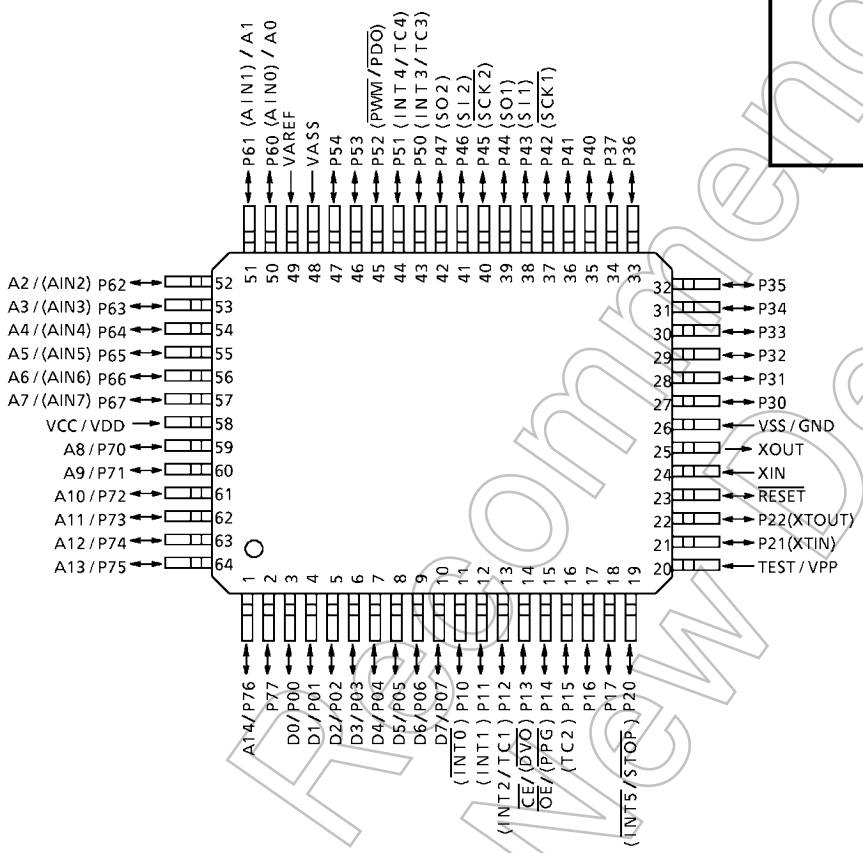
Pin Assignments (Top View) - (2)

P-QFP64-1420-1.00A





Pin Function

The 87PH40A/PM40A have two modes: MCU and PROM.

(1) MCU mode

In this mode, the 87PH40A/PM40A are pin compatible with the 87C840/CC40/CH40/CK40A/CM40A (fix the TEST pin at low level).

(2) PROM mode

Pin Name (PROM mode)	Input/Output	Functions	Pin Name (MCU mode)
A14 to A8	Input	PROM address inputs	P76 to P70
A7 to A0			P67 to P60
D7 to D0	I/O	PROM data input/outputs	P07 to P00
$\overline{CE}$	Input	Chip enable signal input (active low)	P13
$\overline{OE}$		Output enable signal input (active low)	P14
VPP	Power supply	+ 12.5V / 5V (Program supply voltage)	TEST
VCC		+ 5V	VDD
GND		0V	VSS
P37 to P30	I/O	Pull-up with resistance for input processing	
P47 to P40			
P54 to P50			
P11		PROM mode setting pins. Be fixed at high level.	
P21			
P77			
P17 to P15		PROM mode setting pins. Be fixed at low level.	
P12, P10			
P22, P20			
RESET			
XIN	Input	Connect an 8MHz or 4MHz oscillator to stabilize the internal state.	
XOUT	Output		
VAREF	Power Supply	0 V (GND)	
VASS			

Operational Description

The following explains the 87PH40A/PM40A hardware configuration and operation. The configuration and functions of the 87PH40A are the same as those of the 87C840/CC40/CH40, 87PM40A are the same as those of the 87CK40A/CM40A, except in that a one-time PROM is used instead of an on-chip mask ROM.
The 87PH40A/PM40A are placed in the single-clock mode during reset. To use the dual-clock mode, the low-frequency oscillator should be turned on by executing [SET (SYSCR2). XTEN] instruction at the beginning of the program.

1. Operating Mode

The 87PH40A/PM40A have two modes: MCU and PROM.

1.1 MCU Mode

The MCU mode is activated by fixing the TEST / VPP pin at low level.
In the MCU mode, operation is the same as with the 87C840/CC40/CH40/CK40A/CM40A (the TEST / VPP pin cannot be used open because it has no built-in pull-down resistance).

1.1.1 Program Memory

The 87PH40A has a 16 K × 8-bit (addresses $C000_H$ to $FFFF_H$ in the MCU mode, addresses 4000_H to $7FFF_H$ in the PROM mode), the 87PM40A has a 32 K × 8-bit (address 8000_H to $FFFF_H$ in the MCU mode, address 0000_H to $7FFF_H$ in the PROM mode) of program memory (OTP).
To use the 87PH40A/PM40A as the system evaluation for the 87C840/CC40/CH40/CK40A/CM40A, the program should be written to the program memory area as shown in Figure 1-1.

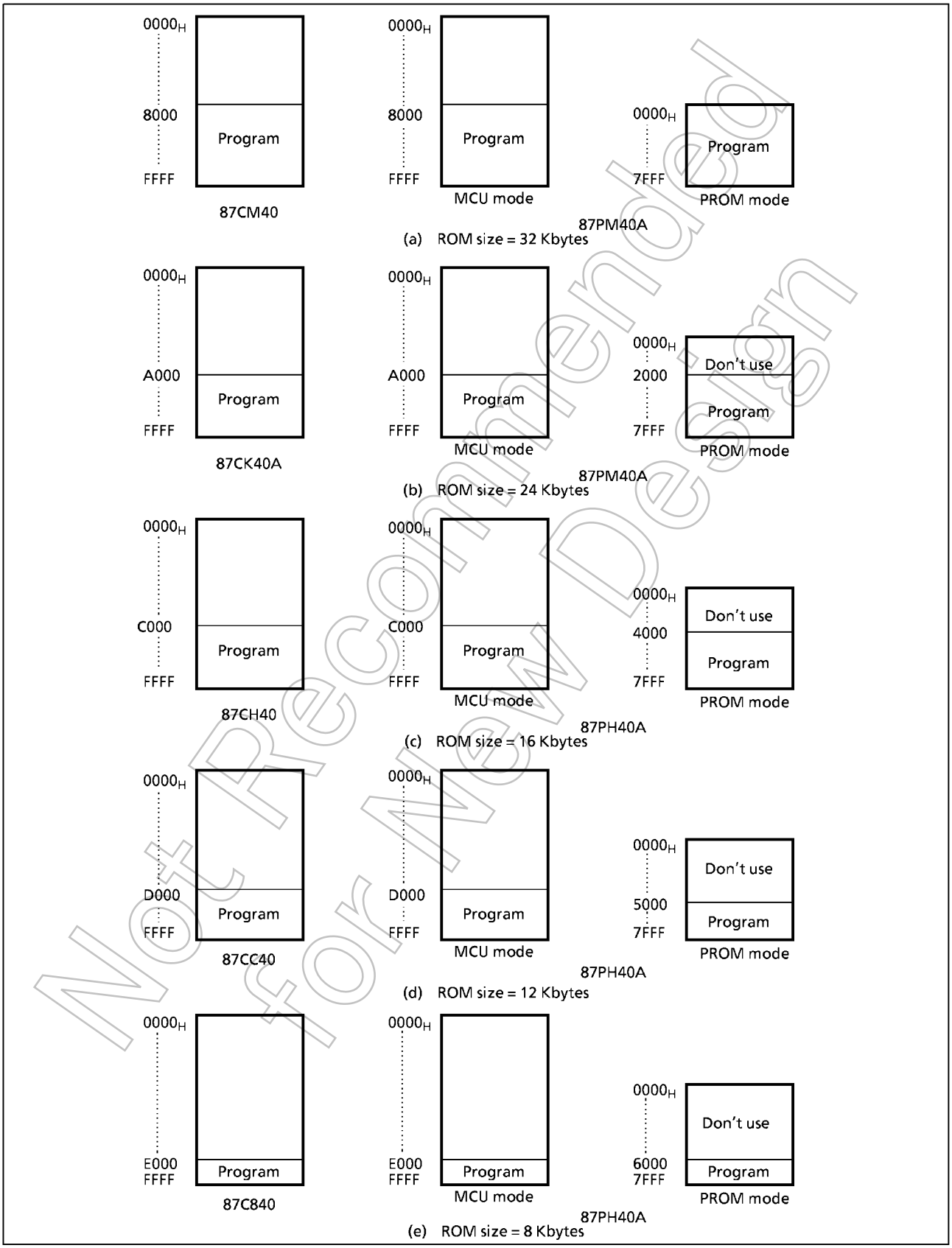


Figure 1-1. Program Memory Area

Note: Either write the data FFH to the unused area or set the PROM programmer to access only the program storage area.

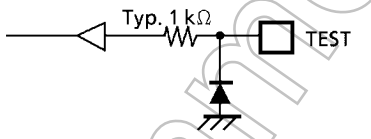
1.1.2 Data Memory

The 87PH40A has an on-chip 512 × 8-bit data memory (static RAM). The 87PM40A has an on-chip 1K × 8-bit data memory (static RAM).

1.1.3 Input/Output Circuitry

(1) Control pins

The control pins of the 87PH40A/PM40A are the same as those of the 87C840/CC40/CH40/CK40A /CM40A except that the TEST pin has is no built-in pull-down resistance.



Note: The 87PH40/PM40 does not have a pull-down resistor for TEST pin.

Figure 1-2. TEST pin

(2) I/O ports

The I/O circuitries of 87PH40A/PM40A I/O ports the are the same as the code A type I/O circuitries of the 87C840/CC40/CH40/CK40A/CM40A.

When using as an evaluator of other I/O codes (B, C, G), external pull-up resistors are required.

Figure 1-3. I/O Circuitry Code and External Circuitry

1.2 PROM Mode

The PROM mode is activated by setting the TEST, $\overline{\text{RESET}}$ pin and the ports P17-P10, P22-P20 and P77 as shown in Figure 1-4. The PROM mode is used to write and verify programs with a general-purpose PROM programmer. The high-speed programming mode can be used for program operation.

The 87PH40A/PM40A are not supported an *electric signature* mode, so the ROM type must be set to TC57256AD.

Set the adaptor socket switch to "P".

Note:	*Please set the high-speed programing mode according to each manual of PROM programmer.*

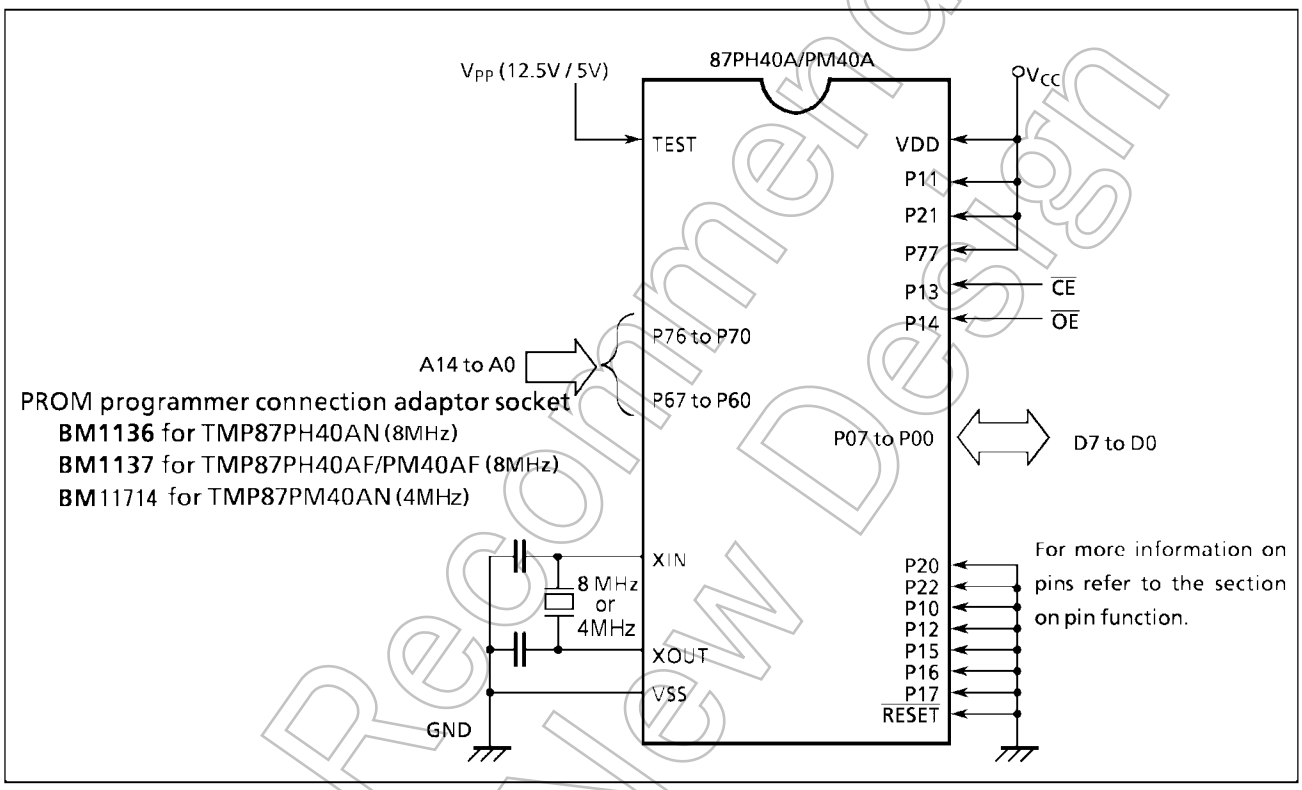


Figure 1-4. Setting for PROM Mode

1.2.1 Programming Flowchart (High-speed Programming Mode-I)

The high-speed programming mode is achieved by applying the program voltage (+ 12.5 V) to the Vpp pin when Vcc = 6 V. After the address and input data are stable, the data is programmed by applying a single 1ms program pulse to the $\overline{CE}$ input. The programmed data is verified. If incorrect, another 1ms program pulse is applied and then the programmed data is verified. This process should be repeated (up to 25 times) until the program operates correctly. Programming for one address is ended by applying additional program pulse with width 3 times that needed for initial programming (number of programmed times × 1 ms). After that, change the address and input data, and program as before. When programming has been completed, the data in all addresses should be verified with Vcc = Vpp = 5 V.

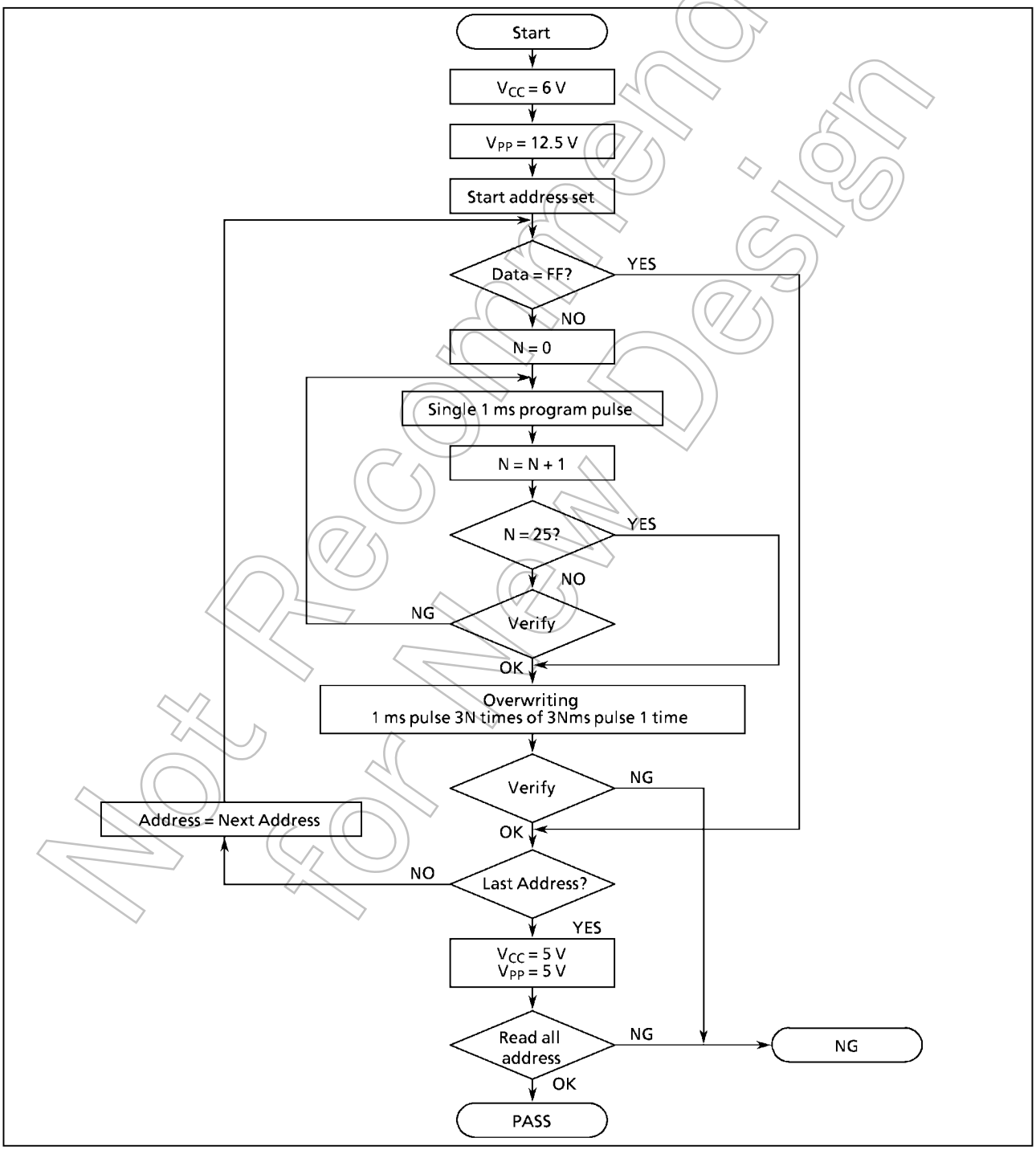


Figure 1-5. Flowchart of High-speed Programming Mode - I

1.2.2 Programming Flowchart (High-speed Programming Mode-II)

The high-speed programming mode is achieved by applying the program voltage (+ 12.75 V) to the Vpp pin when Vcc = 6.25 V. After the address and input data are stable, the data is programmed by applying a single 0.1ms program pulse to the $\overline{CE}$ input. The programmed data is verified. If incorrect, another 0.1ms program pulse is applied and then the programmed data is verified. This process should be repeated (up to 25 times) until the program operates correctly. After that, change the address and input data, and program as before. When programming has been completed, the data in all addresses should be verified with Vcc = Vpp = 5 V.

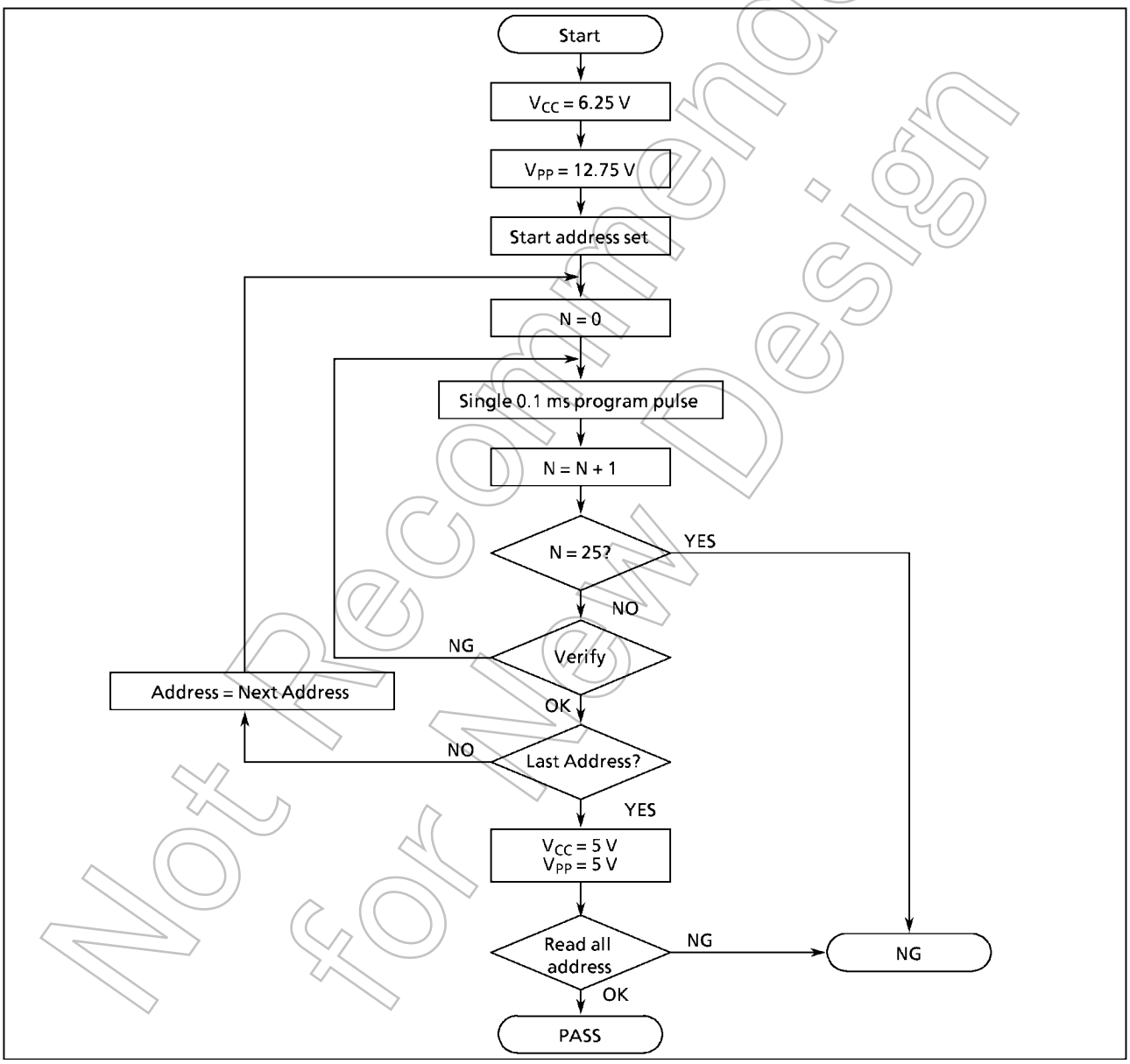


Figure 1-6. Flowchart of High-speed Programming Mode - II

1.2.3 Writing Method for General-purpose PROM Program

(1) Adapters
BM1136: TMP87PH40AN
BM1137: TMP87PH40AF, 87PM40AF
BM11714: TMP87PM40AN

(2) Adapter setting
Switch (SW1) is set to side N.

(3) PROM programmer specifying
i) PROM type is specified to TC57256AD.
Writing voltage: 12.5 V (high-speed program I mode)
12.75 V (high-speed program II mode)

ii) Data transfer (copy) (note 1)
In TMP87PH40A, EPROM is within the addresses 4000 to 7FFFH. In TMP87PM40A, EPROM is within the address 0000 to 7FFFH. Data is required to be transferred (copied) to the addresses where it is possible to write. The program area in MCU mode and PROM mode is referred to "Program memory area" in figure 1-1.

Ex. In the block transfer (copy) mode, executed as below.
ROM capacity of 16KB: transferred addresses C000 to FFFFH to addresses 4000 to 7FFFH

iii) Writing address is specified. (note 1)
TMP87PH40A: Start address: 4000H End address: 7FFFH
TMP87PM40A: Start address: 0000H End address: 7FFFH

(4) Writing
Writing/Verifying is required to be executed in accordance with PROM programmer operating procedure.

Note 1: In case of TMP87PH40A, the specifying method is referred to the PROM programmer description. The data in addresses 0000 to 3FFFH must be specified to FFH.

Note 2: When MCU is set to an adapter or the adapter is set to PROM programmer, a position of pin 1 must be adjusted. If the setting is reversed, MCU, the adapter and PROM program is damaged.

Note 3: TMP87PH40A, 87PM40A do not support the electric signature mode (hereinafter referred to as "signature"). If the signature is used in PROM program, a device is damaged due to applying 12 V ± 0.5 V to the address pin 9 (A9). The signature must not be used.

Electrical Characteristics

Absolute Maximum Ratings (V_{SS} = 0V)

Parameter	Symbol	Conditions	Ratings	Unit
Supply Voltage	V_{DD}		– 0.3 to 7	V
Program Voltage	V_{PP}	TEST / V_{PP} pin	– 0.3 to 13.0	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	Except sink open drain pin , but include P2 and $\overline{RESET}$	– 0.3 to V_{DD} + 0.3	V
	V_{OUT2}	Sink open drain pin except port P2, $\overline{RESET}$	– 0.3 to 10	
Output Current (Per 1 pin)	I_{OUT1}	Ports P0, P1, P2, P4, P5, P6, P7	3.2	mA
	I_{OUT2}	Port P3	30	
Output Current (Total)	ΣI_{OUT1}	Ports P0, P1, P2, P4, P5, P6, P7	120	mA
	ΣI_{OUT2}	Port P3	120	
Power Dissipation [Topr = 70°C]	PD	TMP87PH40AN/PM40AN	600	mW
		TMP87PH40AF/PM40AF	350	
Soldering Temperature (time)	Tsld		260 (10s)	°C
Storage Temperature	Tstg		– 55 to 125	°C
Operating Temperature	Topr		– 30 to 70	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Conditions (V_{SS} = 0V, Topr = – 30 to 70°C)

Parameter	Symbol	Pins	Conditions		Min	Max	Unit
Supply Voltage	V_{DD}		fc = 8 MHz	NORMAL1, 2 mode	4.5	6.0	V
				IDLE1, 2 mode			
			fc = 4.2 MHz	NORMAL1, 2 mode	2.7		
				IDLE1, 2 mode			
			fs = 32.768 kHz	SLOW mode			
				SLEEP mode			
				STOP mode	2.0		
Input High Voltage	V_{IH1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		$V_{DD} \times 0.70$	V_{DD}	V
	V_{IH2}	Hysteresis input			$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5$ V		$V_{DD} \times 0.90$		
Input Low Voltage	V_{IL1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		0	$V_{DD} \times 0.30$	V
	V_{IL2}	Hysteresis input				$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5$ V			$V_{DD} \times 0.10$	
Clock Frequency	fc	XIN, XOUT	V_{DD} = 4.5 to 6 V		0.4	8.0	MHz
			V_{DD} = 2.7 to 6 V			4.2	
	fs	XTIN, XTOUT			30.0	34.0	kHz

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: Clock frequency fc ; Supply voltage range is specified in NORMAL mode and IDLE mode.

D.C. Characteristics

(V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Symbol	Pins	Conditions		Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis inputs	V_{DD} = 5.0V		–	0.9	–	V
Input Current	I_{IN1}	TEST	V_{DD} = 5.5V V_{IN} = 5.5V/0V		–	–	± 2	μA
	I_{IN2}	Open drain ports and tri-state ports						
	I_{IN3}	$\overline{RESET}$, $\overline{STOP}$						
Input Resistance	R_{IN2}	$\overline{RESET}$			100	220	450	kΩ
Output Leakage Current	I_{LO1}	Open drain ports	V_{DD} = 5.5V, VOUT = 5.5V		–	–	2	μA
	I_{LO2}	Tri-state ports	V_{DD} = 5.5V, VOUT = 5.5V/0V		–	–	± 2	
Output High Voltage	V_{OH2}	Tri-state ports	V_{DD} = 4.5V, I_{OH} = – 0.7mA		4.1	–	–	V
Output Low Voltage	V_{OL}	Except XOUT and port P3	V_{DD} = 4.5V, I_{OL} = 1.6mA		–	–	0.4	V
Output Low Current	I_{OL3}	Port P3	V_{DD} = 4.5V, V_{OL} = 1.0V		–	20	–	mA
Supply Current in NORMAL 1 , 2 mode	I_{DD}		V_{DD} = 5.5V fc = 8 MHz fs = 32.768 kHz V_{IN} = 5.3V/0 .2V	87PH40A	–	9	14	mA
				87PM40A	–	12	18	
Supply Current in IDLE 1, 2 mode				87PH40A	–	4	6	mA
				87PM40A	–	4.5		
Supply Current in SLOW mode			V_{DD} = 3.0V fs = 32.768 kHz V_{IN} = 2.8V/0 .2V		–	30	60	μA
Supply Current in SLEEP mode					–	15	30	μA
Supply Current in STOP mode			V_{DD} = 5.5V V_{IN} = 5.3V/0 .2V		–	0.5	10	μA

Note1: Typical values show those at Topr = 25°C .
Note 2: Input Current I_{IN1}, I_{IN3} ; The current through pull-up or pull-down resistor is not included.
Note 3: IDD ; Except for I_{REF}

A / D Conversion Characteristics

(V_{SS} = 0 V, V_{DD} = 2.7 to 5.5 V, Topr = – 30 to 70°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}	$V_{AREF} - V_{ASS} \geqq$ 2.5 V	2.7	–	V_{DD}	V
	V_{ASS}		V_{SS}	–	1.5	
Analog Input Voltage	V_{AIN}		V_{ASS}	–	V_{AREF}	V
Analog Supply Current	I_{REF}	V_{AREF} = 5.5 V, V_{ASS} = 0.0 V	–	0.5	1.0	mA
Nonlinearity Error		V_{DD} = 5.0 V, V_{SS} = 0.0 V V_{AREF} = 5.000 V V_{ASS} = 0.000 V or V_{DD} = 2.7 V, V_{SS} = 0.0 V V_{AREF} = 2.700 V V_{ASS} = 0.000 V	–	–	± 1	LSB
Zero Point Error			–	–	± 1	
Full Scale Error			–	–	± 1	
Total Error			–	–	± 2	

Note : The above errors has no quantizing error.

A.C. Characteristics

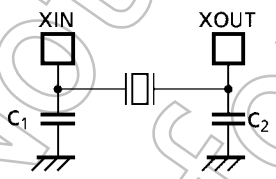
(V_{SS} = 0 V, V_{DD} = 4.5 to 6.0 V, Topr = – 30 to 70°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Machine Cycle Time	t_{cy}	In NORMAL1, 2 modes	0.5	–	10	μs
		In IDLE1, 2 modes				
		In SLOW mode	117.6	–	133.3	
		In SLEEP mode				
High Level Clock Pulse Width	t_{WCH}	For external clock operation (XIN input), fc = 8 MHz	50	–	–	ns
Low Level Clock Pulse Width	t_{WCL}					
High Level Clock Pulse Width	t_{WSH}	For external clock operation (XTIN input), fs = 32.768 kHz	14.7	–	–	μs
Low Level Clock Pulse Width	t_{WSL}					

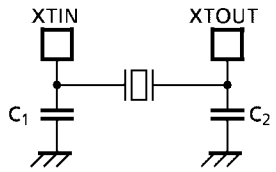
Recommended Oscillating Conditions

(V_{SS} = 0 V, V_{DD} = 4.5 to 6.0 V, Topr = – 30 to 70°C)

Parameter	Oscillator	Oscillation Frequency	Recommended Oscillator		Recommended Constant C_1	Recommended Constant C_2
High-frequency Oscillation	Ceramic Resonator	8 MHz	KYOCERA	KBR8.0M	30pF	30pF
		4 MHz	KYOCERA	KBR4.0MS		
			MURATA	CSA4.00MG		
	Crystal Oscillator	8 MHz	TOYOCOM	210B 8.0000	20pF	20pF
		4 MHz	TOYOCOM	204B 4.0000		
Low-frequency Oscillation	Crystal Oscillator	32.768 kHz	NDK	MX-38T	15pF	15pF



(1) High-frequency Oscillation



(2) Low-frequency Oscillation

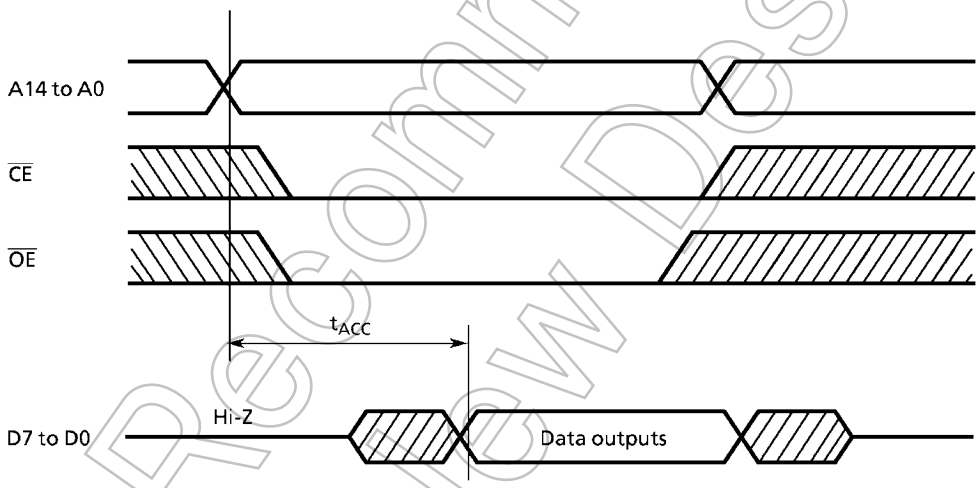
Note: When used in high electric field such as a picture tube, the package is recommended to be electrically shielded to maintain a regular operation.

D.C./A.C. Characteristics (PROM mode) (V_{SS} = 0V)

(1) Read Operation (Topr = – 30 to 70°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Input High Voltage	V_{IH4}		V_{CC} × 0.7	–	V_{CC}	V
Input Low Voltage	V_{IL4}		0	–	V_{CC} × 0.12	V
Power Supply Voltage	V_{CC}		4.75	5.00	5.25	V
Program Power Supply Voltage	V_{PP}		V_{CC} – 0.6	V_{CC}	V_{CC} + 0.6	
Address Access Time	t_{ACC}	V_{CC} = 5.0 ± 0.25V	–	1.5tcyc + 300	–	ns

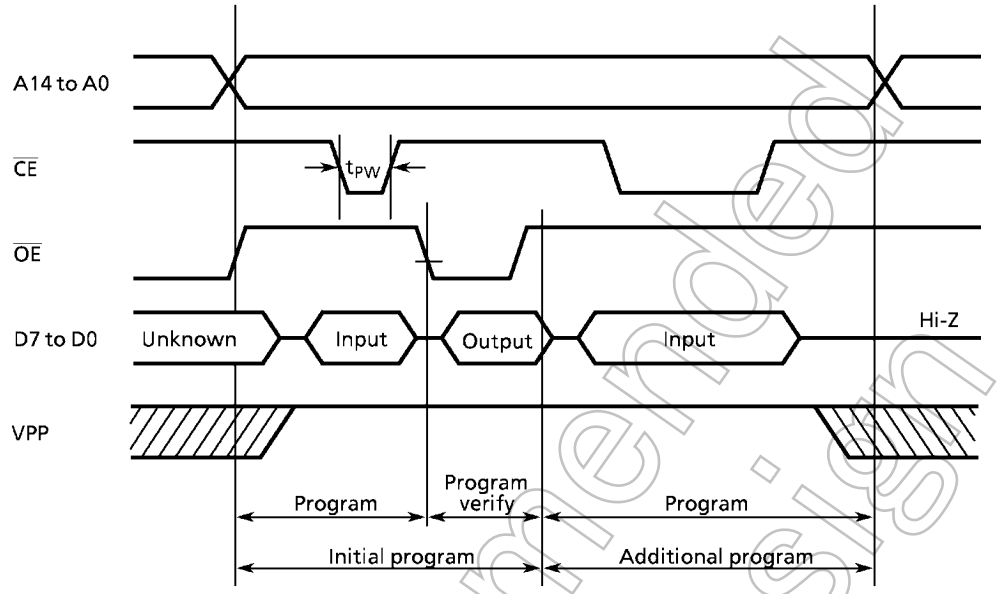
Note: tcyc = 500 ns at 8 MHz



Timing Waveforms of Read Operation

(2) Program Operation (High-Speed Write Mode - Ⅰ) (Topr = 25 ± 5°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Input High Voltage	V_{IH4}		V_{CC} × 0.7	–	V_{CC}	V
Input Low Voltage	V_{IL4}		0	–	V_{CC} × 0.12	V
Power Supply Voltage	V_{CC}		5.75	6.0	6.25	V
Program Power Supply Voltage	V_{PP}		12.0	12.5	13.0	V
Initial Program Pulse Width	t_{PW}	V_{CC} = 6.0 V ± 0.25 V, V_{PP} = 12.5 ± 0.25 V	0.95	1.0	1.05	ms

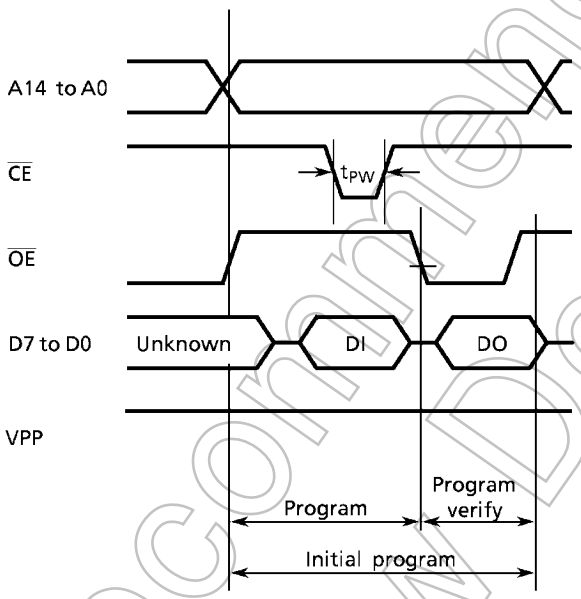


Timing Waveforms of Programming Operation

Note 1: When V_{cc} power supply is turned on or after, V_{pp} must be increased.
When V_{cc} power supply is turned off or before, V_{pp} must be decreased.
Note 2: The device must not be set to the EPROM programmer or picked up from it under applying the program voltage (12.5 V ± 0.5 V) to the V_{pp} pin as the device is damaged.
Note 3: Be sure to execute the recommended programing mode with the recommended programing adaptor. If a mode or an adaptor except the above, the misoperation sometimes occurs.

(3) Program Operation (High speed write mode - II) (Topr = 25 ± 5°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Input High Voltage	V_{IH4}		$V_{CC} \times 0.7$	–	V_{CC}	V
Input Low Voltage	V_{IL4}		0	–	$V_{CC} \times 0.12$	V
Supply Voltage	V_{CC}		6.00	6.25	6.50	V
Program Supply Voltage	V_{PP}		12.50	12.75	13.0	V
Initial Program Pulse Width	t_{PW}	V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.75 V ± 0.25 V	0.095	0.1	0.105	ms



Note: DO ; Data output (I0 to I7)
DI ; Data input (I0 to I7)

Note 1: When V_{cc} power supply is turned on or after, V_{pp} must be increased.
When V_{cc} power supply is turned off or before, V_{pp} must be decreased.
Note 2: The device must not be set to the EPROM programmer or picked up from it under applying the program voltage (12.75 V ± 0.25 V) to the V_{pp} pin as the device is damaged.
Note 3: Be sure to execute the recommended programing mode with the recommended programing adaptor. If a mode or an adaptor except the above, the misoperation sometimes occurs.