TOSHIBA

TOSHIBA Original CMOS 8-Bit Microcontroller

TLCS-870 Series

TMP87PH48UG
TMP87PH48DFG
TMP87PM48UG
TMP87PM48DFG

TOSHIBA CORPORATION

Semiconductor Company

Important Notices

Thank you for your continued patronage of Toshiba microcontrollers.

This page gives you important information on using Toshiba microcontrollers. Please be sure to check each item for proper use of our products.

TOSHIBA Microcontrollers
870 Family
(TMP87CH48U) (TMP87CH48DF) (TMP87CM48U) (TMP87CM48DF) (TMP87CH48I)
(TMP87PH48U) (TMP87PH48DF) (TMP87PM48U) (TMP87PM48DF)

Datasheet Modifications: I²C Bus Mode Control

The following problem is included in the explanation of the I²C bus function of this data sheet.
It will guide the correction as follows. Please read it for the explanation of this data sheet as follows.

Section: "I²C Bus Mode Control"

▪ In the explanation of the Serial Bus Interface Control Register 1

1. Delete the setting examples where the serial clock frequency exceeds 100 kHz.
2. Add the following note.

SCK	Serial clock selection	000 : Reserved (Note) 001 : Reserved (Note) 010 : 58.8 kHz 011 : 30.3 kHz 100 : 15.4 kHz 101 : 7.75 kHz 110 : 3.89 kHz 111 : reserved	at fc = 8MHz (Output on SCL pin)	Write-only

Note: This I²C bus circuit does not support the Fast mode. It supports the Standard mode only. Although the I²C bus circuit itself allows the setting of a baud rate over 100 kbps, the compliance with the I²C specification is not guaranteed in that case.

▪ In "(3) Serial clock"

1. Add the following sentence about the communication baud rate.

a. Clock source

The SCK (bits 2 to 0 in the SBICR1) is used to select a maximum transfer frequency outputed on the SCL pin in the master mode. Set a communication baud rate that meets the I²C bus specification, such as the shortest pulse width of t_{LOW}, based on the equations shown below.

In both master mode and slave mode, a pulse width of at least 4 machine cycles is require for both "H" and "L" levels.

$t_{LOW} = 2^n/f_c$
$t_{HIGH} = 2^n/f_c + 8/f_c$
$fscl = 1/(t_{Low} + t_{HIGH})$

Document Change Notification

The purpose of this notification is to inform customers about the launch of the Pb-free version of the device. The introduction of a Pb-free replacement affects the datasheet. Please understand that this notification is intended as a temporary substitute for a revision of the datasheet.

Changes to the datasheet may include the following, though not all of them may apply to this particular device.

1. Part number

   Example: TMPxxxxxxF → TMPxxxxxxFG

   All references to the previous part number were left unchanged in body text. The new part number is indicated on the prelims pages (cover page and this notification).

2. Package code and package dimensions

   Example: LQFP100-P-1414-0.50C → LQFP100-P-1414-0.50F

   All references to the previous package code and package dimensions were left unchanged in body text. The new ones are indicated on the prelims pages.

3. Addition of notes on lead solderability

   Now that the device is Pb-free, notes on lead solderability have been added.

4. RESTRICTIONS ON PRODUCT USE

   The previous (obsolete) provision might be left unchanged on page 1 of body text. A new replacement is included on the next page.

5. Publication date of the datasheet

   The publication date at the lower right corner of the prelims pages applies to the new device.

1. Part number

2. Package code and dimensions

Previous Part Number (in Body Text)	Previous Package Code (in Body Text)	New Part Number	New Package Code	OTP
TMP87PH48U	P-LQFP64-1010-0.50	TMP87PH48UG	LQFP64-P-1010-0.50E	—
TMP87PH48DF	P-QFP64-1414-0.80A	TMP87PH48DFG	QFP64-P-1414-0.80C	—
TMP87PM48U	P-LQFP64-1010-0.50	TMP87PM48UG	LQFP64-P-1010-0.50E	—
TMP87PM48DF	P-QFP64-1414-0.80A	TMP87PM48DFG	QFP64-P-1414-0.80C	—

*: For the dimensions of the new package, see the attached Package Dimensions diagram.

3. Addition of notes on lead solderability

The following solderability test is conducted on the new device.

Lead solderability of Pb-free devices (with the G suffix)

Test	Test Conditions	Remark
Solderability	(1) Use of Lead (Pb) ·solder bath temperature = 230°C ·dipping time = 5 seconds ·the number of times = once ·use of R-type flux (2) Use of Lead (Pb)-Free ·solder bath temperature = 245°C ·dipping time = 5 seconds ·the number of times = once ·use of R-type flux	Leads with over 95% solder coverage till lead forming are acceptable.

4. RESTRICTIONS ON PRODUCT USE

The following replaces the "RESTRICTIONS ON PRODUCT USE" on page 1 of body text.

RESTRICTIONS ON PRODUCT USE 20070701-EN

- The information contained herein is subject to change without notice.
- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.
  In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the "Handling Guide for Semiconductor Devices," or "TOSHIBA Semiconductor Reliability Handbook" etc.
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- For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance/Handling Precautions.

5. Publication date of the datasheet

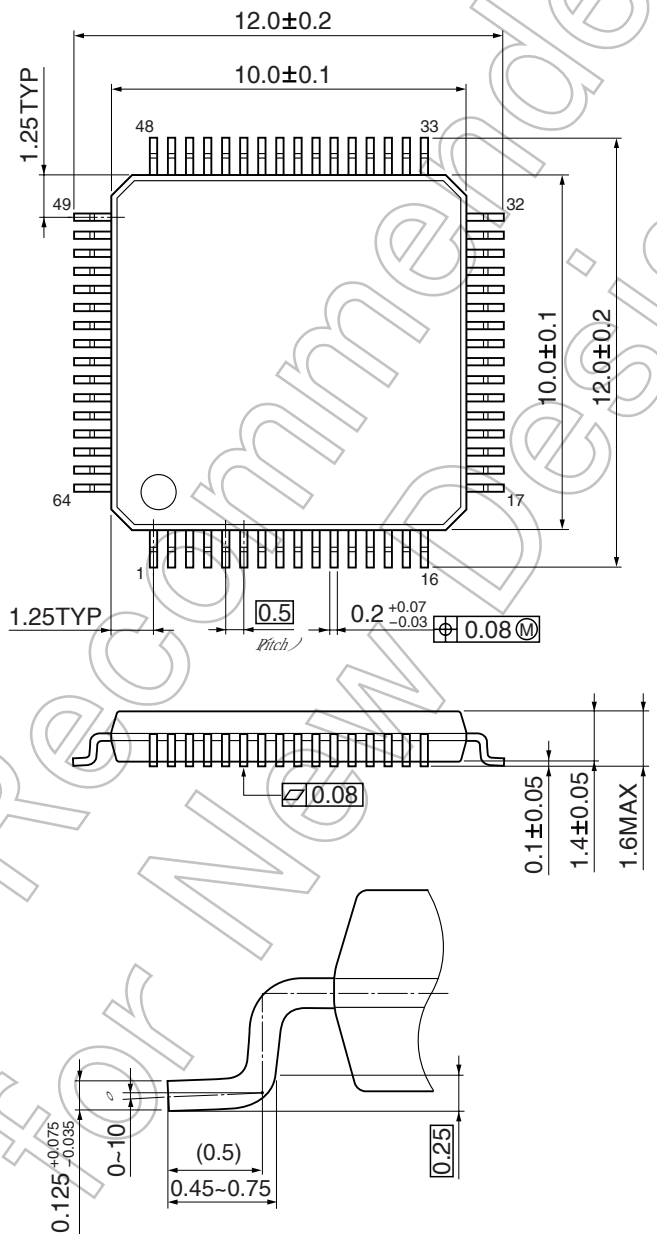
The publication date of this datasheet is printed at the lower right corner of this notification.

(Annex)

Package Dimensions

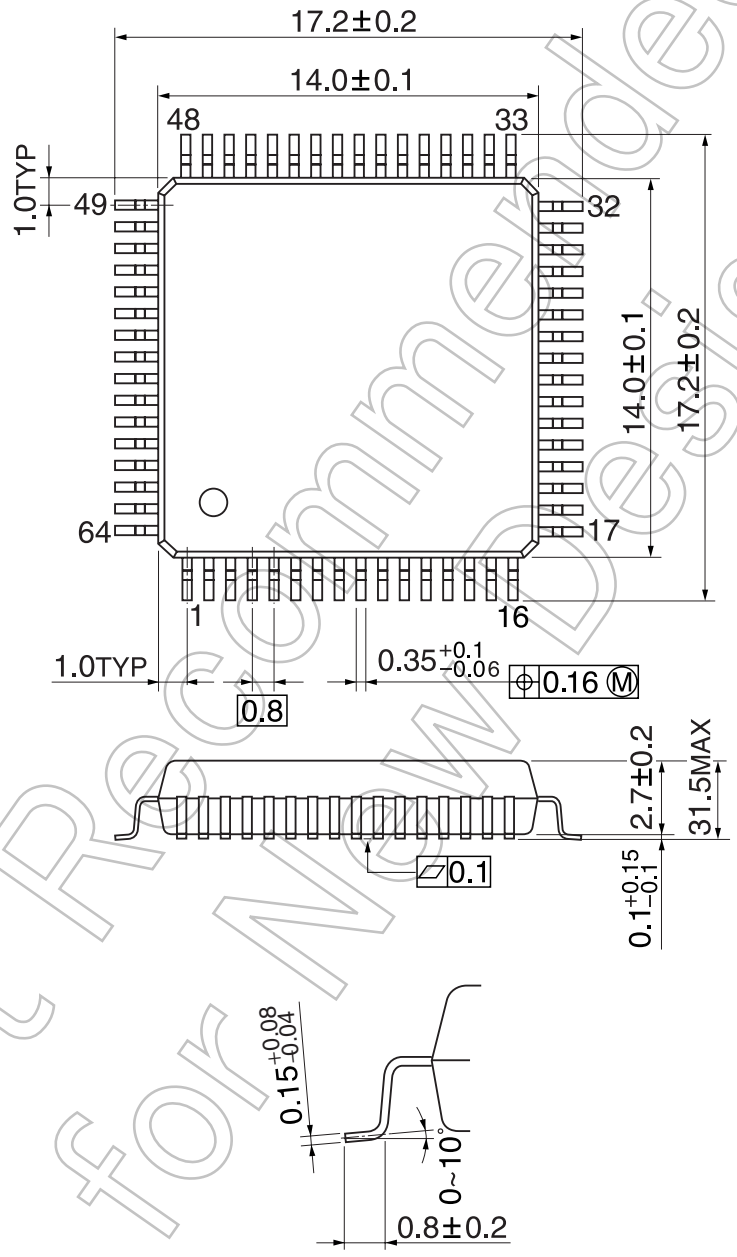
LQFP64-P-1010-0.50E

Unit: mm



QFP64-P-1414-0.80C

Unit: mm



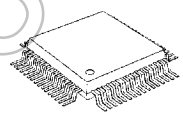
CMOS 8-Bit Microcontroller

TMP87PH48U/DF, TMP87PM48U/DF

The TMP87PH48 is a one-time PROM microcontroller with low-power 128 Kbits (16 Kbytes) electrically programmable read only memory for the TMP87CH48 system evaluation. The TMP87PM48 is a One-time PROM microcontroller with low-power 256 Kbits (32 Kbytes) electrically programmable read only memory for the TMP87CM48 system evaluation. The TMP87PH48/PM48 are pin compatible with the TMP87CH48/CM48. The operations possible with the TMP87CH48/CM48 can be performed by writing programs to PROM. The TMP87PH48/PM48 can write and verify in the same way as the TC57256AD using an adaptor sockets BM11117/BM11147 and an EPROM programmer.

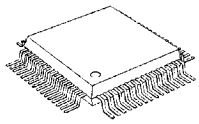
Product No.	ROM	RAM	Package	Adapter Socket
TMP87PH48U	16 K × 8 bits	512 × 8 bits	P-LQFP64-1010-0.50	BM11117
TMP87PH48DF			P-QFP64-1414-0.80A	BM11147
TMP87PM48U	32 K × 8 bits	1 K × 8 bits	P-LQFP64-1010-0.50	BM11117
TMP87PM48DF			P-QFP64-1414-0.80A	BM11147

P-LQFP64-1010-0.50



TMP87PH48U
TMP87PM48U

P-QFP64-1414-0.80A

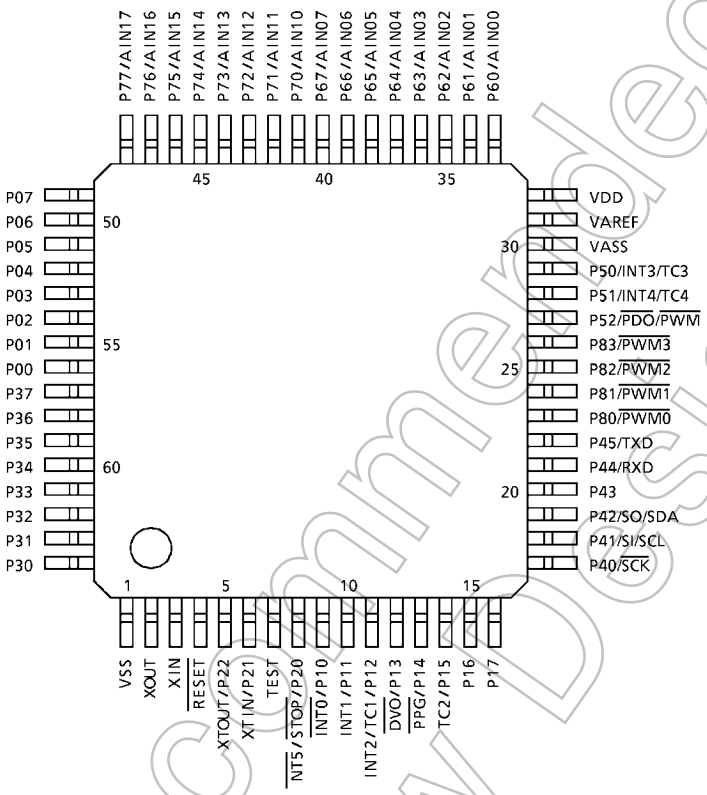


TMP87PH48DF
TMP87PM48DF

030619EBP2

Pin Assignments (Top View)

P-LQFP64-1010-0.50
P-QFP64-1414-0.80A



Pin Function

The TMP87PH48/PM48 have two modes: MCU and PROM.

(1) MCU mode

In this mode, the TMP87PH48/PM48 are pin compatible with the TMP87CH48/CM48 (Fix the TEST pin at low level).

(2) PROM mode

Pin Name (PROM mode)	Input/Output	Functions	Pin Name (MCU mode)
A14 to A8	Input	PROM address inputs	P76 to P70
A7 to A0			P81, P80, P45 to P40
D7 to D0	I/O	PROM data input/outputs	P07 to P00
$\overline{CE}$	Input	Chip enable signal input (active low)	P13
$\overline{OE}$		Output enable signal input (active low)	P14
VPP	Power supply	+ 12.5 V/5 V (Program supply voltage)	TEST
VCC		+ 5 V	VDD
GND		0 V	VSS
P37 to P34	I/O	Open	
P32 to P30			
P52 to P50		Pull-up with resistance R1 for input processing	
P83, P82			
P67 to P60			
P11, P12, P15	I/O	PROM mode setting pins. Be fixed at high level. (Pull-up with resistance R2)	
P21			
P77			
P17, P16, P10		PROM mode setting pins. Be fixed at low level.	
P133			
P22, P20			
RESET			
XIN	Input	Connect an 8 MHz oscillator to stabilize the internal state.	
XOUT	Output		
VAREF	Power Supply	0 V (GND)	
VASS			

Operational Description

The following explains the TMP87PH48/PM48 hardware configuration and operation. The configuration and functions of the TMP87PH48/PM48 are the same as those of the TMP87CH48/CM48, except in that a one-time PROM is used instead of an on-chip mask ROM.

The TMP87PH48/PM48 are placed in the *single-clock* mode during reset. To use the dual-clock mode, the low-frequency oscillator should be turned on by executing [SET (SYSCR2). XTEN] instruction at the beginning of the program.

1. Operating Mode

The TMP87PH48/PM48 have two modes: MCU and PROM.

1.1 MCU Mode

The MCU mode is activated by fixing the TEST/VPP pin at low level.

In the MCU mode, operation is the same as with the TMP87CH48/CM48 (The TEST/VPP pin cannot be used open because TMP87PH48/PM48 have no built-in pull-down resistance).

1.1.1 Program Memory

The TMP87PH48/PM48 have a 16K × 8-bit (Addresses $C000_H$ to $FFFF_H$ in the MCU mode, addresses 4000_H to $7FFF_H$ in the PROM mode) the TMP87PM48 has a 32K × 8 bit (Address 8000_H to $FFFF_H$ in the MCU mode, addresses 0000_H to $7FFF_H$ in the PROM mode) of program memory (OTP).

To use the TMP87PH48/PM48 as the system evaluation for the TMP87CH48/CM48, the program should be written to the program memory area as shown in Figure 1-1.

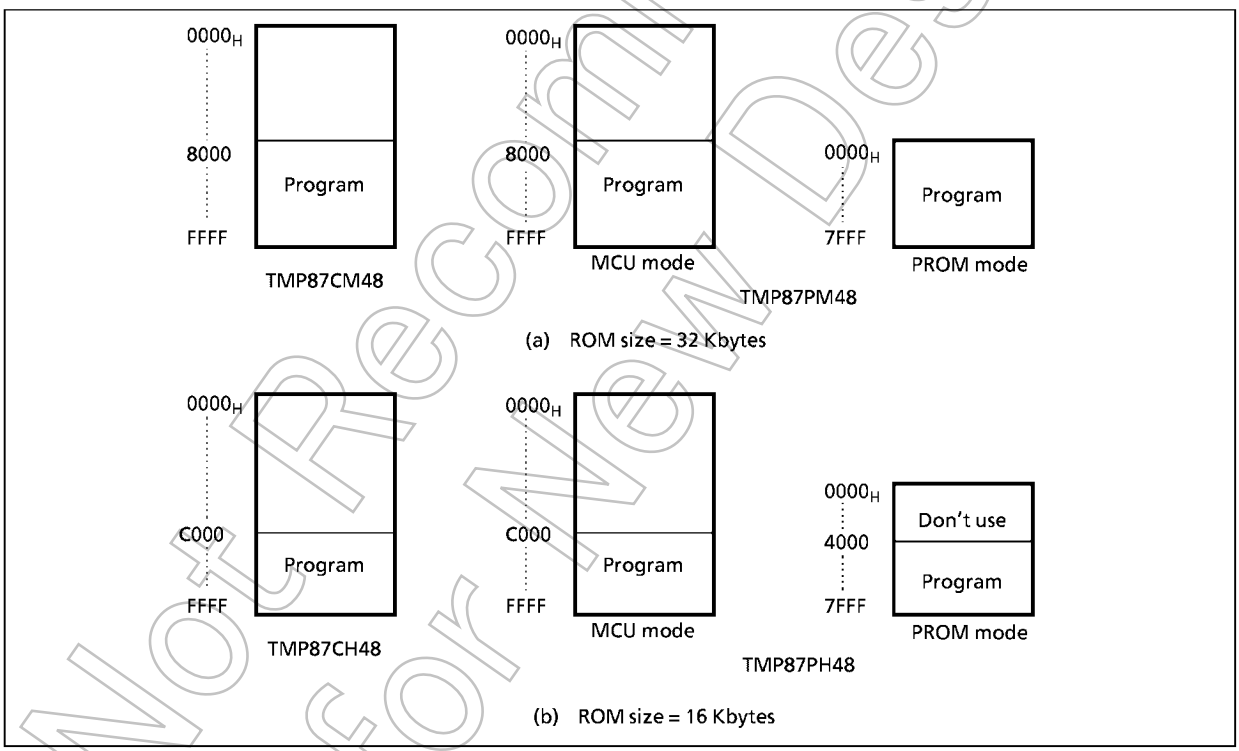


Figure 1-1. Program Memory Area

Note: Either write the data FF_H to the unused area or set the PROM programmer to access only the program storage area.

1.1.2 Data Memory

The TMP87PH48 have an on-chip 512 × 8-bit data memory (Static RAM).
The TMP87PM48 have an on-chip 1K × 8-bit data memory (Static RAM).

1.1.3 Input/Output Circuitry

(1) Control pins

The control pins of the TMP87PH48/PM48 are the same as those of the TMP87CH48/CM48 except that the TEST pin has no built-in pull-down resistance.

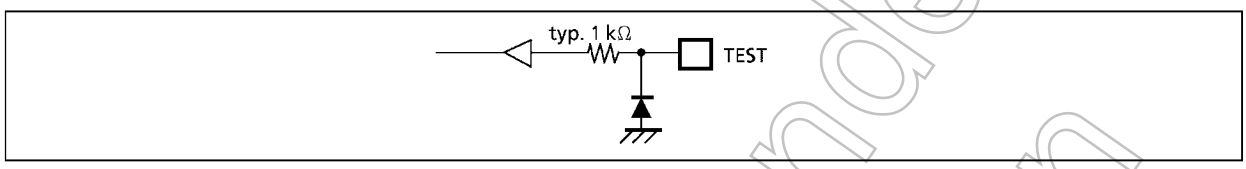


Figure 1-2. TEST Pin

(2) I/O ports

The I/O circuitries of TMP87PH48/PM48 I/O ports are the same as the TMP87CH48/CM48.

1.2 PROM Mode

The PROM mode is activated by setting the TEST, $\overline{\text{RESET}}$ pin and the ports P17 to P10, P22 to P20 and P77 as shown in Figure 1-3. The PROM mode is used to write and verify programs with a general-purpose PROM programmer.

The high-speed programming mode can be used for program operation. The TMP87PH48/PM48 are not supported an *electric signature* mode, so the ROM type must be set to TC57256AD AD.

Set the adaptor socket switch to "N".

Note: Please set the high-speed programming mode according to each manual of PROM programmer.

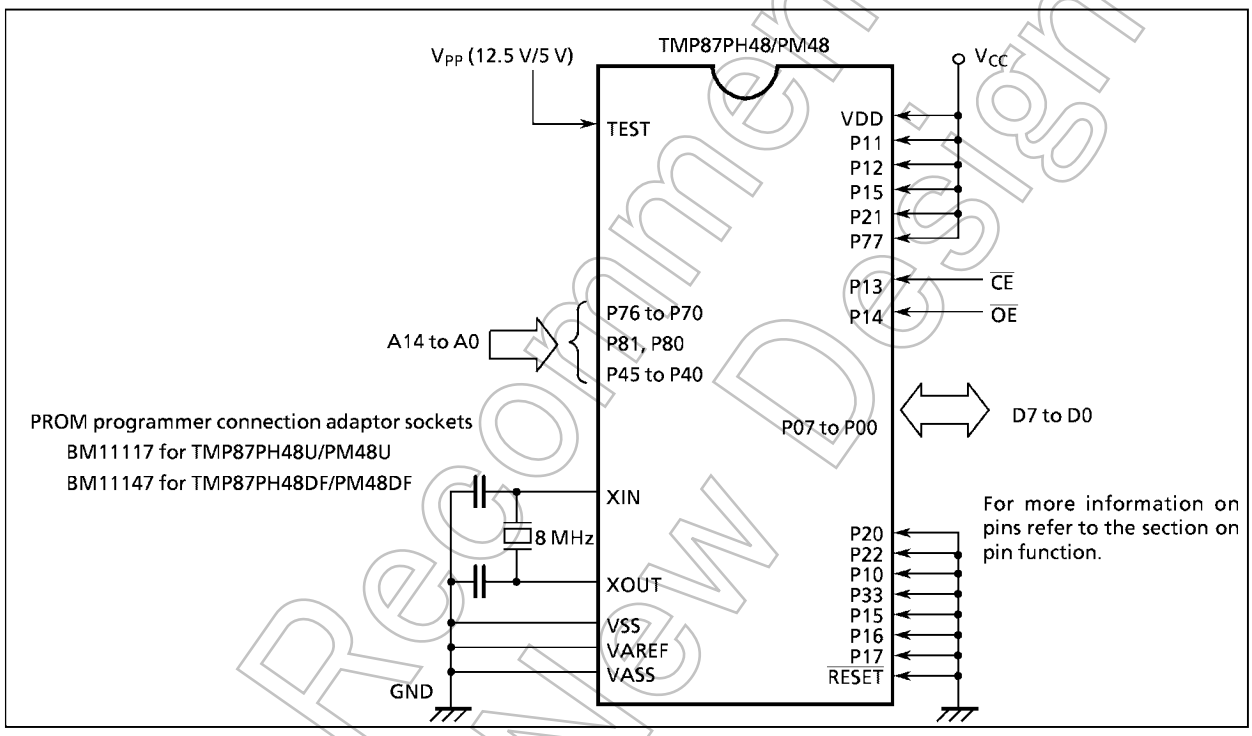


Figure 1-3. Setting for PROM Mode

1.2.1 Programming Flowchart (High-speed programming mode-I)

The high-speed programming mode is achieved by applying the program voltage (+ 12.5 V) to the Vpp pin when Vcc = 6 V. After the address and input data are stable, the data is programmed by applying a single 1ms program pulse to the $\overline{CE}$ input. The programmed data is verified. If incorrect, another 1ms program pulse is applied and then the programmed data is verified. This process should be repeated (Up to 25 times) until the program operates correctly. Programming for one address is ended by applying additional program pulse with width 3 times that needed for initial programming (Number of programmed times × 1 ms). After that, change the address and input data, and program as before. When programming has been completed, the data in all addresses should be verified with Vcc = Vpp = 5 V.

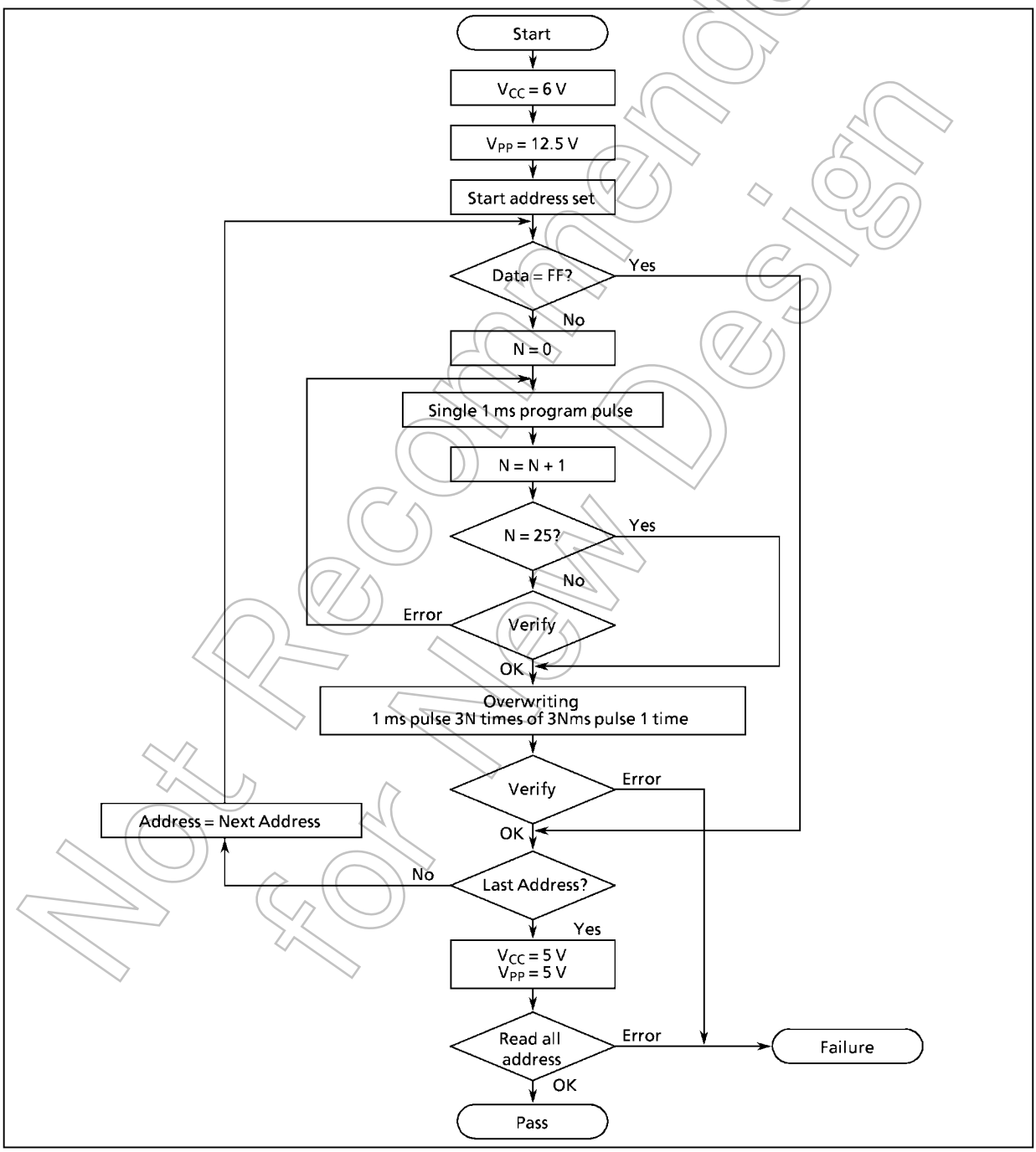


Figure 1-4. Flowchart of High-speed Programming Mode - I

1.2.2 Programming Flowchart (High-speed programming mode-II)

The high-speed programming mode is achieved by applying the program voltage (+ 12.75 V) to the Vpp pin when Vcc = 6.25 V. After the address and input data are stable, the data is programmed by applying a single 0.1ms program pulse to the $\overline{CE}$ input. The programmed data is verified. If incorrect, another 0.1ms program pulse is applied and then the programmed data is verified. This process should be repeated (Up to 25 times) until the program operates correctly. After that, change the address and input data, and program as before. When programming has been completed, the data in all addresses should be verified with Vcc = Vpp = 5 V.

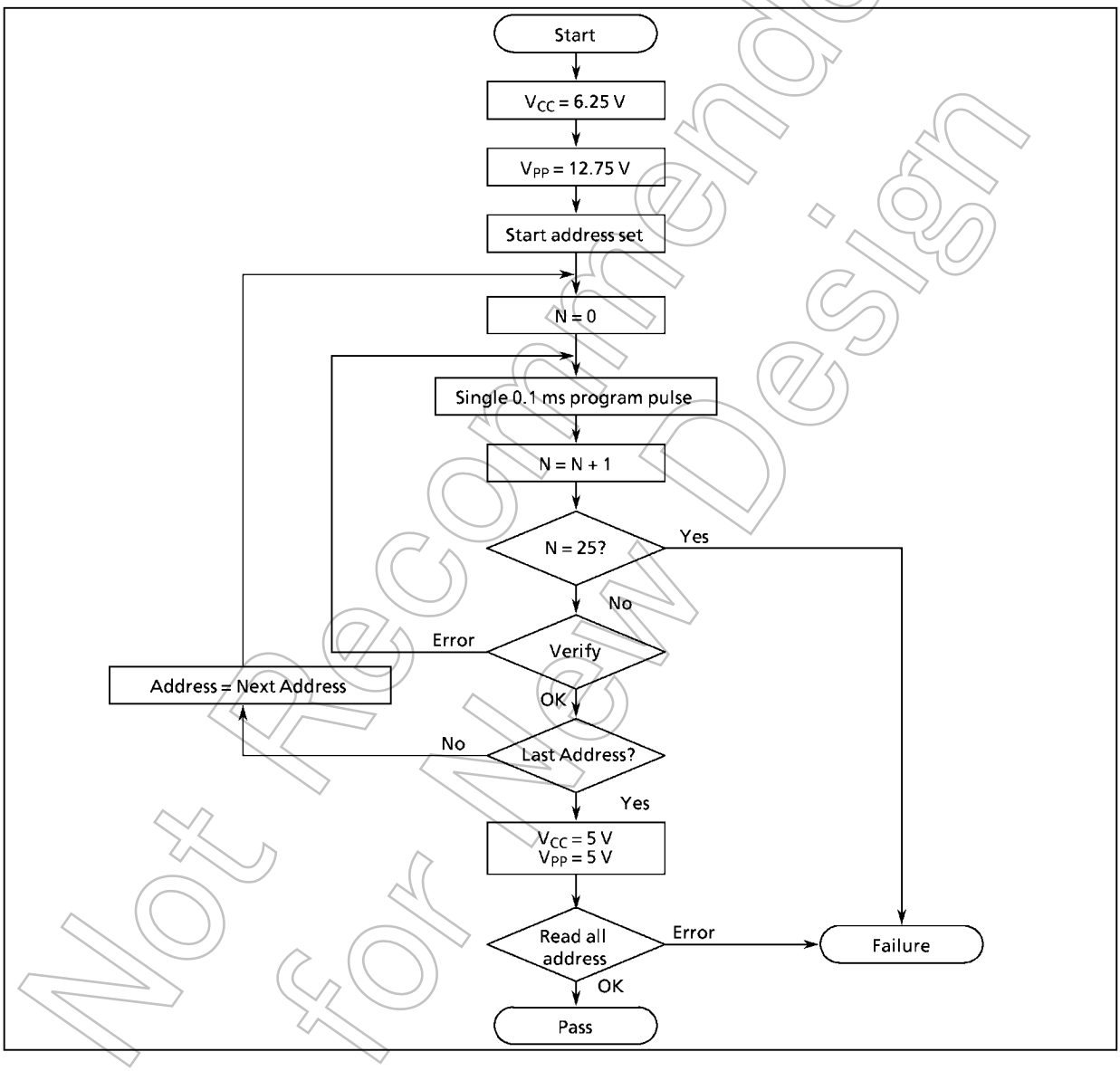


Figure 1-5. Flowchart of High-speed Programming Mode - II

1.2.3 Writing Method for General-purpose PROM Program

(1) Adapters
BM11117: TMP87PH48U, TMP87PM48U
BM11147: TMP87PH48DF, TMP87PM48DF

(2) Adapter setting
Switch (SW1) is set to side N.

(3) PROM programmer specifying
i) PROM type is specified to TC57256AD.
Writing voltage: 12.5 V (High-speed program I mode)
12.75 V (High-speed program II mode)

ii) Data transfer (Copy) (Note 1)
In TMP87PH48, EPROM is within the addresses 4000 to 7FFFH. In TMP87PM48, EPROM is within the addresses 0000 to FFFH. Data is required to be transferred (Copied) to the addresses where it is possible to write. The program area in MCU mode and PROM mode is referred to "Program memory area" in figure 1-1.

Ex. In the block transfer (Copy) mode, executed as below.
ROM capacity of 16KB: transferred addresses C000 to FFFFH to addresses 4000 to 7FFFH

iii) Writing address is specified (Note 1)
TMP87PH48: Start address: 4000H End address: 7FFFH
TMP87PM48: Start address: 0000H End address: 7FFFH

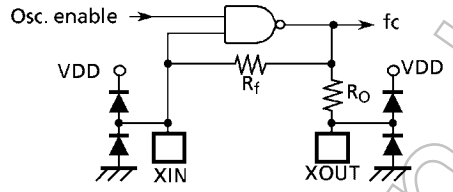
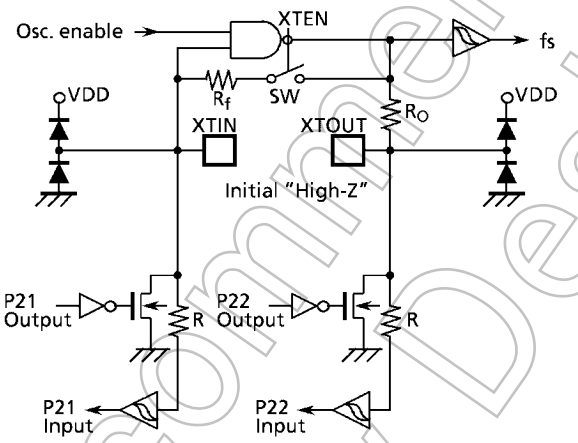
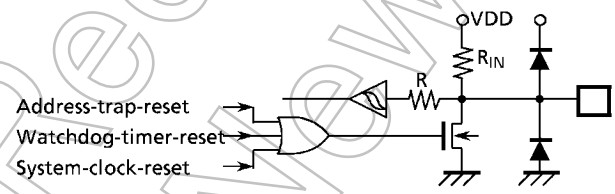
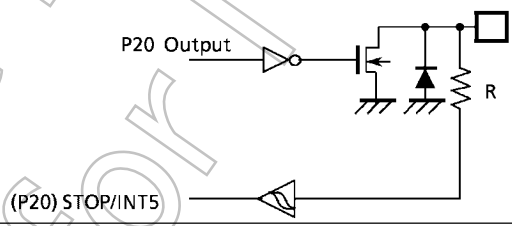
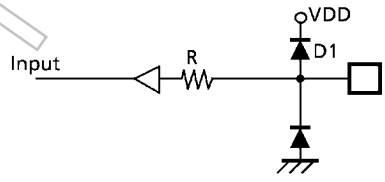
(4) Writing
Writing/Verifying is required to be executed in accordance with PROM programmer operating procedure.

Note 1: The specifying method is referred to the PROM programmer description. The data in addresses 0000 to 3FFFH must be specified to FFH.
Note 2: When MCU is set to an adapter or the adapter is set to PROM programmer, a position of pin 1 must be adjusted. If the setting is reversed, MCU, the adapter and PROM program is damaged.
Note 3: TMP87PH48, TMP87PM48 don't support the electric signature mode (Hereinafter referred to as "signature"). If the signature is used in PROM program, a device is damaged due to applying 12V ± 0.5V to the address pin 9 (A9). The signature must not be used.

Input/Output Circuitry

(1) Control pins

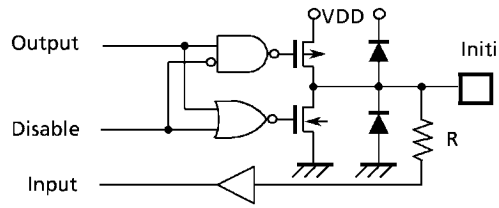
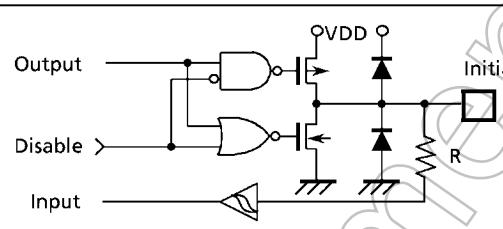
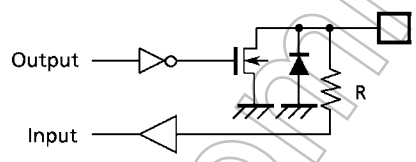
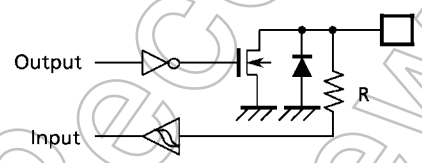
The input/output circuitries of the TMP87PH48/PM48 control pins are shown below.

Control Pin	I/O	Input/Output Circuitry	Remarks
XIN XOUT	Input Output		Resonator connecting pins (high-frequency) R_f = 1.2 MΩ (typ.) R_O = 1.5 kΩ (typ.)
XTIN XTOUT	Input Output		XTIN, XTOUT Resonator connecting pins (low-frequency) R_f = 6 MΩ (typ.) R_O = 220 kΩ (typ.) XTEN (Initial: 0) SW (XTEN = 0: OFF) (XTEN = 1: ON)
P21 P22	I/O I/O		P21, P22 Sink open drain output Hysteresis input R = 1 kΩ (typ.)
RESET	I/O		Sink open drain output Hysteresis input Pull-up resistor R_{IN} = 220 kΩ (typ.) R = 1 kΩ (typ.)
STOP/INT5 (P20)	I/O		Hysteresis input R = 1 kΩ (typ.)
TEST	Input		R = 1 kΩ (typ.)

Note 1: The TMP87PH48/PM48 don't have a pull-down resistor (R_{IN}) and a diode (D_1) for TEST pin.
Note 2: The TMP87PH48/PM48/CH48/CM48 are placed in the single-clock mode during reset.

(2) Input/Output Ports

The input/output circuitries of the TMP87PH48/PM48 input/output ports are shown below.

Port	I/O	Input/Output Circuitry	Remarks
P0 P6 P7 P8	I/O		Tri-state I/O R = 1 kΩ (typ.)
P1	I/O		Tri-state I/O Hysteresis input R = 1 kΩ (typ.)
P3	I/O		Hligh current output only P3 Sink open drain output R = 1 kΩ (typ.)
P4 P5	I/O		Sink open drain output Hysteresis input R = 1 kΩ (typ.)

Electrical Characteristics

(1) TMP87PH48

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		– 0.3 to 6.5	V
Input voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output voltage	V_{OUT}		– 0.3 to V_{DD} + 0.3	V
Output current (Per 1 pin)	I_{OUT1}	Ports P0, P1, P2, P4, P5, P6, P7, P8	3.2	mA
	I_{OUT2}	Port P3	30	
Output current (Total)	ΣI_{OUT1}	Ports P0, P1, P2, P4, P5, P6, P7, P8	120	mA
	ΣI_{OUT2}	Port P3	120	
Power dissipation	PD		350	mW
Soldering temperature (Time)	Tsld		260 (10 s)	°C
Storage temperature	Tstg		– 55 to 125	°C
Operating temperature	Topr		– 40 to 85	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Conditions (V_{SS} = 0 V, Topr = – 40 to 85°C)

Parameter	Symbol	Pins	Conditions		Min	Max	Unit
Supply voltage	V_{DD}		fc = 8 MHz	NORMAL1/2 modes	4.5	5.5	V
				IDLE1/2 modes			
			fc = 4.2 MHz	NORMAL1/2 modes	2.7		
				IDLE1/2 modes			
			f_s = 32.768 kHz	SLOW mode			
				SLEEP mode			
				STOP mode	2.0		
Input high voltage	V_{IH1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		V_{DD} × 0.70	V_{DD}	V
	V_{IH2}	Hysteresis input			V_{DD} × 0.75		
	V_{IH3}		$V_{DD} < 4.5$ V		V_{DD} × 0.90		
Input low voltage	V_{IL1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		0	V_{DD} × 0.30	V
	V_{IL2}	Hysteresis input				V_{DD} × 0.25	
	V_{IL3}		$V_{DD} < 4.5$ V			V_{DD} × 0.10	
Clock frequency	fc	XIN, XOUT	V_{DD} = 4.5 to 5.5 V		0.4	8.0	MHz
			V_{DD} = 2.7 to 5.5 V			4.2	
	fs	XTIN, XTOUT			30.0	34.0	kHz

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (Supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: The condition of clock frequency is in NORMAL1/2 modes and IDLE1/2 modes.

DC Characteristics

(V_{SS} = 0 V, Topr = – 40 to 85°C)

Parameter	Symbol	Pins	Conditions	Min	Typ.	Max	Unit
Hysteresis voltage	V_{HS}	Hysteresis inputs	VDD = 5.0 V	–	0.9	–	V
Input current	I_{IN1}	TEST	VDD = 5.5 V V_{IN} = 5.5 V/0 V	–	–	± 2	μA
	I_{IN2}	Open drain ports, Tri-state ports					
	I_{IN3}	$\overline{RESET}$, $\overline{STOP}$					
Input resistance	R_{IN2}	$\overline{RESET}$	VDD = 5.0 V	100	220	450	kΩ
Output leakage current	I_{LO}	Sink open drain ports	V_{DD} = 5.5 V, V_{OUT} = 5.5 V	–	–	2	μA
		Tri-state ports	V_{DD} = 5.5 V, V_{OUT} = 5.5/0 V	–	–	± 2	
Output high voltage	V_{OH2}	Tri-state ports	V_{DD} = 4.5 V, I_{OH} = – 0.7 mA	4.1	–	–	V
Output low voltage	V_{OL}	Except for XOUT and P3	V_{DD} = 4.5 V, I_{OL} = 1.6 mA	–	–	0.4	mA
Output low current	I_{OL3}	P3	V_{DD} = 4.5 V, V_{OL} = 1.0 V	–	20	–	mA
Supply current in NORMAL 1, 2 modes	I_{DD}		V_{DD} = 5.5 V V_{IN} = 5.3 V/0.2 V fc = 8 MHz fs = 32.768 kHz	–	4.5	5.5	mA
Supply current in IDLE 1, 2 modes				–	2.5	4.0	mA
Supply current in NORMAL 1, 2 modes			V_{DD} = 3.0 V, V_{IN} = 2.8 V/0.2 V V_{IN} = 4.19 MHz fs = 32.768 kHz	–	1.75	3.0	mA
Supply current in IDLE 1, 2 modes				–	1.25	2.0	mA
Supply current in SLOW mode			V_{DD} = 3.0 V V_{IN} = 2.8 V/0.2 V fs = 32.768 kHz	–	20	30	μA
Supply current in SLEEP mode				–	10	20	μA
Supply current in STOP mode			V_{DD} = 5.5 V V_{IN} = 5.3 V/0.2 V	–	0.5	10	μA

Note 1: Typical values show those at Topr = 25°C
Note 2: Input Current I_{IN1},I_{IN3}: The current through resistor is not included, when the input resistor (pull-up or pull-down) is contained.
Note 3: IDD except for I_{REF}.

AD Conversion Characteristics

(V_{SS} = 0 V, V_{DD} = 2.7 to 5.5 V, Topr = – 40 to 85°C)

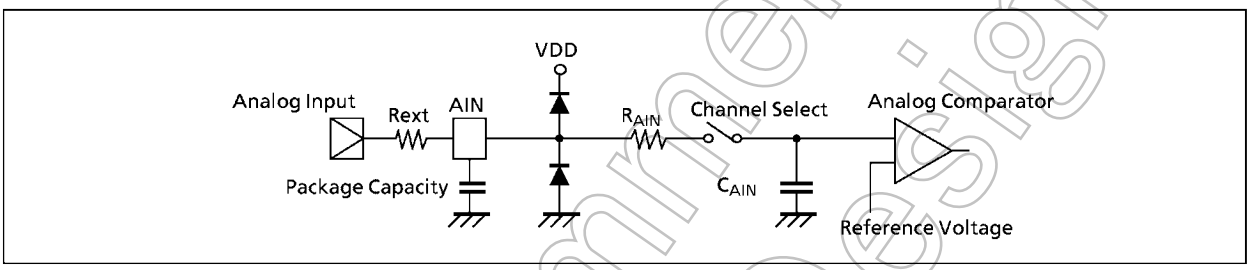
Parameter	Symbol	Conditions	Min	Typ.	Max			Unit
					ADCDR1	ADCDR2		
						ACK = 0	ACK = 1	
Analog reference voltage	V_{AREF}	$V_{AREF} - V_{ASS} \geqq$ 2.5 V	2.7	–	V_{DD}			V
	V_{ASS}		V_{SS}	–	1.5			
Analog input voltage	V_{AIN}		V_{ASS}	–	V_{AREF}			V
Analog supply current	I_{REF}	V_{AREF} = 5.5 V, V_{ASS} = 0.0 V	–	0.5	1.2			mA
Nonlinearity error		V_{DD} = 5.0, V_{SS} = 0.0 V V_{AREF} = 5.000 V V_{ASS} = 0.000 V or V_{DD} = 2.7, V_{SS} = 0.0 V V_{AREF} = 2.700 V V_{ASS} = 0.000 V	–	–	± 1	± 3	± 2	LSB
Zero point error			–	–	± 1	± 3	± 2	
Full scale error			–	–	± 1	± 3	± 2	
Total error			–	–	± 2	± 6	± 4	

Note 1: $\triangle V_{AREF} = V_{AREF} - V_{ASS}$
ADCDR1: 8 bits – AD conversion result (1LSB = $\triangle V_{AREF}/256$)
ADCDR2: 10 bits – AD conversion result (1LSB = $\triangle V_{AREF}/1024$)
Note 2: Quantizing error is not contained in those errors.

AD Input Characteristics (Topr = – 40 to 85°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Input impedance (Resistance)	R_{AIN}	VDD = 5.0 V, Conversion time 23 μs (fc = 8 MHz)	–	5	–	kΩ
		V_{DD} = 2.7 V, Conversion time 43.8 μs (fc = 4.2 MHz)	–	20	–	
Input impedance (Capacity)	C_{AIN}	V_{DD} = 5.0 V, Conversion time 23 μs (fc = 8 MHz)	–	7	–	pF
		V_{DD} = 2.7 V, Conversion time 43.8 μs (fc = 4.2 MHz)	–	7	–	
Source impedance	Rext	V_{DD} = 5.0 V, Conversion time 23 μs (fc = 8 MHz)	–	–	5	kΩ
		V_{DD} = 2.7 V, Conversion time 43.8 μs (fc = 4.2 MHz)	–	–	5	

Note: Input current (Output leak current) error (Max ± 2 μA) and quantizing error (Max ± 4LSB) for AD are contained.



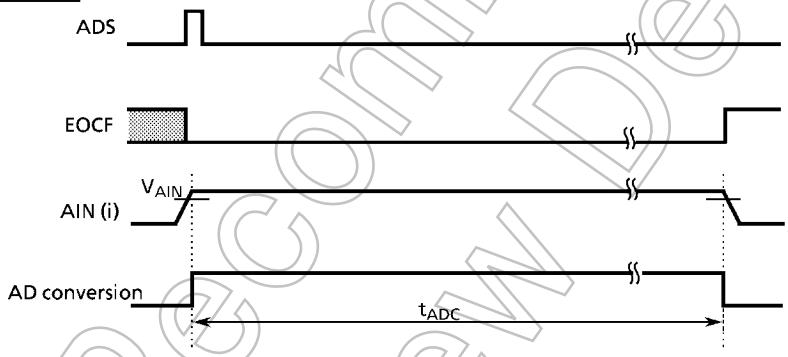
AD Pin Mode

AC Characteristics

(V_{SS} = 0 V, Topr = – 40 to 85°C)

Parameter	Symbol	Conditions	V_{DD}	Min	Typ.	Max	Unit
Machine cycle time	t_{cy}	In NORMAL 1, 2 mode	4.5 to 5.5 V	0.5	–	10	μs
		In IDLE 1, 2 mode					
		In SLOW mode	2.7 to 5.5 V	117.6	–	133.3	
		In SLEEP mode					
High level clock pulse width	t_{WCH}	For external clock operation (XIN input), fc = 8 MHz	4.5 to 5.5 V	62.5	–	–	ns
Low level clock pulse width	t_{WCL}						
High level clock pulse width	t_{WSH}	For external clock operation (XTIN input), fs = 32.768 kHz	2.7 to 5.5 V	14.7	–	–	μs
Low level clock pulse width	t_{WSL}						
AD conversion time	t_{ADC}	ADCCR bit 4; ACK = 0	–	–	49 tcy	–	ns
		ADCCR bit 4; ACK = 1	–	–	196 tcy	–	

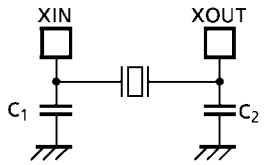
Timing of AD Conversion



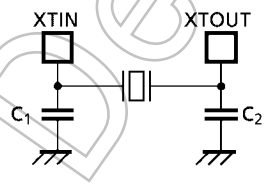
Note 1: During AD conversion, make the level of V_{AIN} stable.
Note 2: i = 17 to 10, 07 to 00

Recommended Oscillating Conditions (V_{SS} = 0 V, Topr = – 40 to 85°C)

Parameter	Oscillator	Oscillation Frequency	VDD	Recommended Oscillator	Recommended Constant C_1	Recommended Constant C_2
High-frequency oscillation	Ceramic resonator	8 MHz	4.5 to 5.5 V	KYOCERA KBR8.0 M	30 pF	30 pF
		4 MHz	2.7 to 5.5 V	KYOCERA KBR4.0 MS		
				MURATA CSA4.00 MG		
	Crystal oscillator	8 MHz	4.5 to 5.5 V	TOYOCOM 210B 8.0000	20 pF	20 pF
		4 MHz	2.7 to 5.5 V	TOYOCOM 204B 4.0000		
Low-frequency oscillation	Crystal oscillator	32.768 kHz	2.7 to 5.5 V	NDK MX-38T	15 pF	15 pF



(1) High-frequency Oscillation



(2) Low-frequency Oscillation

Note 1: When it is used in high electrical field, an electrical shield of the package is recommended to retain normal operations.

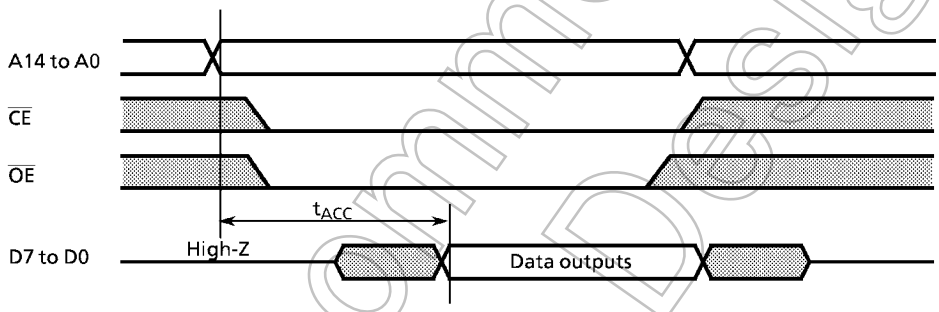
Note 2: TOYAMA MURATA MFG. CO., LTD (JAPAN)
The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change.
For up-to-date information, please refer to the following URL;
http://www.murata.com/

DC/AC Characteristics (PROM mode) (V_{SS} = 0 V)

(1) Read operation

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Input high voltage	V_{IH4}		2.2	–	V_{CC}	V
Input low voltage	V_{IL4}		0	–	0.8	V
Power supply voltage	V_{CC}		4.75	–	6.5	V
Program power supply voltage	V_{PP}					
Address access time	t_{ACC}	V_{CC} = 5.0 ± 0.25 V	–	1.5 tcyc + 300	–	ns

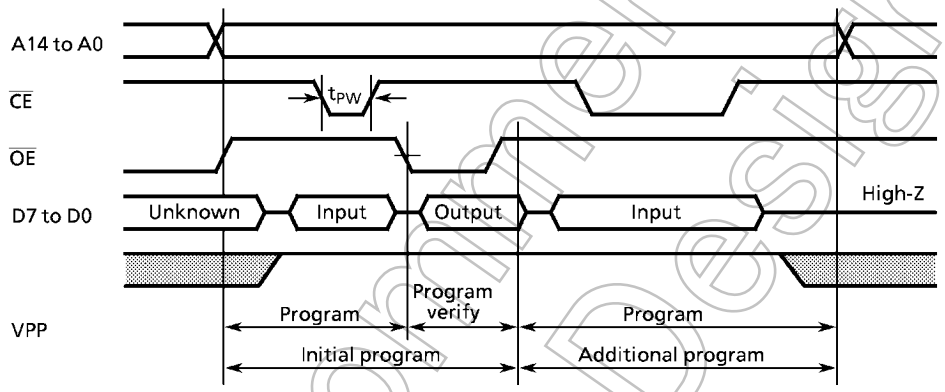
Note: tcyc = 500 ns at 8 MHz



Timing Waveforms of Read Operation

(2) Program Operation (High-speed write mode - I) (Topr = 25 ± 5°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Input high voltage	V_{IH4}		2.2	–	V_{CC}	V
Input low voltage	V_{IL4}		0	–	0.8	V
Power supply voltage	V_{CC}		5.75	–	6.5	V
Program power supply voltage	V_{PP}		12.0	12.5	13.0	V
Initial program pulse width	t_{PW}	V_{CC} = 6.0 V ± 0.25 V, V_{PP} = 12.5 V ± 0.5 V	0.95	1.0	1.05	ms

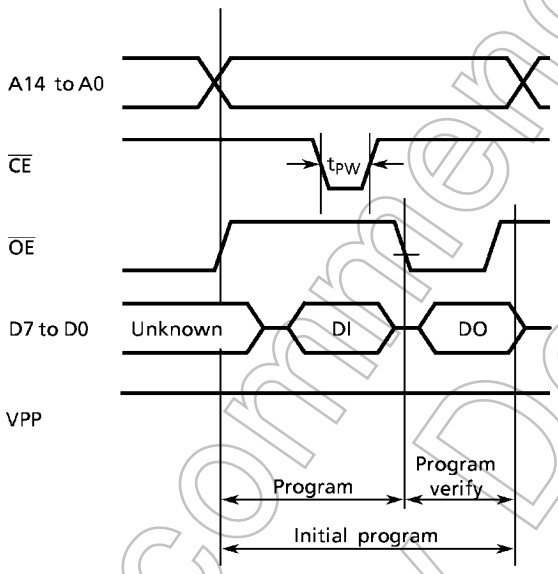


Timing Waveforms of Programming Operation

Note 1: When V_{cc} power supply is turned on or after, V_{pp} must be increased.
When V_{cc} power supply is turned off or before, V_{pp} must be decreased.
Note 2: The device must not be set to the EPROM programmer or picked up from it under applying the program voltage (12.5 V ± 0.5 V) to the V_{pp} pin as the device is damaged.
Note 3: Be sure to execute the recommended programing mode with the recommended programing adaptor. If a mode or an adaptor except the above, the misoperation sometimes occurs.

(3) Program operation (High-speed write mode - II) (Topr = 25 ± 5°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Input high voltage	V_{IH4}		2.2	–	V_{CC}	V
Input low voltage	V_{IL4}		0	–	0.8	V
Supply voltage	V_{CC}		6.00	6.25	6.50	V
Program supply voltage	V_{PP}		12.50	12.75	13.0	V
Initial program pulse width	t_{PW}	V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.75 V ± 0.25 V	0.095	0.1	0.105	ms



Note: DO: Data output (I0 to I7)
DI: Data input (I0 to I7)

Note 1: When V_{cc} power supply is turned on or after, V_{pp} must be increased.
When V_{cc} power supply is turned off or before, V_{pp} must be decreased.

Note 2: The device must not be set to the EPROM programmer or picked up from it under applying the program voltage (12.75 V ± 0.25 V) to the V_{pp} pin as the device is damaged.

Note 3: Be sure to execute the recommended programing mode with the recommended programing adaptor. If a mode or an adaptor except the above, the misoperation sometimes occurs.

Electrical Characteristics

(2) TMP87PM48

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		– 0.3 to 6.5	V
Input voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output voltage	V_{OUT}		– 0.3 to V_{DD} + 0.3	V
Output current (Per 1 pin)	I_{OUT1}	Ports P0, P1, P2, P4, P5, P6, P7, P8	3.2	mA
	I_{OUT2}	Port P3	30	
Output current (Total)	ΣI_{OUT1}	Ports P0, P1, P2, P4, P5, P6, P7, P8	120	mA
	ΣI_{OUT2}	Port P3	120	
Power dissipation	PD		350	mW
Soldering temperature (Time)	Tsld		260 (10 s)	°C
Storage temperature	Tstg		– 55 to 125	°C
Operating temperature	Topr		– 40 to 85	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Conditions (V_{SS} = 0 V, Topr = – 40 to 85°C)

Parameter	Symbol	Pins	Conditions		Min	Max	Unit
Supply voltage	V_{DD}		fc = 8 MHz	NORMAL1/2 modes	4.5	5.5	V
				IDLE1/2 modes			
			fc = 4.2 MHz	NORMAL1/2 modes	2.7		
				IDLE1/2 modes			
			fs = 32.768 kHz	SLOW mode			
				SLEEP mode			
				STOP mode	2.0		
Input high voltage	V_{IH1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		$V_{DD} \times 0.70$	V_{DD}	V
	V_{IH2}	Hysteresis input			$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5$ V		$V_{DD} \times 0.90$		
Input low voltage	V_{IL1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		0	$V_{DD} \times 0.30$	V
	V_{IL2}	Hysteresis input				$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5$ V			$V_{DD} \times 0.10$	
Clock frequency	fc	XIN, XOUT	V_{DD} = 4.5 to 5.5 V		0.4	8.0	MHz
			V_{DD} = 2.7 to 5.5 V			4.2	
	fs	XTIN, XTOUT			30.0	34.0	kHz

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (Supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: The condition of clock frequency is in NORMAL1/2 modes and IDLE1/2 modes.

DC Characteristics

(V_{SS} = 0 V, Topr = – 40 to 85°C)

Parameter	Symbol	Pins	Conditions	Min	Typ.	Max	Unit
Hysteresis voltage	V_{HS}	Hysteresis inputs	VDD = 5.0 V	–	0.9	–	V
Input current	I_{IN1}	TEST	VDD = 5.5 V V_{IN} = 5.5 V/0 V	–	–	± 2	μA
	I_{IN2}	Open drain ports, Tri-state ports					
	I_{IN3}	$\overline{RESET}$, $\overline{STOP}$					
Input resistance	R_{IN2}	$\overline{RESET}$	VDD = 5.0 V	100	220	450	kΩ
Output leakage current	I_{LO}	Sink open drain ports	V_{DD} = 5.5 V, V_{OUT} = 5.5 V	–	–	2	μA
		Tri-state ports	V_{DD} = 5.5 V, V_{OUT} = 5.5/0 V	–	–	± 2	
Output high voltage	V_{OH2}	Tri-state ports	V_{DD} = 4.5 V, I_{OH} = – 0.7 mA	4.1	–	–	V
Output low voltage	V_{OL}	Except for XOUT and P3	V_{DD} = 4.5 V, I_{OL} = 1.6 mA	–	–	0.4	mA
Output low current	I_{OL3}	P3	V_{DD} = 4.5 V, V_{OL} = 1.0 V	–	20	–	mA
Supply current in NORMAL 1, 2 modes	I_{DD}		V_{DD} = 5.5 V V_{IN} = 5.3 V/0.2 V fc = 8 MHz fs = 32.768 kHz	–	4.75	6.4	mA
Supply current in IDLE 1, 2 modes				–	3.25	4.65	mA
Supply current in NORMAL 1, 2 modes			V_{DD} = 3.0 V, V_{IN} = 2.8 V/0.2 V V_{IN} = 4.19 MHz fs = 32.768 kHz	–	1.87	3.2	mA
Supply current in IDLE 1, 2 modes				–	1.35	2.2	mA
Supply current in SLOW mode			V_{DD} = 3.0 V V_{IN} = 2.8 V/0.2 V fs = 32.768 kHz	–	20	30	μA
Supply current in SLEEP mode				–	10	20	μA
Supply current in STOP mode			V_{DD} = 5.5 V V_{IN} = 5.3 V/0.2 V	–	0.5	10	μA

Note 1: Typical values show those at Topr = 25°C
Note 2: Input Current I_{IN1},I_{IN3}: The current through resistor is not included, when the input resistor (pull-up or pull-down) is contained.
Note 3: IDD except for I_{REF}.

AD Conversion Characteristics

(V_{SS} = 0 V, V_{DD} = 2.7 to 5.5 V, Topr = – 40 to 85°C)

Parameter	Symbol	Conditions	Min	Typ.	Max			Unit
					ADCDR1	ADCDR2		
						ACK = 0	ACK = 1	
Analog reference voltage	V_{AREF}	$V_{AREF} - V_{ASS} \geqq$ 2.5 V	2.7	–	V_{DD}			V
	V_{ASS}		V_{SS}	–	1.5			
Analog input voltage	V_{AIN}		V_{ASS}	–	V_{AREF}			V
Analog supply current	I_{REF}	V_{AREF} = 5.5 V, V_{ASS} = 0.0 V	–	0.5	1.2			mA
Nonlinearity error		V_{DD} = 5.0, V_{SS} = 0.0 V V_{AREF} = 5.000 V V_{ASS} = 0.000 V or V_{DD} = 2.7, V_{SS} = 0.0 V V_{AREF} = 2.700 V V_{ASS} = 0.000 V	–	–	± 1	± 3	± 2	LSB
Zero point error			–	–	± 1	± 3	± 2	
Full scale error			–	–	± 1	± 3	± 2	
Total error			–	–	± 2	± 6	± 4	

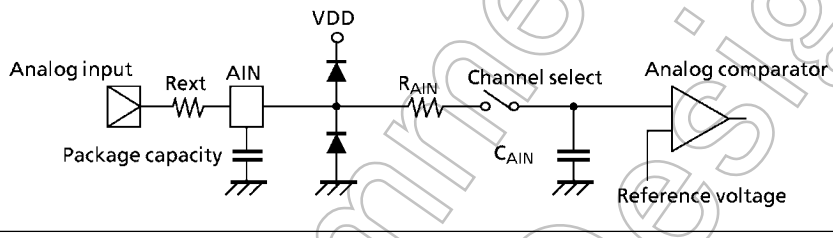
Note 1: $\triangle V_{AREF} = V_{AREF} - V_{ASS}$
ADCDR1: 8 bits – AD conversion result (1LSB = $\triangle V_{AREF}$/256)
ADCDR2: 10 bits – AD conversion result (1LSB = $\triangle V_{AREF}$/1024)
Note 2: Quantizing error is not contained in those errors.

AD Input Characteristics

(Topr = – 40 to 85°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Input impedance (Resistance)	R_{AIN}	VDD = 5.0 V, Conversion time 23 μs (fc = 8 MHz)	–	5	–	kΩ
		V_{DD} = 2.7 V, Conversion time 43.8 μs (fc = 4.2 MHz)	–	20	–	
Input impedance (Capacity)	C_{AIN}	V_{DD} = 5.0 V, Conversion time 23 μs (fc = 8 MHz)	–	7	–	pF
		V_{DD} = 2.7 V, Conversion time 43.8 μs (fc = 4.2 MHz)	–	7	–	
Source impedance	Rext	V_{DD} = 5.0 V, Conversion time 23 μs (fc = 8 MHz)	–	–	5	kΩ
		V_{DD} = 2.7 V, Conversion time 43.8 μs (fc = 4.2 MHz)	–	–	5	

Note: Input current (Output leak current) error (Max ± 2 μA) and quantizing error (Max ± 4LSB) for AD are contained.



AD Pin Mode

AC Characteristics

(V_{SS} = 0 V, Topr = – 40 to 85°C)

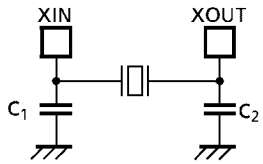
Parameter	Symbol	Conditions	V_{DD}	Min	Typ.	Max	Unit
Machine cycle time	t_{cy}	In NORMAL 1, 2 mode	4.5 to 5.5 V	0.5	–	10	μs
		In IDLE 1, 2 mode					
		In SLOW mode	2.7 to 5.5 V	117.6	–	133.3	
		In SLEEP mode					
High level clock pulse width	t_{WCH}	For external clock operation (XIN input), fc = 8 MHz	4.5 to 5.5 V	62.5	–	–	ns
Low level clock pulse width	t_{WCL}						
High level clock pulse width	t_{WSH}	For external clock operation (XTIN input), fs = 32.768 kHz	2.7 to 5.5 V	14.7	–	–	μs
Low level clock pulse width	t_{WSL}						
AD conversion time	t_{ADC}	ADCCR bit 4 ; ACK = 0	–	–	49 tcy	–	ns
		ADCCR bit 4 ; ACK = 1	–	–	196 tcy	–	

Timing of AD Conversion

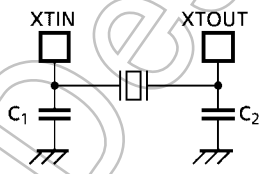
Note 1: During AD conversion, make the level of V_{AIN} stable.
Note 2: i = 17 to 10, 07 to 00

Recommended Oscillating Conditions (V_{SS} = 0 V, Topr = – 40 to 85°C)

Parameter	Oscillator	Oscillation Frequency	VDD	Recommended Oscillator	Recommended Constant C_1	Recommended Constant C_2
High-frequency oscillation	Ceramic resonator	8 MHz	4.5 to 5.5 V	KYOCERA KBR8.0 M	30 pF	30 pF
		4 MHz	2.7 to 5.5 V	KYOCERA KBR4.0 MS		
				MURATA CSA4.00 MG		
	Crystal oscillator	8 MHz	4.5 to 5.5 V	TOYOCOM 210B 8.0000	20 pF	20 pF
		4 MHz	2.7 to 5.5 V	TOYOCOM 204B 4.0000		
Low-frequency oscillation	Crystal oscillator	32.768 kHz	2.7 to 5.5 V	NDK MX-38T	15 pF	15 pF



(1) High-frequency Oscillation



(2) Low-frequency Oscillation

Note 1: When it is used in high electrical field, an electrical shield of the package is recommended to retain normal operations.

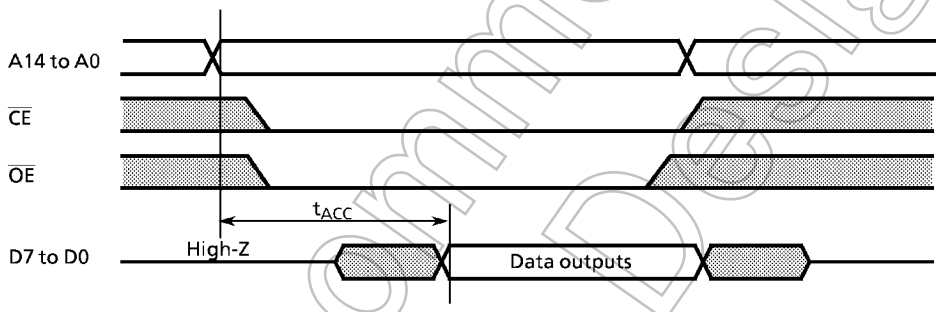
Note 2: TOYAMA MURATA MFG. CO., LTD (JAPAN)
The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change.
For up-to-date information, please refer to the following URL;
http://www.murata.com/

DC/AC Characteristics (PROM mode) (V_{SS} = 0 V)

(1) Read operation

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Input high voltage	V_{IH4}		2.2	–	V_{CC}	V
Input low voltage	V_{IL4}		0	–	0.8	V
Power supply voltage	V_{CC}		4.75	–	6.5	V
Program power supply voltage	V_{PP}					
Address access time	t_{ACC}	V_{CC} = 5.0 ± 0.25 V	–	1.5 tcyc + 300	–	ns

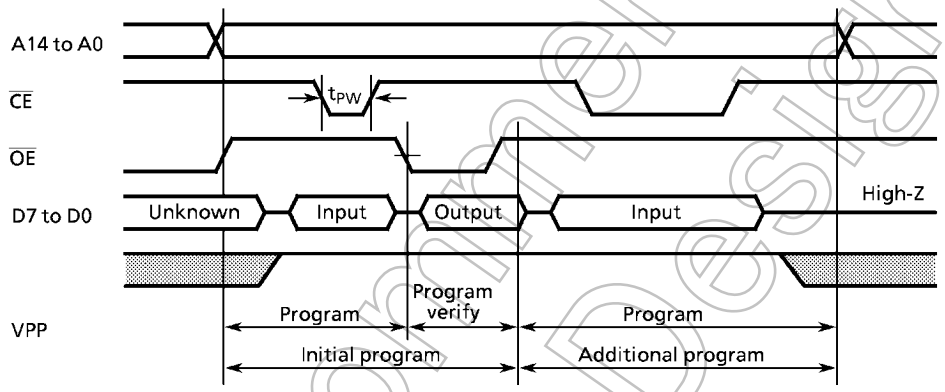
Note: tcyc = 500 ns at 8 MHz



Timing Waveforms of Read Operation

(2) Program Operation (High-speed write mode - I) (Topr = 25 ± 5°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Input high voltage	V_{IH4}		2.2	–	V_{CC}	V
Input low voltage	V_{IL4}		0	–	0.8	V
Power supply voltage	V_{CC}		5.75	6.0	6.25	V
Program power supply voltage	V_{PP}		12.0	12.5	13.0	V
Initial program pulse width	t_{PW}	V_{CC} = 6.0 V ± 0.25 V, V_{PP} = 12.5 ± 0.5 V	0.95	1.0	1.05	ms

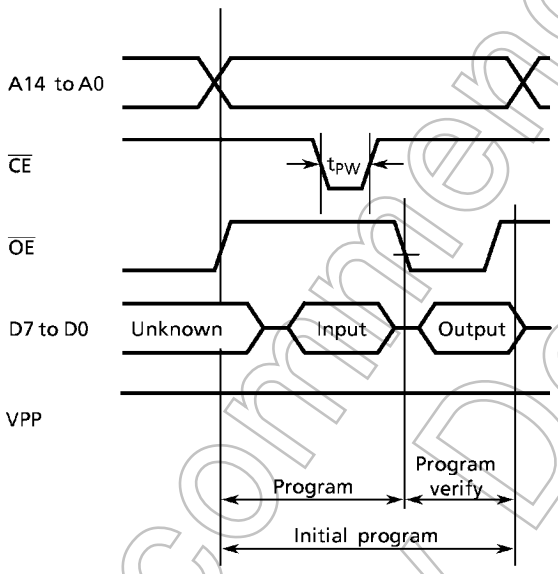


Timing Waveforms of Programming Operation

Note 1: When V_{cc} power supply is turned on or after, V_{pp} must be increased.
When V_{cc} power supply is turned off or before, V_{pp} must be decreased.
Note 2: The device must not be set to the EPROM programmer or picked up from it under applying the program voltage (12.5 V ± 0.5 V) to the V_{pp} pin as the device is damaged.
Note 3: Be sure to execute the recommended programing mode with the recommended programing adaptor. If a mode or an adaptor except the above, the misoperation sometimes occurs.

(3) Program operation (High-speed write mode - II) (Topr = 25 ± 5°C)

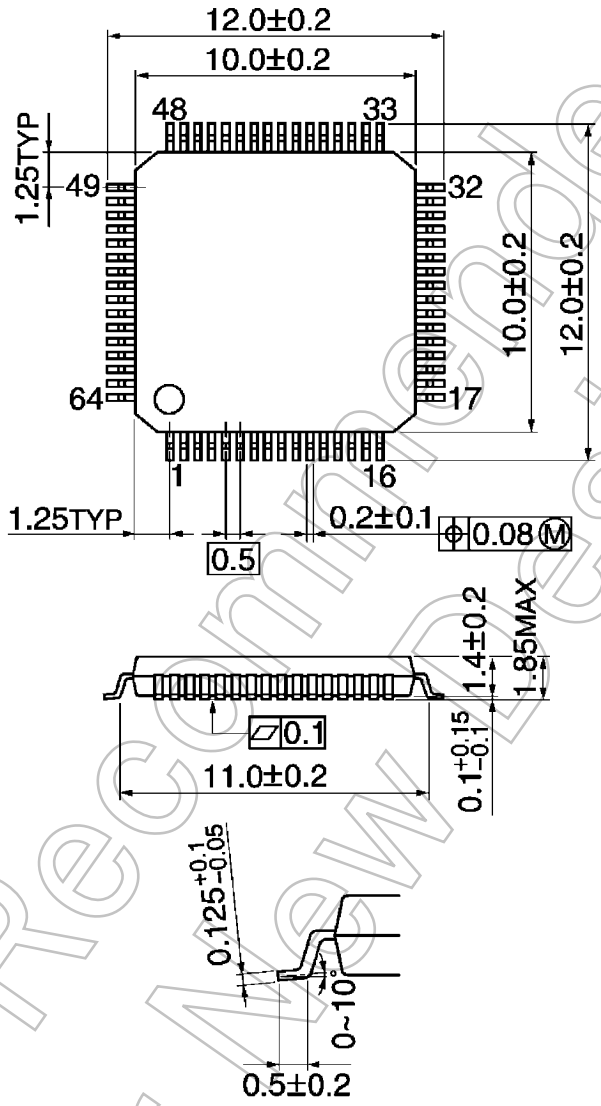
Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Input high voltage	V_{IH4}		2.2	–	V_{CC}	V
Input low voltage	V_{IL4}		0	–	0.8	V
Supply voltage	V_{CC}		6.00	6.25	6.50	V
Program supply voltage	V_{PP}		12.50	12.75	13.0	V
Initial program pulse width	t_{PW}	V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.75 V ± 0.25 V	0.095	0.1	0.105	ms



Note 1: When V_{CC} power supply is turned on or after, V_{pp} must be increased.
When V_{CC} power supply is turned off or before, V_{pp} must be decreased.
Note 2: The device must not be set to the EPROM programmer or picked up from it under applying the program voltage (12.75 V ± 0.25 V) to the V_{pp} pin as the device is damaged.
Note 3: Be sure to execute the recommended programing mode with the recommended programing adaptor. If a mode or an adaptor except the above, the misoperation sometimes occurs.

Package Dimensions

P-LQFP64-1010-0.50 Unit: mm



P-QFP64-1414-0.80A Unit: mm