October 2009

Dear Customer

Important Notices

Thank you for your continued patronage of Toshiba microcontrollers.

This page gives you important information on using Toshiba microcontrollers. Please be sure to check each item for proper use of our products.

Restrictions on the Voltage Detection Circuit (October 2009)

*If your datasheet is dated 30 November 2008 or earlier, please download the latest datasheet or request it from your local Toshiba office.

Datasheet Corrections regarding the 16-Bit Timer Counter (February 2008)

* If your datasheet is dated 2 November 2007 or earlier, please download the latest datasheet or request it from your local Toshiba office.

TOSHIBA Microcontrollers TLCS-870 Family
TLCS-870/C1 Series

TMP89FH40	TMP89FM40	TMP89CH42	TMP89CM42	TMP89FH42
TMP89FH42L	TMP89FM42	TMP89FM42A	TMP89FM42K	TMP89FM42L
TMP89FM43L	TMP89CH46	TMP89CM46	TMP89FH46	TMP89FH46L
TMP89FM46	TMP89FM46A	TMP89FM46K	TMP89FM46L	TMP89FS60
TMP89FM82	TMP89FM82T			
TMP89C900 (Emulation chip)				

October 2009

Restrictions on the Voltage Detection Circuit

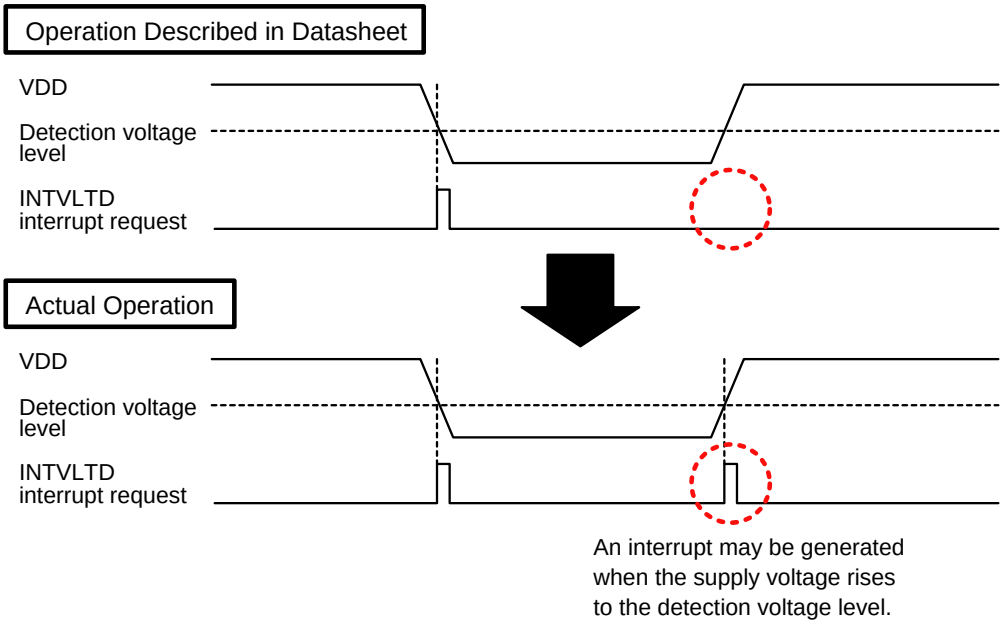
This is to inform you of restrictions on the voltage detection circuit in the TLCS-870/C1 Series of microcontrollers.

If you need any further information, please contact your local Toshiba sales representative.

[Restrictions]

1. INTVLTD Interrupt Request

When interrupt generation is enabled in the voltage detection circuit, an INTVLTD interrupt request may be generated not only when the supply voltage falls to the detection voltage level, but also when it rises to the detection voltage level.
In ICE mode of the In-Circuit Emulator (TMP89C900), no interrupt request is generated when the supply voltage rises to the detection voltage level. Therefore, with products supporting the In-Circuit Emulator (TMP89C900), the interrupt generation operation may differ between the development tool and the actual product.



2. Releasing STOP Mode by Voltage Detection

The SRSS bit in the voltage detection control register 2 (VDCR2) provided for releasing STOP mode by voltage detection cannot be used because it does not function as expected.

[Workarounds]

1. INTVLTD Interrupt Request

Do not use the INTVLTD interrupt for voltage detection. The voltage level should be regularly checked using other timing such as the execution cycle of the main program. VDCR1<VDxSF> (x=1, 2) can be used to check the voltage level. However, if the operating voltage is near the detection voltage, the VDCR1<VDxSF> value may become unstable. It is recommended that VDCR1<VDxSF> be tested multiple times to determine the voltage level.

2. Releasing STOP Mode by Voltage Detection

Always set VDCR2<SRSS> to "00". Use the STOP pin to release STOP mode.

TOSHIBA Microcontrollers TLCS-870 Family
TLCS-870/C1 Series

TMP89FH42 TMP89FM42 TMP89FH46 TMP89FM46 TMP89FS60

February 2008

Datasheet Corrections regarding the 16-Bit Timer Counter

With regard to the TLCS-870/C1 Series microcontrollers listed above, the following corrections for the 16-bit timer counter should be made to the technical datasheets.

If you have any questions or require any further information, please contact your local Toshiba sales representative.

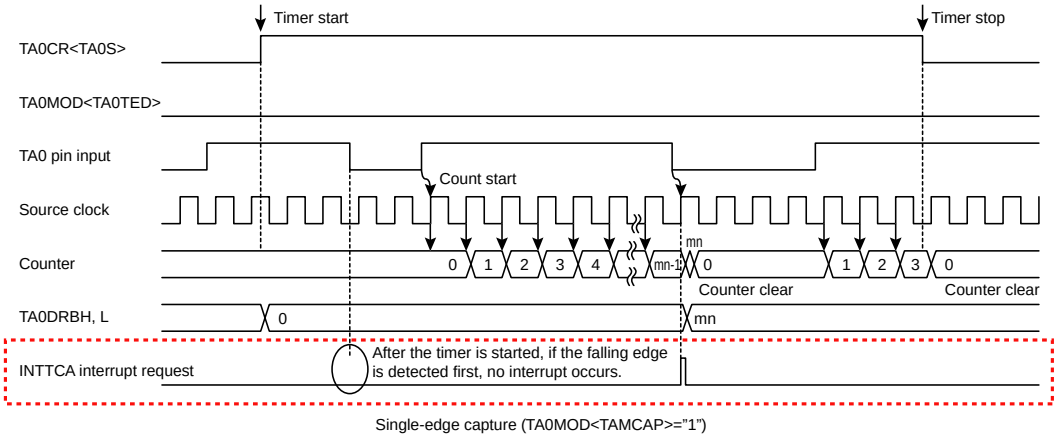
[16-Bit Timer Counter]

Pulse width measurement mode

In the description of the pulse width measurement mode of the 16-bit timer counter, the following two corrections should be made regarding the INTTCA interrupt request generation timing.

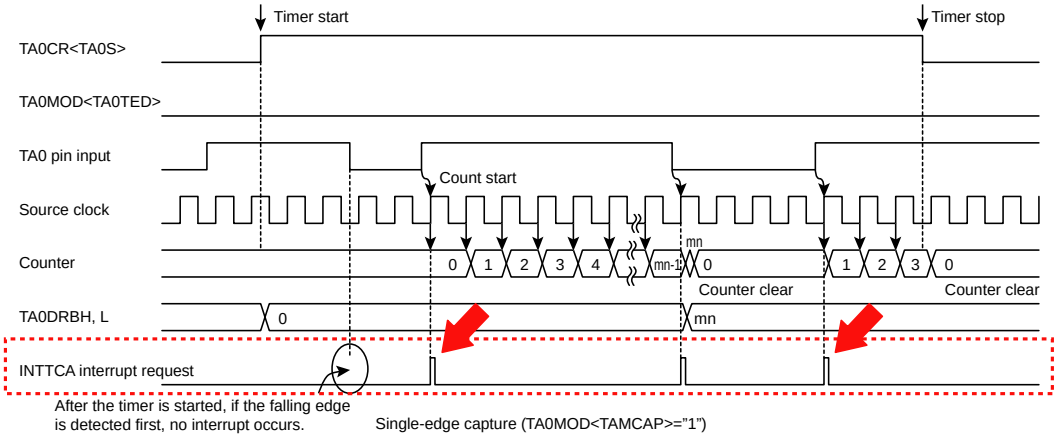
1. The timing diagram for single-edge capture indicates that no interrupt request occurs at the first count start edge and the second count start edge after the timer is started. This should be corrected so that an interrupt request occurs at the first count start edge and the second count start edge, as shown below.

Before correction



Single-edge capture (TA0MOD<TAMCAP>="1")

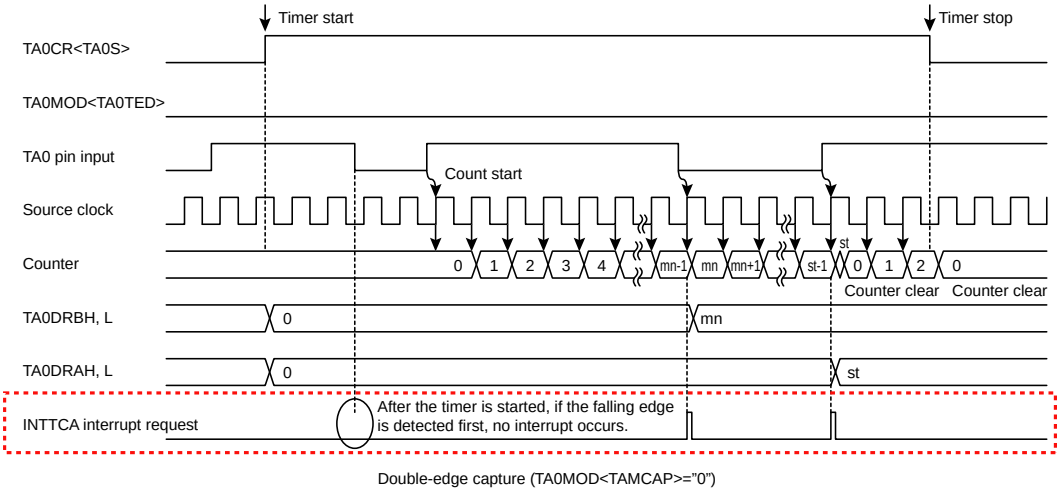
After correction



Single-edge capture (TA0MOD<TAMCAP>="1")

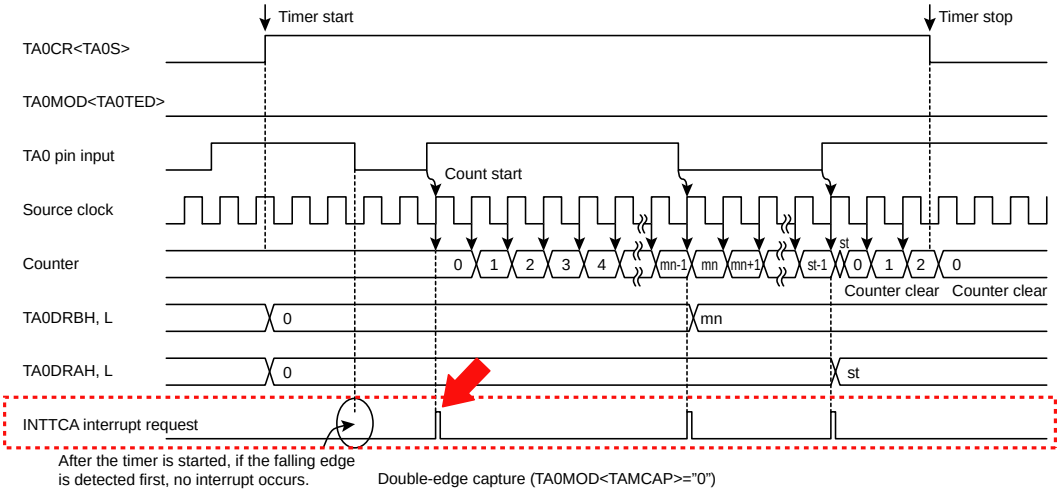
2. The timing diagram for double-edge capture indicates that no interrupt request occurs at the count start edge after the timer is started. This should be corrected so that an interrupt request occurs at the count start edge, as shown below.

Before correction



Double-edge capture (TA0MOD<TAMCAP>="0")

After correction



Double-edge capture (TA0MOD<TAMCAP>="0")