Dear Customer, April 2007

Important Notices

Thank you for your continued patronage of Toshiba microcontrollers.

This page gives you important information on using Toshiba microcontrollers. Please be sure to check each item for proper use of our products.

Restriction for Using DMA Transfer (April 2007)

* If your datasheet is dated 30 March 2007 or earlier, please download the latest datasheet or request it from your local Toshiba office.

TOSHIBA Microcontrollers TX19 Family

TX19, TX19A Series

TMP1940CYAF/FG	TMP1940FDBF/FG	TMP1941AF/FG	TMP1942CYU
TMP1942CZUE	TMP1942FDU	TMP1942CZXBG	TMP1942FDXBG
TMP1962C10BXBG	TMP1962F10AXBG	TMP19A64C1DXBG	TMP19A64F20BXBG
TMP19A71FYFG	TMP19A71FYUG	TMP19A71CYFG	TMP19A71CYUG

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Restriction for Using DMA Transfer

With regard to the TOSHIBA microcontrollers listed above, please be advised that malfunctions may occur on DMA transfer.

[Restriction/ Problem]

TOSHIBA microcontrollers listed above may cause malfunctions on DMA transfer using a memory - to - I/O transfer device if they meet all the conditions shown below.

1) The memory - to - I/O transfer is used as a transfer device.
2) The data destination is one of the following.
   a) Internal RAM
   b) External memory (0 WAIT, ALE assert: 1 clock)
   c) HSIO (excluding SIO and SBI)
3) Two or more transfers are set.
   (BCRn) > (CCRn) <TrSiz>
4) Bus width has the same size as the data to be transferred.
   Data to be transferred (CCRn) <DPS> = Device port size (CCRn) <TrSiz>

[Workaround]

Please change the DMA transfer initial setting as shown below.

1) Fix the destination device to memory.
2) Set the source device depending on the transfer mode.
   a) At single transfer: I/O device
   b) At continuous transfer: Memory

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Datasheet Revision Related to Additional Restriction for DMA Transfer

The following changes will be reflected to the updated technical data sheet.

DMA Controller (DMAC)

1) Transfer Device

The device names "I/O device" and "memory device" are no longer used.

Memory - to - I/O mode will be called as follows.

Single transfer (previous version: I/O - to - memory)

Continuous transfer (previous version: memory - to - memory)

2) Channel Control Registers

Changes to two control bits in CCRn are made.

Previous)

	7	6	5	4	3	2	1	0
Bit symbol	SAC	DIO	DAC		TrSiz		DPS	
Read/Write	R/W	R/W	R/W		R/W		R/W	
After reset	0							
Function	See detailed description.	See detailed description.	See detailed description.					

Bit	Mnemonic	Field name	Description
9	SIO	Source I/O	Source Type: I/O Specifies the source device. 1: I/O device 0: Memory
8 : 7	SAC	Source Address count	Source Address Count (initial value: 00) Specifies the manner of change in a source address. 1x: Address fixed 01: Address decrease 00: Address increase
6	DIO	Destination I/O	Destination Type: I/O (initial value: 0) Specifies a destination device. 1: I/O device 0: Memory

Updated)

	7	6	5	4	3	2	1	0
Bit symbol	SAC		DAC		TrSiz		DPS	
Read/Write	R/W	R/W	R/W		R/W		R/W	
After reset	0							
Function	See detailed description.	Always set this bit to "0".	See detailed description.					

Bit	Mnemonic	Field name	Description
9	SIO	Transfer type selection	Source Type: I/O (initial value: 0) 1: Single transfer 0: Continuous transfer (Data is transferred successively until BCRx becomes "0").
8 : 7	SAC	Source Address Count	Source Address Count (initial value: 00) Specifies the manner of change in a source address. 1x: Address fixed 01: Address decrease 00: Address increase
6	—	(Reserved)	This is a reserved bit. Always set this bit to "0".

3) Combinations of Transfer Modes

Previous)

Transfer request	Edge/level	Address mode	Transfer devices
Internal	—	Dual	Memory → memory
External	"L" level ($\overline{\text{INTDREQn}}$)		Memory → memory
			Memory → I/O
			I/O → memory
External	"L" level ($\overline{\text{DREQn}}$)		Memory → memory
	Falling edge ($\overline{\text{DREQn}}$)		Memory → I/O
			I/O → memory

Updated)

Transfer request	Edge/level	Address mode	Transfer devices
Internal	—	Dual	Continuous transfer
External	"L" level ($\overline{\text{INTDREQn}}$)		Continuous transfer
			Single transfer
External	"L" level ($\overline{\text{DREQn}}$)		Continuous transfer
	Falling edge ($\overline{\text{DREQn}}$)		Single transfer