

Dear Customer,

August 2007

Important Notices

Thank you for your continued patronage of Toshiba microcontrollers.

This page gives you important information on using Toshiba microcontrollers. Please be sure to check each item for proper use of our products.

▶ **Caution in Using an External Clock** (August 2007)

- * If your datasheet is dated 30 August 2007 or earlier, please download the latest datasheet or request it from your local Toshiba office.

▶ **Caution in Using the Two-Phase Counters** (August 2007)

- * If your datasheet is dated 30 August 2007 or earlier, please download the latest datasheet or request it from your local Toshiba office.

▶ **Restriction for Using DMA Transfer** (April 2007)

- * If your datasheet is dated 30 March 2007 or earlier, please download the latest datasheet or request it from your local Toshiba office.

TOSHIBA Microcontrollers TX19 Family**TX19A Series**

TMP19A64C1DXBG

TMP19A64F20AXBG

TMP19A64F20BxBG

August 2007

Dear Customer,

Caution in Using an External Clock

With regard to the TOSHIBA microcontrollers listed above, please be advised that their operation may be unstable when using an external clock.

[Restriction/ Problem]

The time for warm-up is required even when an external clock (oscillator, etc.) is used and providing stable oscillation because the internal PLL is used even in this case.

[Workaround]

Checking and modifying the software are required when using any external clock such as oscillator.

TOSHIBA Microcontrollers TX19 Family**TX19A Series**

TMP19A64C1DXBG

TMP19A64F20AXBG

TMP19A64F20BXXBG

August 2007

Dear Customer,

Datasheet Revision Related to Note on Using an External Clock

The following changes will be reflected to the updated technical datasheet.

System Clock Controller

The note will be revised as shown below.

Current)

Note 1: Warm-up is not required when an oscillator is used for the clock and providing stable oscillation.

Revised)

Note 1: The time for warm-up is required even when an external clock (oscillator, etc.) is used and providing stable oscillation because the internal PLL is used even in this case.

TOSHIBA Microcontrollers TX19 Family

TX19A Series

TMP19A64C1DXBG

TMP19A64F20AXBG

TMP19A64F20BXBG

August 2007

Dear Customer,

Caution in Using the Two-Phase Counters

With regard to the TOSHIBA microcontrollers listed above, please be advised that malfunctions may occur on the two-phase counters.

[Restriction/Problem]

Bits 2 to 0 of each counter RUN register must be set to start counting after bits 7 to 3 have been set to specify counter operating conditions. If bits 7 to 3 and bits 2 to 0 are set simultaneously, counting may not be executed properly.

TMRBA RUN register

		7	6	5	4	3	2	1	0
TBARUN (0xFFFF_F1E0)	bit Symbol	TBARDE		UDACK	TBAUDCE	I2TB	TBAPRUN		TBARUN
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W
	After reset	0	0	0	0	0	0	0	0
	Function	Double Buffer 0: Disable 1: Enable	Write "0."	Sampling clock 0: fs 1: $\phi T0/4$	Enable/disable two-phase counter 0: Disable 1: Enable	IDLE 0: Stop 1: Operate	Timer Run/Stop Control 0: Stop & clear 1: Count * The first bit can be read as "0."		

[Workaround]

Modify the software as appropriate.

TOSHIBA Microcontrollers TX19 Family

TX19A Series

TMP19A64C1DXBG

TMP19A64F20AXBG

TMP19A64F20BxBG

August 2007

Dear Customer,

Datasheet Revision Related to Notes on the Two-Phase Counters

The following changes will be reflected to the updated technical datasheet.

16-bit timer/event counter (TMRB)

The following notes will be added.

TMRBn RUN register (n=0 through 9)

	7	6	5	4	3	2	1	0
TBnRUN (0xFFFF_F1x0)	Bit symbol	TBnRDE			I2TBn	TBnPRUN		TBnRUN
	Read/Write	R/W	R/W	R/W	R/W	R/W	R	R/W
	After reset	0	0	0	0	0	0	0
	Function	Double Buffering 0: Disable 1: Enable	Write "0."	Write "0."	Write "0."	In the IDLE mode 0: Stop 1: Operate	Timer Run/Stop Control 0: Stop & clear 1: Count * The first bit can be read as "0."	

Note: Do not set bits 7 to 3 (counter operating conditions) and bits 2 to 0 (count start) simultaneously.

TMRBA RUN register

	7	6	5	4	3	2	1	0
TBARUN (0xFFFF_F1E0)	bit Symbol	TBARDE		UDACK	TBAUDCE	I2TBA	TBAPRUN	TBARUN
	Read/Write	R/W	R/W	R/W	R/W	R/W	R	R/W
	After reset	0	0	0	0	0	0	0
	Function	Double Buffer 0: Disable 1: Enable	Write "0."	Sampling clock 0: fs 1: $\phi T0/4$	Enable/disable two-phase counter 0: Disable 1: Enable	IDLE 0: Stop 1: Operate	Timer Run/Stop Control 0: Stop & clear 1: Count * The first bit can be read as "0."	

Note: Do not set bits 7 to 3 (counter operating conditions) and bits 2 to 0 (count start) simultaneously.

TMRBn mode register (n=0 through A)

TBnMOD (0xFFFF_F1x2)		7	6	5	4	3	2	1	0
	Bit Symbol			TBnCP0	TBnCPM1	TBnCPM0	TBnCLE	TBnCLK1	TBnCLK0
	Read/Write	R		W	R/W				
	After reset	0	0	1	0	0	0	0	0
	Function	This can be read as "00."		Capture control by software 0: Capture by software 1: Don't care	Capture timing 00: Disable 01: TBnIN0 ↑ TBnIN1 ↑ 10: TBnIN0 ↑ TBnIN0 ↓ 11: CAPTRG ↑ CAPTRG ↓		Up-counter control 0: Clear/disable 1: Clear/enable	Selects source clock 00: TB0IN0 pin input 01: φT1 10: φT4 11: φT16	

Note: Set the <TBnCP0> bit after setting bits 4 to 0.

TOSHIBA Microcontrollers TX19 Family**TX19, TX19A Series**

TMP1940CYAF/FG	TMP1940FDBF/FG	TMP1941AF/FG	TMP1942CYU
TMP1942CZUE	TMP1942FDU	TMP1942CZXBG	TMP1942FDXBG
TMP1962C10BXBG	TMP1962F10AXBG	TMP19A64C1DXBG	TMP19A64F20BXBG
TMP19A71FYFG	TMP19A71FYUG	TMP19A71CYFG	TMP19A71CYUG

April 2007

Dear Customer,

Restriction for Using DMA Transfer

With regard to the TOSHIBA microcontrollers listed above, please be advised that malfunctions may occur on DMA transfer.

[Restriction/ Problem]

TOSHIBA microcontrollers listed above may cause malfunctions on DMA transfer using a memory - to - I/O transfer device if they meet all the conditions shown below.

- 1) The memory - to - I/O transfer is used as a transfer device.
- 2) The data destination is one of the following.
 - a) Internal RAM
 - b) External memory (0 WAIT, ALE assert: 1 clock)
 - c) HSIO (excluding SIO and SBI)
- 3) Two or more transfers are set.
(BCRn) > (CCRn) <TrSiz>
- 4) Bus width has the same size as the data to be transferred.
Data to be transferred (CCRn) <DPS> = Device port size (CCRn) <TrSiz>

[Workaround]

Please change the DMA transfer initial setting as shown below.

- 1) Fix the destination device to memory.
- 2) Set the source device depending on the transfer mode.
 - a) At single transfer: I/O device
 - b) At continuous transfer: Memory

TOSHIBA Microcontrollers TX19 Family**TX19, TX19A Series**

TMP1940CYAF/FG	TMP1940FDBF/FG	TMP1941AF/FG	TMP1942CYU
TMP1942CZUE	TMP1942FDU	TMP1942CZXBG	TMP1942FDXBG
TMP1962C10BXBG	TMP1962F10AXBG	TMP19A64C1DXBG	TMP19A64F20BXBG
TMP19A71FYFG	TMP19A71FYUG	TMP19A71CYFG	TMP19A71CYUG

April 2007

Dear Customer,

Datasheet Revision Related to Additional Restriction for DMA Transfer

The following changes will be reflected to the updated technical data sheet.

DMA Controller (DMAC)**1) Transfer Device**

The device names "I/O device" and "memory device" are no longer used.

Memory - to - I/O mode will be called as follows.

Single transfer (previous version: I/O - to - memory)

Continuous transfer (previous version: memory - to - memory)

2) Channel Control Registers

Changes to two control bits in CCRn are made.

Previous)

	7	6	5	4	3	2	1	0
Bit symbol	SAC	DIO	DAC		TrSiz		DPS	
Read/Write	R/W	R/W	R/W		R/W		R/W	
After reset	0							
Function	See detailed description.	See detailed description.	See detailed description.					

Bit	Mnemonic	Field name	Description
9	SIO	Source I/O	Source Type: I/O Specifies the source device. 1: I/O device 0: Memory
8 : 7	SAC	Source Address count	Source Address Count (initial value: 00) Specifies the manner of change in a source address. 1x: Address fixed 01: Address decrease 00: Address increase
6	DIO	Destination I/O	Destination Type: I/O (initial value: 0) Specifies a destination device. 1: I/O device 0: Memory

Updated)

	7	6	5	4	3	2	1	0
Bit symbol	SAC		DAC		TrSiz		DPS	
Read/Write	R/W	R/W	R/W		R/W		R/W	
After reset	0							
Function	See detailed description.	Always set this bit to "0".	See detailed description.					

Bit	Mnemonic	Field name	Description
9	SIO	Transfer type selection	Source Type: I/O (initial value: 0) 1: Single transfer 0: Continuous transfer (Data is transferred successively until BCRx becomes "0").
8 : 7	SAC	Source Address Count	Source Address Count (initial value: 00) Specifies the manner of change in a source address. 1x: Address fixed 01: Address decrease 00: Address increase
6	—	(Reserved)	This is a reserved bit. Always set this bit to "0".

3) Combinations of Transfer Modes

Previous)

Transfer request	Edge/level	Address mode	Transfer devices
Internal	—	Dual	Memory → memory
External	“L” level (INTDREQn)		Memory → memory
			Memory → I/O
			I/O → memory
External	“L” level (DREQn)		Memory → memory
			Memory → I/O
	Falling edge (DREQn)		I/O → memory

Updated)

Transfer request	Edge/level	Address mode	Transfer devices
Internal	—	Dual	Continuous transfer
External	$\overline{\text{“L” level}} \text{ (INTDREQn)}$		Continuous transfer
			Single transfer
External	$\overline{\text{“L” level}} \text{ (DREQn)}$		Continuous transfer
	Falling edge $\overline{\text{(DREQn)}}$		Single transfer