

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74VHC4051AF, TC74VHC4051AFK TC74VHC4052AF, TC74VHC4052AFK TC74VHC4053AF, TC74VHC4053AFK

TC74VHC4051AF/AFK

8-Channel Analog Multiplexer/Demultiplexer

TC74VHC4052AF/AFK

Dual 4-Channel Analog Multiplexer/Demultiplexer

TC74VHC4053AF/AFK

Triple 2-Channel Analog Multiplexer/Demultiplexer

The TC74VHC4051A/4052A/4053A are high-speed, low-voltage drive analog multiplexer/demultiplexers using silicon gate CMOS technology. In 3 V and 5 V systems these can achieve high-speed operation with the low power dissipation that is a feature of CMOS.

The TC74VHC4051A/4052A/4053A offer analog/digital signal selection as well as mixed signals. The 4051A has an 8-channel configuration, the 4052A has an 4-channel × 2 configuration, and the 4053A has a 2-channel × 3 configuration.

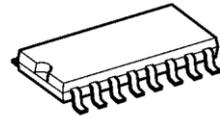
The switches for each channel are turned ON by the control pin digital signals.

All control inputs are equipped with a newly developed input protection circuit that avoids the need for a diode on the plus side (forward side from the input to the VCC). As a result, for example, 5.5 V signals can be permitted on the inputs even when the power supply voltage to the circuits is off. As a result of this input power protection, the TC74VHC4051A/4052A/4053A can be used in a variety of applications, including in the system which has two power supplies, and in battery backup circuits.

Features

- Low ON-resistance: $R_{on} = 45 \Omega$ (typ.) ($V_{CC} = 3 V$)
 $R_{on} = 24 \Omega$ (typ.) ($V_{CC} = 4.5 V$)
- Low power dissipation: $I_{CC} = 2.0 \mu A$ (max) ($T_a = 25^\circ C$)
- Input level: $V_{IL} = 0.8 V$ (max) ($V_{CC} = 3 V$)
 $V_{IH} = 2.0 V$ (min) ($V_{CC} = 3 V$)
- Power down protection is provided on all control inputs

TC74VHC4051AF, TC74VHC4052AF,
TC74VHC4053AF



SOP16-P-300-1.27A

TC74VHC4051AFK, TC74VHC4052AFK,
TC74VHC4053AFK

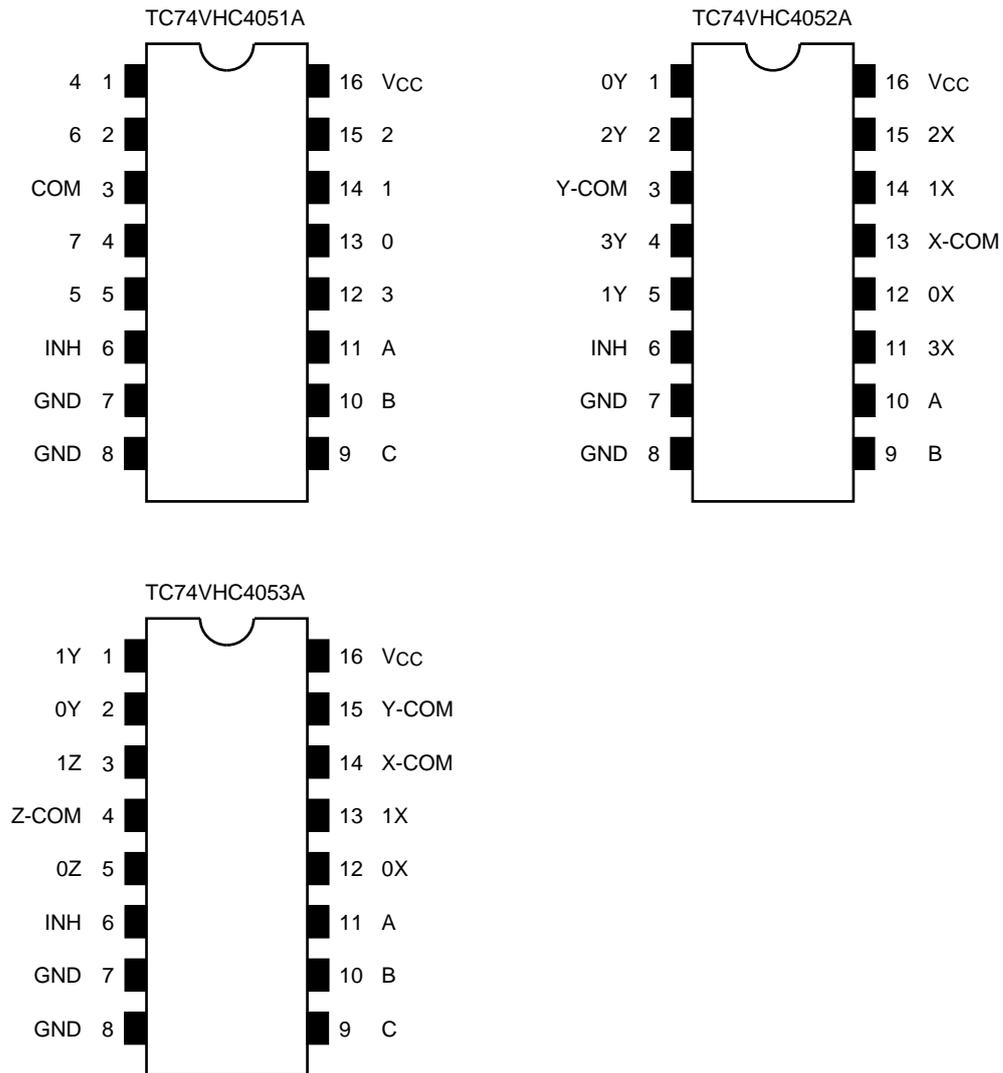


VSSOP16-P-0030-0.50

SOP16-P-300-1.27A : 0.18 g (typ.)
VSSOP16-P-0030-0.50 : 0.02 g (typ.)

Start of commercial production
2007-01

Pin Assignment (top view)



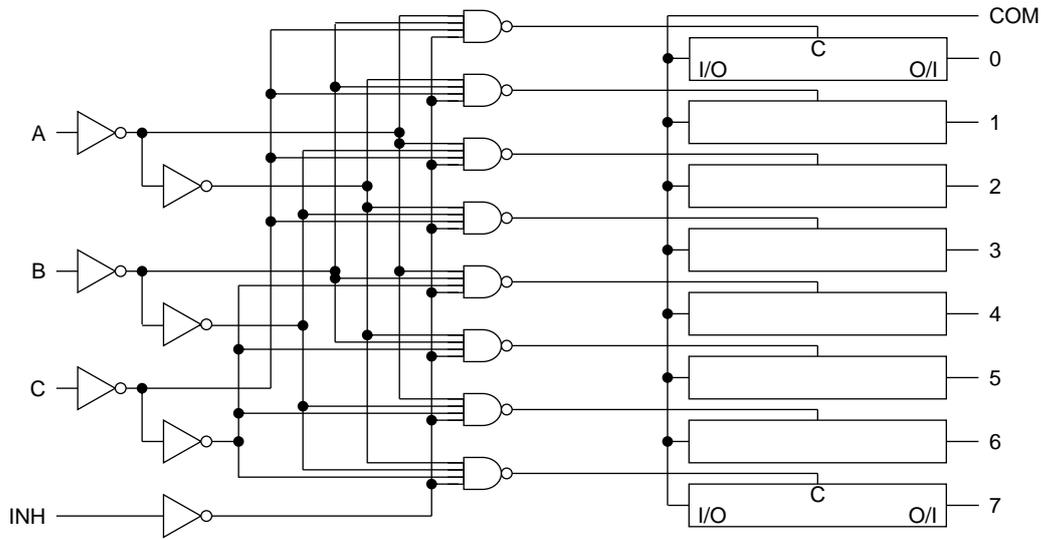
Truth Table

Control Inputs				"ON" Channel		
Inhibit	C*	B	A	VHC4051A	VHC4052A	VHC4053A
L	L	L	L	0	0X, 0Y	0X, 0Y, 0Z
L	L	L	H	1	1X, 1Y	1X, 0Y, 0Z
L	L	H	L	2	2X, 2Y	0X, 1Y, 0Z
L	L	H	H	3	3X, 3Y	1X, 1Y, 0Z
L	H	L	L	4	—	0X, 0Y, 1Z
L	H	L	H	5	—	1X, 0Y, 1Z
L	H	H	L	6	—	0X, 1Y, 1Z
L	H	H	H	7	—	1X, 1Y, 1Z
H	X	X	X	None	None	None

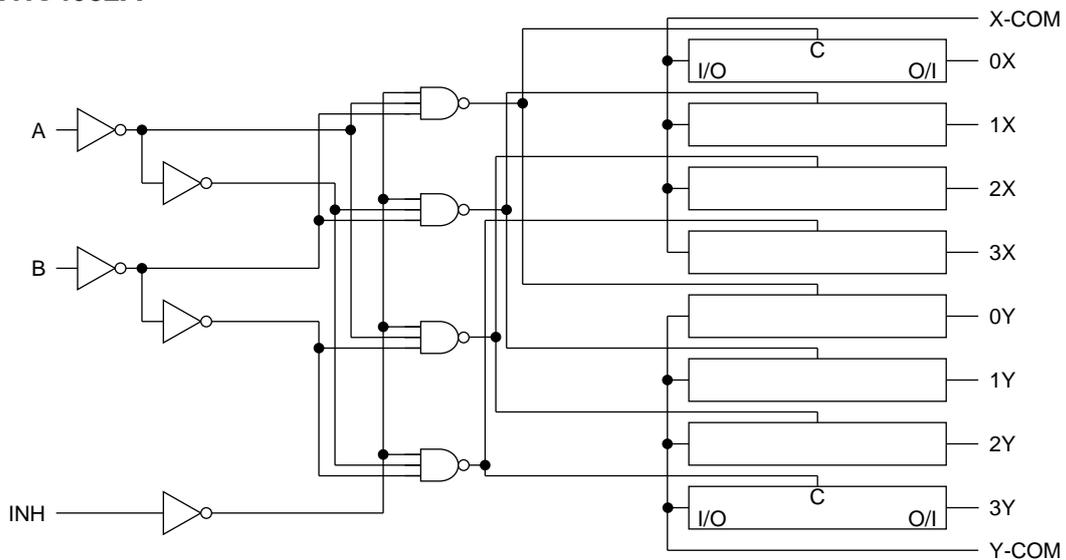
X: Don't care, *: Except VHC4052A

System Diagram

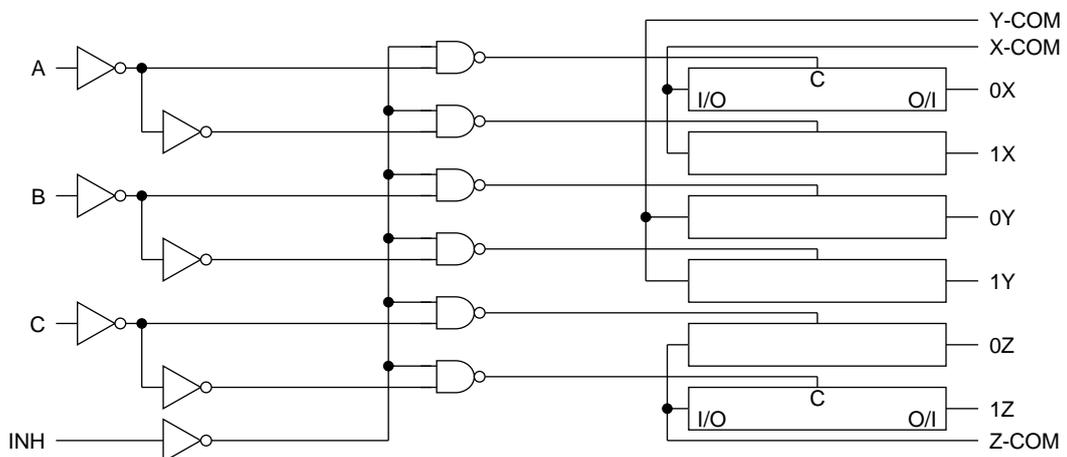
TC74VHC4051A



TC74VHC4052A



TC74VHC4053A



Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V _{CC}	-0.5 to 7.0	V
Control input voltage	V _{IN}	-0.5 to 7.0	V
Switch I/O voltage	V _{I/O}	- 0.5 to V _{CC} + 0.5	V
Input diode current	I _{IK}	-20	mA
I/O diode current	I _{IOK}	±25	mA
Switch through current	I _T	±25	mA
DC V _{CC} or ground current	I _{CC}	±50	mA
Power dissipation	P _D	180	mW
Storage temperature	T _{stg}	-65 to 150	°C

Note : Exceeding any of the absolute maximum ratings, even briefly, may lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V _{CC}	2 to 5.5	V
Input voltage	V _{IN}	0 to 5.5	V
Switch I/O voltage	V _{I/O}	0 to V _{CC}	V
Operating temperature	T _{opr}	-40 to 85	°C
Input rise and fall time	dt/dv	0 to 200 (V _{CC} = 2.5 ± 0.2 V)	ns/V
		0 to 100 (V _{CC} = 3.3 ± 0.3 V)	
		0 to 20 (V _{CC} = 5 ± 0.5 V)	

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused control inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Electrical Characteristics

Characteristics		Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C		Unit	
				V _{CC} (V)	Min	Typ.	Max	Min		Max
Input voltage	High-level	V _{IH}	—	2.0	1.5	—	—	1.5	—	V
				3.0	2.0	—	—	2.0	—	
				4.5	3.15	—	—	3.15	—	
				5.5	3.85	—	—	3.85	—	
	Low-level	V _{IL}	—	2.0	—	—	0.5	—	0.5	
				3.0	—	—	0.8	—	0.8	
				4.5	—	—	1.35	—	1.35	
				5.5	—	—	1.65	—	1.65	
ON resistance	R _{ON}	V _{IN} = V _{IL} or V _{IH} V _{I/O} = V _{CC} to GND I _{I/O} = 2 mA	2.3	—	200	—	—	—	Ω	
			3.0	—	45	86	—	108		
			4.5	—	24	37	—	46		
		V _{IN} = V _{IL} or V _{IH} V _{I/O} = V _{CC} or GND I _{I/O} = 2 mA	2.3	—	28	73	—	84		
			3.0	—	22	38	—	44		
			4.5	—	17	27	—	31		
Difference of ON resistance between switches	ΔR _{ON}	V _{IN} = V _{IL} or V _{IH} V _{I/O} = V _{CC} to GND I _{I/O} = 2 mA	2.3	—	10	25	—	35	Ω	
			3.0	—	5	15	—	20		
			4.5	—	5	13	—	18		
Input/Output leakage current (switch OFF)	I _{OFF}	V _{OS} = V _{CC} or GND V _{IS} = GND to V _{CC} V _{IN} = V _{IL} or V _{IH}	5.5	—	—	±0.1	—	±1.0	μA	
Input/Output leakage current (switch ON, output open)	I _{I/O}	V _{OS} = V _{CC} or GND V _{IN} = V _{IL} or V _{IH}	5.5	—	—	±0.1	—	±1.0	μA	
Control input current	I _{IN}	V _{IN} = V _{CC} or GND	5.5	—	—	±0.1	—	±1.0	μA	
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND	5.5	—	—	2.0	—	20.0	μA	

AC Electrical Characteristics (Input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C		Unit			
			VCC (V)	Min	Typ.	Max	Min		Max		
Phase difference between input and output	ϕ/O	CL = 15 pF RL = 1 k Ω	2.5±0.2	—	1.2	10	—	16	ns		
			3.3±0.3	—	0.8	6	—	10			
			5.0±0.5	—	0.3	4	—	7			
		CL = 50 pF RL = 1 k Ω	2.5±0.2	—	2.6	12	—	18			
			3.3±0.3	—	1.5	9	—	12			
			5.0±0.5	—	0.6	6	—	8			
Output enable time	tpZL tpZH	CL = 15 pF RL = 1 k Ω	Figure 1		2.5±0.2	—	3.3	15	—	20	ns
			Figure 1		3.3±0.3	—	2.3	11	—	15	
			Figure 1		5.0±0.5	—	1.6	7	—	10	
	CL = 50 pF RL = 1 k Ω	Figure 1		2.5±0.2	—	4.2	25	—	32		
		Figure 1		3.3±0.3	—	3.0	18	—	22		
		Figure 1		5.0±0.5	—	2.1	12	—	16		
Output disable time	tpLZ tpHZ	CL = 15 pF RL = 1 k Ω	Figure 1		2.5±0.2	—	6	15	—	23	ns
			Figure 1		3.3±0.3	—	4.5	11	—	15	
			Figure 1		5.0±0.5	—	3.2	7	—	10	
	CL = 50 pF RL = 1 k Ω	Figure 1		2.5±0.2	—	9.6	25	—	32		
		Figure 1		3.3±0.3	—	7.2	18	—	22		
		Figure 1		5.0±0.5	—	5.1	12	—	16		
Control input capacitance	CIN	All types		—	—	2	—	—	10	pF	
COMMON terminal capacitance	CIS	4051A	Figure 2	—	—	23.4	—	—	—	pF	
		4052A				13.1					
		4053A				8.2					
SWITCH terminal capacitance	COS	4051A	Figure 2	—	—	5.7	—	—	—	pF	
		4052A				5.6					
		4053A				5.6					
Feedthrough capacitance	CIOS	4051A	Figure 2	—	—	0.5	—	—	—	pF	
		4052A				0.5					
		4053A				0.5					
Power dissipation capacitance	CPD	4051A	Figure 2 (Note)	—	—	15	—	—	—	pF	
		4052A				24					
		4053A				12					

Note: CPD is defined as the value of the internal equivalent capacitance of IC which is calculated from the operating current consumption without load.

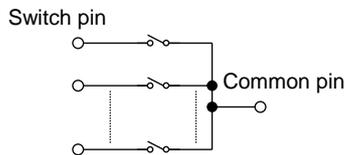
Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

Analog Switch Characteristics (Ta = 25°C) (Note)

Characteristics	Test Condition	V _{CC} (V)	Typ.	Unit	
Sine Wave Distortion (T.H.D)	R _L = 10 kΩ, C _L = 50 pF, f _{IN} = 1 kHz	V _{IN} = 2.0 V _{p-p}	3.0	0.1	%
		V _{IN} = 4.0 V _{p-p}	4.5	0.03	
Frequency response (switch ON)	V _{IN} is centered at (V _{CC} /2). Adjust input for 0dBm. Increase f _{IN} frequency until dB meter reads -3dB. R _L = 50 Ω, C _L = 10 pF, sine wave Figure 3	4051A	3.0	150	MHz
		4052A		200	
		4053A		240	
		4051A	4.5	180	
		4052A		230	
		4053A		280	
Feed through attenuation (switch OFF)	V _{IN} is centered at (V _{CC} /2). Adjust input for 0dBm. R _L = 600 Ω, C _L = 50 pF, f _{IN} = 1 MHz, sine wave Figure 4	3.0	-45	dB	
		4.5	-45		
	R _L = 50 Ω, C _L = 10 pF, f _{IN} = 1 MHz, sine wave	3.0	-65		
		4.5	-65		
Crosstalk (control input to signal output)	R _L = 600 Ω, C _L = 50 pF, f _{IN} = 1 MHz, square wave (t _r = t _f = 6 ns) Figure 5	3.0	60	mV	
		4.5	100		
Crosstalk (between any switches)	V _{IN} is centered at (V _{CC} /2). Adjust input for 0dBm. R _L = 600 Ω, C _L = 50 pF, f _{IN} = 1 MHz, sine wave Figure 6	3.0	-45	dB	
		4.5	-45		

Note: These characteristics are determined by design of devices.



AC Test Circuit

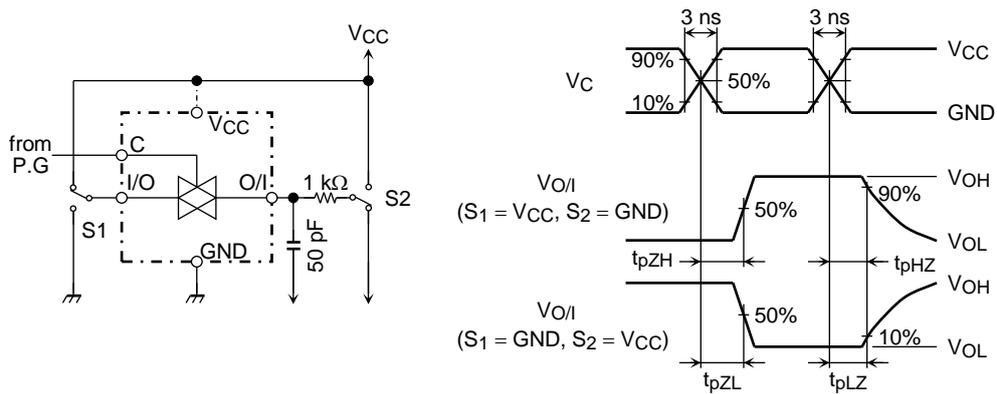


Figure 1 t_{pLZ} , t_{pHZ} , t_{pZL} , t_{pZH}

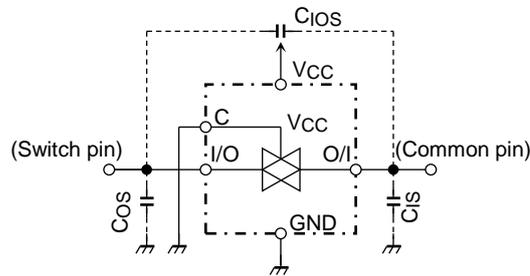


Figure 2 C_{ios} , C_{is} , C_{os}

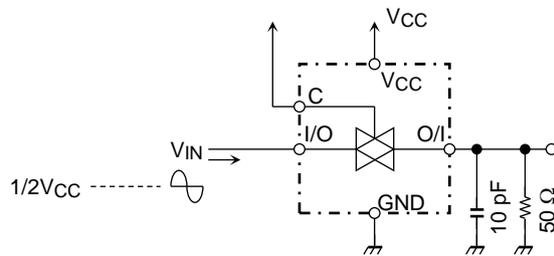


Figure 3 Frequency Response (switch on)

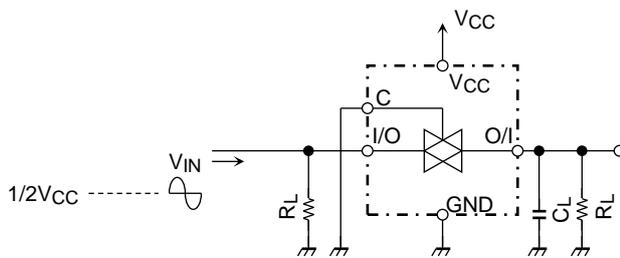


Figure 4 Feedthrough

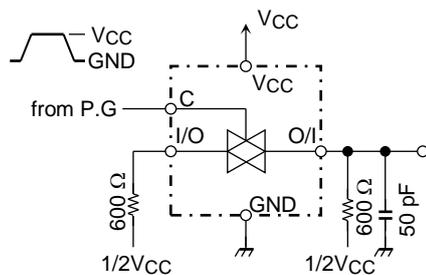


Figure 5 Cross Talk (control input to output signal)

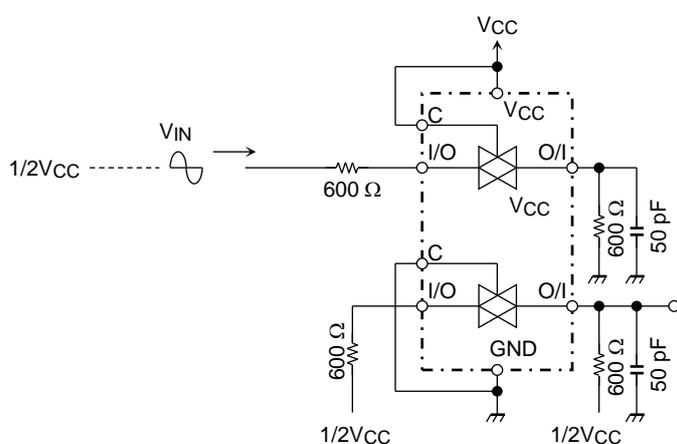
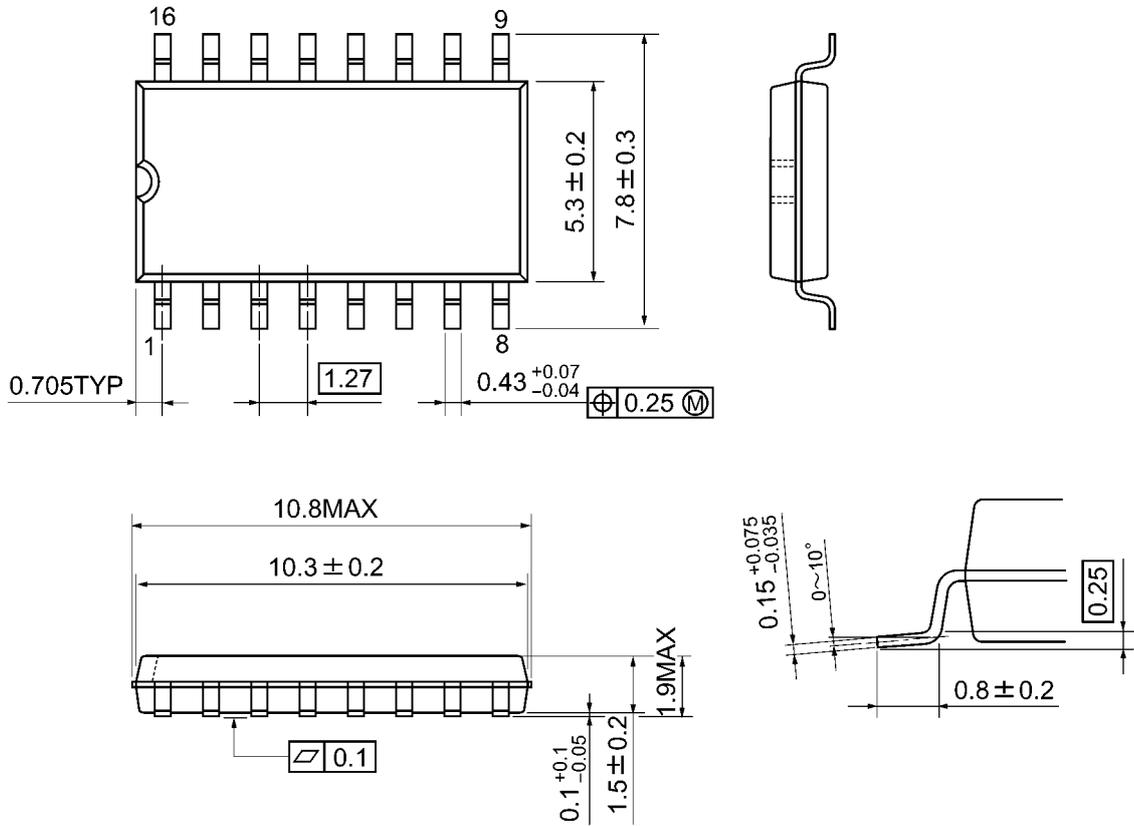


Figure 6 Cross Talk (between any two switches)

Package Dimensions

SOP16-P-300-1.27A

Unit: mm

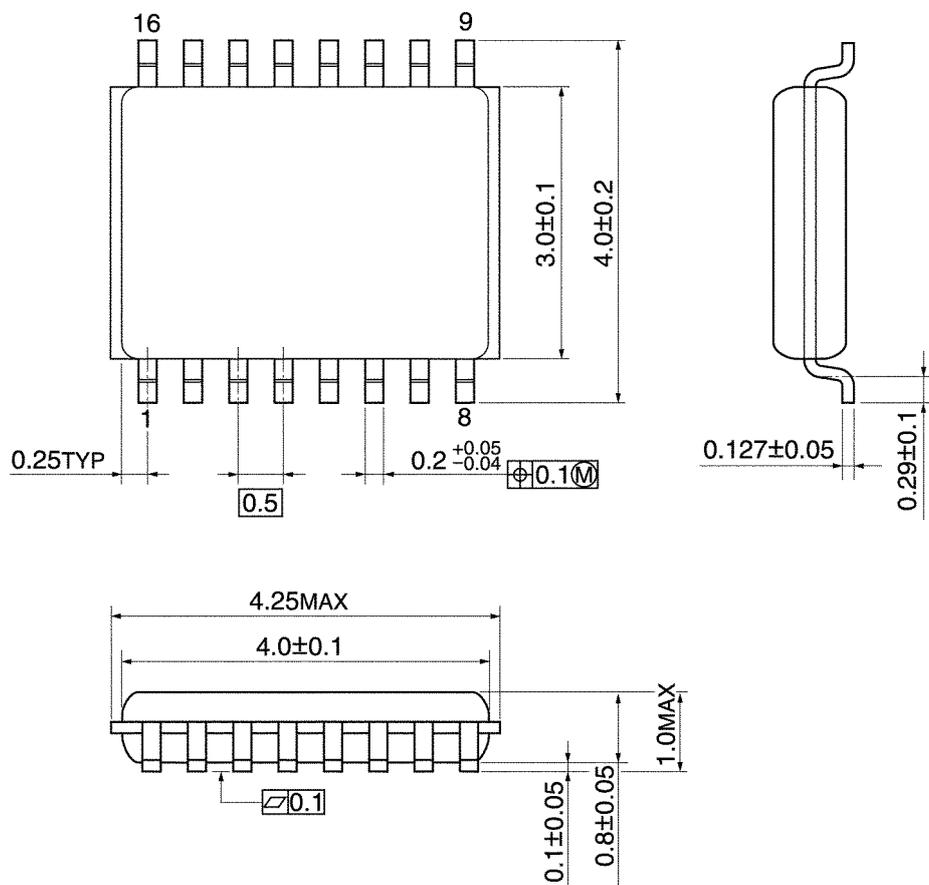


Weight: 0.18 g (typ.)

Package Dimensions

VSSOP16-P-0030-0.50

Unit: mm



Weight: 0.02 g (typ.)

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