Dear Customer January 2007

Important Notices

Thank you for your continued patronage of Toshiba microcontrollers.

This page gives you important information on using Toshiba microcontrollers. Please be sure to check each item for proper use of our products.

Restriction on Use of MAC (January 2007)

* If your datasheet is dated 20 July 2006 or earlier, please download the latest datasheet or request it from your local Toshiba office.

Restriction on Use of SPI Controller (January 2007)

* If your datasheet is dated 20 July 2006 or earlier, please download the latest datasheet or request it from your local Toshiba office.

TOSHIBA Microcontrollers TLCS- 900 Family
TLCS- 900/H1 Series

TMP92CZ26XBG TMP92CZ26AXBG TMP92CF26AXBG TMP92CF29FG TMP92CF29AFG

January 2007

Dear Customer

Restriction on Use of MAC

With regard to the TLCS- 900/H1 Series microcontrollers listed above, we have found a restriction on use of the MAC (multiply and accumulate calculation) unit, as explained below. If you have any questions or require any further information, please contact your local Toshiba sales office.

[Problem]
If the following three conditions are all met, expected calculation results cannot be obtained.

Condition 1: Signed calculation mode is selected(MACCR<MSGMD>=1).
Condition 2: Data is set to the MACMA or MACMB register in word (16-bit) or byte (8-bit) units.
Condition 3: The data that is set in the MACMA or MACMB register is negative.

[Restriction]
When using signed mode, set data to the MACMA and MACMB registers in longword (32-bit) units.

(Example)

```
LD      XWA, xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx b
LD      (MACMA),XWA
```

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Datasheet Modifications on Use of MAC

The following modifications (shown in red) will be made to the technical datasheets in the next revision.

Section: Data registers

	Data Registers							
	Bits<63:56>	Bits<55:48>	Bits<47:40>	Bits<39:32>	Bits<31:24>	Bits<23:16>	Bits<15:8>	Bits<7:0>
Multiplier A Register					(1BE3H)	(1BE2H)	(1BE1H)	MACMA (1BE0H)
Multiplier B Register					(1BE7H)	(1BE6H)	(1BE5H)	MACMB (1BE4H)
MAC Register	(1BEFH)	(1BEEH)	(1BEDH)	MACORH (1BECH)	(1BEBH)	(1BEAH)	(1BE9H)	MACORL (1BE8H)

Note 1: After reset, all the registers are cleared to “0”.

Note 2: Read-modify-write instructions can be used on all the registers.

Note 3: All the registers can be accessed in long word, word, or byte units. **(When signed mode is used, these registers can only be accessed in longword units.)**

Note 4: When MACCR<MSTTG2:0> is set to “0”, “001”, “010” or “011” and the registers are written in word or byte units, the <7:0> bits of each register must be written last.

Note 5: The MACORL register is fixed one system clock (f_{SYS}) after calculation is started, and the MACORH register is fixed two system clocks (f_{SYS}) after calculation is started. Therefore, to read the MACOR register immediately after calculation, be sure to read the MACORL register first.

Note 6: When signed mode is used (MACCR<MSGMD>=1), the MACMA and MACMB registers must be written in longword (32-bit) units.

Section: Sign mode

Use signed mode when the values to be set in the MACMA and MACMB registers are signed (two’s complement) data. Even in unsigned mode it is possible to set signed (two’s complement) data in the MACOR register to perform additions and subtractions in signed mode.

When signed mode is used (MACCR<MSGMD>=1), the MACMA and MACMB registers must be written in longword (32-bit) units.

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Dear Customer

Restriction on Use of SPI Controller

With regard to the TLCS- 900/H1 Series microcontrollers listed above, we have found a restriction on use of the SPI controller, as explained below. If you have any questions or require any further information, please contact your local Toshiba sales office.

[Problem]
If the following three conditions are all met, the SPI controller will unintentionally start a transmit operation.

Condition 1: Operation mode is set to UNIT transmit mode (SPICT<TXMOD>=0).
Condition 2: Transmission is enabled (SPICT<TXE>=1).
Condition 3: A write occurs to one of the registers listed in the attached sheets.

[Restriction]
When transmission is enabled (SPICT<TXE>=1), do not write to the registers listed in the attached sheets. A recommended control sequence in UNIT transmit mode is shown below. In UNIT transmit mode, a transmission once started will be continued until it is completed even if the <TXE> bit is cleared immediately after the start of the transmission.

```
LD      (SPITD0),A      ; Set transmit data
DI                      ; Disable interrupts
SET 3,  (SPICT)         ; Set SPICT<TXE>
RES 3,  (SPICT)         ; Clear SPICT<TXE>
EI
```

(Attachment 1-2)

● Applicable Register List (Shaded areas indicate the applicable registers.)

PORT

address	register name
0010H	P4
1H	
2H	
3H	P4FC
4H	P5
5H	
6H	
7H	P5FC
8H	P6
9H	
AH	P6CR
BH	P6FC
CH	P7
DH	
EH	P7CR
FH	P7FC

address	register name
0030H	PC
1H	
2H	PCCR
3H	PCFC
4H	
5H	
6H	
7H	
8H	
9H	
AH	
BH	
CH	PF
DH	
EH	PFCR
FH	PFFC

address	register name
0050H	PK
1H	
2H	
3H	PKFC
4H	PL
5H	
6H	
7H	PLFC
8H	PM
9H	
AH	
BH	PMFC
CH	PN
DH	
EH	PNCR
FH	PNFC

address	register name
0090H	PGDR
1H	
2H	
3H	PJDR
4H	PKDR
5H	PLDR
6H	PMDR
7H	PNDR
8H	PPDR
9H	PRDR
AH	PZDR
BH	PTDR
CH	PUDR
DH	PVDR
EH	PWDR
FH	PXDR

address	register name
00B0H	PX
1H	
2H	PXCR
3H	PXFC
4H	
5H	
6H	
7H	
8H	
9H	
AH	
BH	
CH	
DH	
EH	
FH	

Note: Do not access no allocated name address.

(Attachment 1-3)

INTC

address	register name
00D0H	INTE12
1H	INTE34
2H	INTE56
3H	INTE7
4H	INTETA01
5H	INTETA23
6H	INTETA45
7H	INTETA67
8H	INTETB0
9H	INTETB1
AH	
BH	INTES0
CH	
DH	
EH	
FH	

address	register name
00F0H	INTE0
1H	INTETC01/INTEDMA01
2H	INTETC23/INTEDMA23
3H	INTETC45/INTEDMA45
4H	INTETC67
5H	SIMC
6H	IIMC0
7H	INTWDT
8H	INTCLR
9H	
AH	IIMC1
BH	
CH	
DH	
EH	
FH	Reserved

TSI

address	register name
01F0H	TSICR0
1H	TSICR1
2H	Reserved
3H	
4H	
5H	
6H	
7H	
8H	
9H	
AH	
BH	
CH	
DH	
EH	
FH	

SDRAMC

address	register name
0250H	SDACR
1H	SDCISR
2H	SDRCR
3H	SDCMM
4H	SDBLS
5H	
6H	
7H	
8H	
9H	
AH	
BH	
CH	
DH	
EH	
FH	

Note: Do not access no allocated name address.

(Attachment 1-4)

LCDC

address	register name
0290H	LCDHSDLY
1H	LCDO0DLY
2H	LCDO1DLY
3H	LCDO2DLY
4H	LCDHSW
5H	LCDLDW
6H	LCDHO0W
7H	LCDHO1W
8H	LCDHO2SW
9H	LCDHWB8
AH	
BH	
CH	
DH	
EH	
FH	

PMC

address	register name
02F0H	PMCCTL
1H	
2H	
3H	
4H	
5H	
6H	
7H	
8H	
9H	
AH	
BH	
CH	
DH	
EH	
FH	

USB

address	register name
0500H to 067FH	Descriptor RAM (384 byte)

The following addresses in the USB descriptor RAM:
xx10H to xx13H, xx30H to xx33H, xx50 to xx53H, xx70H to xx73H, xx90H to xx93H
xxB0H～xxB3H、xxD0H～xxD3H、xxF0H～xxF3H

address	register name
0790H	EP0_STATUS
1H	EP1_STATUS
2H	EP2_STATUS
3H	EP3_STATUS
4H	
5H	
6H	
7H	
8H	EP0_SIZE_L_A
9H	EP1_SIZE_L_A
AH	EP2_SIZE_L_A
BH	EP3_SIZE_L_A
CH	
DH	
EH	
FH	

address	register name
07B0H	
1H	EP1_SIZE_H_B
2H	EP2_SIZE_H_B
3H	EP3_SIZE_H_B
4H	
5H	
6H	
7H	
8H	
9H	
AH	
BH	
CH	
DH	
EH	
FH	

address	register name
07D0H	COMMAND
1H	EPx_SINGLE1
2H	Reserved
3H	EPx_BCS1
4H	Reserved
5H	Reserved
6H	INT_Control
7H	Reserved
8H	Standard Request Mode
9H	Request Mode
AH	Reserved
BH	Reserved
CH	Reserved
DH	Reserved
EH	ID_CONTROL
FH	ID_STATE

address	register name
07F0H	USBINTFR1
1H	USBINTFR2
2H	USBINTFR3
3H	USBINTFR4
4H	USBINTMR1
5H	USBINTMR2
6H	USBINTMR3
7H	USBINTMR4
8H	USBCR1
9H	
AH	
BH	
CH	
DH	
EH	
FH	

Note: Do not access no allocated name address.

(Attachment 1-5)

MMU

address	register name
0890H	LOCALRX
1H	LOCALRX
2H	LOCALRY
3H	LOCALRY
4H	LOCALRZ
5H	LOCALRZ
6H	
7H	
8H	LOCALWX
9H	LOCALWX
AH	LOCALWY
BH	LOCALWY
CH	LOCALWZ
DH	LOCALWZ
EH	
FH	

address	register name
08B0H	LOCALOSX
1H	LOCALOSX
2H	LOCALOSY
3H	LOCALOSY
4H	LOCALOSZ
5H	LOCALOSZ
6H	
7H	
8H	LOCALODX
9H	LOCALODX
AH	LOCALODY
BH	LOCALODY
CH	LOCALODZ
DH	LOCALODZ
EH	
FH	

NANDFC

address	register name
08D0H	NDRSCA0
1H	NDRSCA0
2H	NDRSCD0
3H	
4H	NDRSCA1
5H	NDRSCA1
6H	NDRSCD1
7H	
8H	NDRSCA2
9H	NDRSCA2
AH	NDRSCD2
BH	
CH	NDRSCA3
DH	NDRSCA3
EH	NDRSCD3
FH	

DMAC

address	register name
0910H	HDMAS1
1H	HDMAS1
2H	HDMAS1
3H	
4H	HDMAD1
5H	HDMAD1
6H	HDMAD1
7H	
8H	HDMACA1
9H	HDMACA1
AH	HDMACB1
BH	HDMACB1
CH	HDMAM1
DH	
EH	
FH	

address	register name
0930H	HDMAS3
1H	HDMAS3
2H	HDMAS3
3H	
4H	HDMAD3
5H	HDMAD3
6H	HDMAD3
7H	
8H	HDMACA3
9H	HDMACA3
AH	HDMACB3
BH	HDMACB3
CH	HDMAM3
DH	
EH	
FH	

address	register name
0950H	HDMAS5
1H	HDMAS5
2H	HDMAS5
3H	
4H	HDMAD5
5H	HDMAD5
6H	HDMAD5
7H	
8H	HDMACA5
9H	HDMACA5
AH	HDMACB5
BH	HDMACB5
CH	HDMAM5
DH	
EH	
FH	

I^2S

address	register name
1810H	I2S1BUF
1H	
2H	
3H	
4H	
5H	
6H	
7H	
8H	I2S1CTL
9H	I2S1CTL
AH	I2S1C
BH	I2S1C
CH	
DH	
EH	
FH	

Note: Do not access no allocated name address.

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Datasheet modifications on Use of SPI Controller

In the next revision of the technical datasheets, the following note (shown in red) will be added to the description of the TXE bit and the subsection "Difference points between UNIT transmission and Sequential transmission" in the chapter on the SPI controller.

Important Note:

When UNIT mode is selected (SPICT<TXMOD>=0), the following restriction applies.

After setting SPICT<TXE>=1, do not modify the contents of other registers until the UNIT transmission completes.

Program Sample 1:

```
        LD      (SPITDx), A     ; Set transmit data
        DI                      ; Disable interrupts
        SET 3,  (SPICT)         ; TXE=1 to start transmission

Wait:   BIT 1,  (SPIST)         ; Wait until transmission completes
        JPZ,    Wait            ;
        RES 3,  (SPICT)         ; TXE=0 to disable transmission
        EI                      ; Enable interrupts
```

Program Sample 2 (Recommend):

Check the transmit status flag to make sure that the previous transmission has completed (SPIST<TEND>=1).

```
        LD      (SPITDx), A     ; Set transmit data
        DI                      ; Disable interrupts
        SET 3,  (SPICT)         ; TXE=1 to start transmission
        RES 3,  (SPICT)         ; TXE=0 to disable transmission
        EI                      ; Enable interrupts
```