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e-Learning

Basics of CMOS Logic ICs

Chapter2 Basic Operations of CMOS Logic ICs

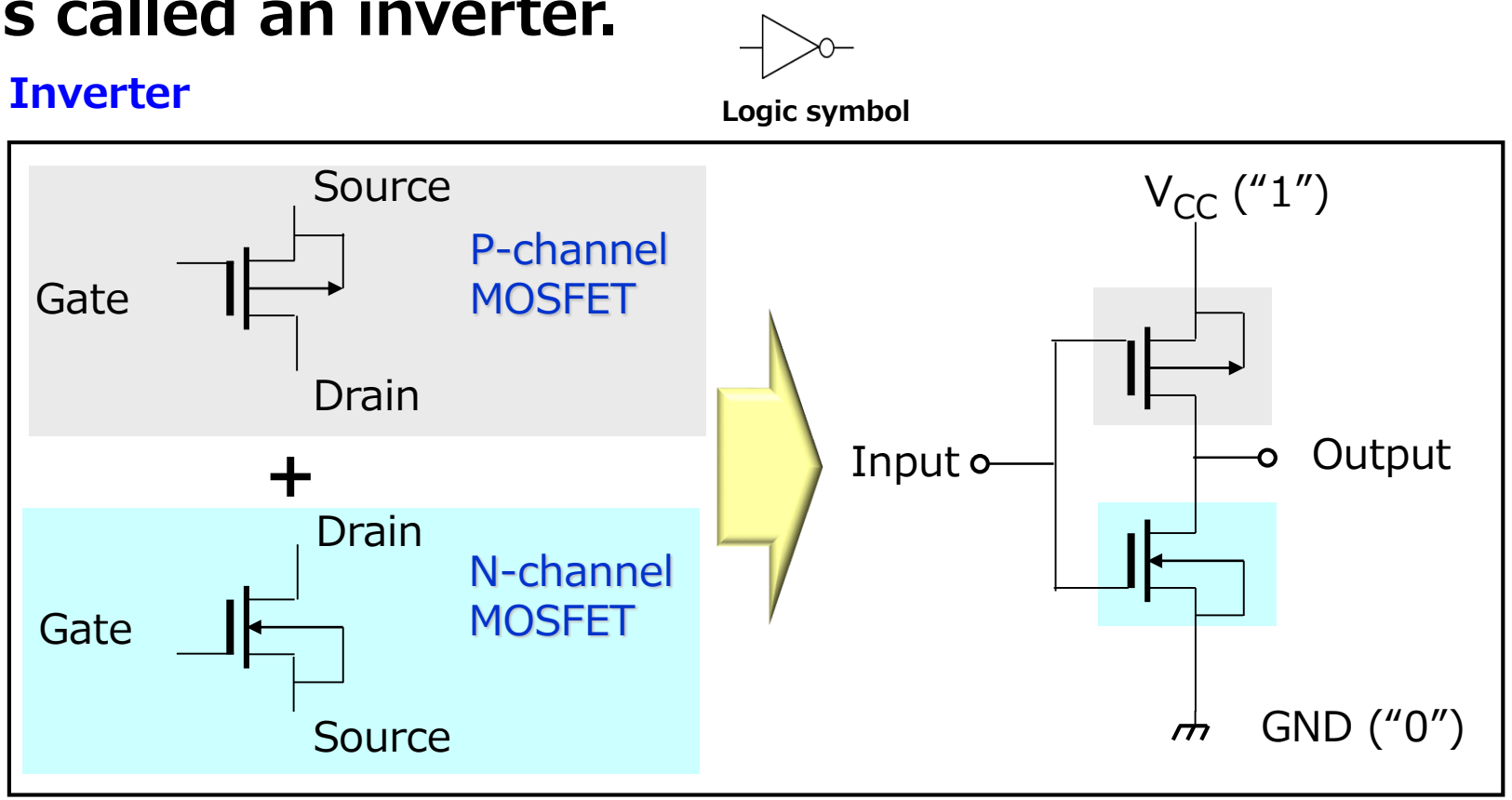
Toshiba Electronic Devices & Storage Corporation

02

Basic operations of CMOS Logic ICs

2.1 What is a CMOS Logic IC?

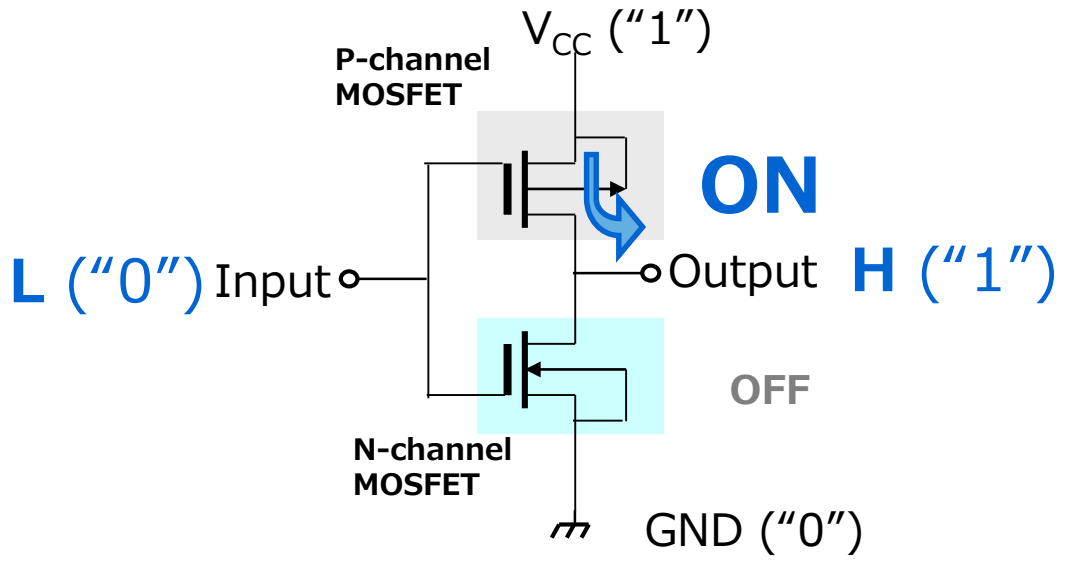
A circuit that uses complementary pairs of p-channel and n-channel MOSFETs is called CMOS (Complementary MOS). CMOS logic ICs combine MOSFETs in various ways to implement logic functions.
A logic gate composed of a single pair of p-channel and n-channel MOSFETs is called an inverter.



2.2 Basic CMOS Logic ICs: #1

The following briefly describes the operation of an **inverter**.

When the input is Low



*** V_{CC}: Supply voltage**

Truth

Input	Output
L	H
H	L

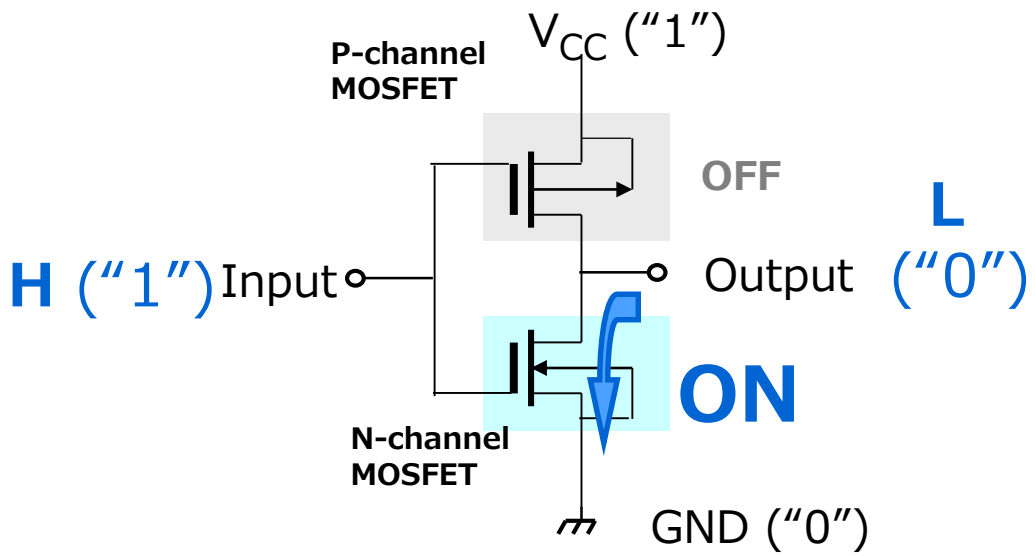
When the input is Low, the n-channel MOSFET is **off**, and the p-channel MOSFET is **on**.

At this time, V_{CC} and the output are electrically connected.

The output signal is driven to High (V_{CC} ”1”).

2.2 Basic CMOS Logic ICs: #1

When the input is High



When the input is High, the n-channel MOSFET is **on**, and the p-channel MOSFET is **off**.

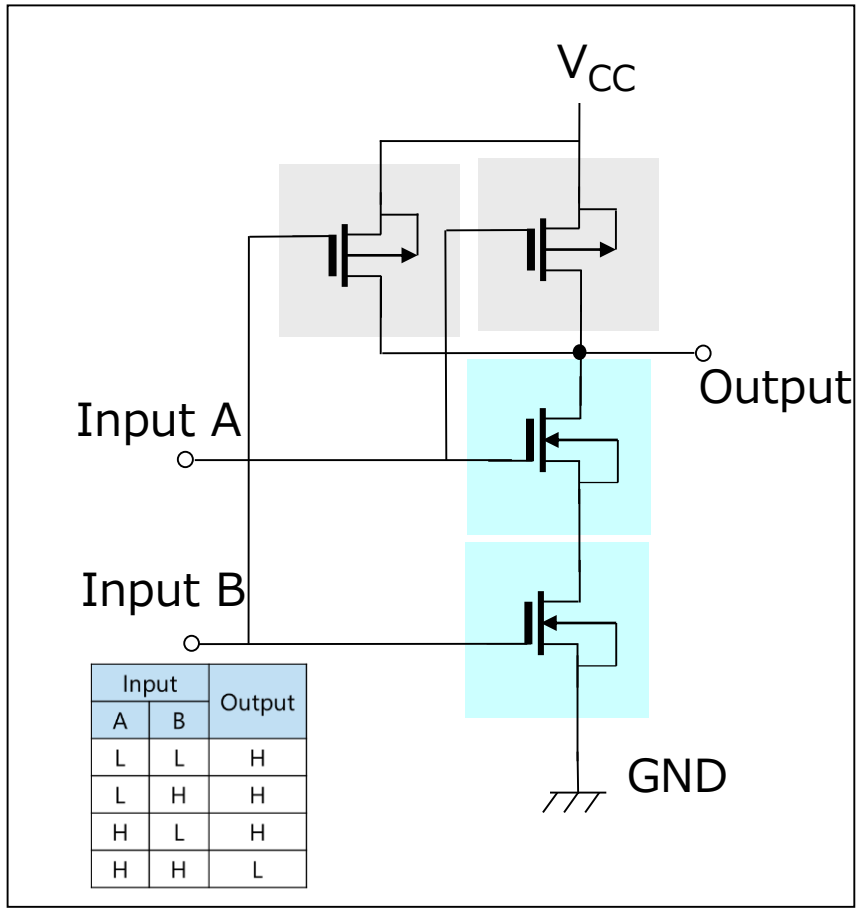
At this time, GND and the output are electrically connected.

The output signal is driven to Low (GND "0").

2.2 Basic CMOS Logic ICs: #2

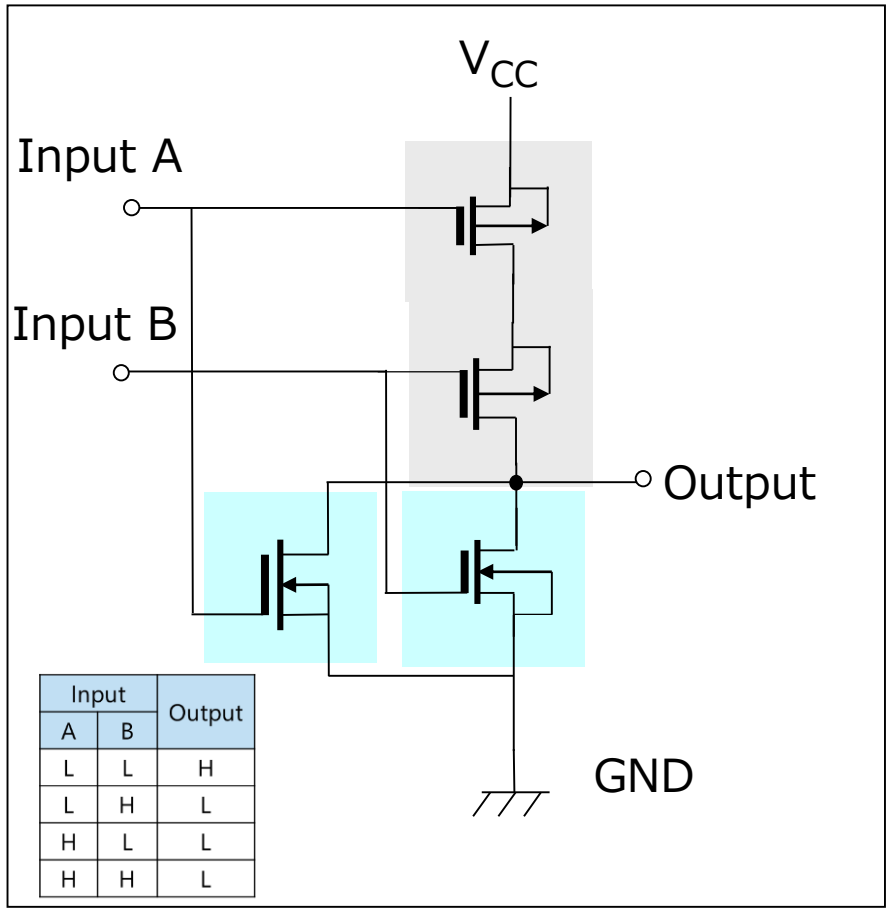
Various logic functions can be implemented by combining p-channel and n-channel MOSFETs.

2-input NAND gate



Input		Output
A	B	
L	L	H
L	H	H
H	L	H
H	H	L

2-input NOR gate



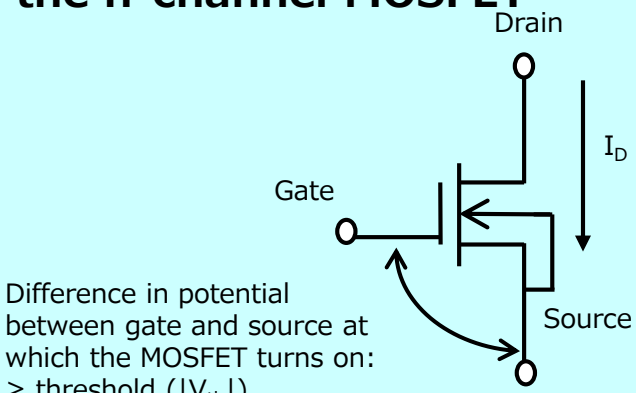
Input		Output
A	B	
L	L	H
L	H	L
H	L	L
H	H	L

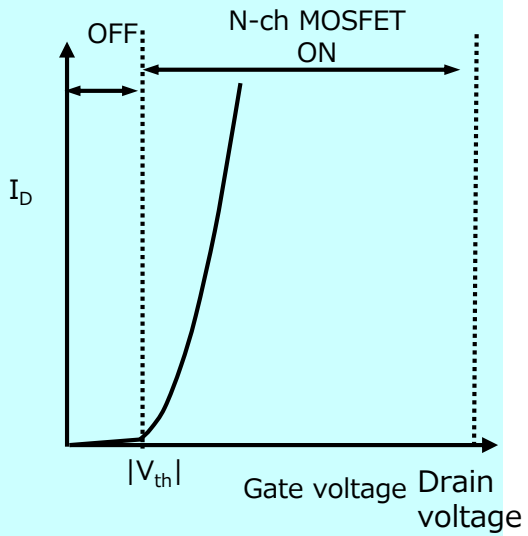
2.3 Basic operations of CMOS Logic ICs: #1

When the gate-source voltage of a MOSFET exceeds a certain voltage (threshold voltage, $|V_{th}|$), the drain-source resistance decreases, causing the MOSFET to turn on. This drain-source resistance is called on-resistance.
The direction of the voltage applied across gate and source differs between n-channel and p-channel MOSFETs. The following figure shows the condition under which a MOSFET turns on.

N-channel MOSFET: When the gate voltage is higher than the source voltage by $|V_{th}|$, the n-channel MOSFET turns on.

Characteristics of the n-channel MOSFET



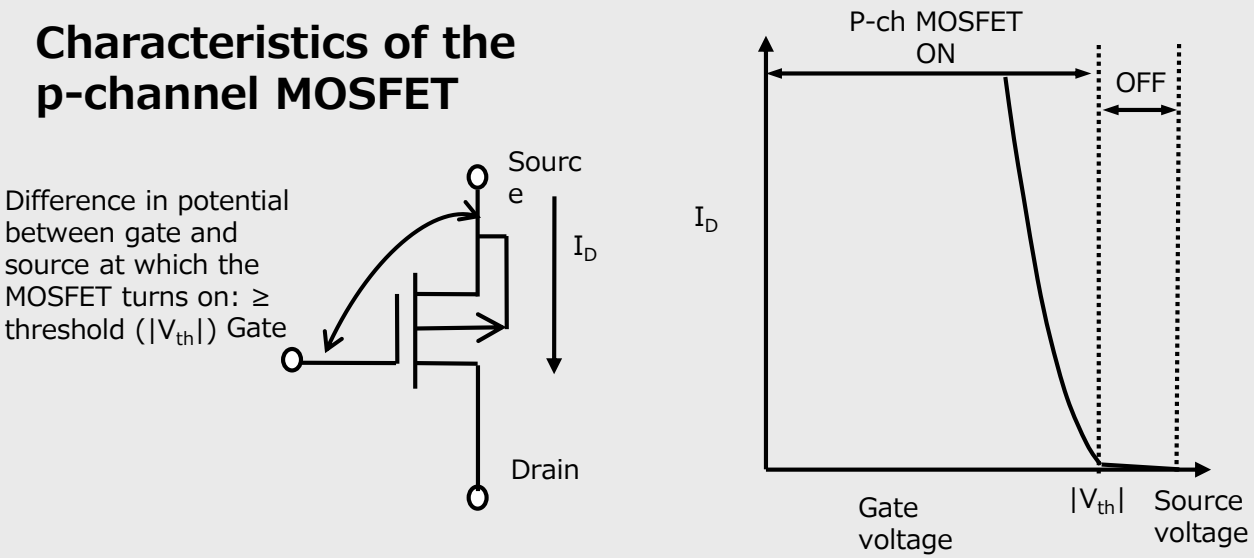


Apply positive voltage to the gate with respect to the source.

2.3 Basic operations of CMOS Logic ICs: #1

P-channel MOSFET: When the gate voltage is lower than the source voltage by $|V_{th}|$, the p-channel MOSFET turns on.

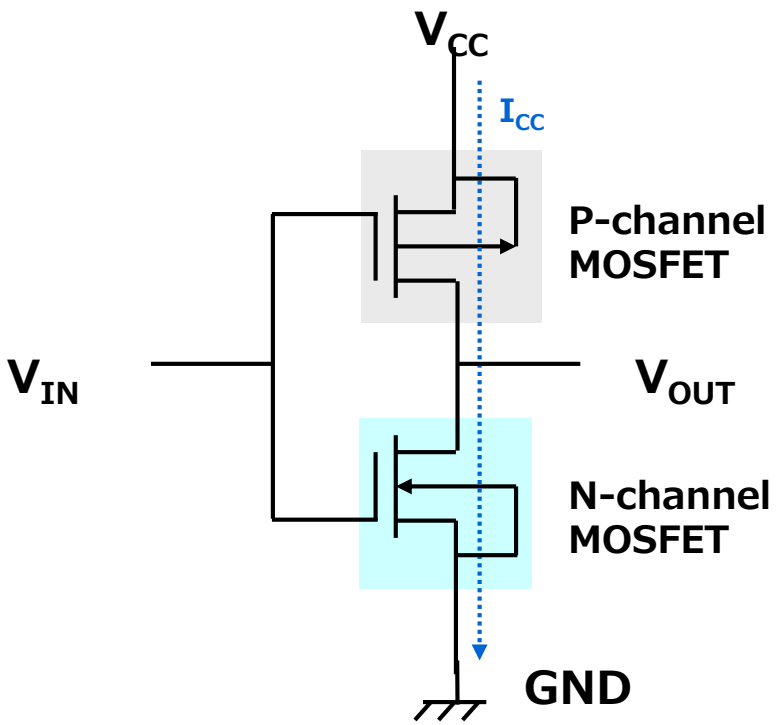
Characteristics of the p-channel MOSFET



Apply negative voltage to the gate with respect to the source.

2.3 Basic operations of CMOS Logic ICs: #2

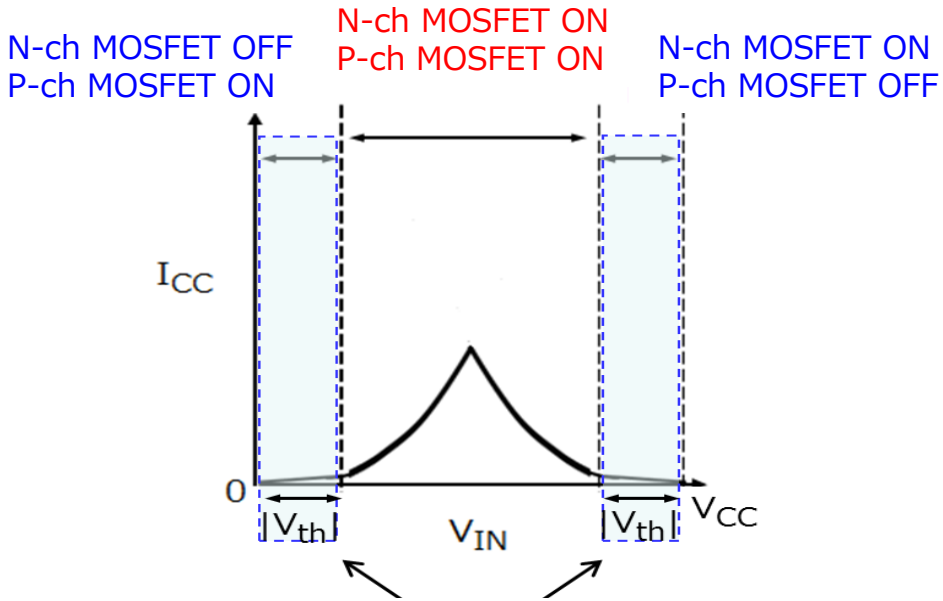
The following figure shows an inverter, a basic building block of CMOS logic ICs.
When V_{IN} is at the V_{CC} or GND level, either the p-channel or n-channel MOSFET is off. Therefore, very little current (I_{CC}) flows between V_{CC} and GND. When the input is in the steady state (at the V_{CC} or GND level), I_{CC} is very low.



Building block of the CMOS logic IC (inverter)

2.3 Basic operations of CMOS Logic ICs: #2

The following figure shows the V_{IN}-I_{CC} curve of CMOS.
When V_{IN} is between 0 and $|V_{th}|$ or between $V_{CC}-|V_{th}|$ and V_{CC}, very little current (I_{CC}) flows between V_{CC} and GND. However, when V_{IN} is between $|V_{th}|$ and $V_{CC}-|V_{th}|$, shoot-through current flows from the p-channel MOSFET to the n-channel MOSFET, increasing I_{CC}. Therefore, care should be exercised to ensure that excessively slowly changing input is not applied to V_{IN}.



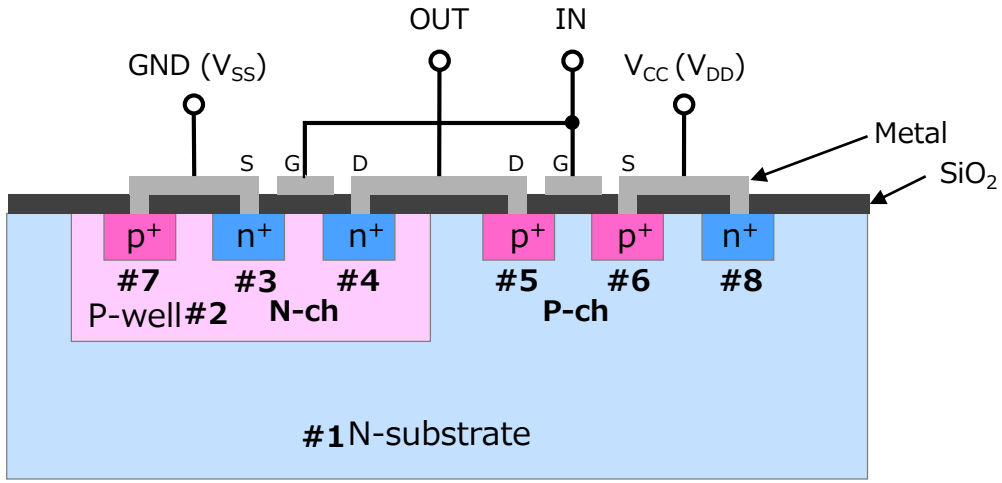
V_{IN}-I_{CC} curve of the CMOS logic IC

2.4 Basic configuration of CMOS Logic ICs

- **Example of the cross section of a CMOS logic IC**

> A wide diffusion region (p-well) is formed in the n-substrate.
> An n-channel MOSFET is formed on the p-well.
> A p-channel MOSFET is formed on the n-substrate.
> An n-well is formed on a p-substrate, depending on the process.
> Since the performance and integration density of MOSFETs are determined by the gate width, the manufacturing process is expressed with the gate width. For example, a CMOS process with a gate width of 1.0 μm is called a 1.0-μm CMOS process.
(In this case, the gate width is the distance between #3 and #4 and between #5 and #6.)

#1. N-substrate: Typically, a wafer substrate
#2. P-well: Region for forming an n-channel MOSEFT
#3. Diffused region for the source of the n-channel MOSFET
#4. Diffused region for the drain of the n-channel MOSFET
#5. Diffused region for the drain of the p-channel MOSFET
#6. Diffused region for the source of the p-channel MOSFET
#7. Diffused region for p-well bias
#8. Diffused region for n-substrate bias



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