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Improved reliability of 1.2kV SiC MOSFET by preventing the intrinsic body diode operation

Masaru Furukawa[1], Hiroshi Kono [1], Kenya Sano [1], Masakazu Yamaguchi [1], Hisashi Suzuki [1], Tadashi Misao [1], and Georges Tchouangue [2]

[1] Toshiba Electronic Devices & Storage Corporation, Japan
[2] Toshiba Electronics Europe GmbH, Germany

Corresponding author: Masaru Furukawa, masaru1.furukawa@toshiba.co.jp

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Abstract

One of the issues of SiC MOSFET is the reliability of its intrinsic body diode when used as a free-wheeling diode (FWD). The reverse current through the SiC MOSFET may cause R_{on} degradation over time. A new structure of a SBD-embedded MOSFET has been proposed that prevents the current conduction through its intrinsic body diode. A low $R_{on}A$ 1.2kV class SBD-embedded SiC MOSFET has been realized that improves its reliability by optimizing the SBD structure.

1 Introduction

As shown in Figure 1, a PN diode exists between the drain and source of a power MOSFET. That PN diode is called a body diode. Body diodes are not used in all application circuits in power electronics, but may be used as free wheel diode in some applications for general motor control for example. When a forward voltage is applied to the body diode of the SiC-MOSFET, a SSF (single shockley stacking fault) takes place at the location of the BPD (basal plane dislocation) [1]. As result, the on-voltage of the body diode and the resistance of the MOSFET increase. We have prototyped a SiC-PN diode sample. The expansion of such dislocations could be monitored before and after energizing the SiC-PN diode. Figure 2 shows the images obtained before and after applying a forward current stress to the SiC-PN diode sample using a electroluminescence measurement tool. The dark triangular area in the figure is the area where dislocations are expanded and a carrier conduction is hindered. When a voltage higher than the diode on-voltage is applied to the PN junction of the body diode, a current flows through the body diode and at the same time, generates energy that expands the dislocations in the epi-layer of the SiC-MOSFET. We have solved those problems by incorporating SBDs in the MOSFET cells. In Si products, Toshiba had released MOSFET products that incorporate SBDs into MOSFET cells as the "SSM5H" and "SSM5G" series [2]. There are also reports of SiC MOSFET products that incorporate SBDs into MOSFET cells for high breakdown voltage products such as 3.3kV or higher [3][4]. (regarding a high breakdown voltage product, since the ratio of the channel resistance to the total resistance is low even at room temperature the effect of the incorporating SBD on the increasing Ron is small). However, for products with a breakdown voltage of less than 1.2kV, there is a problem that Ron increases when SBD is incorporated. We have developed a 1.2kV SiC-MOSFET that overcomes the problem of reliability due to energization while suppressing the increase in Ron by optimizing the structure of the SBD and MOSFET. Chapter 2 explains the principle of operation of the new SiC-MOSFET structure and its important parameters. Chapter 3 describes the results of the device prototyped using the new structure.

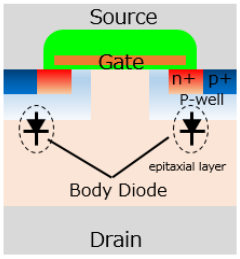

Fig. 1: Cross section of power MOSFET and body diode.

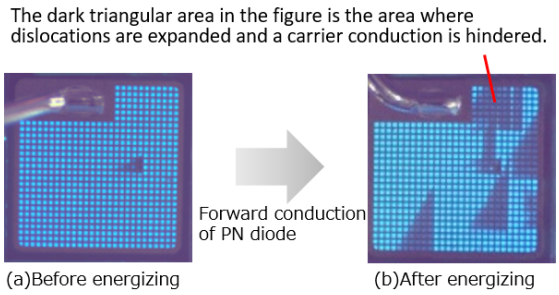

Fig. 2: Electroluminescence images of SiC-PN diode (a) before and (b) after energizing

2 Device structure and operation

2.1 Concept of improvement

The basic design policy is to avoid the body diode to be energized. By incorporating a SBD with a much lower on-state voltage compared to the parallel connected PN diode (about 2.5V) inside the cell, the forward current flow through the body diode has been suppressed. Figure 3 is a cross section view of the SBD-embedded MOSFET, and its equivalent circuit.

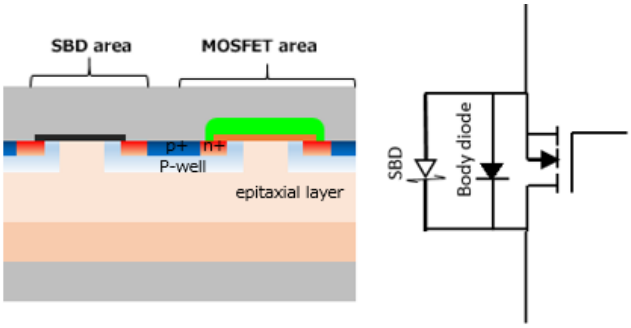

Fig. 3: A cross section view of SBD-embedded MOSFET, and its equivalent circuit

2.2 Operation principle and main parameters of the SBD-embedded MOSFET

When a positive voltage is applied to the source side with respect to the drain, the current flows through the embedded SBD, because it has a lower on-state voltage compared to the PN diode. The current path is as shown by the red arrow in Figure 4. The main resistance components in that current path are R_{jbs}, R_{spread}, and R_{drift}. The voltage V_{pn} across the PN junction when the current I flows can be described as follows.

$$V_{pn} = V_k + (R_{jbs} + R_{spread}) \cdot \mathrm{I} \quad (1)$$

V_k : Schottky barrier of SBD

Assuming that the on-state voltage of the PN diode is V_{on}, the operation of the body diode that causes characteristic degradation does not occur in the following range :

$$V_{on} > V_{pn} = V_k + (R_{jbs} + R_{spread}) \cdot \mathrm{I} \quad (2)$$

By transforming the equation, the range where no current flows through the body diode is as follows:

$$\mathrm{I} < \frac{V_{on} - V_k}{R_{jbs} + R_{spread}} \quad (3)$$

Since the maximum value of the current in the range where the above PN diode does not operate is the maximum value of the unipolar operation current, it is expressed as I_{umax} as

$$I_{umax} = \frac{V_{on} - V_k}{R_{jbs} + R_{spread}} \quad (4)$$

In order to increase the allowable current of the SBD-embedded MOSFET, it is necessary to reduce V_k, R_{jbs}, and R_{spread} as much as possible (from above equation). However, these parameters have a trade-off relation with other characteristics of the power MOSFET. So, it is necessary to determine the optimal design values. R_{jbs} is determined by the distance between the P regions on both sides and the donor concentration in the current path. It also has a trade-off relationship with the SBD electrode electric field during the off state. R_{spread} is the spreading resistance from the SBD region and is determined by the donor concentration in the under region of the P region. It has a trade-off relationship with the electric field at the PN junction. Increasing the donor concentration to lower R_{jbs}, and R_{spread} tends to increase the electric field at the SBD electrode and PN junction during the off state. That increases the leakage current between the drain and source. In order to suppress the operation of the body diode, it is also necessary to consider the mixed ratio of the SBD cells. Increasing I_{umax} requires increasing the mixing ratio of the SBD so

that the current flow can reach below the P region as wide as possible from the SBD. But increasing the SBD mixing ratio increases the overall R_{on} of the SiC-MOSFET.

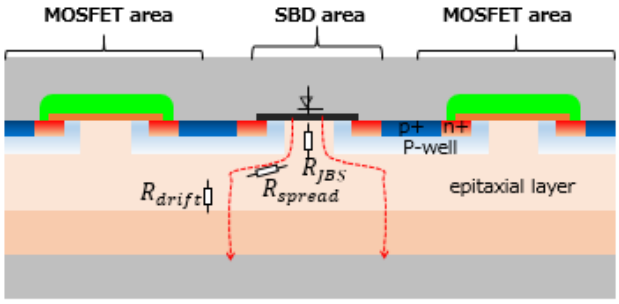

Fig. 4: Current path (red arrow) and main resistance components when current flows through SBD

3 Device evaluation

3.1 Definition of maximum reverse unipolar current

The maximum reverse unipolar current density (J_{umax}) is calculated considering the fact that the slope of the I-V characteristic is different between the unipolar region and the bipolar region. Specifically, it is defined by the change value of the first derivative of I_{sd} by V_{sd} (the value of the 2nd derivative of I_{sd} by V_{sd}), and its validity was verified by long-term reliability evaluation. In addition to a conventional MOSFET with 1.2kV breakdown voltage, we have fabricated and evaluated SBD- embedded MOSFET with the ratio of SBD : MOSFET = 1:N (N = 1 to 4)
(Figure 4 is N=1 SBD- embedded MOSFET)
Figure 5 shows the I-V characteristics of (a) a conventional MOSFET and (b) N=1 SBD-embedded MOSFET at T_j = 175°C. J_{sd} and V_{sd} are the source to drain current density and the related source to drain voltage respectively. Figure 6 illustrates dI_{sd}/dV_{sd}, the first (1st) derivative of I_{sd} (source-drain current) by V_{sd} and $d^2I_{sd}/dV_{sd}{}^2$, the 2nd derivative of I_{sd} by V_{sd} as a function of I_{sd}. I_{sd} value as J_{umax} is defined when the second derivative of I_{sd} by V_{sd} is 2.5.

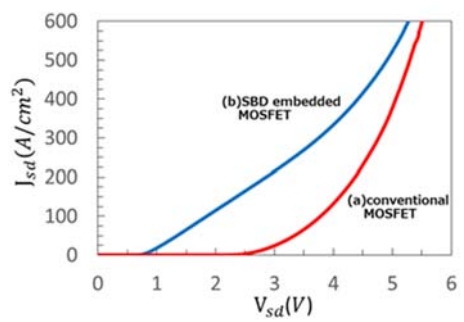

Fig. 5: I-V characteristics of (a) Conventional MOSFET and (b) N=1 SBD-embedded MOSFET at T_j = 175°C.

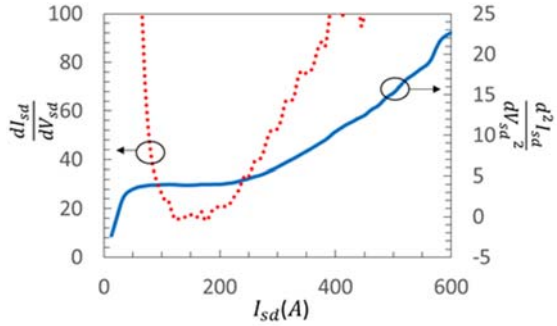

Fig. 6: J_{sd} as the horizontal axis and left side of vertical axis is first derivative of I_{sd} by V_{sd} and right side of vertical axis is 2nd derivative of I_{sd} by V_{sd}

3.2 Characteristics of SBD-embedded MOSFET

The maximum reverse unipolar current is determined by the parameters V_{on}, V_k , R_{jbs}, and R_{spread} as shown in equation (3) in Chapter 2, and each parameter is strongly affected by the temperature. In Figure 7, the maximum reverse unipolar current at each temperature value was calculated according to the method described at the section 3.1 : the I_{sd}-V_{sd} characteristics at a several temperature values in the range of Tj = 80 to 175 ° C. The range below J_{umax} is the safety operating area. We conducted continuous DC energization tests up to 1000 hours under multiple conditions arbitrarily selected in a range smaller than J_{umax} and confirmed that there was no degradation of R_{on} (an example is shown in Figure 11). Figure 8 shows the dependence of the SBD ratio on J_{umax} at T_j = 175°C and R_{on} at T_j = 25°C. The SBD ratio was optimized considering the rated current of the product. Figure 9 shows the temperature dependence of R_{on} in the conventional MOSFET and SBD-embedded

MOSFET. Compared with the conventional MOSFET, the SBD-embedded MOSFET has a lower channel density, so R_{on} increases and the ratio of the channel resistance component increases. However, since the channel resistance component has a negative temperature tendency, Ron in the high temperature region tends to be asymptotic to that of the conventional MOSFET. In fact, in the high temperature range used in applications, the $R_{on}A$ of the SBD-embedded MOSFET is less than 1.2 times of that of the conventional MOSFET. Figure 10 shows the trade-off benchmark between the $R_{on}A$ and V_{th} at T_j = 150°C (comparison with commercialized 1.2kV discrete SiC MOSFETs). Figure 11 shows the results of DC current evaluation up to 1000 hours at a current density of 250 A/cm^2 and T_j = 175°C for (a) conventional MOSFET and (b) SBD-embedded MOSFET. By optimizing the SBD ratio, the reliability of the 1.2kV class SiC MOSFET could be realized.

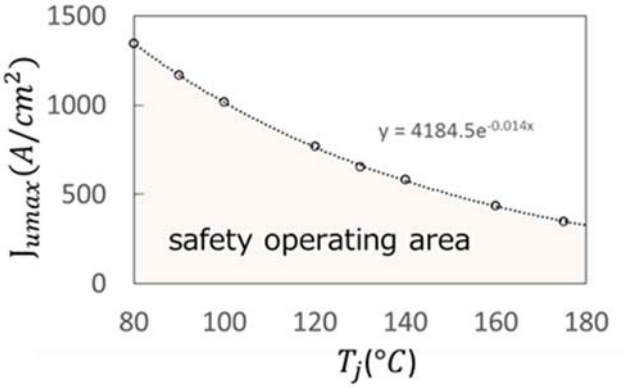

Fig. 7: Temperature dependent of J_{umax}

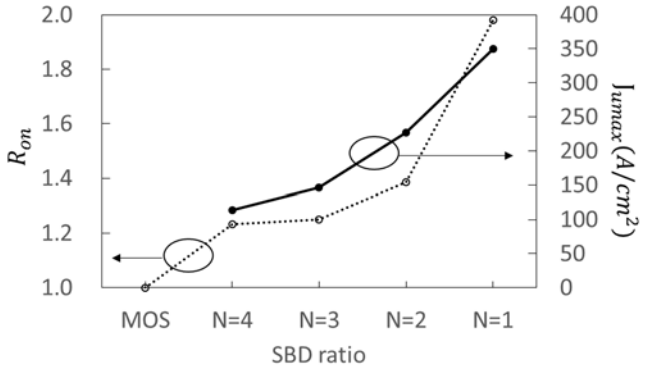

Fig. 8: Dependence of SBD ratio on J_{umax} at T_j = 175°C and R_{on} at T_j = 25°C.
(R_{on} is expressed by normalizing MOSFET to 1)

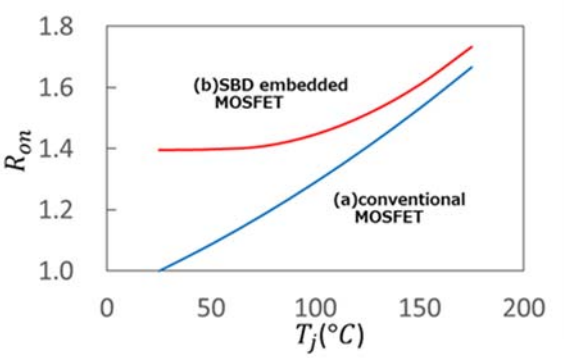

Fig. 9: Temperature dependence of R_{on} in the conventional MOSFET and SBD-embedded MOSFET

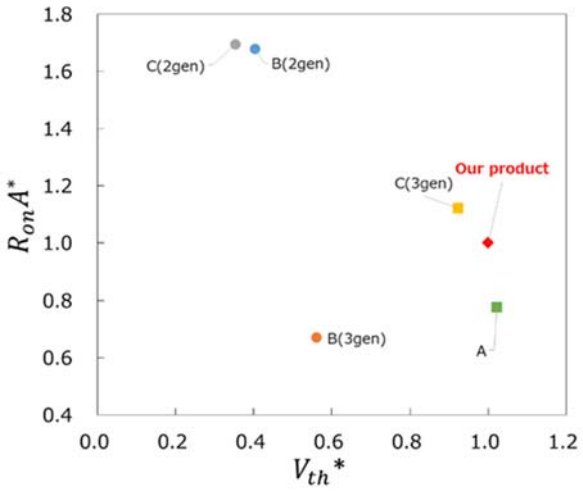

Fig. 10: Trade-off benchmark between the $R_{on}A$ * and V_{th}* at T_j = 150°C comparison with commercialized 1.2kV discrete SiC MOSFETs
(* $R_{on}A$ and Vth are normalized to 1 (device under test))

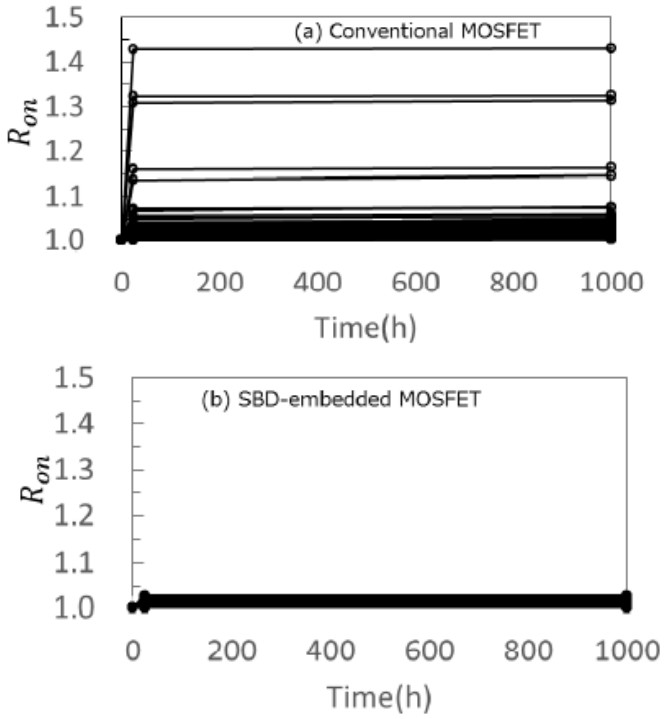

Fig. 11 : R_{on} stability test by DC current stress up to 1000 hours at a current density is 250 A/cm^2 and T_j = 175°C for (a) Conventional MOSFET and (b) SBD-embedded MOSFET

4 Conclusion

We have solved the reliability problem caused due to energizing the body diode of the SiC-MOSFET by adopting a structure in which the SBD cells are arranged in parallel with the MOSFET cells. In addition, by optimizing the structure of the SBD, the Ron has been minimized to achieve the best trade-off.

5 References:

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