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Study of Unique ESD Tolerance Dependence on Backgate Ratio for RESURF LDMOS with Rated Voltage Variation

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***Abstract*—This paper describes that an unique ESD tolerance dependence on a backgate ratio of fully isolated RESURF LDMOS for various cases of rated voltage. For the LDMOS of rated voltage below 60V, the ESD tolerance increases as the backgate ratio increases, which is well-known method to achieve the highly-ESD tolerant devices though scarifying the on-resistance. However, the LDMOS of rated voltage above 80V shows no dependence on the backgate ratio. The mechanism of this phenomenon has been investigated utilizing 2D TCAD simulation and found that the electrical potential of a floating N+buried layer contributes to parasitic bipolar action during ESD events and determines the ESD tolerance. The LDMOS design has to be carefully performed with considering this unique ESD tolerance dependence on the backgate ratio.**

Keywords—fully isolated RESURF LDMOS, backgate ratio, ESD tolerance, parasitic bipolar action, breakdown voltage, on-resistance

I. INTRODUCTION

Low on-resistance (RonA), high breakdown voltage (BVdss) and high electrostatic discharge (ESD) tolerance are important features of LDMOS, especially which is used for output devices [1-3]. In addition, for the use of automotive products, the requirement of high breakdown voltage to negative bias is also increasing. In case of nLDMOS, an isolated P-RESURF (Reduced Surface Field) layer is formed between an N+buried layer (NBL) and an N+drain region and the thickness and/or dopant concentration increase are general methods to achieve a high breakdown voltage to negative bias input [4-5] (Fig. 1). As for a RESURF nLDMOS case, P-RESURF concentration increase also leads to a higher BVdss and a higher rated voltage. Because higher P-RESURF concentration contributes to increasing N+drain/P-RESURF/NBL punch-through voltage. On the contrary, high P-RESURF concentration causes ESD tolerance degradation due to the high electrical field under the drain during the ESD events [6]. This is because the device with higher P-RESURF layer isolates the drain from NBL region further than the device with lower P-RESURF concentration so that the current flow concentrates only in the drain region. To resolve this problem, it is widely known that the backgate (BG) ratio (Fig. 2) increase is effective, although it has a trade-off relation with RonA [7]. In this study, the characteristics of various rated voltage fully isolated RESURF nLDMOSs were investigated focusing on BG ratio and found that ESD tolerance dependence on the BG ratio differs by the LDMOS's rated voltage. The reason why the behavior differs among the several rated voltage LDMOS is investigated by using 2D TCAD simulation and clarify that the parasitic bipolar actions due to the electrical potential of NBL during the ESD events play an important role to determine the ESD tolerance.

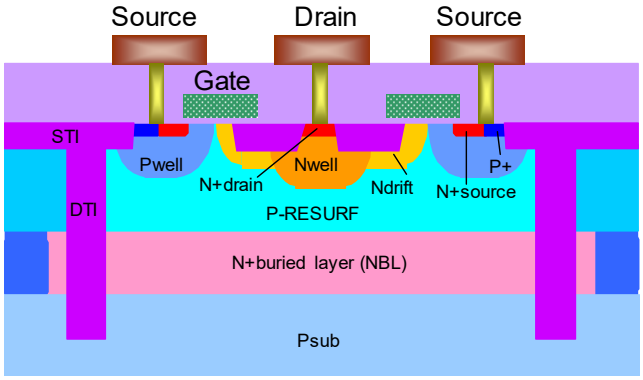


Fig. 1. Cross-sectional view of a fully isolated RESURF nLDMOS.

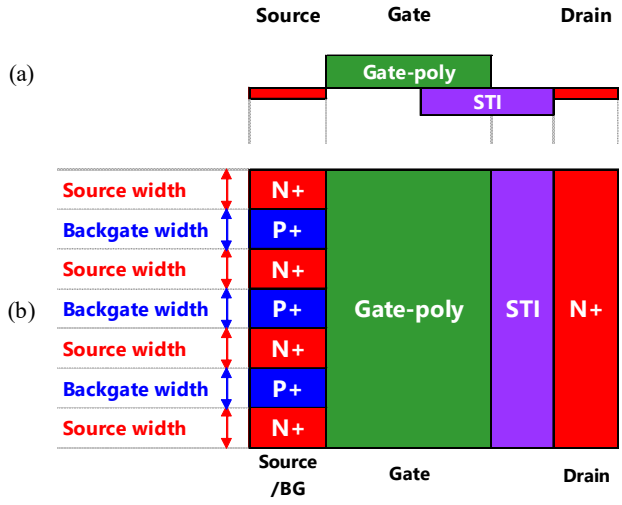


Fig. 2. (a) Cross-sectional view and (b) plain view of nLDMOS. Defined BG ratio = total BG width / (total source width + total BG width).

II. Device Structure and Experiment

The device was fabricated with 0.13μm Bipolar-CMOS-DMOS technology [6]. Schematic cross-sectional and plain views of the studied LDMOS are shown in Figs 1 and 2. Source and BG region are alternately repeated in the width direction. BG ratio is defined by a ratio of the total BG width to the sum of the total source and BG width as shown in Fig. 2 (b). The studied LDMOS rated voltages vary from 25V to 96V, which realize appropriate BVdss by adjusting STI length between the drain and source. In addition, in case of the higher rated voltage LDMOS above 50V, P-RESURF doping concentration is also optimized in order to maintain the N+drain/P-RESURF/NBL vertical punch-through voltage higher than the source/drain breakdown voltage in lateral direction. For evaluating ESD characteristics, Human Body Model (HBM) is used. For the measurement, a wafer ESD tester, 'HED W5100D (Hanwa Electronic Industries)' was used. The measurement circuit for HBM test is described in Fig. 3. Source/BG and gate electrodes were connected to 100 kΩ resistance respectively by layout design. In the test, positive surge was injected to the drain electrode, while the source/BG electrode was grounded. The surge voltage was applied with an increment of 100V until the device was destroyed. HBM results were defined from its drain-source leakage current change. Fig. 4 is the HBM tolerance dependence on the BG ratio and it is noted that the quite different behavior in LDMOS design for each rated voltage were shown. Below 60V case, HBM tolerance and BG ratio has a positive correlation, nevertheless, almost no dependence is observed in above 80V case. In order to understand these characteristics, 2D TCAD (Synopsys Sentaurus) was carried out.

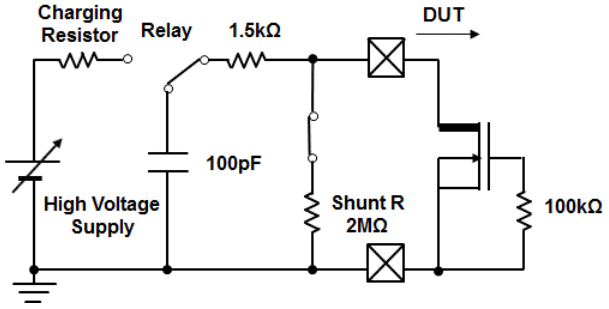


Fig. 3. Illustration of the measurement circuit for HBM test.

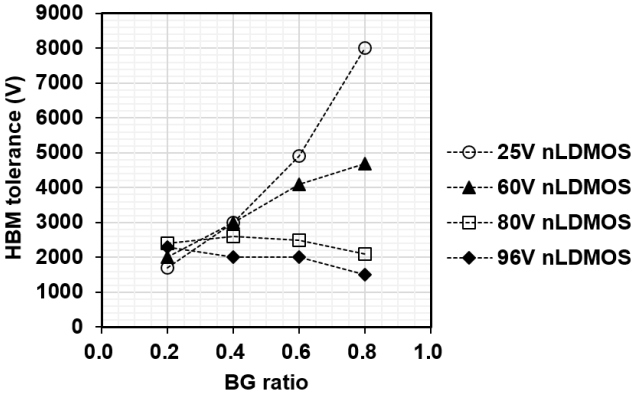


Fig. 4. HBM tolerance dependence on BG ratio.

III. Results and Discussion of TCAD Simulations

A. Electron current density during the HBM events

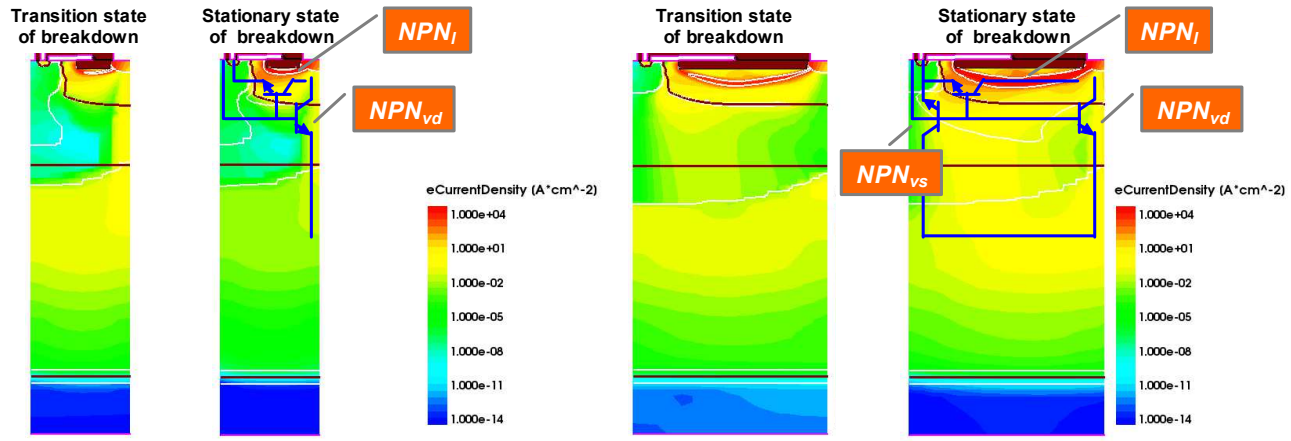
Fig. 5 (a) and (b) show the electron current density of transition and stationary state of the breakdown during the HBM events of (a) 40V and (b) 96V nLDMOS, respectively. For both cases, a lateral NPN (NPN_l), which consists of drain/channel/source, is a main current path. Regarding a vertical NPN action, which consists of drain or source/P-RESURF/NBL, as for the 40V nLDMOS, the electron flows vertically only under the drain region (NPN_{vd}), where the potential condition is N+drain>P-RESURF>NBL. On the other hand, in 96V nLDMOS case, the vertical current flow occurs not only under the drain (NPN_{vd}) but also under the source region (NPN_{vs}), where the potential condition is N+source<P-RESURF<NBL. This behavior can be explained with considering in-depth electrical potential profiles.

B. Electrical potential profile during the HBM events

Fig. 6 (a) shows the electrical potential distribution of 96V nLDMOS after the breakdown during the HBM events. Fig. 6 (b) and (c) show in-depth profiles of electrical potential at drain and source region of 40V and 96V nLDMOS, respectively. During the HBM measurement, NBL and Psub are floating and thus the potential of NBL follows P-RESURF potential [8]. Furthermore, the P-RESURF potential follows N+drain potential as well. In both 40V and 96V nLDMOS cases, the voltage applied to N+drain is equivalently high as the BVdss. In Fig. 6 (b) and (c), *Vce* is defined as an electrical potential difference between NPN_{vs} emitter (N+source) and collector (NBL), and the *Vce* values have big difference between 40V and 96V nLDMOS. Since source electrode is grounded during the measurement, N+source potential is nearly 0V and thus the *Vce* difference is due to NBL potential difference. As mentioned above, the floating NBL potential is raised and determined by the LDMOS's BVdss value. Moreover, the voltage-drop from N+drain to NBL has no big difference between 40V and 96V nLDMOS cases so that the NBL potential greatly differs between the devices having different rated voltage. In 96V nLDMOS case, the *Vce* is high enough to trigger the NPN_{vs} (N+source<P-RESURF<NBL). On the contrary, as for 40V nLDMOS, *Vce* is too low to turn on the NPN_{vs} due to the lower BVdss.

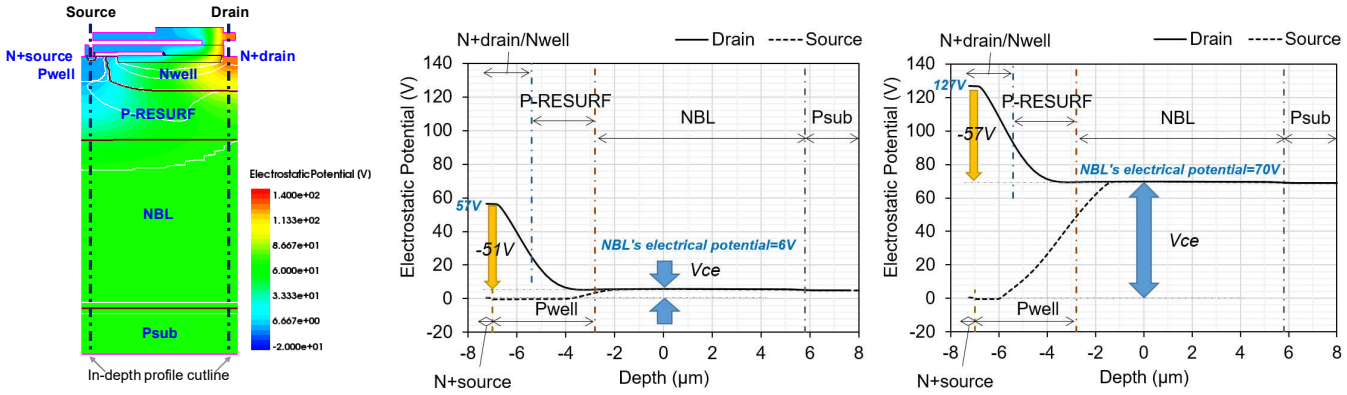
IV. Discussion of Backgate Ratio Dependence

The reason why the HBM tolerance dependence on BG ratio differs related to the rated voltage is considered in Fig. 7. In the case of rated voltage below 60V, NPN_l is the main current path as shown in Fig. 7 (a) so that lowering NPN_l base resistance by increasing the BG ratio and suppressing NPN_l *Vbe* has a strong influence on avoiding device destruction during HBM test. On the other hand, above 80V case, the additional current path NPN_{vs} via NPN_{vd} exists and the bipolar transistors act as shown in Fig. 7 (b), which is determined only by the potential relation among the drain or source/P-RESURF/NBL which consist NPN_{vd} and NPN_{vs}. Therefore, the device has no HBM tolerance dependence on the BG ratio. Thus, other approaches are needed to achieve high HBM tolerance in above 80V nLDMOS cases. In order to increase



(a) 40V nLDMOS (b) 96V nLDMOS

Fig. 5. The electron current density of the transition state and the stationary state of the breakdown during HBM event calculated using 2D TCAD simulation: (a) 40V nLDMOS and (b) 96V nLDMOS.



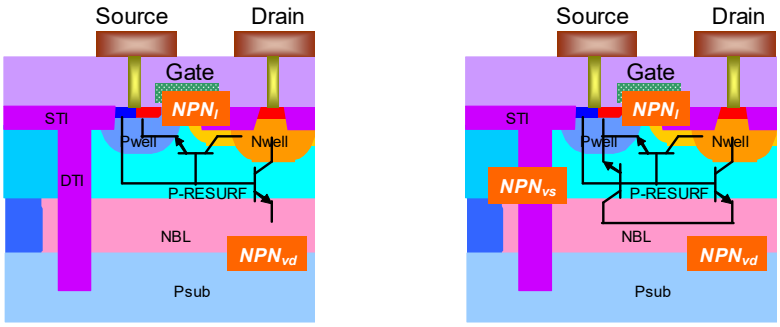
(a) (b) 40V nLDMOS (c) 96V nLDMOS

Fig. 6. (a) The 2D electrical potential distribution and the location of the index profile (source and drain side). The in-depth electrical potential profiles cut in the drain and source region (Fig. 6 (a)) of (b) 40V nLDMOS and (c) 96V nLDMOS. *Vce* is defined as an electrical potential difference between NPN_{vs} emitter (N+source) and collector (NBL).

HBM tolerance in 96V nLDMOS, P-RESURF doping concentration dependence has been studied (Fig. 8). The HBM tolerance increases as the P-RESURF concentration decreases. It is due to the *Vce* value increase of NPN_{vs}, and thus the collector current of NPN_{vs} increases. Consequently, the collector current of NPN_I decreases, and suppress the current concentration at the channel surface, which causes HBM destruction. The BVdss is another concern for improving HBM tolerance because they have a trade-off relation that lower P-RESURF concentration decreases the BVdss [6]. Therefore, the balance of both HBM tolerance and BVdss should be taken into account. Fig. 9 shows the DC characteristics dependence on BG ratio of the 96V nLDMOS, which has no BG ratio dependence on HBM tolerance (Fig. 4). As BG ratio increases, RonA increases because of the drain current lowering due to source area sacrifice. BVdss is independent from BG ratio because it is defined by an electric field distribution balance between drain and source. In conclusion, it is found that the HBM tolerance dependence on the BG ratio differs by the rated voltage of the fully isolated RESURF LDMOS. In case of rated voltage below 60V, the preferable BG ratio is determined by the criteria window of both HBM and RonA results, however, above 80V case, the BG ratio can be chosen only by considering RonA value.

V. Conclusion

BG ratio dependence on fully isolated RESURF LDMOS characteristics, such as ESD tolerance, RonA and BVdss for various rated voltages has been studied and found that ESD tolerance dependence differs by the rated voltage. For the LDMOS of rated voltage below 60V, the ESD tolerance increases as the BG ratio increases, which is well-known method to achieve the highly-ESD tolerant devices though scarifying the RonA. However, the LDMOS of rated voltage above 80V, shows no dependence on BG ratio. The mechanism of this phenomenon has been investigated utilizing 2D TCAD simulation and found that the electrical potential of a floating N+buried layer contributes to parasitic bipolar action during ESD events and determines the ESD tolerance. The LDMOS design has to be carefully performed by considering this unique ESD tolerance dependence on the BG ratio.



(a) Below 60V nLDMOS (b) Above 80V nLDMOS

Fig. 7. Cross-sectional views of fully isolated RESURF nLDMOS under the HBM measurement for the LDMOS with rated voltage (a) below 60V and (b) above 80V. Parasitic NPNs exist in both structures.

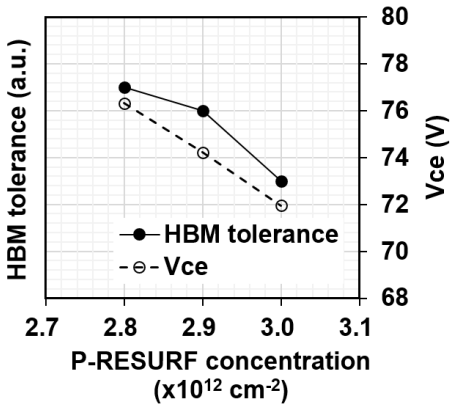


Fig. 8. Measured HBM tolerance and calculated *Vce* dependence on P-RESURF concentration.

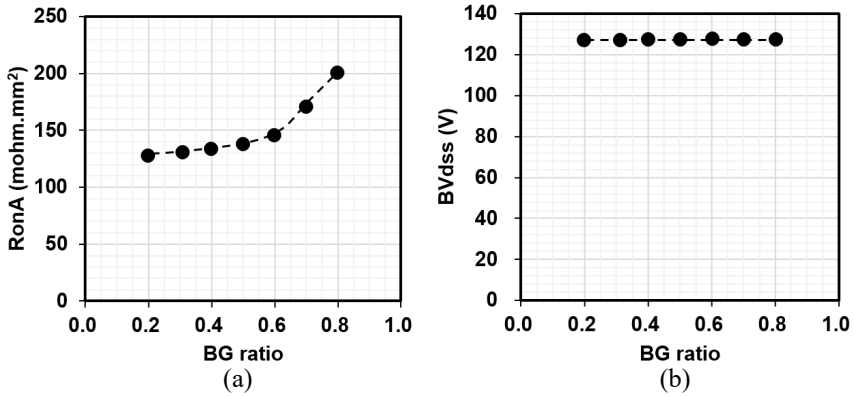


Fig. 9. Backgate ratio dependence of (a) RonA and (b) BVdss of 96V nLDMOS.

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