TOSHIBA

Process Technology for MOS-Type GaN Devices Offering High Channel Mobility and High Reliability

Gallium nitride (GaN) power semiconductor devices are expected to contribute to the realization of small, low-loss power electronics equipment. In particular, metal-oxide semiconductor (MOS)-type GaN devices are promising candidates for next-generation power devices that can achieve normally-off operation by themselves in addition to high-speed switching.
The Toshiba Group has developed a process technology for MOS-type GaN devices that makes it possible to selectively control the crystallization of an aluminum nitride (AlN) film on the recessed gate structure. Through evaluation tests of prototypes fabricated using this process technology, we have confirmed that it has the potential to achieve high channel mobility at the gate as well as high reliability under high-temperature, high-drain-voltage conditions.

1. Introduction

GaN power devices provide low on-resistance and low switching loss because of a high electric breakdown field and the two-dimensional electron gases[*1] (2DEGs) with high electron mobility generated below the gate electrode. Therefore, power supply units using GaN power devices are capable of switching at high frequency. The low power loss of GaN power devices makes them a promising candidate as new devices that will help reduce the power consumption and the size of power supply units.
However, while power supply units require normally-off operation, GaN devices are inherently normally on. To date, the semiconductor industry has developed pseudo-normally-off devices that combine a GaN device with a low-voltage silicon (Si) power device as well as normally-off devices with a p-type GaN layer under the gate electrode[(1)]. While working on pseudo-normally-off GaN high-electron-mobility transistors (HEMTs)[(2)], the Toshiba Group is also developing next-generation GaN metal-oxide-semiconductor field-effect transistors (MOSFETs) that provide normally-off operation by themselves and are capable of switching at high speed with a small amount of charge for gate drive[(3)].

In order to achieve normally-off operation with GaN MOSFETs, it is necessary to reduce the 2DEGs generated immediately below the gate electrode by forming a deep recessed gate structure. However, since phonon scattering causes the channel mobility at the interface between the insulating and GaN layers to drop to a level on the order of 100 $cm^2/(V{\cdot}s)$, it was previously difficult to realize normally-off GaN MOSFETs with low on-resistance.
To solve this issue, we have developed a unique process based on an atomic layer deposition (ALD) technique to selectively deposit a high-quality monocrystalline AlN film in the recessed gate structure and amorphous AlN films in the non-gate regions. This process made it possible to increase the channel mobility from 105 $cm^2/(V{\cdot}s)$ to 490 $cm^2/(V{\cdot}s)$ while maintaining normally-off operation. In addition, because of the amorphous AlN layers in the non-gate regions, the newly developed GaN MOSFET achieved high device reliability even under high-temperature, high-voltage conditions.
This report describes the process used to fabricate the new GaN MOSFET and its characteristics.

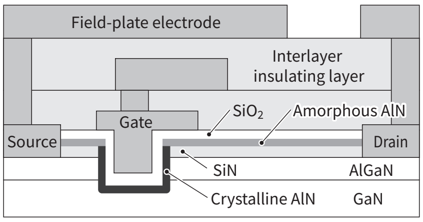
(*1) A layer of electrons in a semiconductor that are free to move in two dimensions and appear to be a 2D sheet

2. Structure of the newly developed GaN MOSFET

Figure 1 shows the cross-sectional structure of the newly developed GaN MOSFET. In order to achieve normally-off operation, the new GaN MOSFET has a deep recessed gate structure. A gate dielectric of silicon dioxide (SiO_2) is formed in the gate recess. In addition, the GaN MOSFET has a field-plate electrode for the enhancement of breakdown voltage. **Figure 2** shows the flow for forming the recessed gate. First, a silicon nitride (SiN) protection layer is deposited on the surface. After SiN deposition, a recessed gate structure is dry-etched until it extends into the GaN layer. Then, an ALD technique is employed to deposit an AlN layer in the gate recess and elsewhere. The AlN layer is formed as a monocrystalline layer in the gate recess in order to match the crystallinity between the AlN and GaN layers. The other AlN layers on the SiN layer are deposited as amorphous layers. We have developed a process technology to selectively control the crystallinity of the AlN layers as described above.

Following the deposition of the AlN layers, an SiO_2 gate insulating layer is deposited using the ALD technique. Next, the gate, source, and drain electrodes are formed, followed by an interlayer insulating layer and a field-plate electrode.

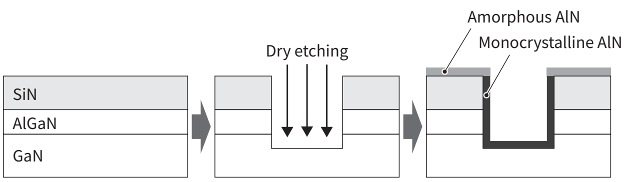
Figure 3 shows the cross-sectional transmission electron microscope (TEM) images of the recessed gate region and the region between the gate and drain electrodes. The composition of each layer was identified through elemental analysis. The images of Figure 3 provide an enlarged view of the AlN layer between the GaN and SiO_2 layers and the one between the SiN and SiO_2 layers, respectively. As shown in Figure 3(a), the AlN layer in the recessed gate region exhibits crystallinity, i.e., a regularly arranged atomic-scale structure, as in the GaN layer. In contrast, Figure 3(b) indicates that the AlN layer above the SiN layer between the gate and drain electrodes is amorphous with a disordered atomic-scale structure.



AlGaN: Aluminum gallium nitride

Figure 1. Cross-sectional structure of GaN MOSFET

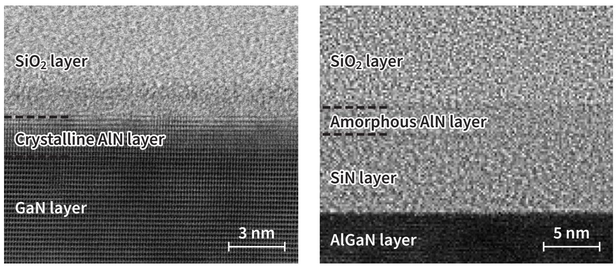
The deep recessed gate structure reduces 2DEGs to achieve normally-off operation.



Deposition of SiN layer — Formation of recessed gate structure — Deposition of AlN layer

Figure 2. Flow of processes for fabrication of recessed gate structure

We achieved high channel mobility and reliability by selectively forming a monocrystalline AlN layer only in the recessed gate and amorphous AlN layers elsewhere.



(a) Recessed gate region

(b) Region between gate and drain electrodes

Figure 3. Cross-sectional TEM images of AlN filmfabricated areas

The AlN layer in the recessed gate is crystalline whereas the ones above the SiN layer are amorphous.

3. AlN layers providing high channel mobility

Figure 4 shows the output characteristics of the newly developed GaN MOSFET. **Figure 5** shows its transfer characteristics at a drain voltage of 1 V. As shown in Figure 4, when the gate voltage is 0 V, the GaN MOSFET maintains the drain current at zero, achieving normally-off operation. Also, from the drain current curve of Figure 5, its threshold voltage (V_{th}) is extrapolated to be 1.6 V.

Figure 6 shows the results of evaluation of the channel mobility obtained when the carrier concentration below the gate was changed by changing the gate voltage. For the sake of comparison, Figure 6 also shows the results of evaluation of a GaN MOSFET without AlN layers. The GaN MOSFET without AlN layers had a maximum channel mobility of 105 $cm^2/(V•s)$ whereas the newly developed GaN MOSFET with AlN layers exhibited a channel mobility of 490 $cm^2/(V•s)$. These results indicate that a high channel mobility was achieved at the AlN-GaN interface because of the high-quality AlN layers. We infer that the enhancement of the channel mobility mainly resulted from the reduced phonon scattering[4]. Because the newly developed process provides a reduction in the specific on-resistance contributed by the gate, we succeeded in reducing the specific on-resistance of a 650 V GaN MOSFET by roughly 20%.

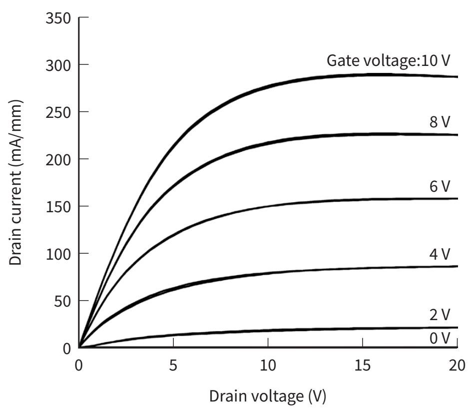


Figure 4. Output characteristics of GaN MOSFET

When the gate voltage is 0 V, the GaN MOSFET cuts off the drain current, achieving normally-off operation.

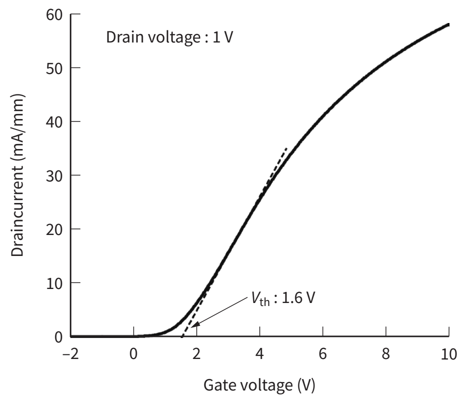


Figure 5. Transfer characteristics of GaN MOSFET

From the drain current curve, the V_{th} was extrapolated to be 1.6 V.

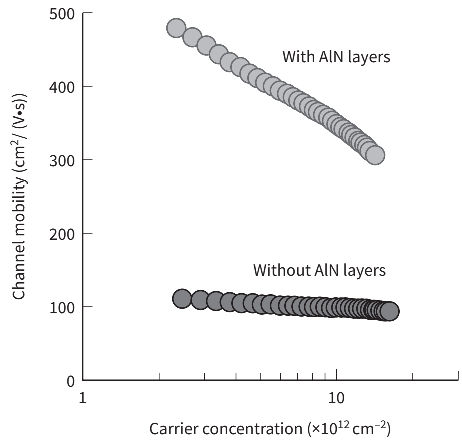


Figure 6. Dependence of channel mobility on carrier density

A GaN MOSFET with AlN layers exhibited a considerably higher channel mobility than the one without AlN layers.

4. Achieving high reliability

As described in Section 3, while the newly developed GaN MOSFET achieved normally-off operation and high channel mobility, it also exhibited high reliability at the same time.

Figure 7 shows its breakdown characteristics at 25°C and 150°C. At both these temperatures, the new GaN MOSFET exhibited a breakdown voltage of roughly 1,200 V, which is sufficient for a 650 V power device.

Figure 8 shows the results of acceleration tests under high-temperature, high-voltage conditions. It is a plot of time-to-failure when a constant drain voltage is applied at 150°C. The time-to-failure shown is the estimated amount of time that it will take for 0.1% of the devices under test to fail. According to the test results, the GaN MOSFET is estimated to have a life of more than 10 years at a temperature of 150°C and a drain voltage of 650 V. This compares favorably with the pseudo-normally-off GaN HEMTs that are already in commercial use[5] or the gate injection transistors that achieve normally-off operation by means of a p-type GaN layer formed below the gate[6]. Therefore, the newly developed GaN MOSFET provides sufficient device reliability.

As shown in Figure 3, this GaN MOSFET achieved an enhanced channel mobility because of the monocrystalline AlN layer in the gate recess. In contrast, the AlN layers between the gate and drain electrodes are amorphous. We consider that the uniform amorphous AlN layers between the gate and drain electrodes that are exposed to a high-intensity electric field at high voltage help improve the device reliability under high-temperature, high-voltage conditions. Therefore, the process technology that enables selective control of the crystallinity of AlN layers makes it possible to realize highly reliable low-on-resistance GaN MOSFETs.

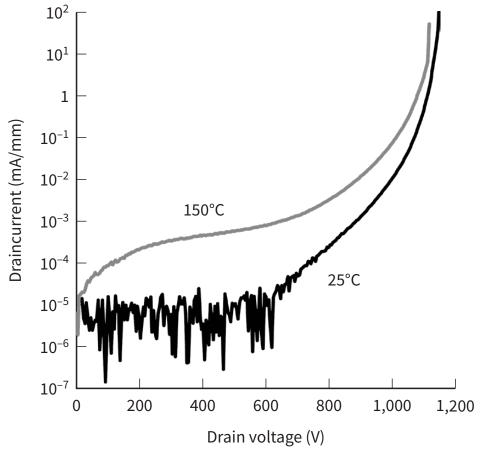
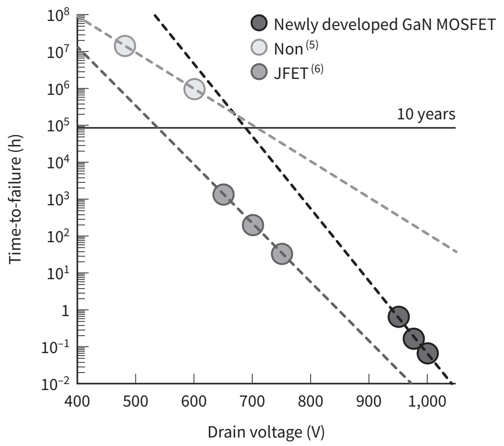


Figure 7. Breakdown characteristics of GaN MOSFET

The GaN MOSFET exhibited a breakdown voltage of roughly 1,200 V at both 25°C and 150°C. Therefore, it provides sufficient withstand voltage for a 650 V power device.



Non : Normally-On Transistor
JFET : Junction Field Effect Transistor

Figure 8. Results of reliability tests when high voltage was applied at high temperature

As a result of acceleration tests under high-temperature, highvoltage conditions, we confirmed that the new GaN MOSFET has high potential to achieve sufficient lifetime for practical applications.

5. Conclusion

We have developed a GaN MOSFET with a recessed gate structure having AlN layers and confirmed that it is promising as a next-generation device in terms of both performance and reliability.

In order to achieve practical applications, it is necessary to further improve its reliability, including a reduction in V_{th} variations. We will continue to develop process technologies to commercialize high-speed power GaN MOSFETs capable of normally-off operation on their own and thereby contribute to the field of power electronics in which reductions in both size and power consumption are required.

References

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