# Miniaturization of Photorelay Packages Using Chip Stacking Technologies

**Relays that turn an electric circuit on or off in accordance with external commands are widely applied in the field of electric actuators. A trend toward the replacement of conventional mechanical relays with photorelays, which provide several advantages including smaller size, higher speed switching, longer lifetime, and lower power consumption, has recently been progressing in line with the introduction of photorelays offering more sophisticated and more efficient functions. However, as the rated on-state current of photorelays is presently smaller than that of mechanical relays, it is necessary to overcome the trade-off between reduction of size and increase of rated on-state current in such products.**

**Toshiba Electronic Devices & Storage Corporation has developed new photorelay products that achieve smaller size and higher rated on-state current by utilizing its proprietary chip stacking technologies to attach photodiode array (PDA) and light-emitting diode (LED) chips to a metal-oxide-semiconductor field-effect transistor (MOSFET) chip, in addition to a package structure that dissipates the heat of parts more efficiently. These photorelays also contribute to higher density packaging of electric circuits by incorporating a small resistor chip into a package of the same size as that of conventional photorelays, which require an external resistor.**

## 1. Introduction

A relay is an electrically operated switch to turn on and off an electric circuit. Relays are used in a wide range of applications, including measuring instruments, industrial equipment, and communication systems. Conventionally, mechanical relays consisting of a coil and metal contacts have been utilized. Although mechanical relays are still widely used, they have many drawbacks such as difficulty in reducing their physical size, slow switching speeds because of mechanical contact operation, and short service life as their contacts wear out over time. Care is also required as to arcing between the contacts, noise due to contact bounce, and back-electromotive force (EMF) induced by the electromagnetic coil that moves the contacts (**Figure 1**). Furthermore, mechanical relays are susceptible to external magnetic interference, shock, and vibration. When arranging multiple mechanical relays on a printed circuit board (PCB), it is necessary to allow sufficient spacing between them in order to avoid mutual magnetic interference, making it difficult to achieve high-density board assembly[1].

Lately, mechanical relays are being replaced by photorelays to solve these issues. A photorelay is a type of contactless solid-state relay that consists of a LED optically coupled with a PDA. Like a mechanical relay, a photorelay also controls the on/off of an electric circuit, but its input and output sides are galvanically isolated. Photorelays are physically smaller than mechanical relays and offer many other advantages such as fast switching and

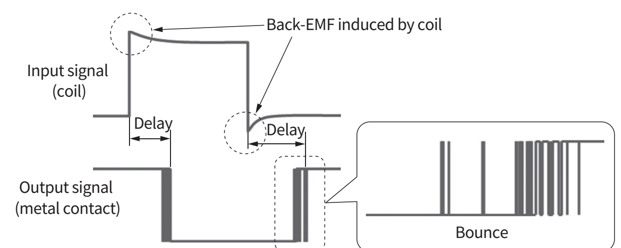


**Figure 1. Switching waveform of mechanical relay**

Mechanical relays have back-EMF induced by the coil and contact bouncing during switching. Care is required to ensure that they do not affect the output signal.

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long service life because of the absence of mechanical contacts. Photorelays are also free from magnetic interference and allow high-density board assembly. Moreover, photorelays, which employ an LED as a source of light, work with an input current of several milliamperes whereas mechanical relays, which use a coil on the input side, require several tens to several hundreds of milliamperes. Therefore, photorelays provide a reduction in power consumption in addition to size reduction, fast switching, and long life.

However, photorelays have their own drawbacks. For example, photorelays have less rated on-state current capacity than mechanical relays because, being a type of solid-sate relay, the output side of a photorelay has electrical resistance even when it is in the "on" state. Reducing the size of photorelays causes a further reduction in rated on-state current capacity.

Toshiba Electronic Devices & Storage Corporation has overcome these conflicting requirements by using chip stacking technology. As a result, the latest photorelays are suitable as a replacement for mechanical relays even in applications requiring a large on-state current and thereby help reduce system power consumption. This report provides a chronicle of our products and describes the performance enhancement achieved.

# 2. Photorelay structure

**Figure 2** shows the cross-sectional view of a photorelay, and **Figure 3** shows its equivalent circuit. A photorelay consists of an LED on the input side and a PDA and a MOSFET on the output side. The LED emits light when it receives an input electrical signal. The PDA receives the light and converts it back into an electrical signal. This electrical signal drives the gate of the MOSFET, switching the output to the "on" state.

The input and output sides of a photorelay are galvanically isolated since the photorelay uses light to transfer an electrical signal between them.

The photorelay uses a MOSFET on the output side, which has drain-source resistance (on-resistance). Therefore, the electrical energy lost due to resistance is converted into heat when the MOSFET conducts. This heating constrains the on-state current of a photorelay.

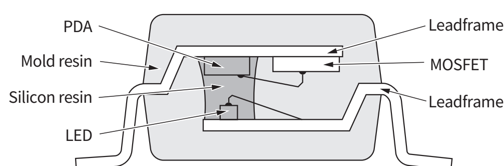


**Figure 2. Cross-sectional structure of photorelay**

A photorelay consists of an LED on the input side and a PDA-MOSFET pair on the output side and is housed in a plastic package.

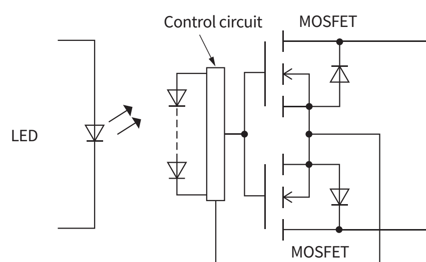


**Figure 3. Equivalent circuit of photorelay**

A photorelay transfers an electrical signal between the isolated input and output sides by using light to drive the integrated MOSFET.

# 3. Reducing the size of photorelays

## 3.1 Trends in size reduction

**Figure 4** shows the trends in the size of photorelays. In order to meet the market requirements for small photorelays, we have released successive generations of photorelays in progressively smaller packages. In addition to photorelays in thin surface-mount small-outline packages (SOPs), those in shrink small-outline packages (SSOPs) and ultra-small-outline packages (USOPs) were released in the 2000s.

In the SOP, SSOP, and USOP packages, an LED and a PDA face each other as shown in Figure 2. In contrast to the SOP package (Figure 2), the subsequent SSOP package houses a PDA and a MOSFET on

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the bottom and an LED above the PDA as shown in Figure 4. The size of the SSOP package was reduced by reducing the spacing between these chips. We further reduced the size of the PDA and modified the shape of the internal leadframe in order to realize photorelays in the USOP package.

At this point, it became difficult to further reduce the package size using existing technology since it was no longer possible to further push the limit for the chip size and modify the leadframe shape.

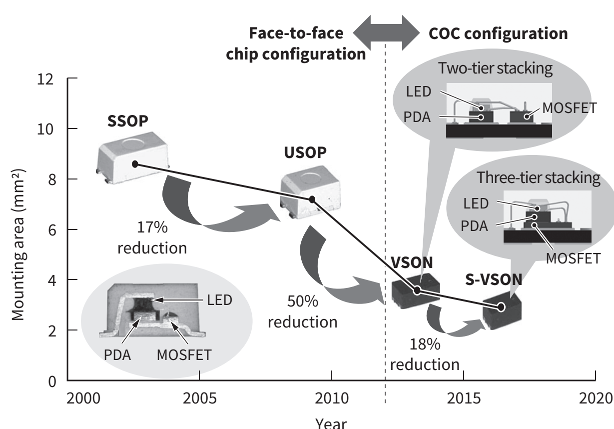


**Figure 4. Trends in miniaturization of photorelay packages**

A chip-on-chip (COC) configuration has been employed for the VSON and subsequent packages to reduce the required mounting area.

## 3.2 Using chip stacking technology to reduce the package size

In contrast to the conventional LEDs that were designed to emit light from the top side, we developed LEDs that provide light from the bottom to make it possible to stack an LED on the PDA in a chip-on-chip (COC) configuration as shown in **Figure 5**. The very-small-outline non-leaded (VSON) package with a COC configuration achieved a dramatic 50% reduction in mounting area, compared with the previous USOP package.

In order to further reduce the package size, we also developed the shrink VSON (S-VSON) package in which PDA and LED chips are stacked on a MOSFET chip in a three-tier configuration. The S-VSON package requires 18% less mounting area than the VSON package.

There are two MOSFETs on the output side of the S-VSON package, which need to be placed with sufficient spacing because they have different potentials. It is therefore necessary to place a PDA chip across these MOSFET chips in order to stack them on top of each other. In order to wire-bond these chips in such an unstable arrangement, sufficient adhesion and bonding strength are required. Therefore, we developed a new bonding technology to realize the S-VSON package by optimizing the capillary shape as well as the ultrasonic application and capillary loading conditions.

Since three-tier chip stacking helps save package space, it became possible to put a larger MOSFET chip in the S-VSON package than in the VSON package. As a result, the MOSFET chip in the S-VSON package has lower on-state resistance, making it possible to increase the rated on-state current despite the shrunk package size.

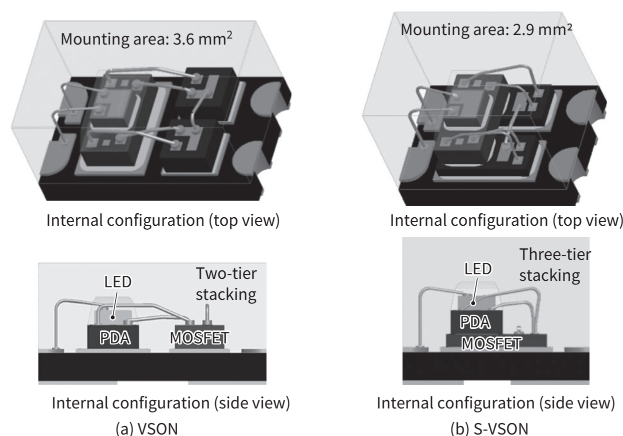


**Figure 5. Comparison of structure of VSON and S-VSON packages**

The S-VSON package employs a three-tier chip stacking configuration to reduce the required mounting area and increase the on-state current capacity.

## 3.3 S-VSON package with a built-in resistor

A resistor is necessary to limit the input current of the LED. Previously, an external resistor required additional board space.

Therefore, we developed a small resistor chip using a silicon (Si) wafer process that is 71% smaller than the conventional resistor and incorporated it in the S-VSON package (**Figure 6**). This eliminated the need for an external resistor, enabling board assembly with even higher density.

The S-VSON package with a built-in resistor made it possible to further reduce the size of system applications and to use a photorelay in space-limited systems that did not previously have enough space for a photorelay.

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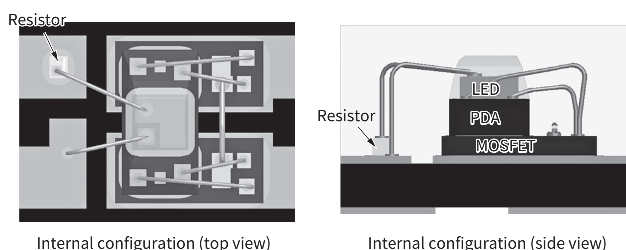


**Figure 6. Structure of S-VSON package with built-in resistor**

Photorelays in the S-VSON package incorporate a small resistor chip, eliminating the need for an external resistor.

## 3.4 Thermally enhanced P-SON package with an increased rated on-state current

Although the photorelays in the VSON and S-VSON packages described in Section 3.2 are small, their rated on-state current is at most on the order of 1 A. As packages become progressively smaller from SOP to SSOP and then to USOP, the internal MOSFET chip has also become progressively smaller. As a result, it was previously necessary to use photorelays in the large SOP package for applications requiring a rated on-state current of several amperes.

As described in Section 3.2, the three-tier chip stacking technology made it possible to put as large a MOSFET chip in the S-VSON package as in the SOP package.

In addition, the newly developed power small-outline non-leaded (P-SON) package incorporates a MOSFET chip with multiple thermal vias on the backside and provides larger outer electrodes in order to facilitate heat dissipation to a PCB. Therefore, the P-SON package efficiently dissipates the heat from the MOSFET chip in the "on" state, achieving higher thermal performance than the conventional packages.(**Figure 7**)

Furthermore, photorelays in the P-SON package incorporate a MOSFET chip fabricated using the ninth-generation trench-gate process, achieving low on-state resistance despite the compact size.

As a result, these photorelays deliver as large a rated on-state current as those in the 6-pin SOP package while requiring 83.8% less mounting area (**Figure 8**). We have commercialized 4.5 A/30 V, 3.0 A/60 V, and 2.0 A/100 V surface-mount photorelays with the industry's smallest mounting area(*1).

(*1) As of July 2020 for photorelays with a rated on-state current of 2 A or more (as surveyed by Toshiba Electronic Devices & Storage Corporation)

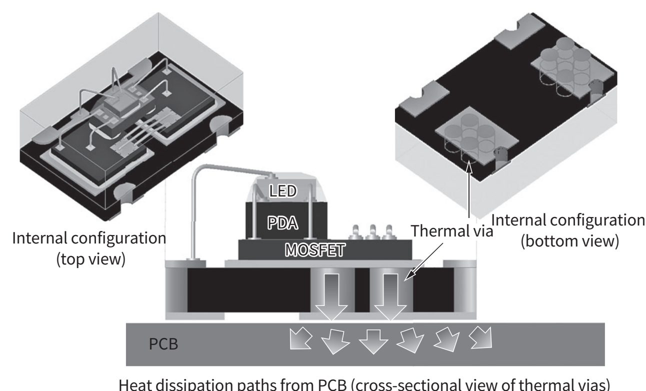


**Figure 7. Structure and heat path of P-SON package**

The P-SON package efficiently dissipates heat via the thermal vias on the backside of the MOSFET chip to the PCB, achieving large on-state current despite the small package size.

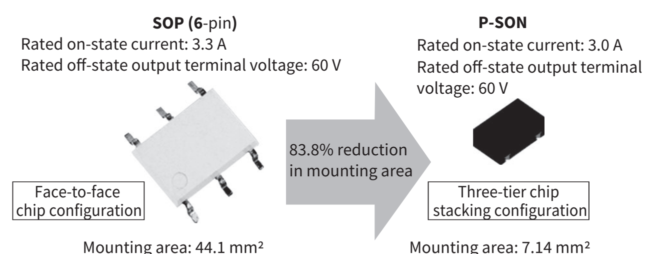


**Figure 8. Comparison of 6-pin SOP and P-SON package**

The P-SON package with three-tier chip stacking requires 83.8% less mounting area than the 6-pin SOP package with an equivalent rated on-state current.

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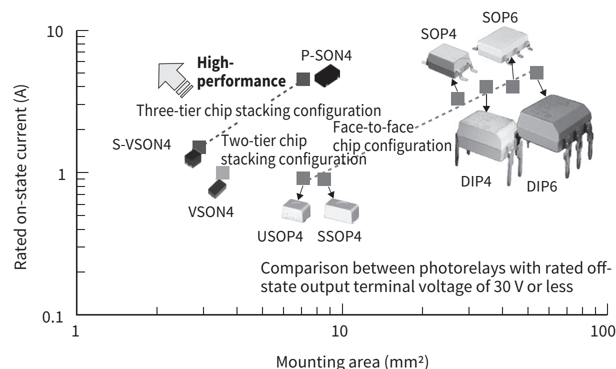
# 4. Mounting area and rated on-state current of photorelays

**Figure 9** shows the relationship between the mounting area and the rated on-state current of photorelays. Since photorelays with a larger rated off-state output terminal voltage have lower rated on-state current, Figure 9 compares those with a rated off-state output terminal voltage of 30 V or less.

In the case of photorelays with the conventional face-to-face chip configuration, a reduction in the size of photorelays causes their rated on-state current to decrease. In contrast, the VSON package in which LED and PDA chips are vertically stacked became smaller than the preceding package without compromising the rated on-state current. Furthermore, the S-VSON and P-SON packages, which allow three-tier stacking of LED, PDA, and MOSFET chips, succeeded in overcoming these conflicting requirements.




DIP: package name

* The number following package name indicates number of pins.

**Figure 9. Relationship between photorelay mounting area and rated on-state current**

Photorelays with a three-tier chip stacking configuration are smaller than those with a face-to-face chip configuration but provide higher on-state current.

# 5. Conclusion

Photorelays are expected eventually to replace mechanical relays. This report has discussed the technologies that we have utilized to reduce the size and increase the rated on-state current of photorelays. At present, we offer photorelays that are suitable as a replacement for mechanical relays even in applications requiring a rated current higher than before.

We will continue to actively develop photorelays with even higher performance in order to meet customer requirements.

## References

(1) Toshiba Electronic Devices & Storage Corporation. 2020. “Basics of photorelays and their usage considerations as replacements for mechanical relays.” Promotional website. Accessed July 17, 2020. https://toshiba.semiconstorage.com/jp/concept/media-003.html.

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