# Low-Capacitance TVS Diodes for High-Speed Data Communications

**Although the need for electronic devices with higher performance and greater compactness continues to increase, the ongoing miniaturization of electronic components is accompanied by the risk of vulnerability to electrostatic discharge (ESD). The widespread dissemination of mobile devices has consequently led to growing demand for countermeasures against ESD generated by the frequent contact of such devices with the human body.**
**Toshiba Electronic Devices & Storage Corporation is actively focusing on the development of transient voltage suppression (TVS) diodes that can improve the reliability of electronic devices by protecting them against ESD. In order to support the development of high-speed data communication equipment, we are launching a lineup of low-capacitance TVS diodes that can be used in high-speed signal lines to improve performance while reducing the vulnerability of electronic components to ESD.**

## 1. Introduction

Electronic devices are becoming progressively more sophisticated and smaller, contributing to the progress of society and industry. This trend is driving the need to enhance the functionality and reduce the size of ICs and other electronic components. As a result, IC interconnects are becoming progressively thinner, making them more susceptible to ESD strikes.

In addition, because of the prevalence of mobile and IoT devices, Universal Serial Bus (USB), High-Definition Multimedia Interface (HDMI®), and other ports are frequently touched by a charged human body. As a result, electronic devices are exposed to an increasingly greater risk of ESD.

Since ESD strikes could cause mobile electronics to malfunction or be permanently damaged, it is essential to protect them from ESD. Toshiba Electronic Devices & Storage Corporation is committed to the development of ESD protection devices. This report describes low-capacitance TVS diodes suitable for the protection of signal lines for high-speed data communication.

## 2. Reducing the capacitance of TVS diodes to maintain the integrity of high-speed signals

### 2.1 Requirements for reducing the capacitance of TVS diodes

When TVS diodes are used to protect signal lines from ESD, it is necessary to choose ones with appropriate capacitance according to the frequency of the signals so that they will not cause a delay or degradation of their waveforms. For example, the USB data communication standard has come a long way since the release of USB 1.0 in 1996, with each version adding higher signaling rates to support faster transfer speeds and higher data communication capacities. USB lines with higher signaling rates require TVS diodes with lower capacitance.

In response, we have steadily reduced the capacitance of TVS diodes as shown in **Figure 1**(a) since the first release of TVS diodes in 1997. Capacitance reduction has been achieved through the development of a new device structure and the optimization of the

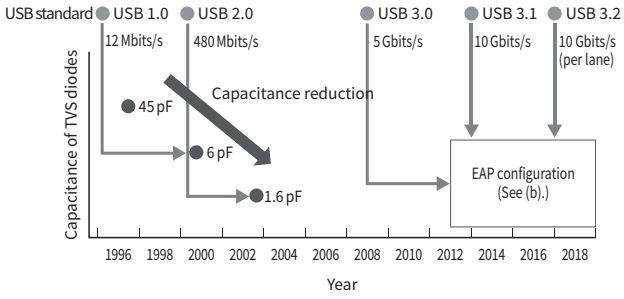
dopant concentration profile and device parameters. USB 3.0 released in 2008 necessitated TVS diodes with a capacitance of 1 pF or less. In response, we developed the ESD diode array process (EAP) in order to realize TVS diodes with even lower capacitance as shown in Figure 1(b).

## 2.2 EAP to reduce the capacitance of TVS diodes

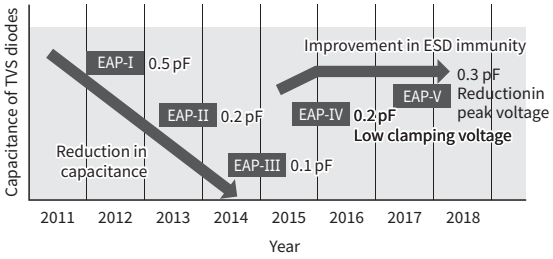
In order to reduce the capacitance of a diode, it is generally necessary to reduce the area of the pn junction (p: p-type semiconductor, n: n-type semiconductor) or increase the reverse breakdown voltage ($V_{BR}$), but either way results in the degradation of its ESD immunity. We overcame this dilemma by means of the EAP, which combines multiple diodes to reduce capacitance without compromising the ESD immunity.

**Figure 2**(a) shows the circuit diagram of a low-capacitance TVS diode in an EAP configuration. It consists of three diodes: low-capacitance Diode 1 and Diode 2 (with a capacitance of $C_1$ and $C_2$ respectively) and high-capacitance Diode 3 (with a capacitance of $C_3$). Diode 1 and Diode 2 have a small pn junction area and high $V_{BR}$ whereas Diode 3 has a large pn junction area and adequate $V_{BR}$. The ESD current applied to the anode flows through Diode 1 in the forward direction whereas the one applied to the cathode flows through Diode 2 in the forward direction and then through Diode 3 in the reverse direction since the $V_{BR}$ of Diode 3 is lower than that of Diode 1. Typically, diodes are less tolerant of ESD energy in the reverse direction than in the forward direction. Since the pn junction area of Diode 1 and Diode 2 is small, they are even less tolerant of ESD energy in the reverse direction. However, when a TVS diode is configured as shown in Figure 2(a), ESD current does not flow through Diode 1 and Diode 2 in the reverse direction. Therefore, this circuit provides high ESD immunity as a whole.

Figure 2(b) shows the equivalent capacitance circuit of this TVS diode. The combined capacitance can be reduced by connecting low-capacitance Diode 2 and Diode 3 in series. Also, since the $V_{BR}$ of this circuit is determined by the $V_{BR}$ of Diode 3, the ESD immunity can be increased by adjusting the $V_{BR}$ of Diode 3 according to the signal line to be protected.



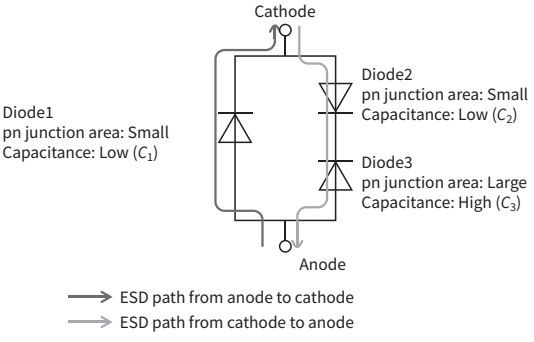

(a) Roadmap of TVS diodes for USB lines



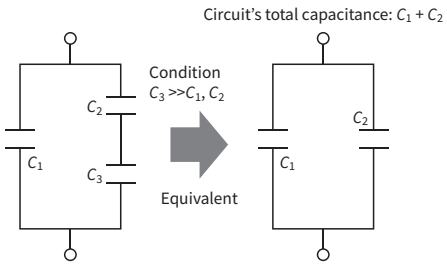

(b) Roadmap of TVS diodes in EAP configuration

**Figure 1. Roadmaps of Toshiba TVS diodes**

We have steadily reduced the capacitance of TVS diodes according to the market trends. The EAP configuration helps not only reduce the capacitance of TVS diodes but also increase their ESD immunity.




(a) Circuit diagram




(b) Equivalent capacitance circuits

**Figure 2. Circuit diagram of TSV diode applying ESD diode array process (EAP) and its equivalent circuits**

A low-capacitance TVS diode with high ESD immunity was realized by combining three diodes.

## 2.3 Technology to further reduce the capacitance of TVS diodes

Generally, the capacitance ($C$) between two parallel plate conductors is expressed as follows using permittivity ($\varepsilon$), the plate area ($S$), and the distance between the two plates ($d$).

$$C=\varepsilon(S/d) \quad (1)$$

When considering the capacitance of a diode, $S$ is regarded as the pn junction area, and $d$ is regarded as equivalent to the width of the depletion layer formed across the pn junction (**Figure 3**). In order to reduce the capacitance of a diode without changing its material, it is necessary to reduce the pn junction area or increase the width of the depletion layer. However, there is a trade-off between the pn junction area and ESD immunity; i.e., reducing the pn junction area causes a reduction in ESD immunity. On the other hand, the width of the depletion layer does not have such a trade-off. The depletion layers of Diode 1 and Diode 2 determine the capacitance of a TVS diode. Since they expand greatly into the $n^-$ (lightly doped n-type semiconductor) layer, a key to reducing the capacitance of a TVS diode lies in reducing the dopant concentration of the $n^-$ layer. The $n^-$ layer of the EAP-III series has roughly 1/20th the dopant concentration of that of the EAP-I series. Therefore, the EAP-III series has an improved trade-off between capacitance and ESD immunity, thereby achieving a capacitance as low as 0.1 pF (**Figure 4**).

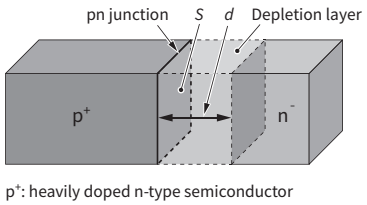



**Figure 3. Depletion layer formed at pn junction**

Reducing the dopant concentration of the $n^-$ layer causes the depletion layer to expand, resulting in a reduction in capacitance.

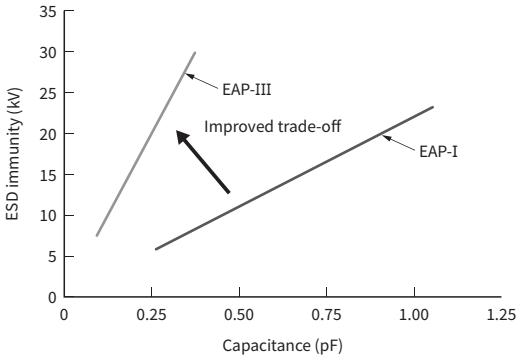



**Figure 4. Comparison of trade-off between capacitance and ESD immunity**

The $n^-$ layer of the EAP-III series has roughly 1/20th the dopant concentration of that of the EAP-I series. Therefore, the EAP-III series has an improved trade-off between capacitance and ESD immunity and therefore lower capacitance.

# 3. Performance for the protection of ICs

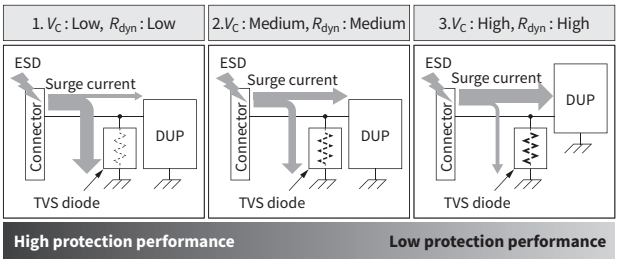
## 3.1 Importance of ESD protection performance

In order to ensure reliable protection of ICs, we have been not only reducing the capacitance of TVS diodes steadily but also improving their ESD protection performance through successive optimization of the EAP as shown in Figure 1(b).

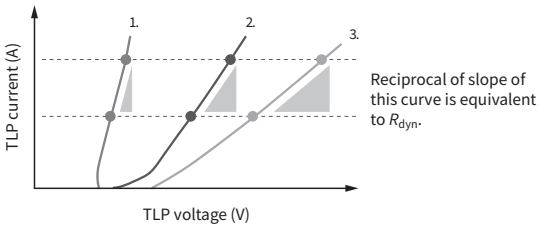
$R_{dyn}$ and $V_C$ indicate the ESD protection performance of a TVS diode. $R_{dyn}$ represents the dynamic resistance of a TVS diode during a transient ESD event. $V_C$ is the clamping voltage; i.e., the voltage applied to a device under protection (DUP) when a TVS diode stabilizes after an ESD event. **Figure 5** illustrates the amount of ESD energy shunted through TVS diodes with different $R_{dyn}$ values. Since a TVS diode with high $R_{dyn}$ cannot shunt a sufficient amount of ESD energy to ground, much of the ESD energy is applied to the DUP. Therefore, TVS diodes with low $R_{dyn}$ are preferred.

$V_C$ is the voltage applied to the DUP after ESD energy is shunted through a TVS diode. $V_C$ can be used as a guide to estimate how many volts could be applied to the DUP. TVS diodes with lower $V_C$ provide higher ESD protection performance. As IC interconnects are becoming progressively thinner, attention has also focused on

transient voltage lately. **Figure 6** shows $V_C$ curves. It is necessary to reduce $V_{peak}$, the peak voltage of $V_C$ curves, since an ESD transient with high $V_{peak}$ could destroy a DUP in just several nanoseconds.



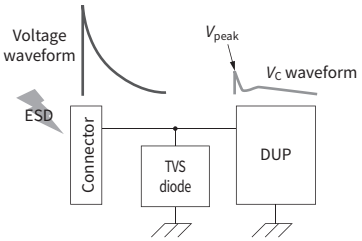

(a) Relationship between ESD immunity and amount of ESD energy absorbed



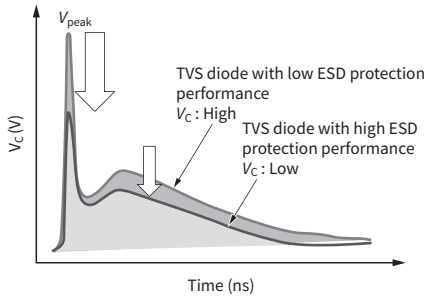

(b) Comparison of current-voltage curves through transmission line pulse (TLP) measurement

**Figure 5. Comparison of ESD suppression of TVS diodes with different protection performance**

TVS diodes with lower $R_{dyn}$ and $V_C$ shunt more current through the TVS diode than those with higher $R_{dyn}$ and $V_C$ and therefore provide higher ESD protection performance.




(a) $V_C$ waveform in event of ESD strike




(b) Reducing $V_{peak}$ using TVS diode with high ESD protection performance

**Figure 6. Differences in clamping voltage waveforms with TVS diodes with different protection performance used at time of ESD**

Since an ESD strike causes a sudden change in voltage, a fast TVS diode is required to clamp $V_{peak}$.

## 3.2 Technology to enhance ESD protection performance

As the $V_C$ of a TVS diode depends on its $V_{BR}$ it is necessary to reduce $V_{BR}$ to decrease $V_C$. On the other hand, a TVS diode should have an appropriate working peak reverse voltage ($V_{RWM}$) so that it does not interfere with a signal line. In order to reduce $V_C$ without compromising $V_{RWM}$, it is necessary to intentionally use the snapback behavior of the diode; i.e., a drop in voltage after breakdown. **Figure 7** shows the snapback characteristics of the EAP-IV series, which provides a reduction in $V_C$ while maintaining $V_{RWM}$. This was achieved by optimizing the dopant concentration profile of Diode 3 shown in Figure 2(a).

We also developed the EAP-V series, which exhibits roughly 50% lower $V_{peak}$ than the EAP-IV series because the EAP-V series is designed to operate at a higher speed by optimizing the thickness and the dopant concentration of both the p-type and n-type regions (**Figure 8**).

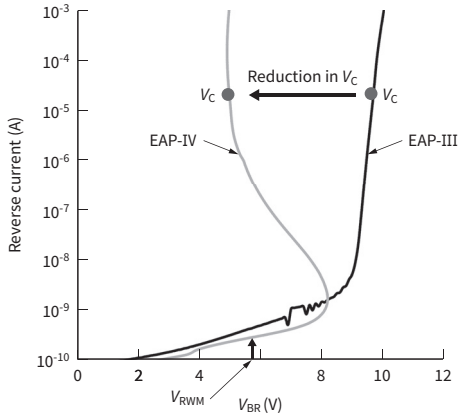



**Figure 7. Comparison of current-voltage (*I*-*V*) curves of conventional and low-clamping-voltage products**

The EAP-IV series intentionally uses the snapback behavior to reduce $V_C$ while maintaining $V_{RWM}$ at a level suitable for a signal line.

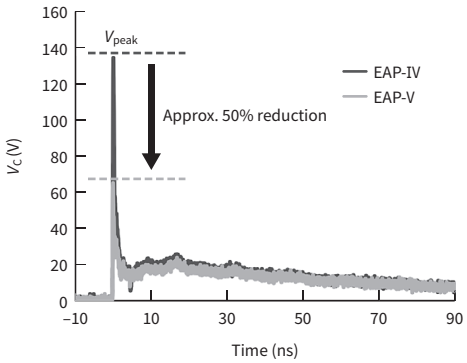


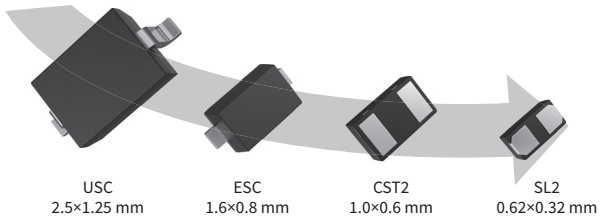

**Figure 8. Comparison of clamping waveforms of conventional and low-peak-voltage products**

The EAP-V series exhibits roughly 50% lower $V_{peak}$ than the EAP-IV series because of the optimized device parameters and a higher operating speed.

## 4. Reducing the size of TVS diodes to support high-density board assembly

As electronic devices become progressively more sophisticated and smaller, their connectors are also becoming progressively smaller with densely packed contacts, driving the need for smaller TVS diodes (**Figure 9**).

However, small packages impose a constraint on the chip size. The ESD immunity of a TVS diode in an EAP configuration is proportional to the pn junction area of Diode 3 through which ESD flows in the reverse direction. Since a sufficient pn junction area is necessary to increase ESD immunity, it is difficult to house the TVS diode in a small package. Previously, Diode 3 was formed on the surface of a chip. To increase its pn junction area and reduce the chip size, we have formed it inside the silicon substrate. As a result, the latest TVS diodes are available in small packages.




* USC, ESC, CST2, and SL2 are package names.

**Figure 9. Trends in TVS diode packages**

Packages for TVS diodes are becoming progressively smaller. While USC measures 2.5 × 1.25 mm, SL2 measures only 0.62 × 0.32 mm.

## 5. Conclusion

As electronic devices become progressively more sophisticated and smaller, the importance of ESD protection devices is increasing.

We will continue to develop low-capacitance TVS diodes with high ESD immunity according to the market trends in order to contribute to the enhancement of the reliability of electronic devices.

* HDMI is a trademark or a registered trademark of HDMI Licensing Administrator, Inc.