# Low-Voltage Power MOSFET Technologies for Next-Generation Large-Capacity Communication Systems

**Commercial operation of fifth-generation (5G) mobile communications commenced in Japan in March 2020 in response to the increasing volume of content requiring large-capacity and high-speed communication capability such as for video streaming services. As increased data traffic volumes lead to a dramatic increase in the power consumption of base stations for mobile communications, it has become necessary to further improve the efficiency of power supply units in these base stations. Highly efficient low-voltage power devices with a drain-source voltage of 80 V or 150 V are required not only for AC-DC converters to convert the AC voltage fed from a commercial power supply into the -48 V DC reference potential used in base stations but also for DC-DC converters to convert the -48 V DC into the various voltages necessary for high-frequency amplifiers and system controllers.**

**Toshiba Electronic Devices & Storage Corporation has developed 80 V power metal-oxide-semiconductor field-effect transistor (MOSFET) products featuring superior on-resistance, gate charge, and reverse recovery charge characteristics by utilizing its proprietary U-MOS X-H process. We are also developing 150 V power MOSFET products based on the same device structure.**

## 1. Introduction

In the field of telecommunication, video streaming and content distribution require high-speed network connections. Accompanying the ever-increasing content volume, the network traffic is expected to increase at an annual rate of 20 to 40% until 2025.

The 5G cellular network is attracting much attention as a technology standard that satisfies the required data transfer speeds. The increased 5G speeds are achieved through high-frequency radio waves, an increased bandwidth, and massive multiple-input and multiple-output (MIMO)(*1). The high-frequency radio waves of 5G travel much less distance and are more susceptible to noise than the Long-Term Evolution (LTE) waves. In order to compensate for these shortcomings, a 5G network employs a beamforming technique using multiple antennas. As shown in **Figure 1**, the existing base stations for fourth-generation (4G) and LTE cellular networks consist of radio units (RUs) in a two-transmitter (2T)/two-receiver (2R) configuration.

In contrast, in order to utilize a higher frequency band, a 5G radio unit incorporates an array of 64T64R or even 128T128R antennas, each with a relatively small output power. The 5G RU consumes more power than the 4G and LTE counterparts because of the increased number of antennas and the need for more complicated control. Furthermore, 5G requires far more base stations than 4G and LTE. Therefore, 5G networks consume more power than 4G and LTE networks. This is driving the need to reduce the power consumption of the power supplies for 5G radio units, requiring a further increase in the efficiency of low-voltage power MOSFETs.

Under these circumstances, Toshiba Electronic Devices & Storage Corporation has developed tenth-generation 80 V low-loss MOSFETs for these power supply applications. We are also developing 150 V MOSFETs. This report discusses the newly developed low-voltage MOSFETs as well as the technical trends in the power supplies for telecommunication applications.

## 2. Trends in the power supplies for telecommunication applications

Power supplies for the base stations for conventional landline and mobile telephone networks are referenced to –48 VDC. Since the deployment of the initial landline infrastructure, a negative reference voltage has been used to prevent the ionization of long copper telephone lines. Power supplies for all communications infrastructure, including the current wireless base stations, also use a reference voltage of –48 VDC. Therefore, an AC-DC switched-mode power supply is installed at a base station in order to generate –48 VDC from a 200 to 240 VAC utility supply voltage. A radio unit incorporates DC-DC converters to convert the –48 V reference voltage generated by the AC-DC switched-mode power

(*1) A technique using multiple antennas to transmit and receive data simultaneously in order to increase a data transfer rate

supply to the 52 to 56 VDC required for a transmitter's high-frequency amplifier as well as to the 5 to 12 V required for a receive/transmit controller and other systems. Up to around ten years ago, diodes had been generally used for the rectifier circuit in the AC-DC switched-mode power supply mainly because MOSFETs did not have sufficient performance and high-power output was not required for the power supplies of wireless base stations to meet the communication traffic demand. Nowadays, almost all communication base stations, particularly those requiring high power efficiency, utilize a synchronous rectification circuit because of the improvements made in control technology and MOSFET characteristics.

**Figure 2** shows examples of topologies of typical AC-DC converters for generating a –48 VDC reference voltage. The circuit in Figure 2 (a) is an AC-DC converter with a center-tapped rectifier, which is composed of 150 V-tolerant devices since a voltage twice as high as its output voltage is applied across rectifier devices. The circuit in Figure 2(b) is a full-bridge AC-DC converter, which is composed of 80 V-tolerant devices since a voltage equal to its output voltage is applied across rectifier devices.

**Figure 3** shows examples of topologies of typical first-stage DC-DC converters that receive –48 V from the AC-DC converter. The circuit in Figure 3(a) is a full-bridge DC-DC converter rectifier, which is composed of 150 V-tolerant devices to allow for more than double the margin relative to the input voltage. The circuit in Figure 3(b) is a buck-boost DC-DC converter, which is composed of 150 V-tolerant devices since a difference between the input and output voltages is applied across them.

In order to improve the efficiency of the AC-DC and DC-DC converters, it is necessary to reduce the conduction loss that occurs while the constituent devices are in the "on" state as well as the switching loss that occurs when they are turned on and off. In the case of MOSFETs, a conduction loss is affected by the on-resistance ($R_{on}$). The switching loss of the primary switch is mainly affected by the gate input charge ($Q_g$) and the gate switch charge ($Q_{sw}$) of the MOSFETs whereas the switching loss of the synchronous rectifier is mainly affected by the reverse recovery charge ($Q_{rr}$) of the MOSFETs. It is therefore essential to improve these characteristics.

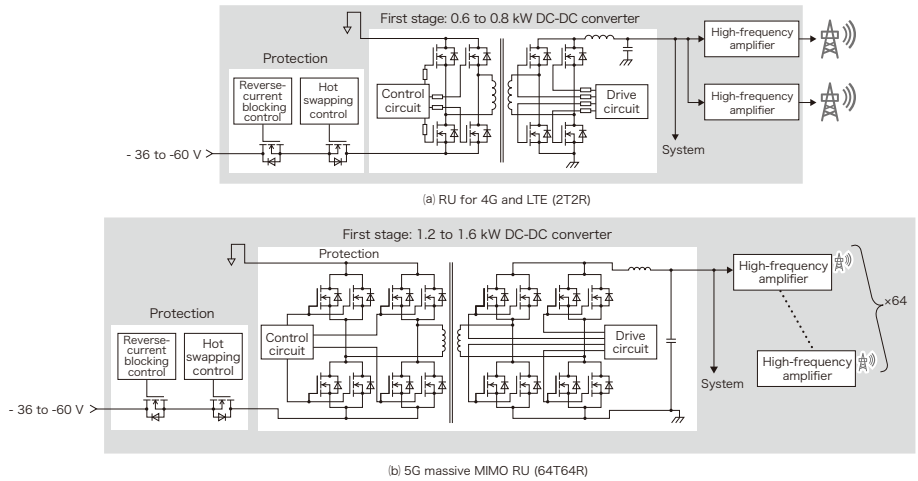



**Figure 1. Configuration of power supply for 5G radio unit (RU)**

A 5G RU incorporates an array of many antennas, for example, in a 64T64R configuration and has doublethe number of internal power supply outputs.

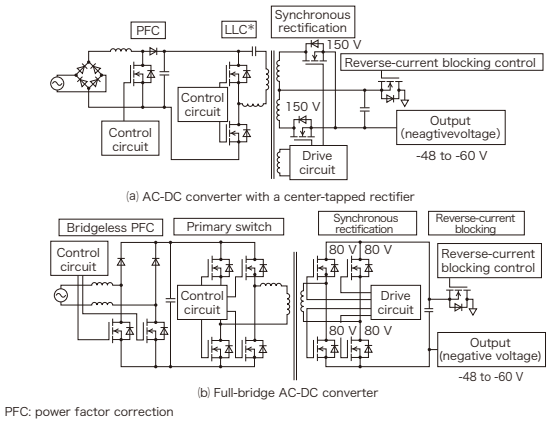



**Figure 2. Examples of typical AC-DC converter topologies**

The withstand voltage required for rectifier devices is more than double the output voltage in the case of the AC-DC converter with a center-tapped rectifier and equal to the output voltage in the case of the full-bridge AC-DC converter. Therefore, the full-bridge AC-DC converter can use rectifier devices with half the withstand voltage.

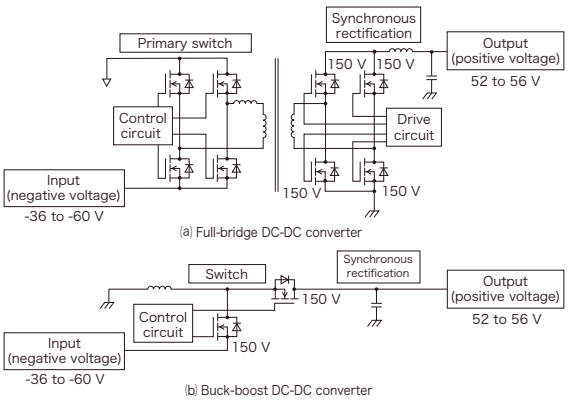
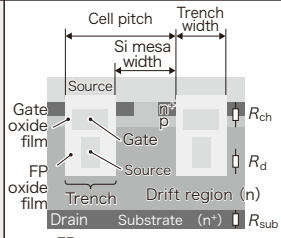
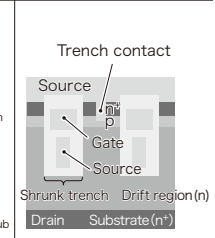
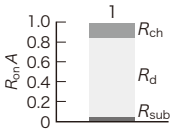
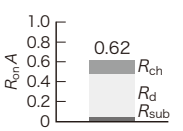



**Figure 3. Examples of typical first-stage DC-DC converter topologies**

There are two types of DC-DC converters: full-bridge and buck-boost DC-DC converters. Which type to select depends on the board area requirement, efficiency, and cost.

# 3. Reducing the conduction loss of 80 V MOSFETs

Typical silicon (Si) power MOSFETs have a vertical structure. Therefore, current flows vertically through the silicon chip. In order to reduce the conduction loss of a Si power MOSFET, it is effective to increase its integration level through geometry scaling. It is difficult, however, to scale the geometries of power MOSFETs because of their vertical, stepped structure. $R_{on}$, a contributing factor for a conduction loss, consists of the channel resistance ($R_{ch}$) and the drift resistance ($R_d$) of the MOSFET on the surface of a chip as well as the substrate resistance ($R_{sub}$). We have been offering successive generations of trench-gate MOSFETs called the U-MOS series, with each generation having progressively smaller on-resistance per area ($R_{on}A$). Up to the U-MOS VII-X series, we had relied on nanofabrication technology to reduce $R_{ch}$. Specifically, we had gradually reduced the cell pitch of the trench-gate structure to increase the channel density. For the U-MOS VIII-H series, a process node preceding the latest U-MOS X-H series, we employed a trench field-plate (FP) structure to increase the dopant concentration in the drift region in order to achieve a substantial reduction in $R_d$. Wafer-thinning technology was also utilized to reduce the chip thickness to roughly 50 µm, less than half that of the previous series, in order to reduce $R_{sub}$. For the launching of the latest U-MOS X-H series, we have further reduced the cell pitch of the FP structure. **Figure 4** compares the structure and on-resistance of the 80 V MOSFETs fabricated using the U-MOS VIII-H and U-MOS X-H processes. Since the trench of the FP structure is inactive when a MOSFET is in the "on" state, it is desirable that the ratio of the trench width to the cell pitch be small. In order to reduce the FP trench width of the U-MOS X-H series, we have increased the taper angle of the trench and buried a polysilicon layer in the trench. However, a reduction in the trench width causes its aspect ratio to increase, making it more difficult to form the internal polysilicon electrodes. We have overcome this difficulty by developing a new technology for burying the polysilicon layer in the trench. We have also reduced the Si mesa width by means of a trench contact structure using tungsten. Furthermore, we have optimized the dopant profile in the drift region and multiple design factors, thereby achieving a 38% reduction in $R_{on}A$ compared to the previous U-MOS VIII-H series.

| Generation | U-MOS VIII-H | U-MOS X-H |
|---|---|---|
| Device structure (new technologies adopted) |  <br>・FP structure<br>・Chip thinning |  <br>・Shrunk FP structure<br>・Si mesa width reduction (trench contact)<br>・Trench width reduction (increased taper angle, buried polysilicon layer) |
| $R_{on}A$* ($V_{GS}$ = 10 V) |  |  |
| $R_{on}Q_{oss}$* | 1 | 0.83 |
| $R_{on}Q_{sw}$* | 1 | 0.89 |

p: p-type semiconductor n: n-type semiconductor
$n^+$: heavily doped n-type semiconductor
$V_{GS}$: gate-source voltage
* Normalized such that $R_{on}A$ of U-MOS VIII-H is equal to 1

**Figure 4. Comparison of structure and on-resistance characteristics of 80 V MOSFETs fabricated using previous and new processes**

The latest U-MOS X-H series has 38% lower $R_{on}A$ than the previous UMOS VIII-X series because of a shrunk trench field-plate structure and optimized design factors.

# 4. Reducing the switching loss of 80 V MOSFETs

A side effect of the increased MOSFET integration level is an increase in junction capacitance, causing $Q_{sw}$ and the output charge ($Q_{oss}$) to increase. This, in turn, causes an increase in switching loss. Therefore, each generation of U-MOS has been designed to reduce not only $R_{on}$ but also $Q_{sw}$ and $Q_{oss}$. For the U-MOS VIII-H series, we buried the source electrode under the gate electrode in the trench to achieve a substantial reduction in $Q_{sw}$.

Because of the optimized design, the latest 80 V U-MOS X-H series provides a 17% reduction in $R_{on}Q_{sw}$, a performance index for conduction and switching losses, and an 11% reduction in $R_{on}Q_{sw}$, a performance index for conduction and output charge losses, compared to the U-MOS VIII-H series.

A transient surge of the drain-source voltage ($V_{DSpeak}$) during switching affects a system's stability and reliability. In order to reduce the $V_{DSpeak}$ of the U-MOS X-H series, we have optimized the resistance of the internal gate and the source wire. As a result, the U-MOS X-H series has 26% lower $V_{DSpeak}$ than a typical device from another manufacturer as shown in **Figure 5** when compared at a switching rate of 300 A/µs. Therefore, the U-MOS X-H series helps improve system reliability. This means that, given two MOSFETs with the same $V_{DSpeak}$, the U-MOS X-H series allows faster switching and therefore contributes to reducing a switching loss.

A power MOSFET has a pn body diode between the source and the drain (p: p-type semiconductor, n: n-type semiconductor). This diode enters reverse recovery mode when it is reverse-biased while current is flowing through it.

This causes the residual carriers to be swept out of the body diode, causing reverse current. If the reverse recovery charge ($Q_{rr}$) is large, a reverse recovery loss contributes to an increase in switching loss. Because of the shrunk cell pitch and the optimized dopant profile in the drift region, the U-MOS X-H series exhibits 12% lower $Q_{rr}$ than an existing MOSFET from another manufacturer as shown in **Figure 6** when compared at a switching rate of 300 A/μs.

**Figure 7** shows the results of a hardware evaluation of a full-bridge rectifier circuit for a 300 W DC-DC converter. As a result of improving various electrical characteristics, the U-MOS X-H series provides an equivalent or higher power conversion efficiency than the existing MOSFET from another manufacturer, achieving a peak power conversion efficiency of 94.83%. As described above, the U-MOS X-H process has successfully achieved a reduction in conduction and switching losses as well as an improvement in power conversion efficiency in an actual application. As a result, we released 80 V MOSFETs fabricated using the U-MOS X-H process in March 2020.

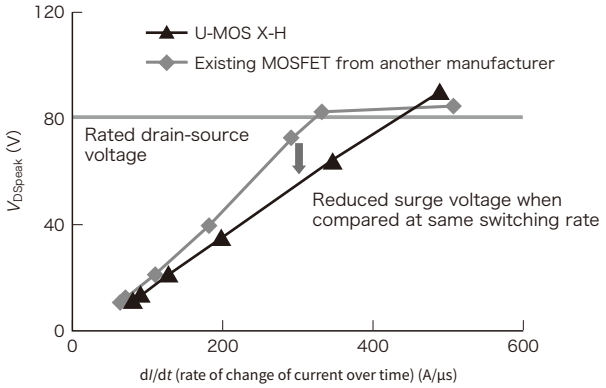



**Figure 5. Surge voltage at time of switching of 80 V MOSFETs**

Because of the optimized internal wire resistance, the U-MOS X-H series provides 26% lower $V_{DSpeak}$ than an existing MOSFET from another manufacturer when compared at a switching rate of 300 A/μs.

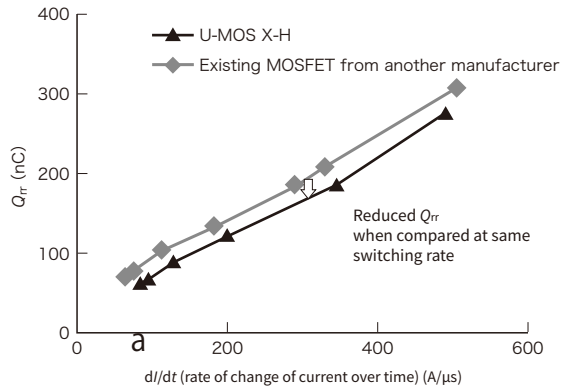



**Figure 6. Recovery charge of characteristics of 80 V MOSFETs**

Because of the shrunk cell pitch and the optimized dopant profile in the drift region, the U-MOS X-H series provides 12% lower $Q_{rr}$ than an existing MOSFET from another manufacturer when compared at a switching rate of 300 A/μs.

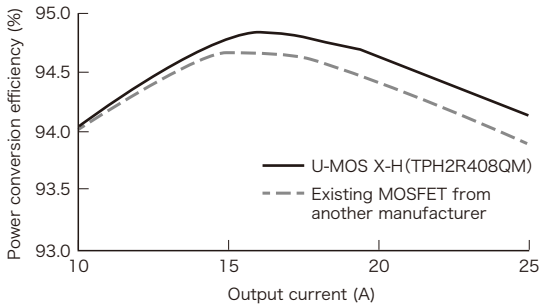
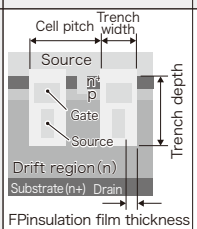
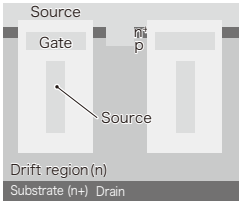



**Figure 7. Power conversion efficiency of 80 V MOSFETs**

The TPH2R408QM of the U-MOS X-H series provides an equivalent or higher performance than the existing MOSFET from another manufacturer, achieving a peak power conversion efficiency of 94.83%.

# 5. Development of a 150 V MOSFET

We have also developed a 150 V MOSFET based on the device structure of 80 V MOSFETs. Our focus was on reducing an increase in $R_{on}$ due to an increase in withstand voltage. **Figure 8** compares the cell structure of 80 V and 150 V MOSFETs. In order to increase the withstand voltage, it is necessary to increase the thickness of the drift region (n) and accordingly the trench depth. On the other hand, a reduction in the cell pitch to increase the cell aspect ratio (i.e., trench depth divided by cell pitch) helps reduce $R_{on}$[(1)]. Therefore, in addition to the process technologies developed for the 80 V MOSFETs, it was necessary to develop additional technologies in order to realize a 150 V MOSFET. For example, in order to reduce the cell pitch and thereby $R_{on}$, we have developed an etching technology to control the shape of the high-aspect-ratio trench and a technology to form a thick,

| Generation /withstand voltage | U-MOS X-H 80 V | U-MOS X-H 150 V |
|---|---|---|
| Device structure |  |  |
| Cell pitch* | 1 | 1.8 |
| Trench width* | 1 | 2.1 |
| Trench depth* | 1 | 1.9 |
| FP insulation film thickness* | 1 | 2.1 |



*Normalized such that the insulation film thickness of 80 V U-MOS X-H MOSFET is equal to 1

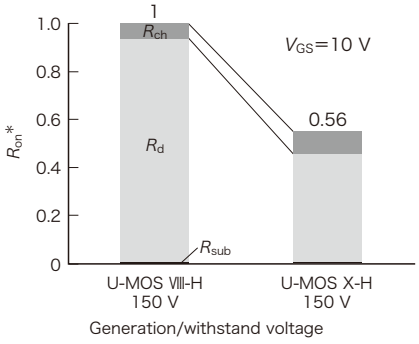
**Figure 8. Comparison of cell dimensions of 80 V and 150 V MOSFETs**

The width and depth of the trench is larger than the cell pitch, and the Si mesa between trenches has a high aspect ratio.

uniform insulation layer for trench isolation.

**Figure 9** compares the on-resistance characteristics of 150 V MOSFETs fabricated using the U-MOS X-H and U-MOS VIII-H processes. As a result of the foregoing, the 150 V U-MOS X-H MOSFET is expected to exhibit 56% lower $R_{on}$ than the counterpart of the U-MOS VIII-H series.

We will release the 150 V U-MOS X-H MOSFET fabricated using these technologies in April 2021.




* Normalized such that the $R_{on}$ of 150 V U-MOS VIII-H MOSFET is equal to 1

**Figure 9. Comparison of on-resistance characteristics of 150 V MOSFETs fabricated using previous and new processes**
Because of the considerably reduced $R_d$, the U-MOS X-H series is expected to provide a 56% lower $R_{on}$ than the U-MOS VIII-H series.

# 6. Conclusion

We have developed 80 V U-MOS X-H MOSFETs that will contribute to reducing the power consumption of base stations for high-capacity wireless mobile communications. Compared to the previous series, these MOSFETs provide a 17% reduction in $R_{on}Q_{sw}$, a performance index for power efficiency. In order to shrink device geometries and thereby reduce both conduction and switching losses, we modified the device structure and improved process technologies based on the existing FP structure. Based on these technologies, we are also developing a 150 V MOSFET with a Si mesa having a higher aspect ratio. We will continue to further improve these technologies to develop power devices with even higher power efficiency that will satisfy the market requirements for a reduction in power consumption so that we can contribute to the realization of a society in which energy-saving is the norm.

## References

(1) Saito, W. 2013. "Comparison of theoretical limits between superjunction and field plate structures". 2013 25th International Symposium on Power Semiconductor Devices & IC's (ISPSD 2013). Kanazawa, 2013-05, IEEE. 2013: 241–244.