TOSHIBA

Basic Knowledge of Discrete Semiconductor Device

Chapter III

Transistors

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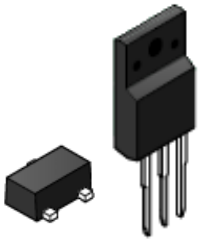
Toshiba Electronic Devices & Storage Corporation

Types of Transistors

Transistors are roughly classified into three types: bipolar, field effect and insulated gate bipolar.
Bipolar transistors are current-driven devices. Field-effect transistors (FET) and insulated-gate bipolar transistors (IGBT) are voltage-driven devices.

Transistors

- **Bipolar transistors (BJTs)**
  - **Bipolar transistors (BJTs)**
  - **Bias Resistor Built-in Transistors (BRTs)**
- **Field-effect transistors (FETs)**
  - **MOSFETs**
    Metal-oxide-semiconductor field-effect transistors
  - **Junction FETs (JFETs)**
    Junction field-effect transistors
- **Insulated-gate bipolar transistors (IGBTs)**



Bipolar Transistors (BJTs)

There are two types of bipolar transistors: NPN type and PNP type. NPN-type products have low withstand voltage to high withstand voltage. PNP-type products with withstand voltage of 400 V or less, and particularly those with withstand voltage of 200 V or less, are mainstream.

There is an amplification function to convert small signals to large signals. The ratio of collector current IC and base current I_B (I_C/I_B) is called DC current gain, denoted as h_{FE}.

When small current (IB) flows from base to emitter, current of I_B x h_{FE} flows from collector to emitter.

BJTs are current-driven devices driven by base current.

Operation of NPN transistor

Base current: Current from base to emitter

Collector current: Current from collector to emitter

Operation of PNP transistor

Base current: Current from emitter to base

Collector current: Current from emitter to collector

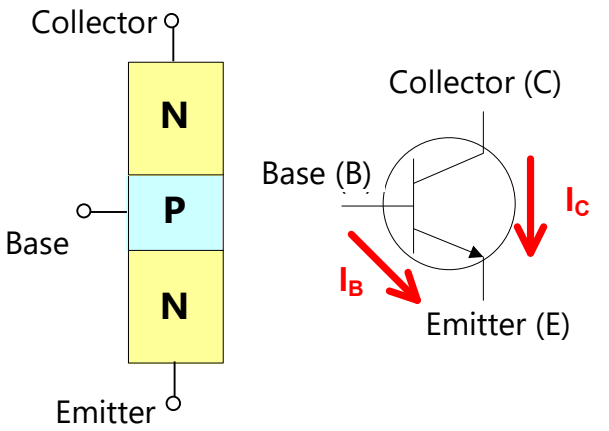


Fig. 3-1(a) Symbol and structure of NPN transistor

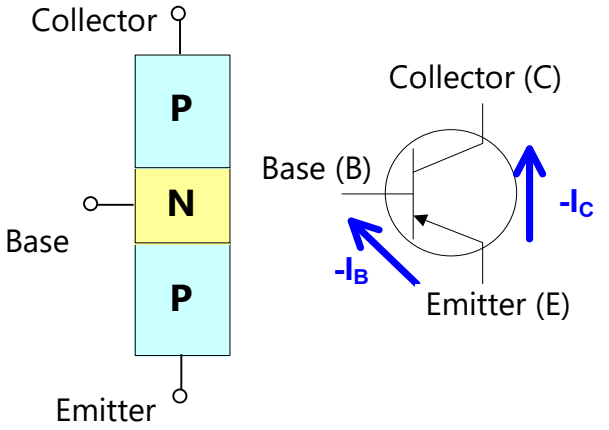


Fig. 3-1(b) Symbol and structure of PNP transistor

Bias Resistor Built-in Transistors (BRTs)

BRTs are bias resistor built-in transistors. BJTs are often used together with resistors in electronic equipment. The mounting area can be reduced by using BRTs, which integrate a transistor and a resistor.

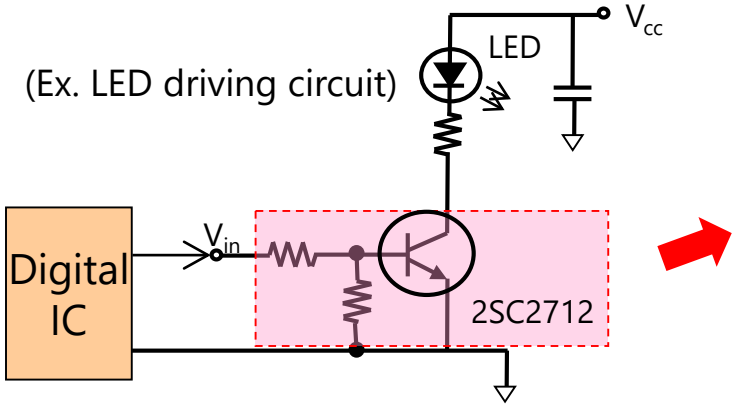


Fig. 3-2(a) Application example of BJT

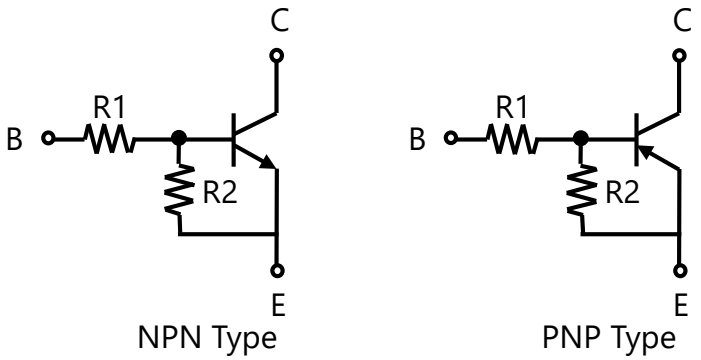
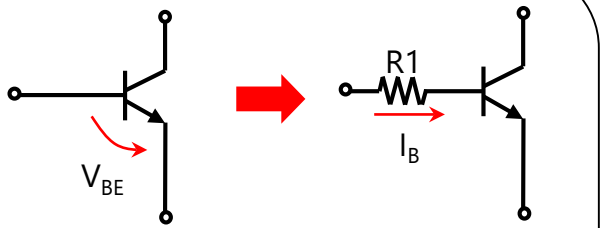


Fig. 3-2(b) Equivalent circuit of BRT

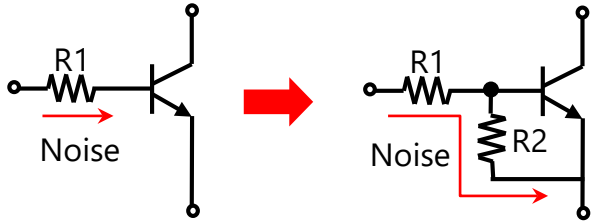


Unstable operation

It is difficult to control without current limitation.

Stable operation

It is easier to control input current by inserting input resistance.



Tend to malfunction, affected by noise of base.
Current directly flows to base of transistor, and it turns on.

Rare malfunction

Malfunction is rare, because noise goes through R2, which works as a bypass.

Fig. 3-2(c) Why BJT needs resistance in its base circuit

Junction Field-Effect Transistors (JFETs)

<Operation of JFETs>

JFET: Junction Field-Effect Transistor

(1) In the N-channel junction field-effect transistor (Figure 3-3 (a)), when a voltage is applied between the drain and the source, electrons flow from the source to the drain.

(2) When a reverse bias is applied between the gate and source, the depletion layer expands and suppresses the electron flow in (1). (Narrowing path of electron flow)

(3) If the reverse bias voltage between the gate and source is further increased, the depletion layer blocks the channel and the flow of electrons stops.

As shown above, voltage applied between gate and source controls the condition between drain and source. So FETs are voltage-driven devices.

(Note: Direction of current flow is opposite to that of electron flow. The mechanism of widening of the depletion layer is the same as for diode.)

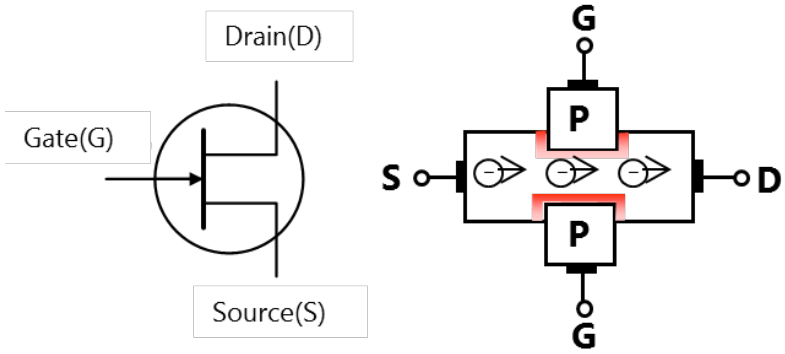


Fig. 3-3(a) Symbol and operation of N-channel-type JFET

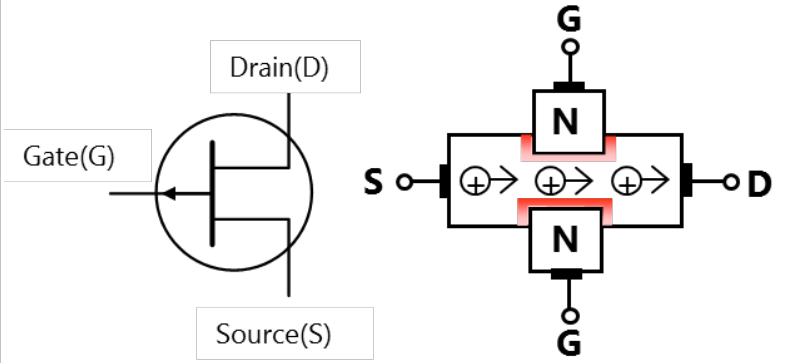


Fig. 3-3(b) Symbol and operation of P-channel-type JFET

Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs)

The Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is currently attracting the most attention among transistors.
There are two types of MOSFET: N channel (See Fig.3-4(a) Nch below) and P channel (See Fg.3-4(b) Pch below).
Nch is widely used for AC/DC power supplies, DC/DC converters, inverter equipment, etc., whereas Pch is used for load switches, high-side switches, etc.
The differences between the bipolar transistor and the MOSFET are shown in Table 3-1.

Table 3-1 Comparison of BJT and MOSFET

BJT (Current-driven device)	**MOSFET (Voltage-driven device)**
•Low input impedance •Large reverse transfer capacitance •Narrow safe operating region •Enables low-voltage operation (On voltage is 0.6-0.7 V)	•**High input impedance** •Small reverse transfer capacitance •**Wide safe operating region** •**Low gate power consumption** •**Easy driving**

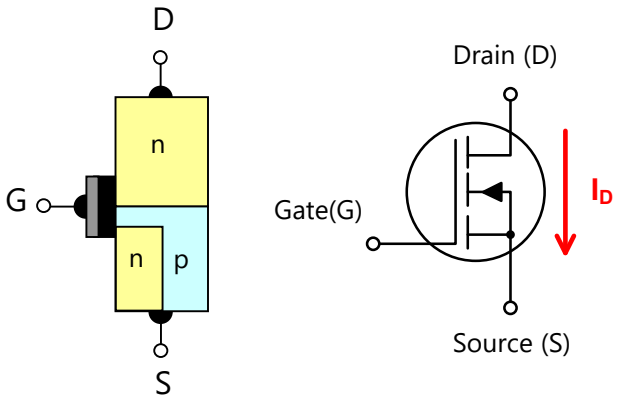


Fig. 3-4(a) Symbol and operation of N-channel MOSFET

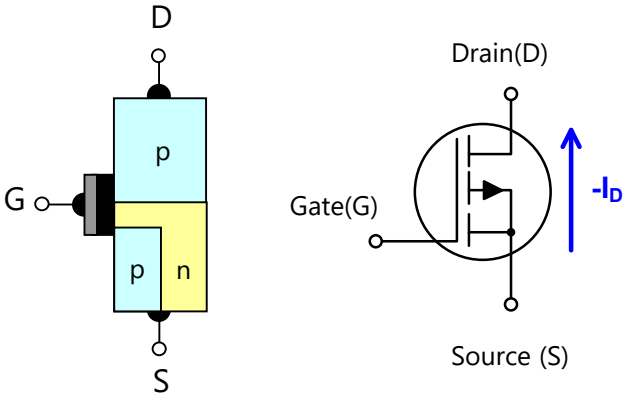


Fig. 3-4(b) Symbol and operation of P-channel MOSFET

Differences between BJT and MOSFET

Explanation of the differences between ON/OFF operation of BJT and MOSFET.

(1) Base current of BJT starts flowing when base voltage increases, and collector current is in proportion to this base current. This flow starts at about 0.7 V. This voltage is called the base-emitter threshold voltage (VBE). In order to make collector current flow, it is necessary to supply the base current and continuous driving power is required. (Low drive voltage, continuous driving power required)

(2) Since the MOSFET forms a channel according to the gate-source voltage, this voltage must be a certain voltage or more. Once the channel is formed, the ON state continues and the drain current continues to flow, and so the power required for the driving is small. By discharging the charge accumulated in the gate and removing the channel, it shifts to the OFF state. (Driving voltage higher than BJT, small driving power)

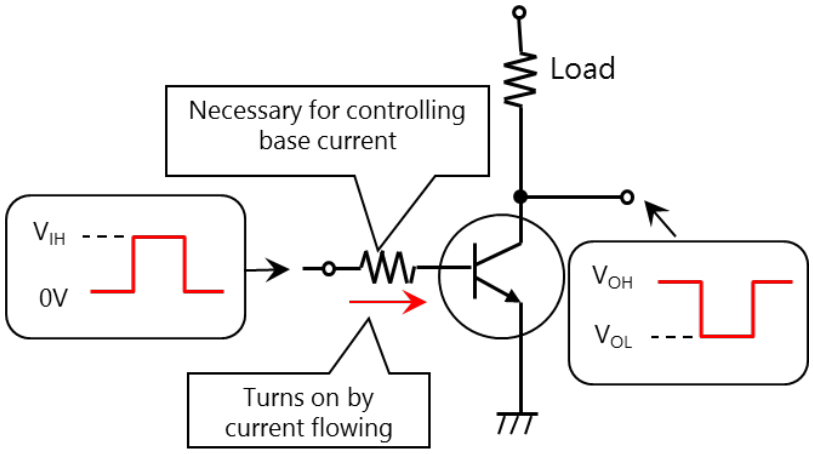


Fig. 3-5(a) Switching operation of BJT

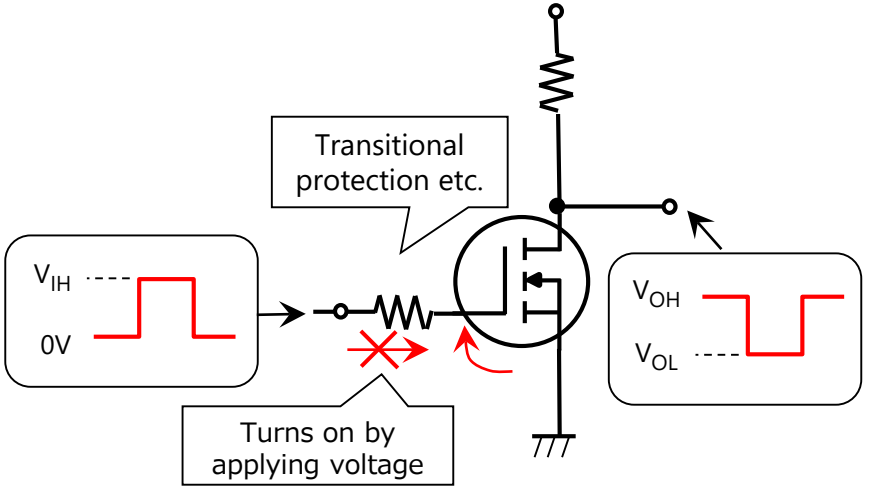


Fig. 3-5(b) Switching operation of MOSFET

Structure and Operation of MOSFET

Here we explain the operation of the MOSFET, referring to Fig. 3-6(a).

(1) Apply voltage between drain and source with positive drain polarity. (Drain-source voltage: VDS)

(2) Apply voltage between gate and source with positive gate polarity. (Gate-source voltage: VGS)

(3) As a result, electrons are attracted to the p-type layer just under the gate insulator film, and part of the p-type layer is turned into n-type region. (This n-type region in this p-type layer is called the "inversion layer (channel)".)

(4) As this inversion layer is completed, an n-layer path is formed from the drain to the source of the MOSFET.
(n + ⇔ n - ⇔ inversion layer (n) ⇔ n +)

(5) As a result, the MOSFET works at low resistance, and drain current is determined by applied VDS and load flows.

Planar gate MOSFET (π-MOS)

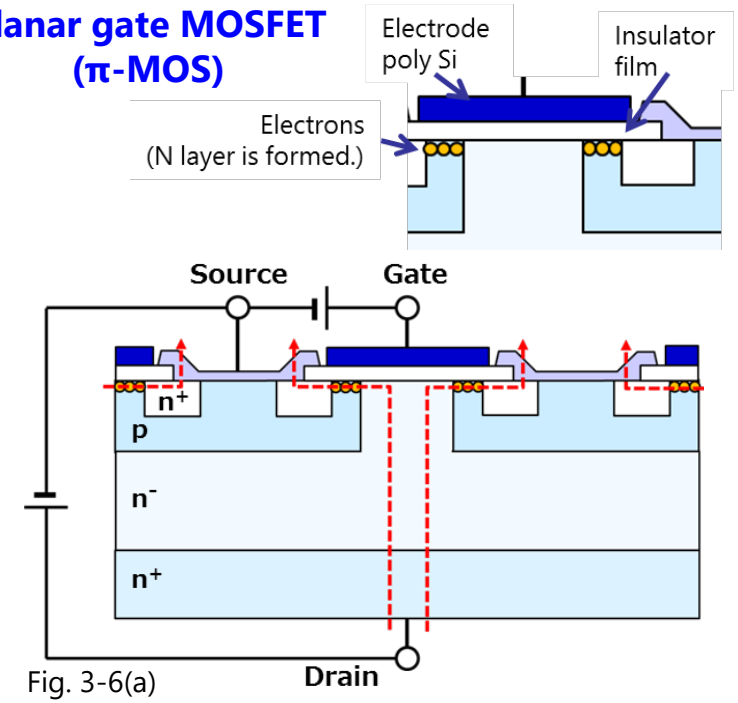


Fig. 3-6(a)
Structure and operation of planar gate MOSFET

Trench gate MOSFET (U-MOS)

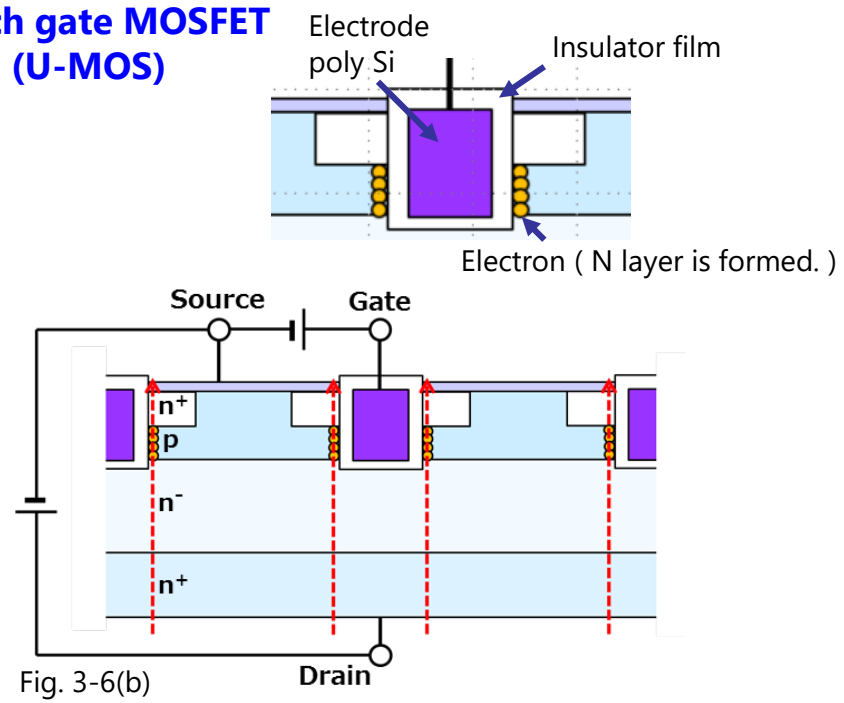


Fig. 3-6(b)
Structure and operation of trench gate MOSFET

MOSFET Performance Improvement: Decision Factors of $R_{DS(ON)}$

1) The MOSFET device structure is selected according to the required voltage rating(V_{DSS}). For example, many middle and high voltage MOSFETs (V_{DSS}=250V or higher) have planar gate MOS(π-MOS) structure, and products with less than V_{DSS}=200V have more trench gate MOS(U-MOS).
2) The factor that determine the on-resistance $R_{DS(ON)}$ are shown in Fig.3-7 and Equation 3-(1). Depending on the structure and V_{DSS} of MOSFET, the ratio of factors determining $R_{DS(ON)}$ will change. When the π-MOS structure is chosen, R_{drift} becomes the dominant factor in V_{DSS}=600V products, while the ratio of R_{ch}+$R_{J\text{-}FET}$ is high in V_{DSS}=30V products. However by applying U-MOS structure, R_{ch} will be very small.

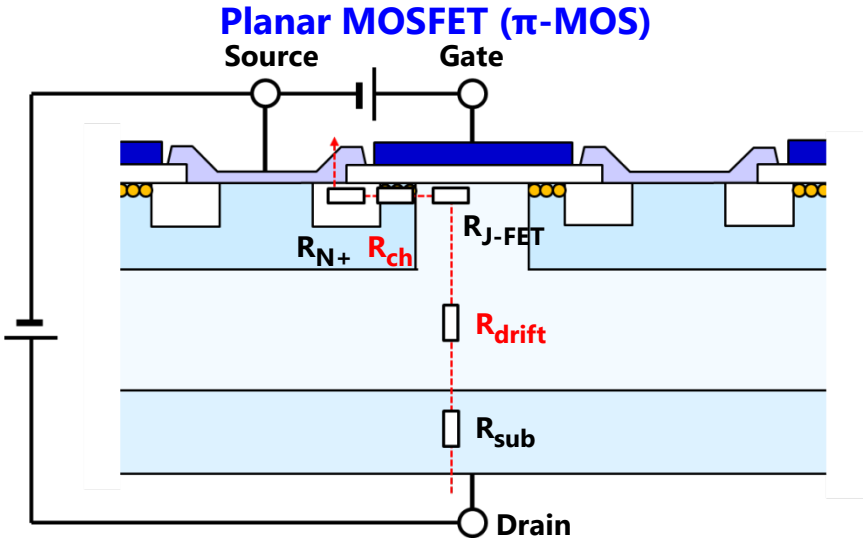


Fig. 3-7(a) $R_{DS(ON)}$ decision factors of π-MOS

$R_{DS(ON)}=R_{sub}+R_{drift}+R_{J\text{-}FET}+R_{ch}+R_{N+}$ --- Equ.3-(1)a

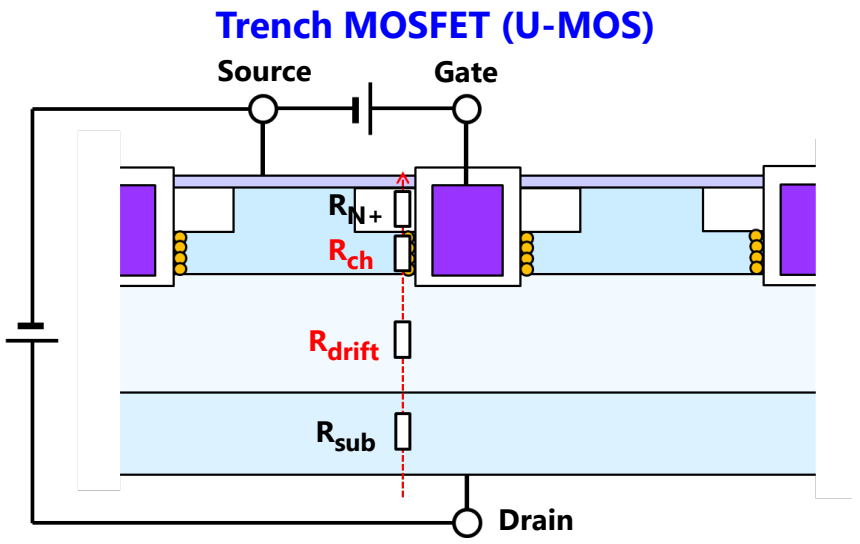


Fig. 3-7(b) $R_{DS(ON)}$ decision factors of U-MOS

$R_{DS(ON)}= R_{sub}+R_{drift}+R_{ch}+R_{N+}$ --- Equ.3-(1)b

@ V_{DSS}=600 V : R_{drift} >> R_{ch} > $R_{J\text{-}FET}$, R_{N+} , R_{sub} ➔ $R_{DS(ON)}$ depends on R_{drift}

@ V_{DSS}= 30V : ●π-MOS --- R_{ch} + $R_{J\text{-}FET}$ > R_{drift} >> R_{N+} , R_{sub}. ●U-MOS --- R_{ch}≈ R_{drift} >> R_{sub}, R_{N+}

➔ Dependence of $R_{DS(ON)}$ on R_{ch} can be minimized by fine patterning of U-MOS structure.

MOSFET Performance Improvement: Approach to Low $R_{DS(ON)}$

Summary of approach to low ON resistance

$$R_{ON} = R_{sub} + R_{drift} + R_{J\text{-}FET} + R_{ch} + R_{N+}$$

Methods	Disadvantages	Improvements
Fine pattern	Increment of C_{iss}	Shorter channel
Fine pattern Trench	Same as above	Trench & shorter channel
Super junction	Long production TAT	Single epitaxial
Thin wafer (High density of N++)	Difficult to produce	Thin-wafer technology

We are pursuing the following countermeasures for the biggest problem of MOSFET: "How to effectively reduce on-resistance by effectively utilizing the element area"

1. High voltage: Reduce resistance of Rdrift by the advanced super-junction process explained on the next page.
2. Low voltage: Minimize resistance of Rch by fine patterning of trench structure and reduce resistance of Rsub by thinning wafer

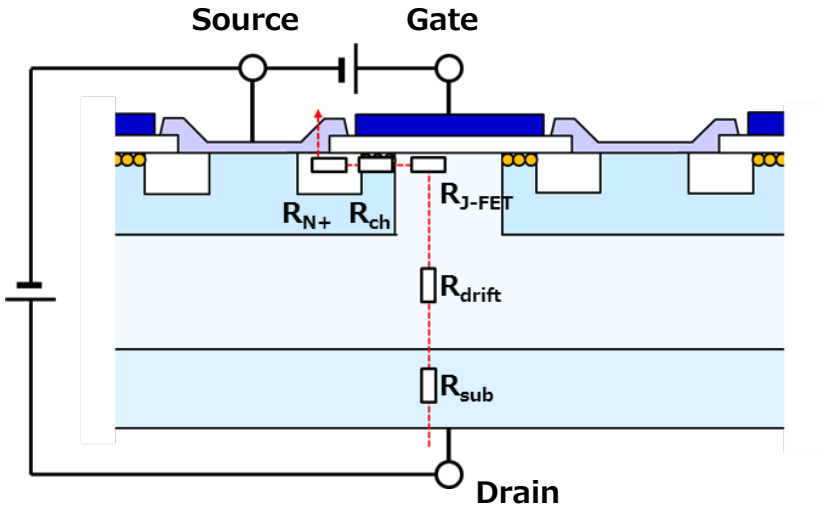


Fig. 3-8 Factors for ON resistance of MOSFET

MOSFET Performance Improvement: Super-Junction MOSFETs (SJ-MOS)

(1) SJ-MOS has pillar-shaped P layer (P pillar layer) in N layer. P and N layers are aligned alternately. (See Fig. 3-9(b).)

(2) Depletion layer spreads in N- layer by applying V_{DS}, but the way it spreads in SJ-MOS is different from the case of general D-MOS. (See Fig. 3-9(a)/(b) for electric field intensity. Electric field intensity indicates the status of depletion layer.)

(3) In the case of D-MOS the electric field intensity is the strongest at P/N- layer interface. When the electric field intensity exceeds the limit of silicon, break-over phenomenon (breakdown phenomenon) occurs, and this is the voltage limit. On the other hand, in the case of SJ-MOS, the electric field intensity is uniform in N layer.

(4) As a result, SJ-MOS can be designed with N layer that has lower resistance, realizing low-ON-resistance products. SJ-MOS can realize lower ON resistance with the same size chip as DMOS.

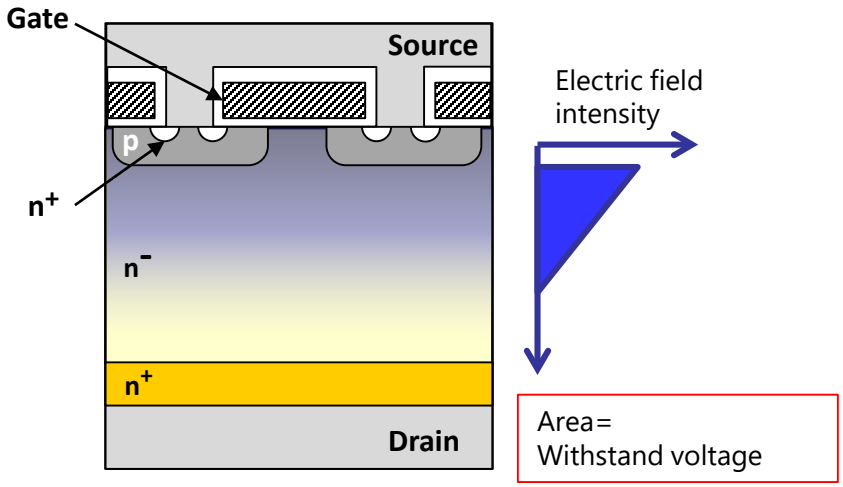


Fig. 3-9(a) Structure and electric field of D-MOS (π-MOS)

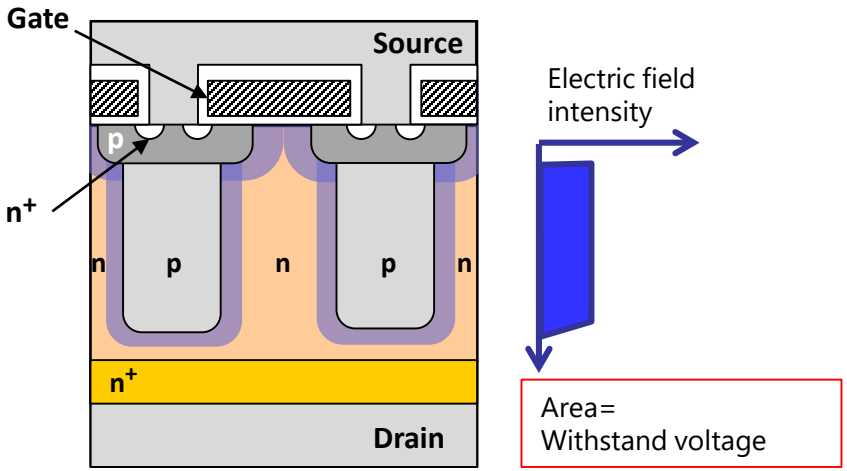


Fig. 3-9(b) Structure and electric field of SJ-MOS (DTMOS)

Summary of MOSFET Features by Structure

Features and main applications based on the structure of various MOSFETs are shown in Table 3-2.
・Withstand voltage: The optimum structure is selected for the target withstand voltage.
・Low On-Resistance: U-MOS for products with 250 V or less, SJ-MOS (or DTMOS) are advantageous for products with more than that.
・High current: The same tendency as for low ON resistance.
・High Speed: U-MOS is disadvantageous for high-speed switching because of large gate capacity (Ciss).
Depending on the product, it is also commercialized for high-speed switching designed for small "Ron × Ciss" by taking advantage of the low ON resistance characteristic.

Table 3-2. Advantages and applications of MOSFETs by structure

Names at Toshiba		U-MOS	π-MOS	DTMOS
General name		Trench gate MOS	D-MOS Planer gate MOS	SJ-MOS
Withstand voltage		Better up to 250 V	Excellent up to 900 V	Excellent 600 V or higher
Low ON voltage		Excellent	Fair	Excellent
High current		Excellent	Fair	Excellent
High speed		Good/Excellent	Good	Excellent
Application	Field	Battery applications	Small- to medium-capacity converters	Medium- to large-capacity converters
	Equipment	PCM, NBPC, DC/DC converters, motor equipment for automobiles	Chargers, adaptors small- to medium-size TVs, LED lighting	Base station & server power supplies, medium- to large-size TVs, power conditioners

Performance of MOSFETs: Drain Current and Power Dissipation

Permissible loss and drain current, which are typical maximum ratings of MOSFET, are calculated as follows.
(A different expression of current is adopted for some products.)
Power dissipation is calculated by thermal resistance and channel temperature. Drain current is calculated by the calculated power dissipation and ON resistance, using Ohm's law.

P_D: Power dissipation

⇒ **Power loss allowed in designated temperature condition of the device**

Q) How much is P_D of MOSFET with $T_{ch(max)}$=150℃, T_c=25 ℃, $R_{th(ch-c)}$=3.13 ℃/W?

A) $P_D = \dfrac{T_{ch(max)} - T_c}{R_{th(ch-c)}} = \dfrac{150℃ - 25℃}{3.13℃/W}$ = 39.9 W ≒ 40 W

I_D: Drain current

⇒ DC rating: DC current that flows in forward direction. (defined at room temperature)

Q) How much is I_D rating of MOSFET with P_D=40 W, $R_{DS(ON)}$=0.16 Ω Max?

A) $I_D = (P_D/R_{DS(ON)})^{1/2} = (40\ W/0.16\ Ω)^{1/2} = 15.8$ A

I_{DP}: Pulse drain current

⇒ Maximum drain current at designated pulse width. Generally, about 4 times DC current

Q) How much is I_{DP} of MOSFET with I_D=15.8 A?

A) $I_D \times 4 = 15.8\ A \times 4 = 63.2$ A

Performance of MOSFETs: Avalanche Capability

As a feature of MOSFET * 1, if it is within a certain energy, drain current ID and below the rated channel temperature Tch, there is performance that does not break even if it exceeds the rated voltage VDSS. This is called avalanche capability, the allowable energy is called avalanche energy, and the current is called avalanche current.

*1: Some products do not guarantee the avalanche capability

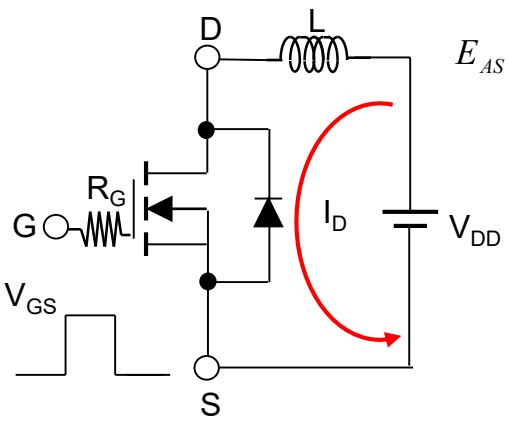
Avalanche energy

⇒ **Allowable maximum energy even when applied voltage exceeds V_{DSS} under designated conditions**

Avalanche current

⇒ **Allowable maximum current under avalanche condition**

SJ - MOS has a larger current density than D - MOS (π - MOS), but at the same current rating it has smaller avalanche capability.



$$E_{AS} = \int_0^{t_a} i_a(t) V_{BR} dt, \quad i_a(t) = I_{AR}\left(1 - \frac{t}{t_a}\right)$$

$$E_{AS} = \int_0^{t_a} I_{AR} V_{BR}\left(1 - \frac{t}{t_a}\right) dt$$

$$= I_{AR} V_{BR}\left[t - \frac{t^2}{2t_a}\right]_0^{t_a}$$

$$= \frac{t_a}{2}(I_{AR} V_{BR})$$

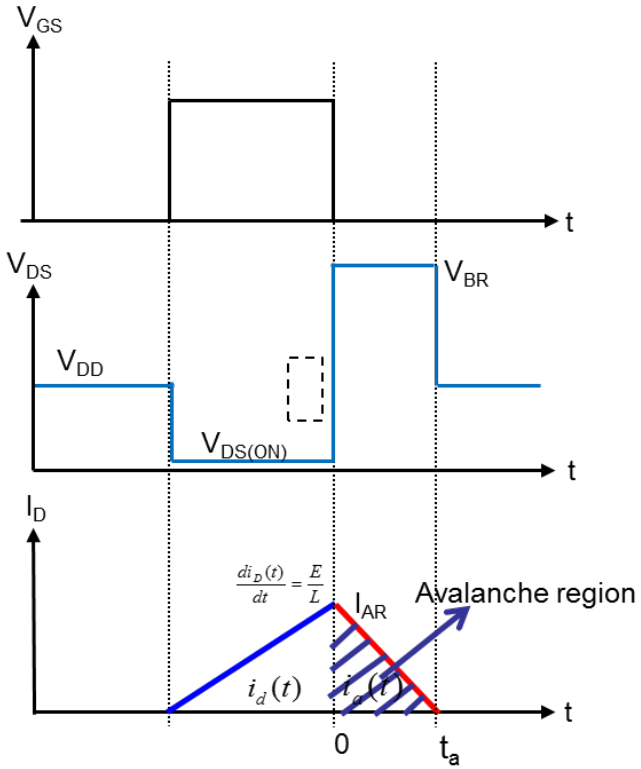


Fig. 3-10 Avalanche capability (energy, current) test circuit, waveform and calculation formula

Performance of MOSFETs: Characteristic of Capacitance

Capacitance characteristics of C_{iss}, C_{rss} and C_{oss} are important factors affecting switching characteristics of MOSFET.

C_{iss}: input capacitance ($C_{iss} = C_{gd} + C_{gs}$)

⇒Sum of gate-drain and gate-source capacitance: It influences delay time; the bigger the C_{iss}, the longer the delay time.

C_{rss}: Reverse transfer capacitance ($C_{rss} = C_{gd}$)

⇒Gate-drain capacitance: The bigger the C_{rss}, the more the characteristic of drain current rising deteriorates, which is disadvantageous for MOSFETs' loss. Low capacitance is needed to drive at high speed.

Coss: Output capacitance ($C_{oss} = C_{gd} + C_{ds}$)

⇒Sum of gate-drain and drain-source capacitance: It influences turn-off characteristic, and loss with light load. In the case of large C_{oss}, turn-off dv/dt decreases, which is advantageous for noise. But loss with light load increases.

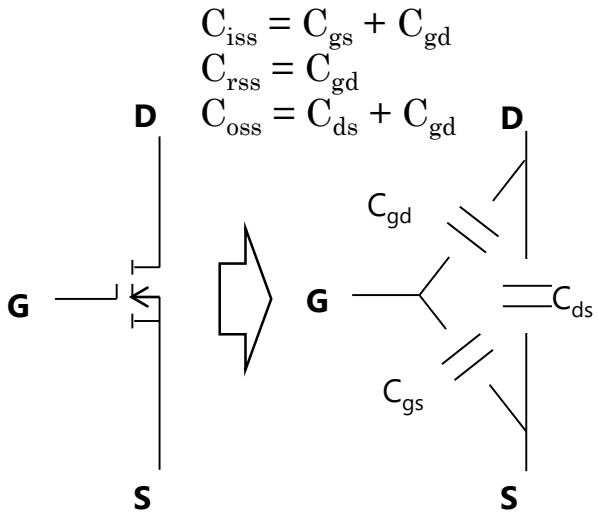


Fig. 3-11(a) Capacitance model of MOSFET

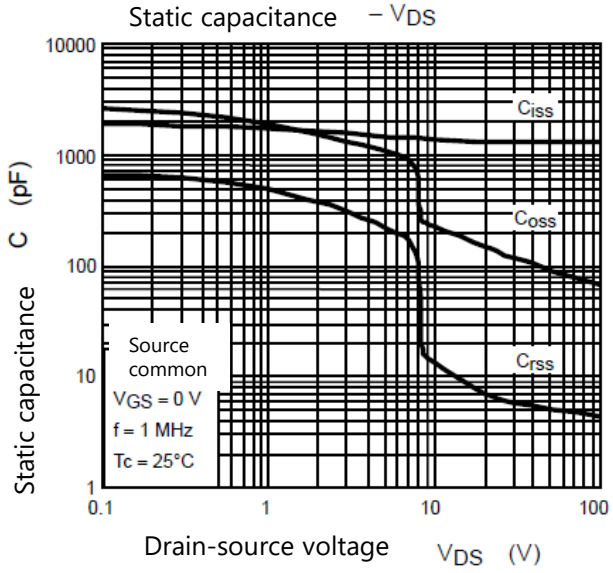


Fig. 3-11(b) Typical capacitance characteristic of MOSFET

Performance of MOSFETs: Safe Operating Area
(or Area of Safe Operation)

There are two modes of safe operating area (SOA).
1. Forward Bias SOA (F.B. SOA): Usable area of current and voltage at ON status.
2. Reverse Bias SOA (R.B. SOA): Usable area of current and voltage at turn-off operation. Applied pulse width is very narrow because of use under switching operation.

Each mode can be defined as shown in Fig. 3-12(a).

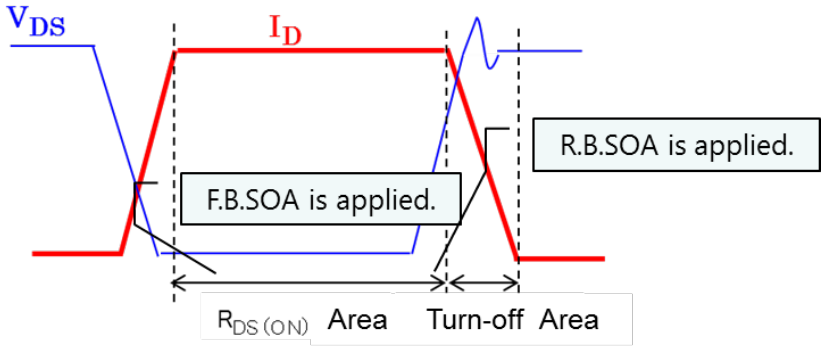


Fig. 3-12(a) Defining SOA in actual operation

- As for the guarantee of avalanche, rated voltage / current operation (short time) at turn-off is generally guaranteed as for the MOSFET, but R. B. SOA has not been announced.
- F.B.SOA consists of three restriction areas, rated current, rated voltage and thermal resistance areas, and secondary breakdown area.
- The three restriction areas are limited by ratings of device or calculated from thermal resistance. But secondary breakdown area is obtained by measurement of the actual device.

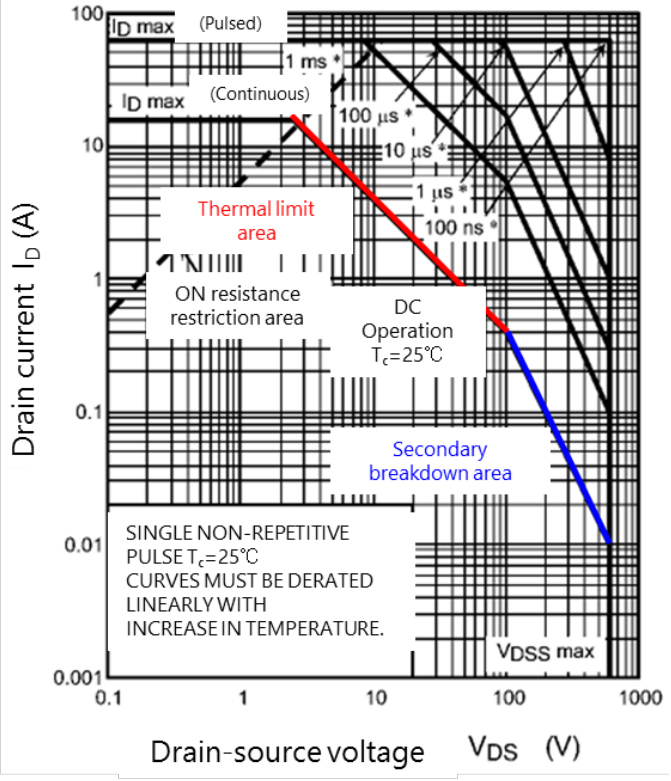


Fig. 3-12(b) Example of MOSFET's F.B.SOA

Insulated-Gate Bipolar Transistors (IGBTs)

An IGBT is a device suitable for high-current control combining a voltage-driven MOSFET in the front stage and a transistor allowing a large current to flow in the rear stage.

[Equivalent circuit and operation details]

•The equivalent circuit of the IGBT is shown in Figure 3-13 (b). The RBE value is set so that the NPN Tr does not turn on.

•Applying ON signal to gate of an Nch MOSFET turns on conduction state.

•As a result, current flows from the emitter to the base of PNP Tr. This base current works to lower the ON resistance of Nch MOSFET. (Conductivity modulation effect)

[Comparison with MOSFET]

•Gate driving operation is the same as Nch MOSFETs.

•In ON state, decrement of ON resistance of Nch MOS enables high current flow.

•Voltage drop across the emitter and base of PNP Tr occurs in the entire current region.(Approximately 1.0 V is added up as ON voltage.)

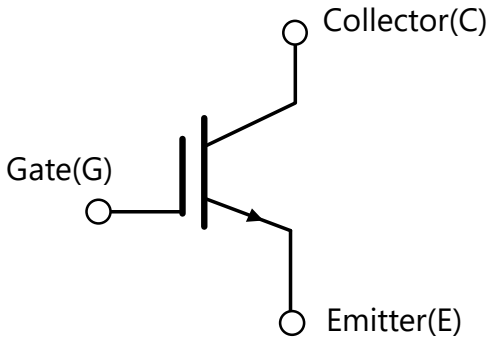


Fig. 3-13(a) Symbol of IGBT

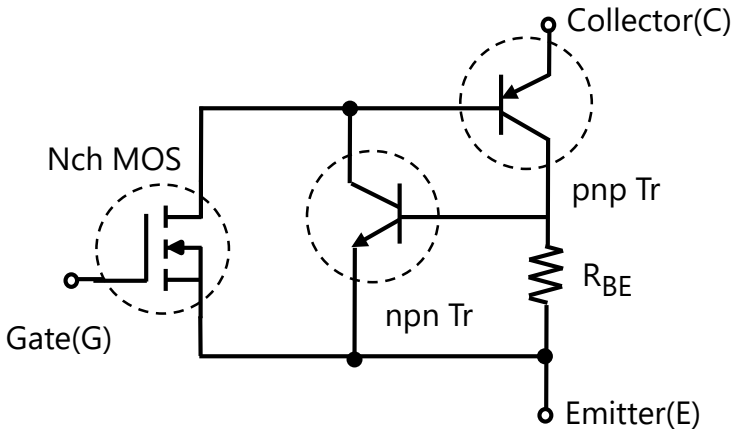


Fig. 3-13(b) Internal equivalent circuit of IGBT

Operation of Insulated-Gate Bipolar Transistors (IGBTs)

Operation of the IGBT connected as in Fig. 3-14(a) is shown below.

(1) Inversion layer is made in P layer under gate by applying positive voltage to gate. The Nch MOSFET in Fig. 3-14(b) turns on like a normal Nch MOSFET.

(2) When the Nch MOSFET is ON status, collector's potential is positive. So, holes are injected from P+ through N+ to N-, and this injection accelerates injection of electrons from emitter.

(3) As a result, increment of carriers (electrons and holes) decreases resistance of N- layer that normally has high resistance (conductivity modulation effect).

Thus, ON resistance of the Nch MOSFET varies to lower as shown in Fig. 3-14(b).

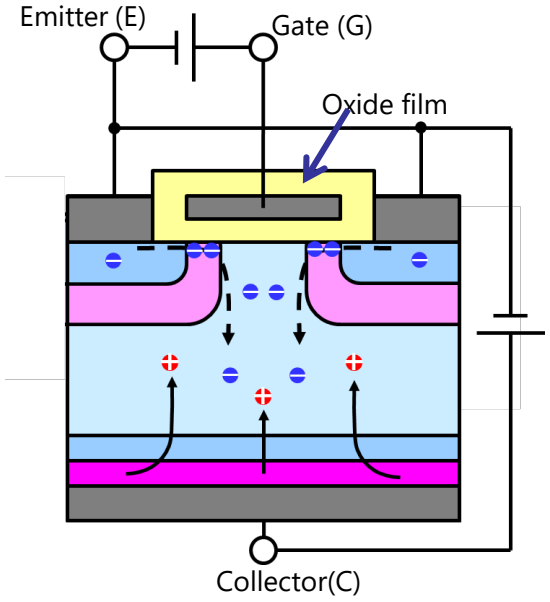


Fig. 3-14(a) Operation of IGBT

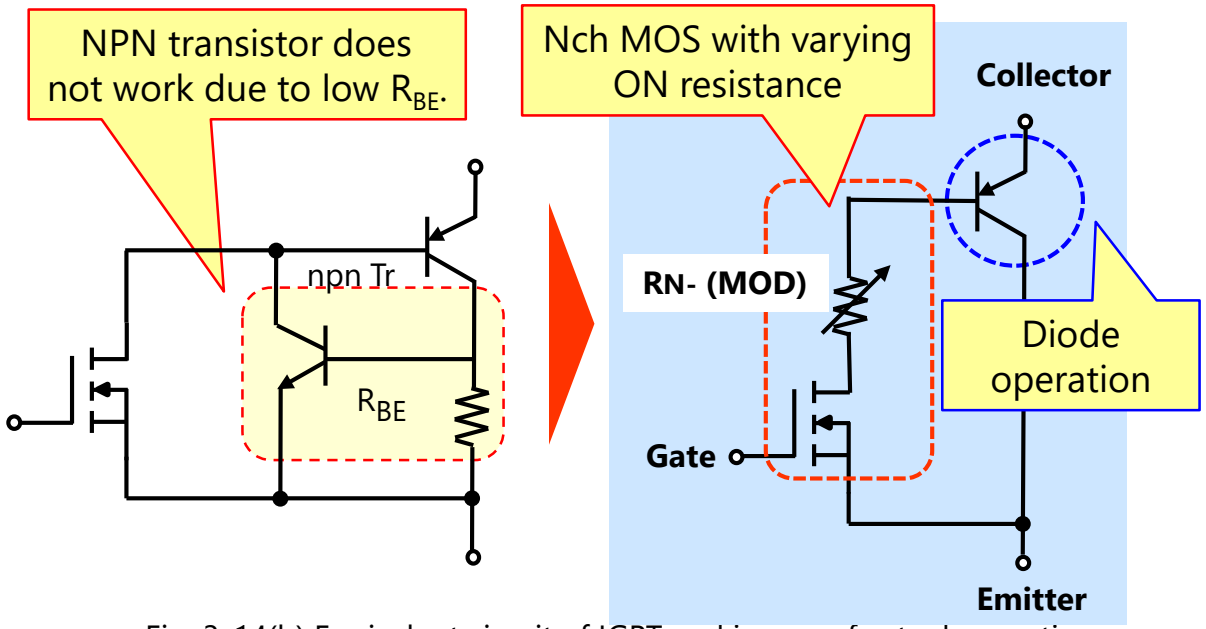


Fig. 3-14(b) Equivalent circuit of IGBT and image of actual operation

Performance Improvement of IGBTs: Evolution of Vertical Design

As shown in Figure 3-15 (a), the vertical design of the IGBT has been evolving.
Starting from the PT structure, thin PT (generally called "Field Stop") structure is becoming mainstream as thin wafers are now used. (Gate structure is the same as MOSFET.)

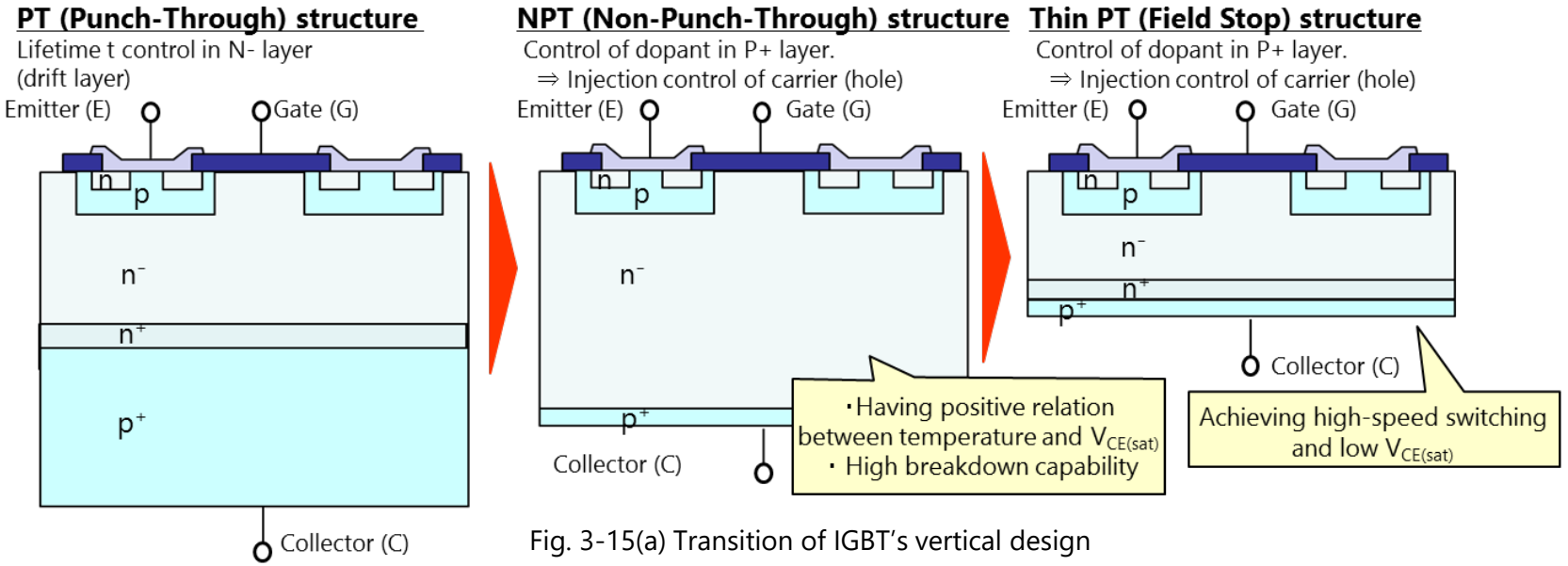


Fig. 3-15(a) Transition of IGBT's vertical design

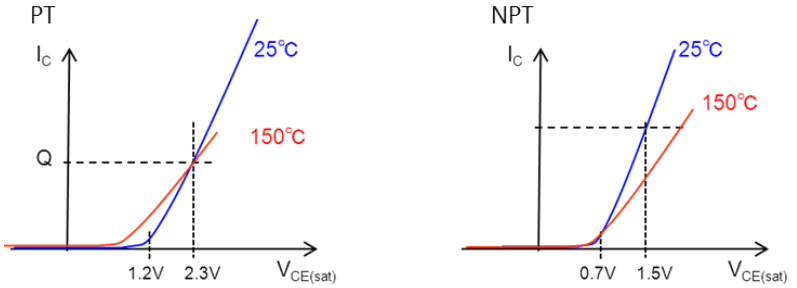


Fig. 3-15(b) Difference of forward characteristic between PT type and NPT type

VCE(sat) characteristic of PT type has a current value (called "Q point") that crosses at high temperature and at room temperature.

Since the high-temperature VCE (sat) is always high in the NPT type (like MOSFET), it is easier to balance the collector current even when operating in parallel.

Note: $V_{CE(sat)}$ characteristic - voltage drop when collector current flows in forward direction.

What are RC-IGBTs and IEGTs?

Reverse conductive IGBT: RC-IGBT

•The structure of the RC-IGBT is shown in Figure 3-16 (a). A diode is formed by making a part of the p-type layer, which is the collector of the IGBT, n-type. This diode has the same function as FWD * 1, which is generally inserted in the IGBT.

•With the introduction of thin wafer technology, it became possible to commercialize this configuration. Since the diode and the IGBT are one chip, it is easy to assemble. Because it is difficult to control the performance of the diode and the IGBT separately, the RC-IGBT is unsuitable for certain applications.

*1: FWD—Free-Wheeling Diode. Generally, it is used to send reflux current generated by a reactor.

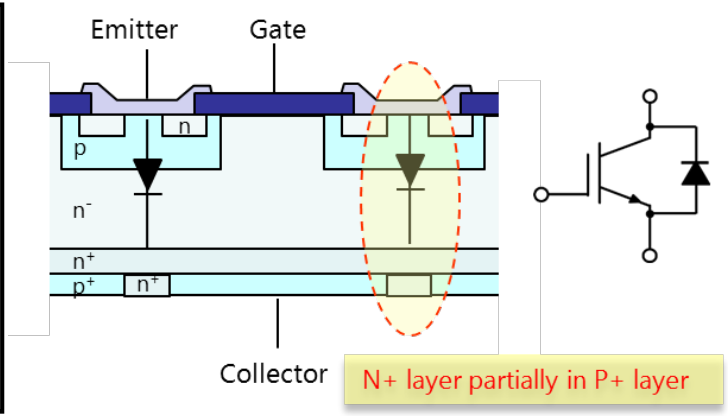


Fig. 3-16(a) Structure of RC-IGBT

Injection-enhanced gate transistor: IEGT

•Generally, in the high-voltage IGBT, it is difficult to obtain low VCE (sat) characteristics because the carrier concentration of the drift layer (n-type layer) on the emitter side is low.

•The IEGT was developed to obtain low VCE (sat) performance at high withstand voltage (generally 1200 V or higher).

• Fig. 3-16(b) shows the IEGT's structure and principle.

•It has a trench gate structure. Drawing out of the gate electrode is thinned out. As a result, carriers are accumulated just under the thinned gate electrode, increasing the carrier concentration on the emitter side.

•This high carrier density decreases resistance of drift layer, and makes VCE(sat) low.

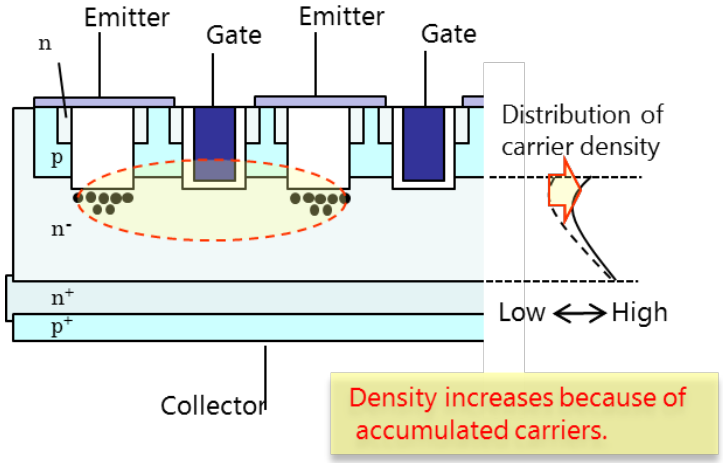


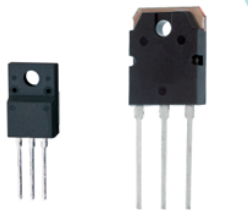
Fig. 3-16(b) Structure and carrier density of IEGT

Application of IGBTs

IGBTs are suitable for applications that have easy driving circuit and need high current. They are currently used in IH (Induction Heating) equipment adopting soft-switching under 50kHz, home appliances, vehicles, and a wide variety of AC drives. In future, their application fields are expected to expand to include various AC drives.

Table 3-3. Typical application of IGBTs

	Home appliance and induction heating equipment	General inverter
Features	**(1) Only for soft switching (voltage/current resonance)** **(2) Low switching loss** **(3) Includes an FWD**	**(1) For hard switching** **(2) High breakdown capacity** **(3) Includes an FRD**
Voltage	**600V to 1800V**	**600V**
Appli-cation	Cooking equipment, IH rice cooker, Inverter microwave oven, IH heating of copier	Inverter washer, UPS, Inverter controller, Inverter air conditioner, Air conditioner for automobile

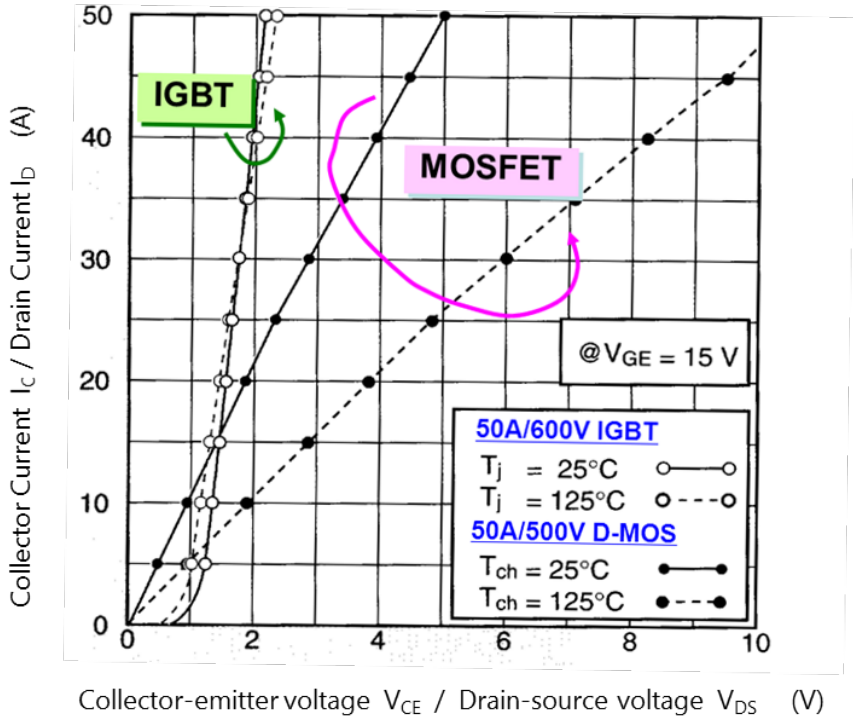


Note: IGBTs are less suitable for high-speed switching than MOSFETs because of bipolar operation.

Comparison of Forward Characteristics of IGBTs and MOSFETs

This page compares the forward characteristics of the MOSFET(D-MOS) and the IGBT at voltage from 500 to 600 V. In the low-current area, the MOSFET has small voltage drop, and has an advantage. On the other hand, the forward voltage characteristic of the IGBT is better than that of the MOSFET in the high-current area, as shown in Fig. 3-17. As the forward characteristic of the MOSFET has strong positive dependence on temperature, the difference in performance of IGBT and MOSFET widens as temperature increases.

Forward characteristic



This figure compares medium- and high-voltage products.

Low-voltage MOSFETs, such as trench MOSFETs, have much lower ON resistance than IGBTs in working current area.

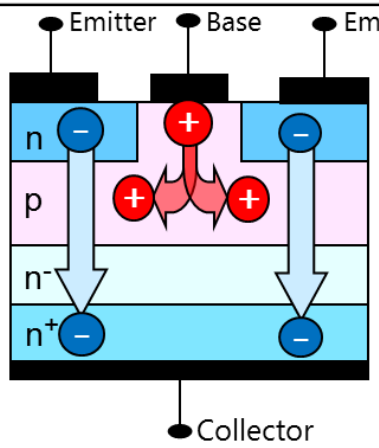
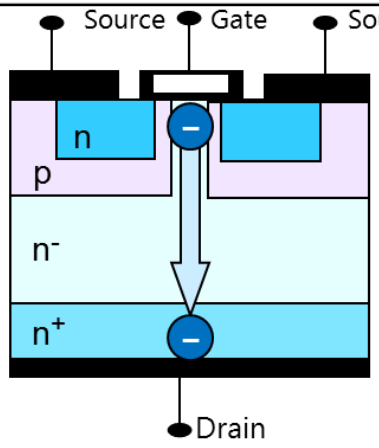
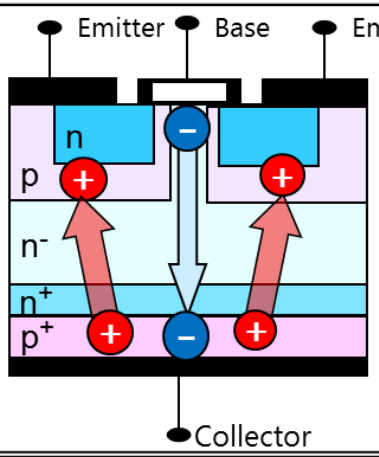
In view of these characteristics and switching performances:

•MOSFETs are adopted for applications such as switching power supply operating at about 100 kHz and at low current density.

•IGBTs are adopted for applications such as AC drive operating under 20 kHz and at high current density.

Fig. 3-17 Comparison of forward characteristics between MOSFET and IGBT

Comparison of Transistors by Structure

	Bipolar Transistor (BJT)	MOSFET	IGBT
Structure of transistors			
Gate (base) driving method	**Current driving** (Low input impedance)	**Voltage driving** (High input impedance)	**Voltage driving** (High input impedance)
Gate (base) driving circuit	Complicated (High part counts)	Simple	Simple
Forward characteristic	**Low $V_{CE(sat)}$**	**High ON voltage** (High current region) No threshold voltage	**Low $V_{CE(sat)}$** With threshold voltage
Switching speed	**Low speed** (with carrier accumulation effect)	**Ultra high speed** (Unipolar operation)	**High speed** (Middle of MOSFET and BJT)
FWD (Include body diode)	**No**	**Yes** (Body diode)	**No** (**Yes** in RC structure)
Safe operating area	**Narrow**	**Wide**	**Middle**

Datasheets of MOSFET: Maximum Ratings

<Absolute maximum ratings>

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	600	V
Gate-source voltage		V_{GSS}	±30	V
Drain current	DC (Note 1)	I_D	12	A
	Pulse (Note 1)	I_{DP}	48	
Drain power dissipation (Tc = 25°C)		P_D	45	W
Single pulse avalanche energy (Note 2)		E_{AS}	359	mJ
Avalanche current		I_{AR}	12	A
Repetitive avalanche energy (Note 3)		E_{AR}	4.5	mJ
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

Note 1: Ensure that the channel temperature does not exceed 150℃.
Note 2: V_{DD} = 90 V, T_{ch} = 25℃(initial), L = 4.36 mH, R_G = 25 Ω, I_{AR} = 3.0 A
Note 3: Repetitive rating: pulse width limited by maximum channel temperature
This transistor is an electrostatic-sensitive device. Please handle with caution.

- **Drain-source voltage (V_{DSS})**
  Maximum voltage of drain to source that can be applied
- **Gate-source voltage(V_{GSS})**
  Maximum voltage of drain to source that can be applied
  Circuit must be designed not to exceed this voltage including surge voltage.
- **Drain current (I_D)**
  Maximum drain current
- **Drain current (pulsed) (I_{DP})**
  Maximum pulsed drain current
  Normally, pulse width is described in safe operating area.
- **Power dissipation (P_D)**
  Power loss allowed to generate in the device
  Allowable thermal capability at T_c=25℃.
- **Avalanche energy, single-pulse and continuous (E_{AS})**
  Maximum allowed energy under designated condition
- **Avalanche current (I_{AR})**
  Maximum current at avalanche operation
- **Channel temperature (T_{ch})**
  Maximum channel temperature at which the device can operate
- **Storage temperature (T_{tsg})**
  Temperature range for storage without operating the MOSFET

Datasheets of MOSFET: Electrical Characteristics

<Thermal Characteristics>

Used to calculate channel temperature

Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th\ (ch\text{-}c)}$	2.78	°C/W
Thermal resistance, channel to ambient	$R_{th\ (ch\text{-}a)}$	62.5	°C/W

<Electrical characteristics>

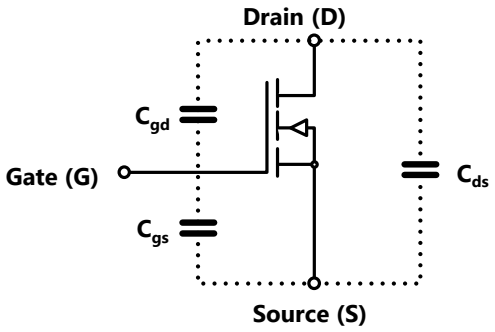
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	I_{GSS}	V_{GS} = ±30 V, V_{DS} = 0 V	—	—	±1	μA
Drain cut-off current	I_{DSS}	V_{DS} = 600 V, V_{GS} = 0 V	—	—	10	μA
Drain-source breakdown voltage	$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	600	—	—	V
Gate threshold voltage	V_{th}	V_{DS} = 10 V, I_D = 1 mA	2.0	—	4.0	V
Drain-source ON resistance	$R_{DS\ (ON)}$	V_{GS} = 10 V, I_D = 6 A	—	0.45	0.55	Ω
Forward transfer admittance	$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 6 A	1.9	7.5	—	S

- **Gate leakage current (I_{GSS})**
  Cut-off current from gate to source
- **Drain cut-off current (I_{DSS})**
  Cut-off current from drain to source
- **Drain-source breakdown voltage ($V_{(BR)DSS}$)**
  Breakdown voltage between drain and source
  Gate and source are shorted so as not to make a channel.
- **Gate threshold voltage (V_{th})**
  Gate-source voltage that can send designated drain current
- **Drain source ON resistance ($R_{DS(ON)}$)**
  It corresponds to collector-emitter saturation voltage ($V_{CE(sat)}$) of bipolar transistor. Voltage drop is expressed as resistance under designated condition. It has positive thermal coefficient.
- **Forward transfer admittance ($|Y_{fs}|$)**
  The ratio of change of output current to change of gate input voltage. Its unit is "S: siemens", same as [A]/[V].

Datasheets of MOSFET: Capacitance and Switching Characteristics

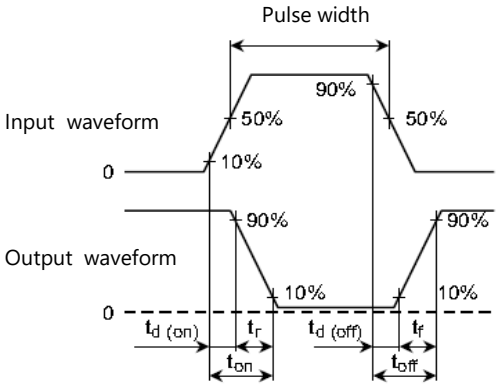
<Electrical characteristics>

Input capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	—	1800	—	pF
Reverse transfer capacitance	C_{rss}		—	9	—	
Output capacitance	C_{oss}		—	190	—	



- **Input capacitance (C_{iss}) equivalent to C_{gd} + C_{gs}**
  Gate-drain and gate-source capacitance
- **Reverse transfer capacitance (C_{rss}) equivalent to C_{gd}**
  Gate-drain capacitance
- **Output capacitance (C_{oss}) equivalent to C_{gd} + C_{ds}**
  Gate-drain and drain-source and gate-drain capacitance

Switching time	Rise time	t_r	10 V, V_{GS}, 0 V, 50 Ω, I_D = 6 A, V_{OUT}, R_L = 33 Ω, V_{DD} ≈ 200 V, Duty ≤ 1%, t_w = 10 μs	—	40	—	ns
	Turn-on time	t_{on}		—	80	—	
	Fall time	t_f		—	15	—	
	Turn-off time	t_{off}		—	110	—	

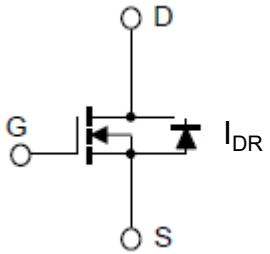


- **Rise time (t_r)**
  It is the time when drain-source voltage varies from 90% to 10%.
- **Turn-on time (t_{on})**
  It is the time between the instant when gate-source voltage rises to 10% and the instant when drain-source voltage falls to 10%.
- **Fall time (t_f)**
  It is the time when drain-source voltage varies from 10% to 90%.
- **Turn-off time (t_{off})**
  It is the time between the instant when gate-source voltage falls to 90% and the instance when drain-source voltage rises to 90%.

Datasheets of MOSFET: Body Diode

<Electrical characteristics>

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I_{DR}	—	—	—	12	A
Pulse drain reverse current (Note 1)	I_{DRP}	—	—	—	48	A
Forward voltage (diode)	V_{DSF}	I_{DR} = 12 A, V_{GS} = 0 V	—	—	−1.7	V
Reverse recovery time	t_{rr}	I_{DR} = 12 A, V_{GS} = 0 V, dI_{DR}/dt = 100 A/μs	—	1200	—	ns
Reverse recovery charge	Q_{rr}		—	13	—	μC



- **Continuous drain reverse current (I_{DR})**
  Forward current of drain-source diode with DC

- **Pulse drain reverse current (I_{DRP})**
  Forward current of drain-source diode with pulse

- **Forward voltage (diode) (V_{DSF})**
  Voltage dropdown of drain-source diode with forward current

- **Reverse recovery time (t_{rr})**
  Reverse recovery time of drain-source diode under designated condition

- **Reverse recovery charge (Q_{rr})**
  Reverse recovery charge of drain-source diode under designated condition

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